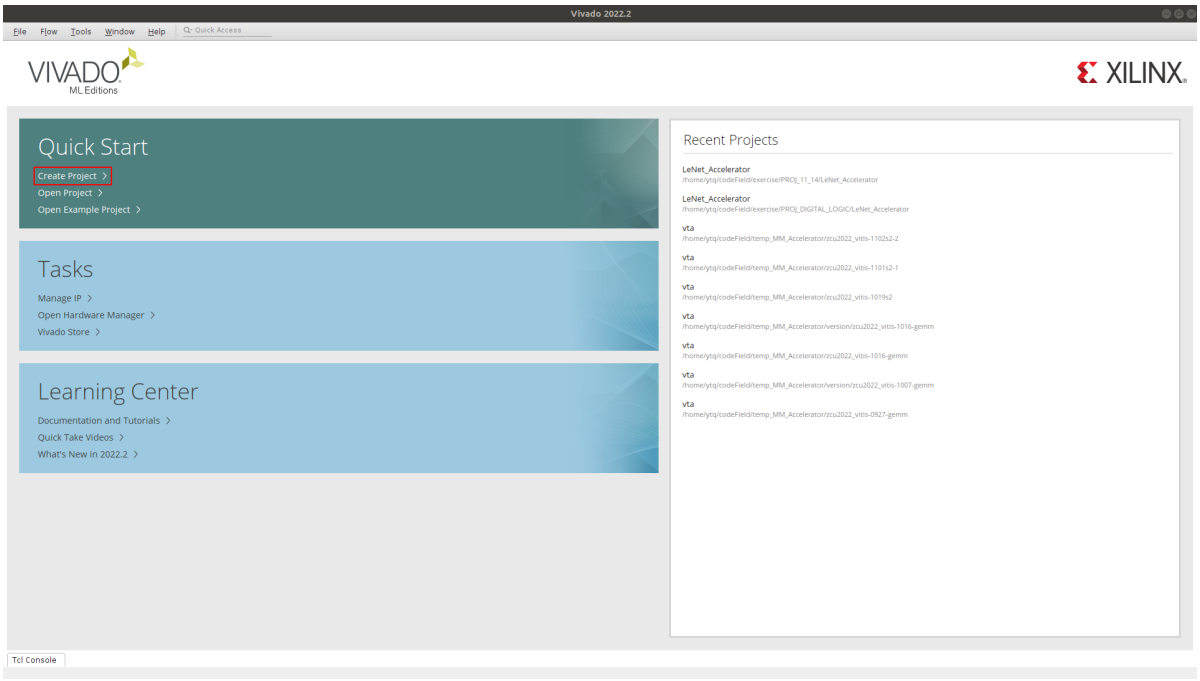
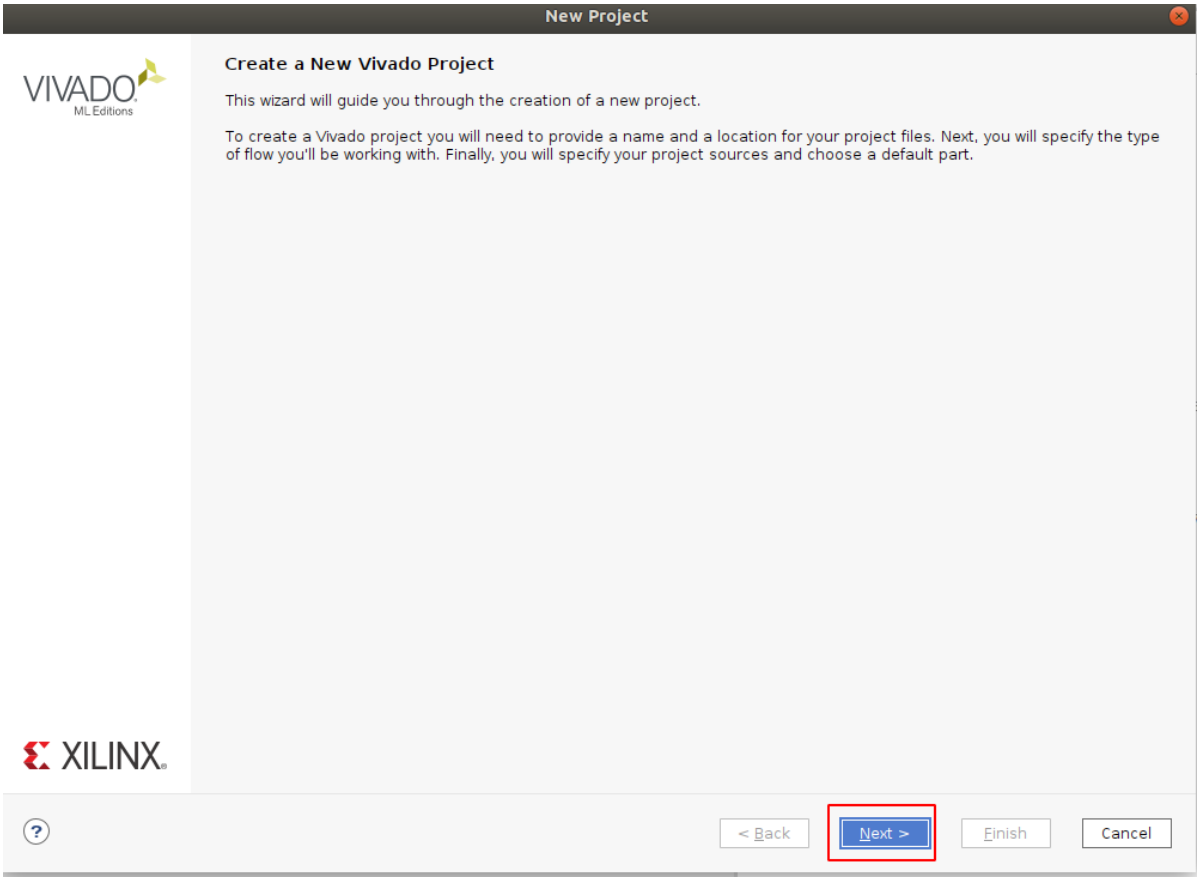
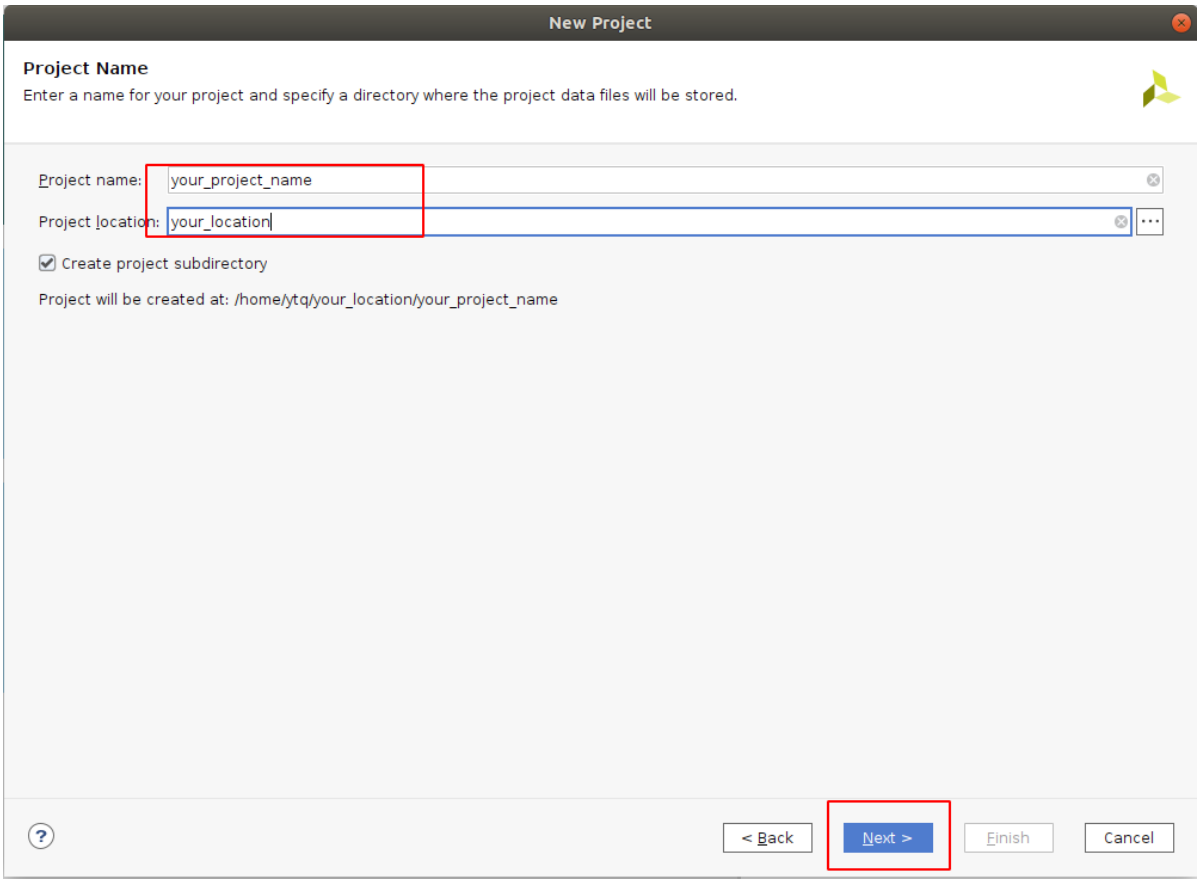
创建一个vivado工程

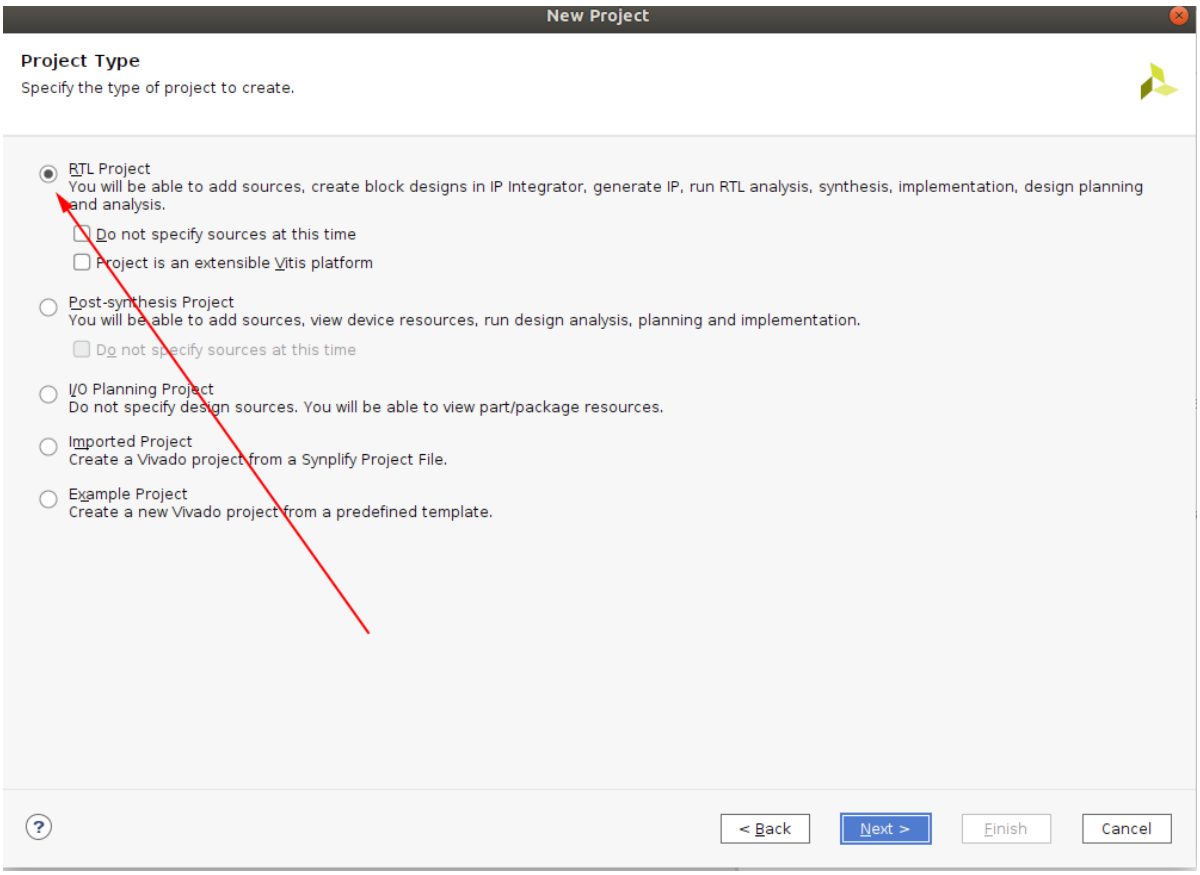
1. 创建RTL仿真工程

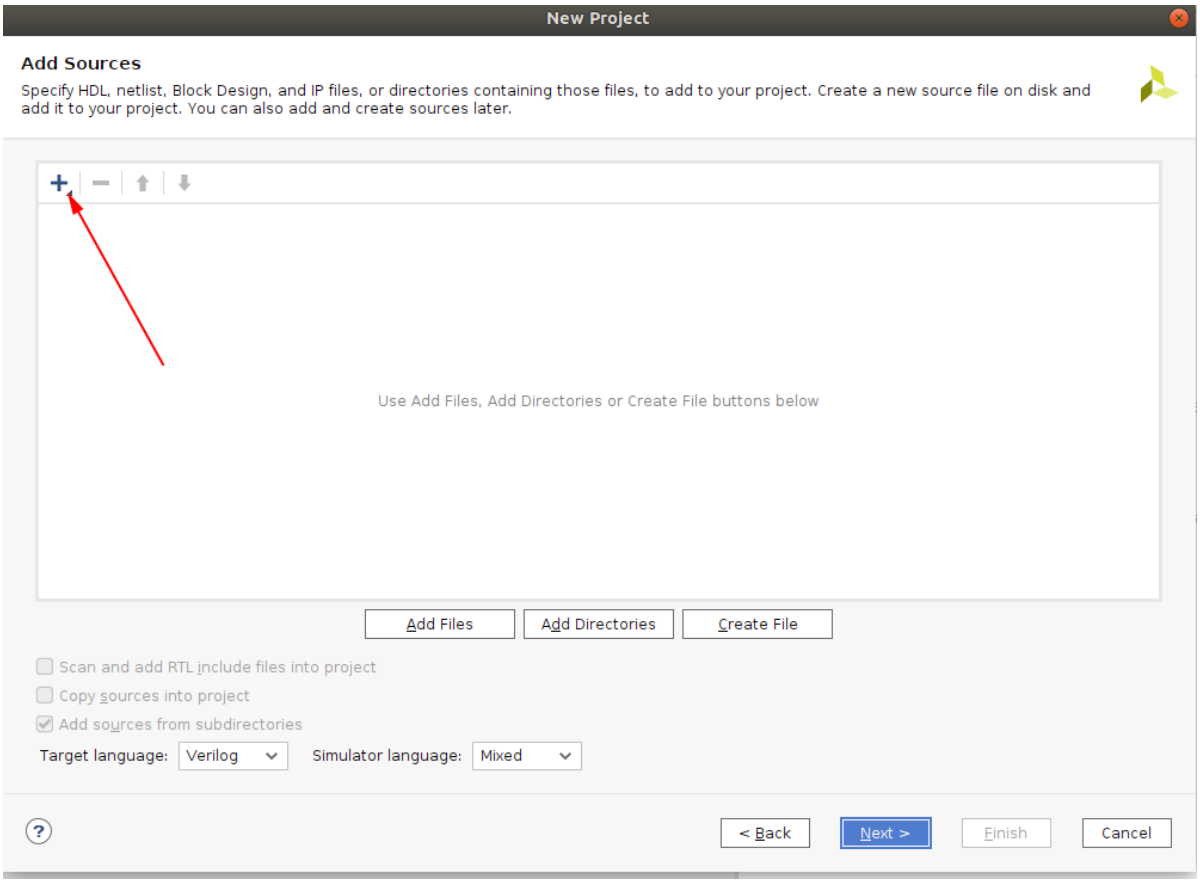
也可以参考files/Basys3实验官方指导手册.pdf中的第二章内容



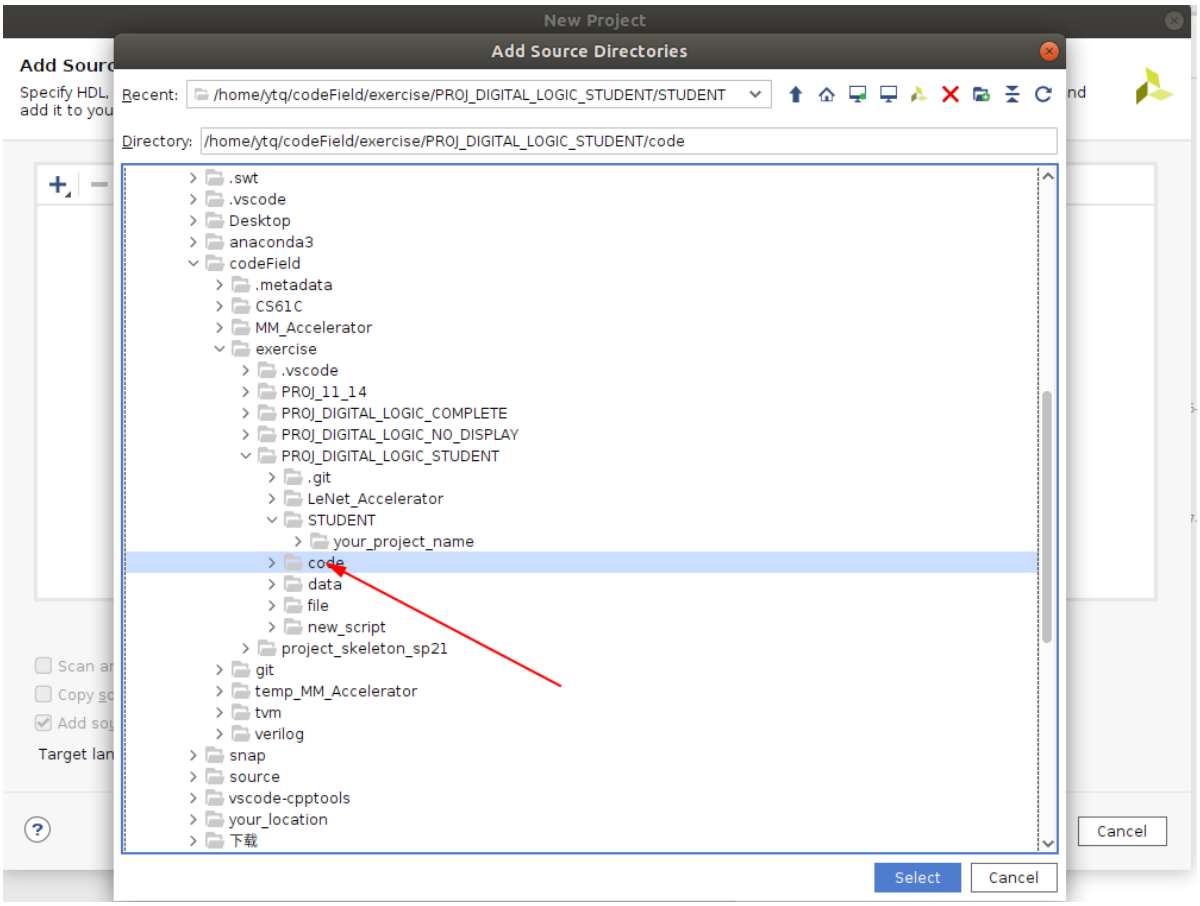


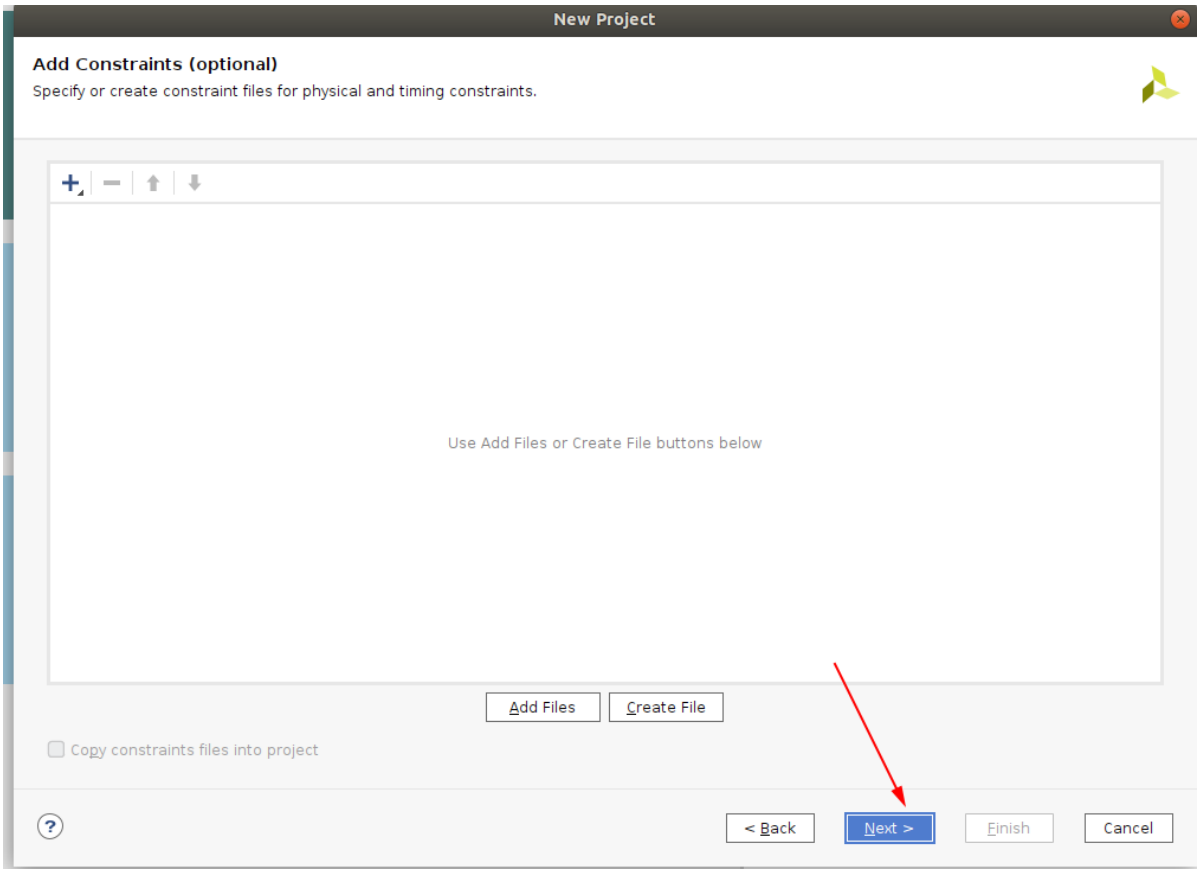

New Project
Project Name
Enter a name for your project and specify a directory where the project data files will be stored.
Project name:
your_project_name
Project location:
your_location
Create project subdirectory
Project will be created at: /home/ytq/your_location/your_project_name
< Back
Next >
Finish
Cancel


New Project
Project Type
Specify the type of project to create.
RTL Project
You will be able to add sources, create block designs in IP Integrator, generate IP, run RTL analysis, synthesis, implementation, design planning and analysis.
Do not specify sources at this time
Project is an extensible Vitis platform
Post-synthesis Project
You will be able to add sources, view device resources, run design analysis, planning and implementation.
Do not specify sources at this time
I/O Planning Project
Do not specify design sources. You will be able to view part/package resources.
Imported Project
Create a Vivado project from a Synplify Project File.
Example Project
Create a new Vivado project from a predefined template.
< Back
Next >
Finish
Cancel

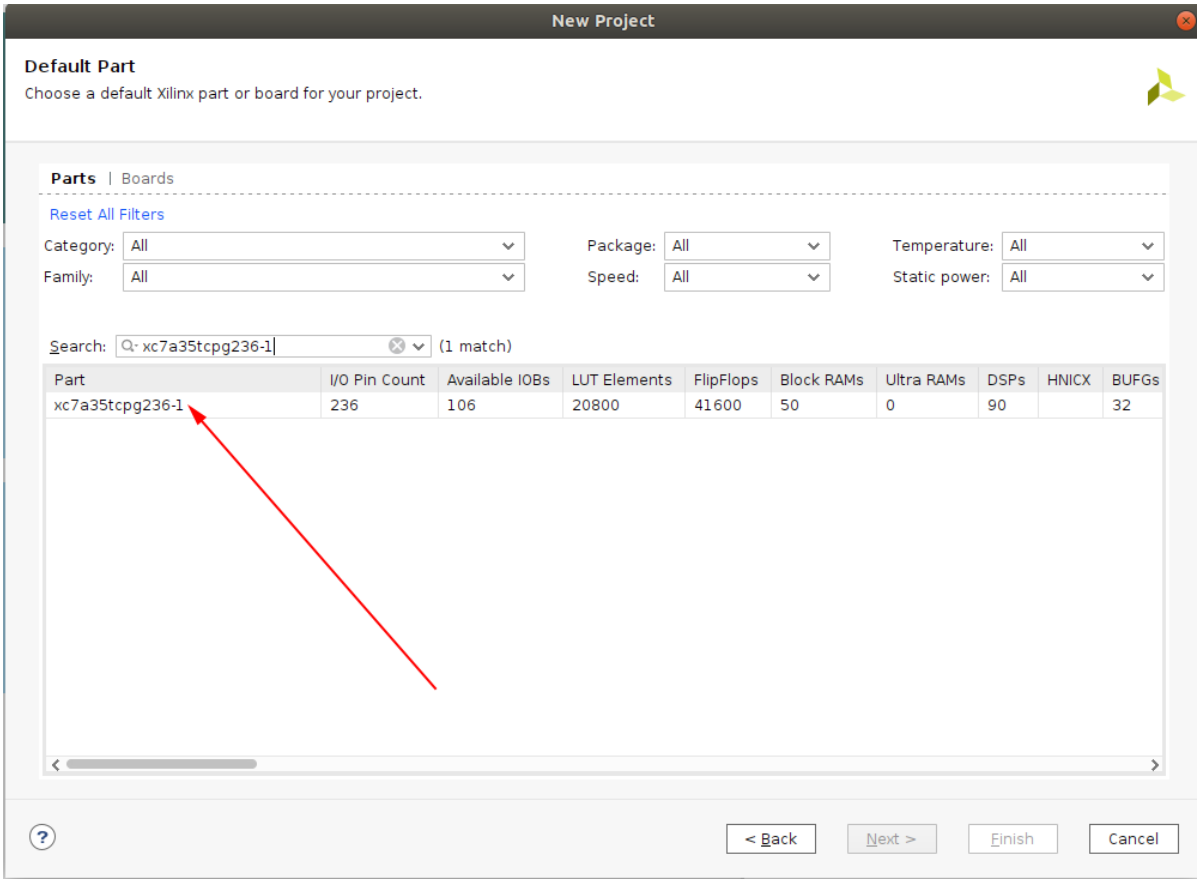


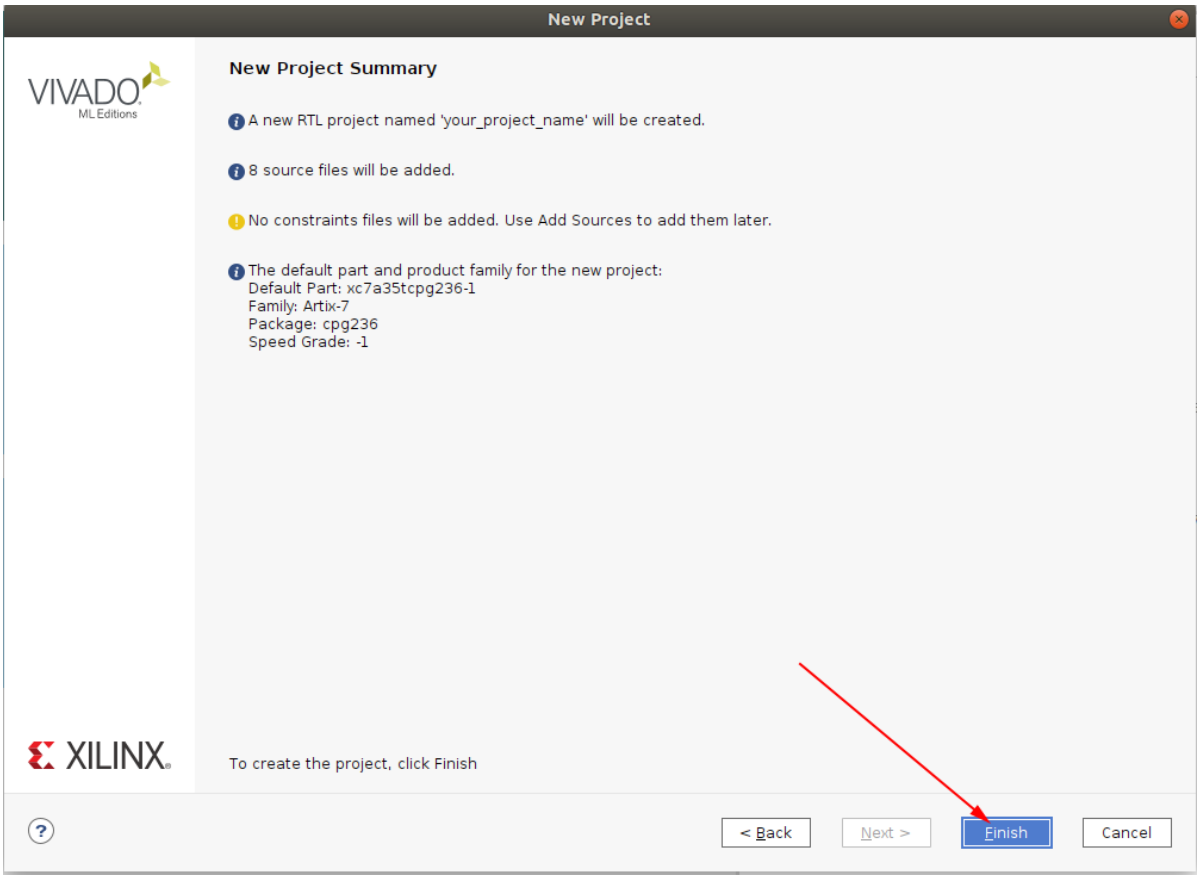
选择add directories，把我们的code文件夹加入项目中



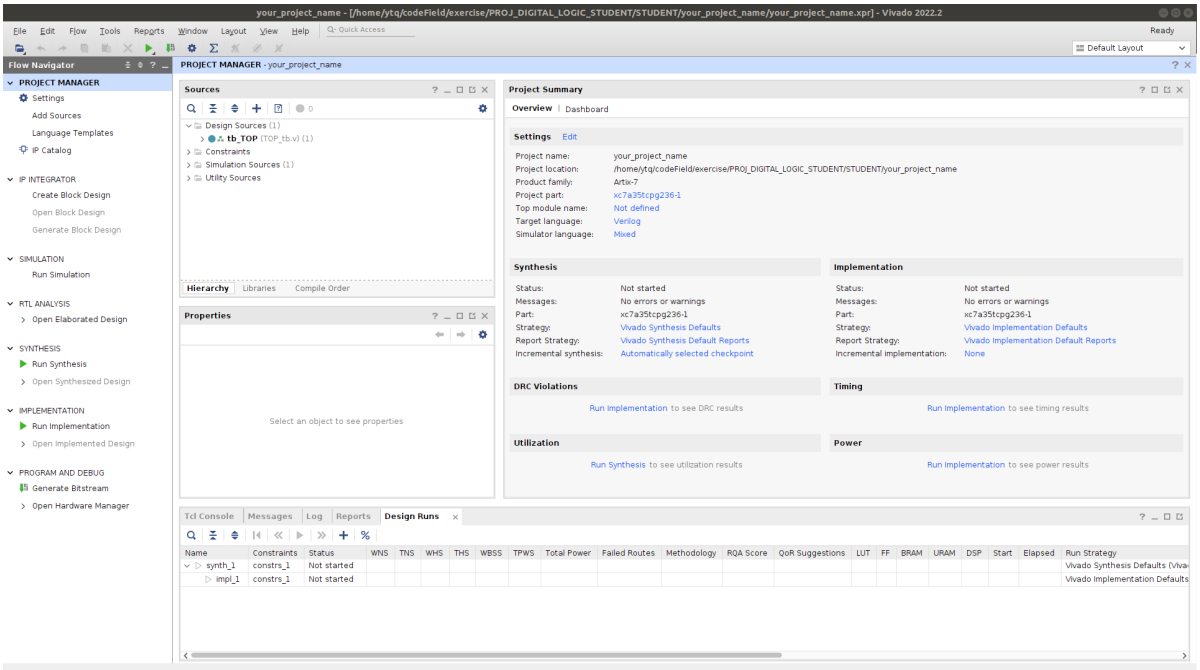

New Project
Add Constraints (optional)
Specify or create constraint files for physical and timing constraints.
Use Add Files or Create File buttons below
Add Files
Create File
Copy constraints files into project
< Back
Next >
Finish
Cancel

选择相应的开发板型号

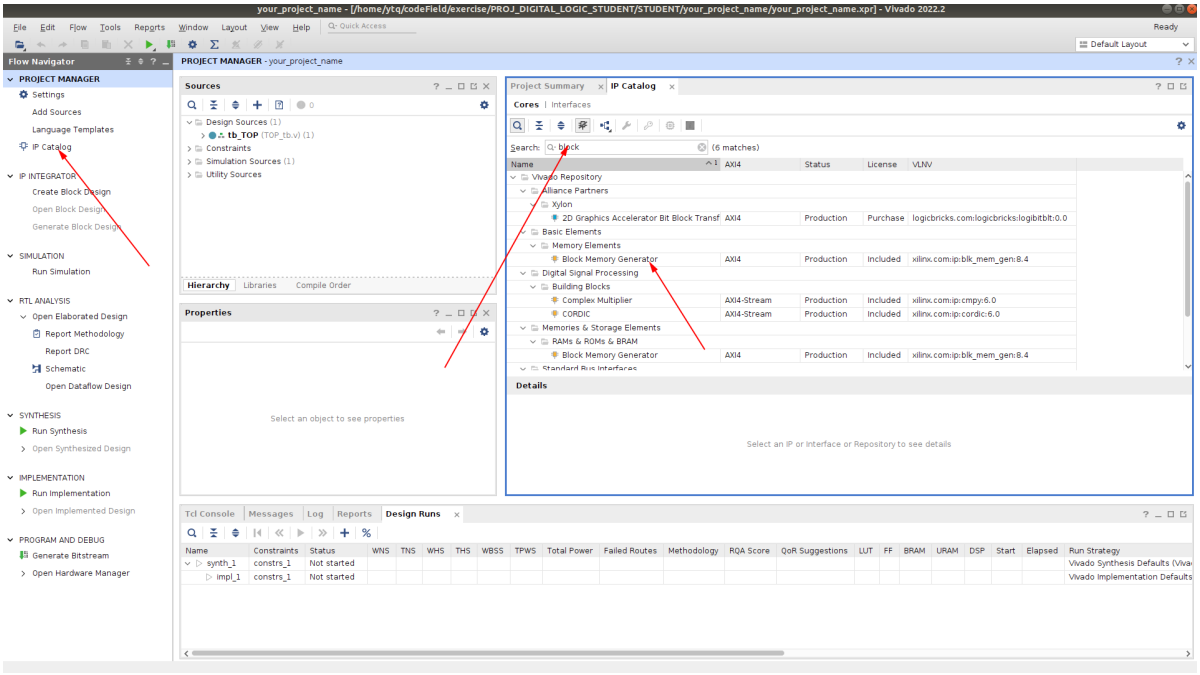

New Project
Default Part
Choose a default Xilinx part or board for your project.
Parts | Boards
Reset All Filters
Category: All
Family: All
Package: All
Speed: All
Temperature: All
Static power: All
Search: xc7a35tcpg236-1 (1 match)
Part I/O Pin Count Available IOBs LUT Elements FlipFlops Block RAMs Ultra RAMs DSPs HNICX BUFGs
xc7a35tcpg236-1 236 106 20800 41600 50 0 90 32
< Back
Next >
Finish
Cancel

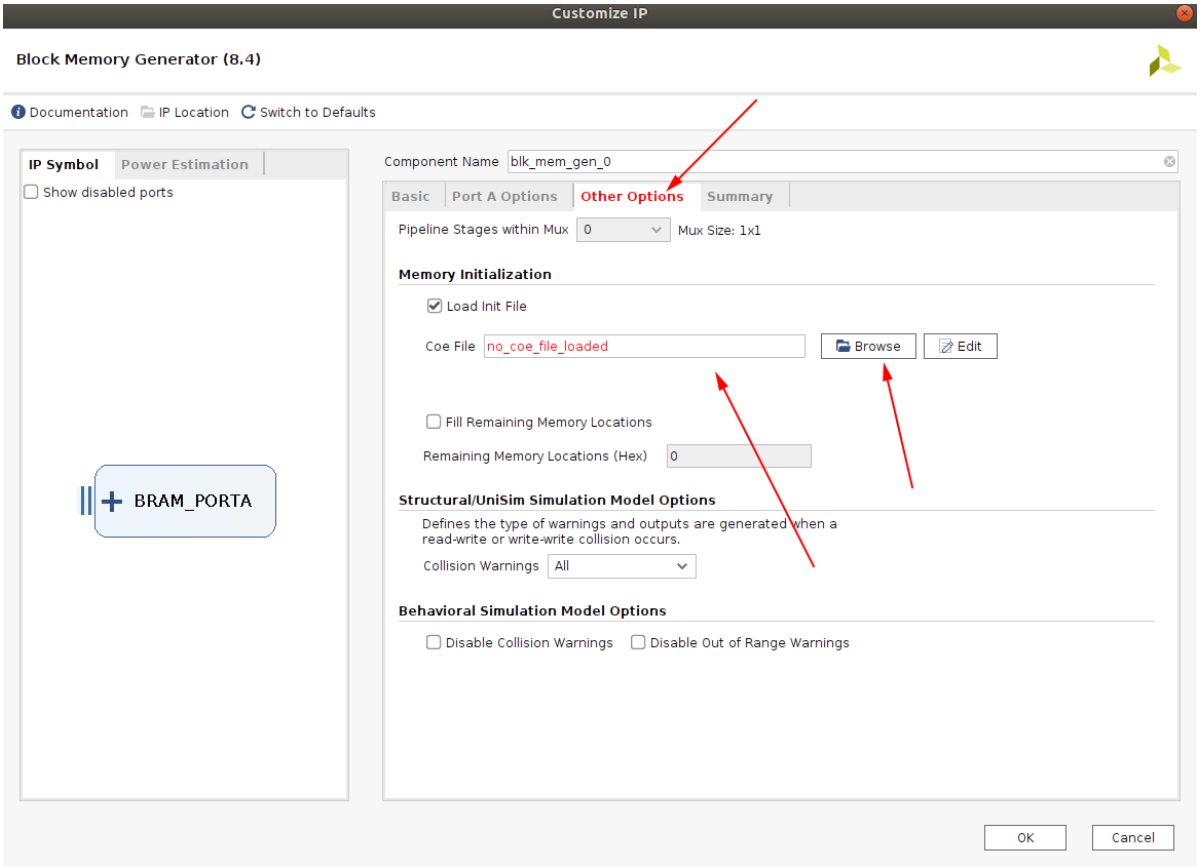


这样就成功创建了一个RTL project



2. 创建ram rom





用文件对rom进行初始化，只需通过browse找到脚本生成的coe文件即可。

具体操作可参考：https://blog.csdn.net/m0_66360845/article/details/126022035