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An ultra-high-speed FPGA based digital correlation processor

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Abstract: This paper presents an ultra-high-speed correlation processor for FPGA (Field-Programmable Gate Array) which is based on MDF (multiple-path delay feedback) pipelined FFT (fast Fourier transform) architecture. In order to decrease the resource cost and processing delay, the FFT processor is based on DIF (Decimation in Frequency) decomposition method, and the IFFT processor is based on DIT (Decimation in Time) decomposition method. The data input and output of the correlation processor are both in natural order. The main clock speed of the processor FPGA implementation can be higher than 200 MHz and is able to process continuous complex input at more than 1.6Gsps (giga samples per second).

Keywords: FPGA, FFT, Correlation
Classification: Integrated circuits

References

[1] A. Benz, P. Grigis, V. Hungerbühler, H. Meyer, C. Monstein, Bruno Stuber, Dino Zardet, "A broadband FFT spectrometer for radio and millimeter astronomy", Astronomy & Astrophysics, vol. 442, pp. 767-773, 2005

[2] Wei Li, Haibing Zhu, Jun Wang; Shaohong Li, "The GPS code acquisition based on pipelined FFT processor", SPIE, Second International Conference on Space Information Technology, vol. 6795, 2007

[3] FanWang, Huotao Gao, Lin Zhou, Qingchen Zhou, Jie Shi, Yuxiang Sun, "Design and FPGA implementation of digital correlation for HF chirp radar based on modified orthogonal transformation", IEICE Electronics Express, vol.8, pp.1736-1742, Oct.2011

[4] Escamilla-Hernández, Enrique et al. "Signal Compression in Radar Using FPGA", Revista Facultad de Ingenieria. vol. 3, núm. 55, pp. 134-143, 2010. ISSN 0120-6230.

[5] Fan Ding, Xiaojing Huang, Biyang Wen, Zhisheng Yan."Design and FPGA implementation of digital pulse compression for chirp radar based on CORDIC ", IEICE Electronics Express (Impact Factor: 0.39). 01/2009; 6(11):780-786.

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[6] S. G. Qadir, J. K. Kayani, and S. Malik, "Digital implementation of pulse compression technique for X-band radar," in Int. Appl. Sci. Technol. Bhurban Conf., Jan. 2007, pp. 35–39.

[7] Xiujie Qu, Cuimei Ma, Shixin Zhang, and Sitong Lian, "High Real-Time Design of Digital Pulse Compression Based on FPGA," Mathematical Problems in Engineering, Article ID 792862, in press.

[8] S. He, M.Torkelson. "Designing pipeline FFT processor for OFDM (de)modulation", ISSSE, pp.257-262. 2001

[9] Yu-Wei Lin, Hsuan-Yu Liu, and etc. "A 1-GS/s FFT/IFFT Processor for UWB Applications", IEEE Journal of Solid-State Circuits, vol. 40, pp.1726-1735, Aug.2005.

[10] Li Wei, Sun Jinping, Wang Jun, Li Shaohong. "Implementation of 32 k points ultra high speed FFT processor based on FPGA devices". Journal of Beijing University of Aeronautics and Astronautics. Vol.33.pp.1440-1443. Dec.2007

[11] Fredrik Kristensen, et al. "Reduced Transceiver-Delay for OFDM Systems", Vehicular Technology Conference, pp. 1242-1245, 2004.

[12] Wei Li. "Research on the Key Technique of SAR real-time raw data simulation system", PostDoc Report, pp.48-52, Dec.2010

[13] J.Y.Oh, M.S.Lim. "Area and Power Efficient Pipeline FFT Algorithm", Proc. IEEE Workshop on Signal Processing System Design and Implementation, pp.520-525, 2005.

1 Introduction

In astronomy, atomic physics, radar processing, GPS (Global Positioning System) direct acquisition and many other fields, high-speed real-time digital correlation or convolution is an important digital signal processing method [1,2]. In these applications, the intensity of these signals is very weak, and a long time accumulation is required to detect a signal. In some applications, signal bandwidth is close to or more than 1GHz. Therefore, an ultra-high-speed long point correlation processor is needed in order to decrease processing time. There are many research have been done for real-time digital correlation or pulse compression, however because of high resource cost, the long point correlation processor with speed higher than 1 GHz is still challenging and with little research [1-7].

The correlation can be performed using the direct time domain correlation or the fast correlation method using FFT [2]. The former needs great resource, but has less latency when the operation can be performed in parallel. The latency of the later is increased, while the resource is greatly reduced. In this paper, we will focus on the FFT-based method.

Over the last decade, FPGA has been one of the most powerful devices for digital signal processing with the development of semiconductor technology. A lot of computation and storage unit within the FPGA makes it very suitable for FFT

The current FFT hardware structures fall into two types: recursive structure, pipeline structure. Recursive structure is also known as the shared memory structure, which consists of only one butterfly operation unit and one or two memory block. All stages of the FFT use the same butterfly operation unit and

intermediate results of every stage is read and written to the same memory block. The main advantage of this structure is low hardware resource cost; but since only one operation unit is used, operation time is longer. In the pipeline structure, every stage of FFT is processed by an operation unit with butterflies and memory blocks. The result of every operation unit can be used for the next stage without having to wait for the whole stage to complete. The pipelined FFT architecture mainly includes multipath delay commutator (MDC), single-path delay feedback (SDF) and multiple-path delay feedback (MDF) [7,8]. In order to realize the FPGA-based high-speed correlation with more than 1GHz sampling rate input, MDC or MDF FFT processor structures are frequently used. The MDF structure, which is combined with MDC structure and SDF structure, can work at very high speed, with relatively low resource cost of memory and multipliers [8,9].

One of the drawbacks of the pipelined MDF or SDF FFT processor when used for correlation is that the output order of the FFT processor is bit-reversed. If we use the same structure for the FFT and IFFT, there needs to be additional memory to reorder the output result of FFT, and the latency is greatly increased. So the DIT and DIF structures are presented for the FFT and IFFT processor respectively [11,12].

In this paper, a new correlation processor will be proposed based on MDF structure with DIT/DIF decomposition method. The processor is designed in FPGA, which can process 32K-points pipelined correlation with more than 1.6Gs/s complex data rate.

2 Correlation processor architecture

As shown in (1-2) the FFT based digital circular correlation between $s(n)$ and $h(n)$ method mainly consists of two FFT, one complex multiplication and one IFFT.

$$y(n) = \sum_{i=0}^{N-1} s(n+i)h^*(i) \tag{1}$$

$$y(n) = IFFT\{FFT[s(n)] \cdot conj(FFT[h(n)])\} \tag{2}$$

The FFT and IFFT processor both can be designed based on MDF architecture, where the FFT using DIF structure and IFFT using DIT structure. The parallel complex multiplication results of the two FFT output can be directly connected to the MDF IFFT input. No memory need for data re-order and the output of the IFFT is in natural order.

2.1 MDF FFT/IFFT processor algorithm description

The expression of DFT is shown as follows, where N is number of points of FFT and IFFT:

$$X[k]=\sum_{n=0}^{N-1}x[n]W_N^{nk}$$

$$x[n]=\frac{1}{N}\sum_{n=0}^{N-1}X[K]W_N^{-nk} \tag{3}$$

In the MDF FFT/IFFT processor, N points FFT/IFFT is divided into N_1 parallel blocks:

$$\begin{cases} N=N_1\cdot N_2 \\ n=n_2N_1+n_1 \\ k=k_1N_2+k_2 \end{cases}, \tag{4}$$

where

$n_1=0\cdots N_1-1$, $n_2=0\cdots N_2-1, k_1=0\cdots N_1-1, k_2=0\cdots N_2-1$.

Substituting equation (4) into equation (3):

$$X[k_1N_2+k_2]=\sum_{n_1=0}^{N_1-1}\left[\left(\sum_{n_2=0}^{N_2-1}x[n_2N_1+n_1]W_{N_2}^{n_2k_2}\right)W_N^{n_1k_2}\right]W_{N_1}^{n_1k_1} \tag{5}$$

$$x[n_2N_1+n_1]=\frac{1}{N}\sum_{k_2=0}^{N_2-1}\left[\left(\sum_{k_1=0}^{N_1-1}X[k_1N_2+k_2]W_{N_1}^{-n_1k_1}\right)W_N^{-n_1k_2}\right]W_{N_2}^{-n_2k_2} \tag{6}$$

In equation (5), the N points FFT is decomposed into two FFT. First, the internal N_2 point FFT is computed. Then, the result is multiplied by the phase factor $W_N^{n_1k_2}$. Next a N_1 point FFT is computed. In equation (6), first the internal N_1 point IFFT is computed. Then, it is multiplied by the phase factor $W_N^{-n_1k_2}$. Next, a N_1 point IFFT is computed.

2.2 Implementation structure

From equation (5) and (6), it can be seen that the processing steps of MDF FFT and IFFT are reversed, but both of them can be decomposed into N_1 parallel parts. The MDF FFT processor architecture has been discussed in several papers [9,10]. In this paper, as an example, we will show the implementation of the 32K-points DIT-based MDF IFFT processor [12]. In order to be able to process more than 1Gsps complex data rate in the FPGA device and decrease the resource cost, the FFT/IFFT is decomposed into 8 parallel pipelined parts, where $N_1=8$.

According to equation (6), the 32K-points IFFT processor is divided into three

modules: the first part is a 8-points parallel IFFT, the second part is the multiplication with the phase factor $W_N^{-n_1 k_2}$ and the third part is 8 parallel 4K IFFT.

In order to reduce the cost of memory and multipliers, the 4K IFFT using R2^{2}SDF pipelined FFT structure is used. Each module is described in detail below.

Module 1

Module 1 is an 8-points parallel IFFT, which can use the standard radix-8 butterfly operation unit. It can process eight input data and output eight results every clock period, and through this the input data can be divided into eight parallel modules. The structure of Module 1 is shown in Figure 1.

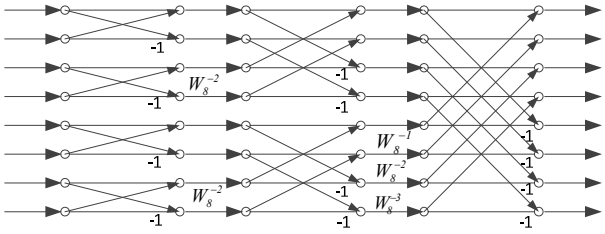

Figure 1. Structure of Module 1

Module 2

Module 2 consists of 8 multiplications between outputs of Module 1 and the phase factors $W_N^{-n_1 k_2}, n_1 = 0...7$. We use ROMs in the FPGA to store the phase factor, and because n_1=0, there is only a need for 7 blocks of ROM.

Module 3

Module 3 is composed of 8 parallel SDF parts; each part adopts R2^{2}SDF structure. The structure of R2^{2}SDF is described in detail in [13]. Since the feedback unit length of each channel is one-eighth of the total length, the total memory cost is similar to the same points of the R2^{2}SDF structure. Different from DIF FFT architecture, in the DIT FFT architecture, the feedback memory depth is increased with the IFFT stage and the address for the phase factor is in bit-reverse order.

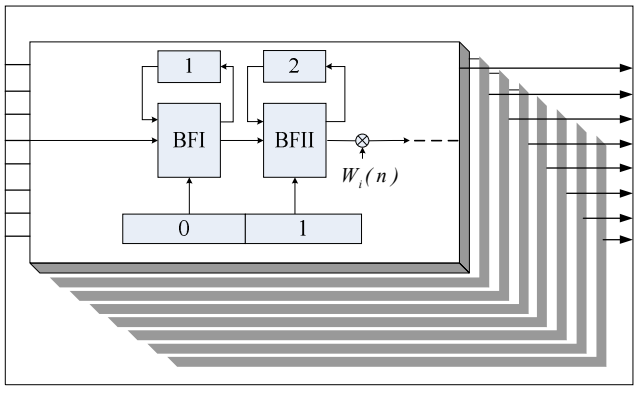

Figure 2. R2^{2}SDF DIT FFT structure

2.3 Correlation processor

The correlation processor mainly consists of two FFT processors and one IFFT processor. The input of two FFT processors is fed in with natural order. In Figure 3,

the output of the FFT processor A is multiplied with the conjugation of the output of FFT processor B. Then, the result will be input into the IFFT processor. The FFT processors are based on MDF DIF architecture, and the IFFT processor is based on MDF DIT architecture. The outputs of FFT processors are in bit-reverse order, and the outputs of the IFFT processor are in natural order.

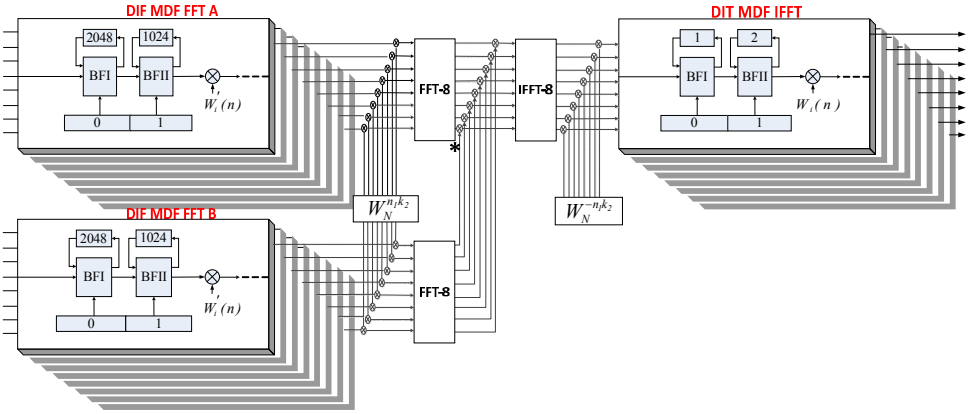

Figure 3. Correlation processor architecture

3 FPGA implementation and performance test

The 32K-points complex correlation processor is implemented using Xilinx FPGA Virtex 5. The details of the FPGA implementation and optimization are given below.

3.1 FPGA design

(1) Data memory

FPGA memory is mainly composed of BRAM and distributed memory. In Xilinx Virtex 5, BRAM is 36-Kbit block memory, and distributed memory is small volume memory using logic resources. In Module 3 of the IFFT processor, the memory width of every stage is set to 2*18bits for complex data. According to the structure of R2^{2}SDF, the feedback memory length of the first stage is 1 and is increased by two times for every stage. In the FPGA implementation, memory of the first 7 stages use distributed memory, and the remaining 5 stages use BRAM.

(2) Phase factor memory

There are two kinds of phase factor in the FFT/IFFT processor. The first is the internal phase factor $W_{N_2}^{n_2k_2}$ of the FFT or $W_{N_2}^{-n_2k_2}$ of IFFT SDF processor. These phase factors can be designed using the Xilinx sine and cosine table IP kernel implementation. Because of symmetry, only N/8 depth memory is needed for N points phase factor. In the correlation processor, the two FFT processors are working synchronous, so the phase factor memory can be shared between the FFT processors. The second kind of phase factor is $W_N^{n_1k_2}$ in equation (5) or is $W_N^{-n_1k_2}$ in equation (6). It can be designed using ROM. In the FPGA implementation, both of the phase factors are of 12-bit width.

(3) Multiplier

In the FPGA Virtex 5, there are lots of DSP48E slice resources, mainly used for hardware multiplication. In order to reduce the cost of the logic resource of the FPGA implementation, these resources are primarily used for complex multiplication between the butterfly operation results and the phase factor. The complex multiplication can be designed with 3 or 4 multipliers. In order to reduce the cost of the multipliers, this paper adopts the 3 multipliers method.

3.2 The performance of FPGA implementation

The correlation processor is implemented by VHDL language programming using FPGA XC5VSX240T-2 with the ISE12.4 Xilinx design platform. The resource cost of the implementation is shown in Table 1, according to the synthesis report. As can be seen from Table I, the memory cost using the DIF/DIT hybrid architecture can be decreased greatly. According to the time analysis report, the highest working frequency of the processor can be 216MHz. Because of the 8-parallel MDF FFT architecture, it can process 1728Ms/s complex input data.

Table I. FPGA resource report

	FFT	IFFT	Correlation processor based on DIF FFT	Correlation processor based on DIF/DIT FFT
Slice Flip Flops	38336	38580	118024	114290
Slice LUTs	32938	33278	102081	98077
36k BRAMs	72	72	312	216
DSP48Es	156	156	492	492

The MDF hybrid DIF/DIT FFT correlator architecture can be customized with different correlation length. Compared to existing digital correlator designs, it can process more than 1.6 GHz bandwidth continuous input data with long correlation length and optimized resource cost. In [3-7], input data rate of the FPGA based pulse compression processors is lower than 200MHz. In [2], a 64K points FFT based correlator is designed but can only work below 200MHz. In [8], a 1.6GHz bandwidth FPGA time domain based digital correlator which can only process short point correlation.

4 Conclusion

This paper presents a FPGA-based ultra-high-speed correlation processor. The processor is based on MDF FFT processor architecture. In this processor, the FFT processor is based on DIF MDF FFT architecture, and the IFFT processor is based on DIT MDF FFT architecture. The processor is optimized according to FPGA internal structure in order to decrease resource cost. The processor can process 32K-points pipelined correlation with more than 1.6Gs/s complex input rate. It can be used in applications such as atomic physics, Radar processing and GPS direct acquisition.