

Yaotian Liu

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Education

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| Arizona State University
<i>PhD</i> in Computer Engineering
• GPA: 4.0/4.0 | 2023/08 – 2028/06 (Expected)
Tempe, Arizona, US |
| Shanghai Jiao Tong University
<i>Bachelor of Engineering</i> in Microelectronics Science and Engineering
• GPA: 3.7/4.3. Rank 19/67.
• Outstanding Graduates | 2019/09 – 2023/06
Shanghai, China |

Work Experience

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| Shanghai Taize Semiconductor
Digital IC Design Intern
• Developed the micro-architecture for the data link layer of the company's proprietary inter-chip connection, supporting 1024 chips. Co-author of a related patent. The design has been successfully taped out using TSMC 16 nm.
• Developed an accelerator for elliptic curve accumulation in Elliptic Curve Cryptography (ECC). | 2022/06 – 2022/09, 2023/03 – 2023/06
Shanghai, China |
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Research Experience

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| Arizona State University, ECEE
Research Assistant, advised by Prof. Jeff Zhang
• Skip-SCAR: Hardware-Friendly High-Quality Embodied Visual Navigation , in submission to ICRA 2025. <ul style="list-style-type: none">▶ The first computation-efficient ObjectNav system features a skip mechanism and a novel SCAR-based predictor that leverage sparsity to significantly reduce memory usage.▶ Currently No.1 among all published methods in the online leaderboard. • Intel 16nm Tapeout <ul style="list-style-type: none">▶ Designed, implemented and verified a systolic array with AXI interfaces in SystemC.▶ Designed, implemented and verified a RISC-V & AXI based SoC design in SystemVerilog, which supports arbitrary number of accelerators and memories.▶ Developed an agile physical design flow using Synopsys Fusion Compiler.▶ Setup multiple automatic scripts to speed up relative flows.<ul style="list-style-type: none">– A flow to transfer memory IPs from SystemVerilog to Verilog and then generate a Catapult memory library by automatically extracting relevant information from the Verilog code and datasheet.– An automatic Docker-based RISC-V cross-compilation flow, able to run on any type of host machine.– A flow to run CVA6 (a RISC-V code) simulation with Verilator to generate waveform. • LLM-VeriPPA <ul style="list-style-type: none">▶ Developed a Python workflow to automatically extract information from Verilog code, perform logic synthesis for PPA (Power, Performance, and Area), and iteratively reduce the clock period to find the fastest possible timing. | 2023/08 – Now
Tempe, AZ, US |
| Shanghai Jiao Tong University, Department of Micro/Nano Electronics
Final Year Project, advised by Prof. Yongfu Li
• Implemented a functional ECO system with a Verilog parser written in PEG grammar, accepted by AICAS 2023.
• An ABC-based algorithm for efficient circuit pruning by removing functionally equivalent sub-circuits, which increase the performance of functional ECO. | 2023/01 – 2023/05
Shanghai, China |
| Shanghai Jiao Tong University, AI Institute
Undergraduate Research Assistant, advised by Prof. Yunbo Wang
• Implemented a reinforcement learning algorithm for automatically stock trading.
• Reproduced an baseline algorithm ytliu/FactorVAE (57 stars) from AAAI 2022. | 2022/05 – 2022/09
Shanghai, China |

Publications

- [Liu, Y.](#), Cao, Y., Zhang, J., “Skip-SCAR: Hardware-Friendly High-Quality Embodied Visual Navigation.” *arXiv preprint arXiv: 2405.14154*, in submission to ICRA 2025.

Update time: 2024-12-16

- Nalla, P., Haque, E., [Liu, Y.](#), Sapatnekar S., Zhang, J., Chakrabarti, C., Cao, Y., “CLAIRE: Composable Chiptlet Libraries for AI Inference” *2025 Design Automation and Test in Europe Conference (DATE)*
- Wang, Z., Sun, J., Goksoy, A., Mandal, S., [Liu, Y.](#), Seo, J., etc. “Exploiting 2.5D/3D Heterogeneous Integration for AI Computing,” *2024 29th Asia and South Pacific Design Automation Conference (ASP-DAC)*
- Thorat, K., Zhao, J., [Liu, Y.](#), Peng, H., Xie, X., Lei, B., Zhang, J. and Ding, C.. “Advanced Language Model-Driven Verilog Development: Enhancing Power, Performance, and Area Optimization in Code Synthesis.” *arXiv preprint arXiv:2312.01022*.
- [Liu, Y.](#), Zhang, Y., Zhang, Q., Chen, R. and Li, Y., 2023, June. “FEEP: Functional ECO synthesis with efficient patch minimization.” In *2023 IEEE 5th International Conference on Artificial Intelligence Circuits and Systems (AICAS)*.

Open-Source Project

obsidian-pseudocode [ytliu74/obsidian-pseudocode](#) (91 stars)

- An Obsidian plugin that renders LaTeX-style pseudocode in a code block, offering various auxiliary features.

simple SPICE [ytliu74/SimpleEDA](#) (7 stars)

- A basic SPICE tool for circuit simulation supports DC, AC, and TRAN analysis for linear and nonlinear devices with a GTK interface.

Skills

Programming Languages: Verilog, Python, C/C++, Javascript/Typescript.

Tech Skills: Git, Digital Logic Design, Pytorch, Linux, Docker, Matlab, RTL to GDSII flow...