Floating-Point Multiply-Accumulate Unit: Assessing Non-Optimized Operations

IEEE 754 single-precision floating-point

Sign Exponent Mantissa
       8-bit   23-bit
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Feature

Weight
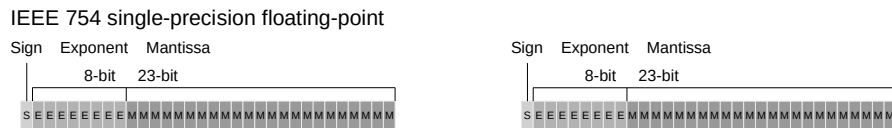
Loop pipelining:

Latency = (**II** x (**N** − 1)) + **IL**

Latency = 8N + 4

MAC

4 clk

Multiplier
Xilinx LogiCORE IP

Increase area with mantissa size

8 clk

Accumulator
Xilinx LogiCORE IP

Increase latency with mantissa alignment

$$\sum_{j=0}^{N-1} h(j)W(j)$$