Low-Power Neural Network Accelerators: Advancements in Custom Floating-Point Techniques

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Universität Bremen

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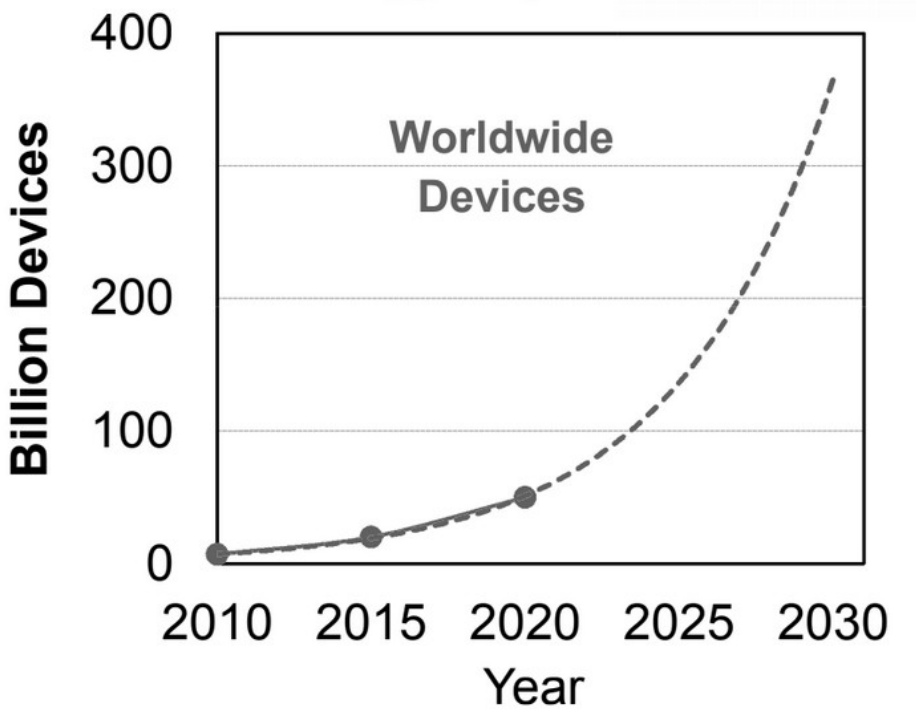
ITEM.IDS

Expansion of IoT and TinyML: Requirements, Accelerators, and Challenges

Internet-of-Things (IoT) in Smart Cities and Industry 4.0

Any device	Anybody	Anywhere	Any business	Any network	Anytime



Loh, Kou-Hung Lawrence. "1.2 Fertilizing AIoT from roots to leaves." In 2020 IEEE International Solid-State Circuits Conference-(ISSCC), pp. 15-21. IEEE, 2020.

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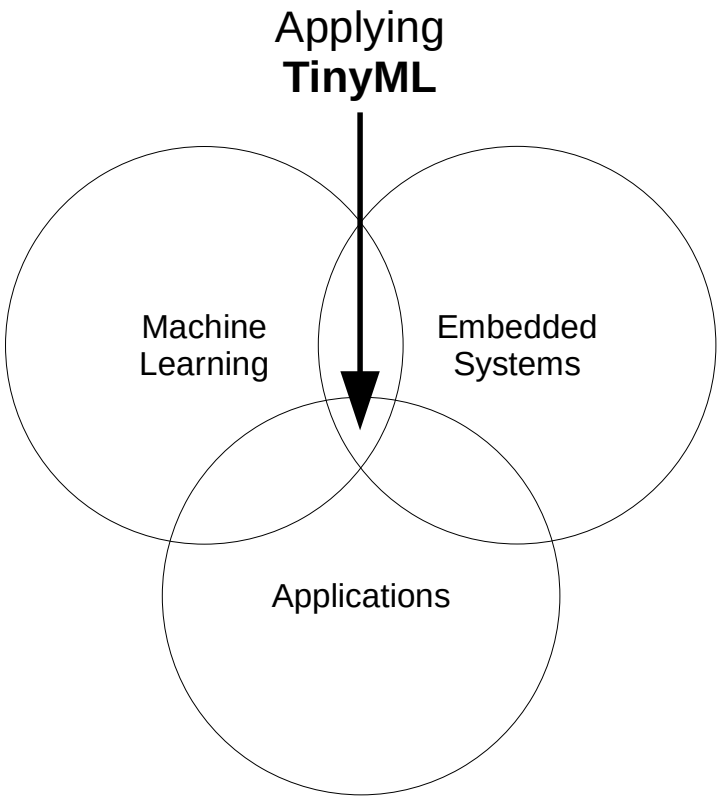

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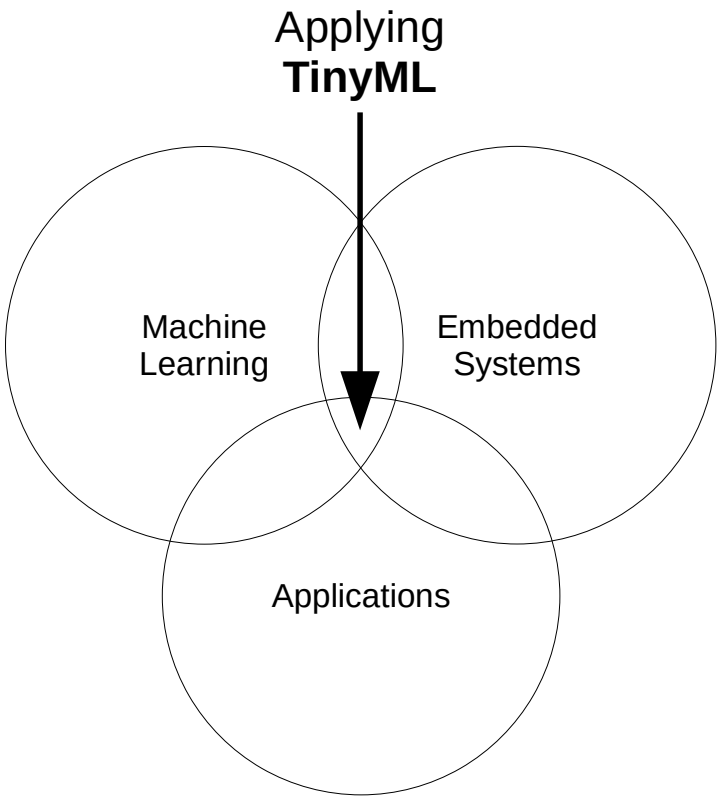

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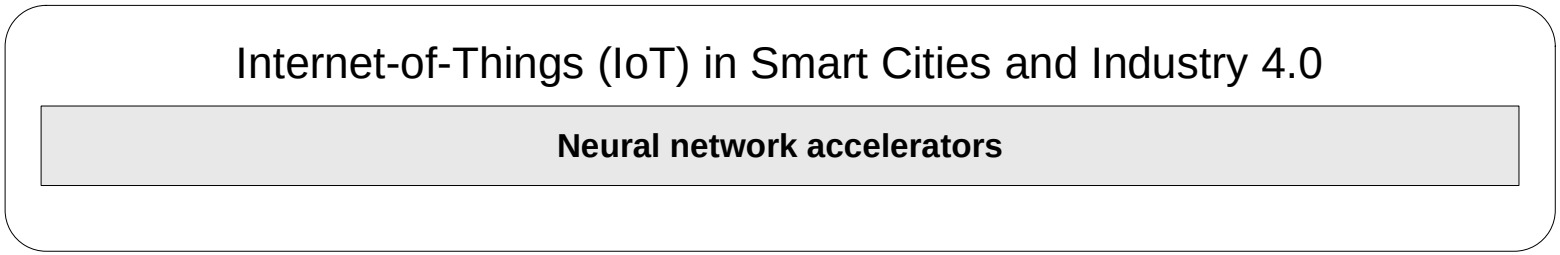

Aspects for long-term sustainability:

- Energy and resource efficiency
- Quality preservation
- Application versatility
- Platform compatibility
- On-device training

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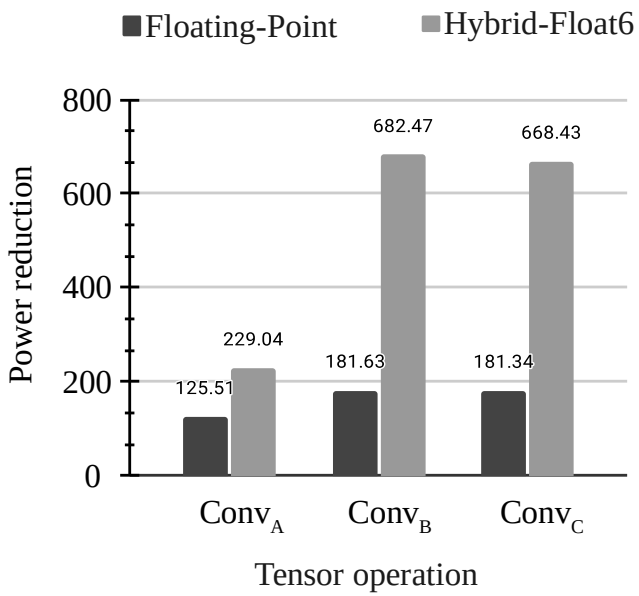
Power reduction relative to CPU



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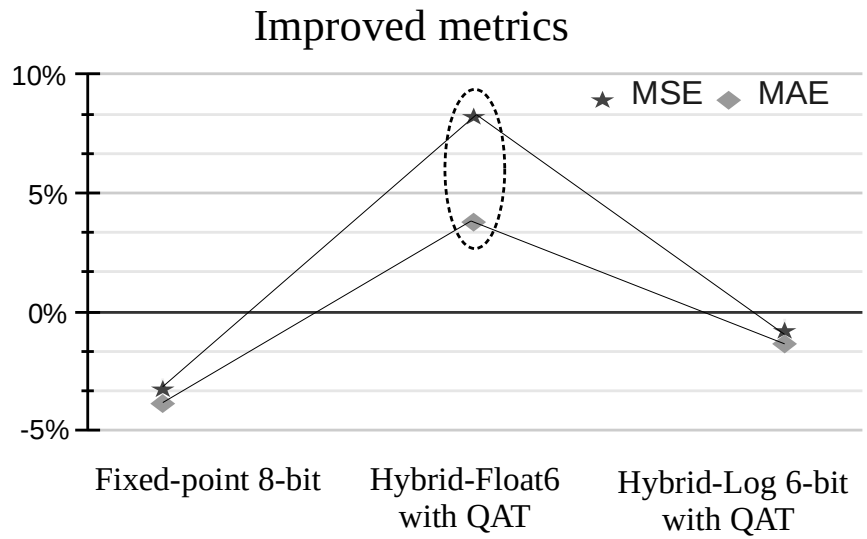

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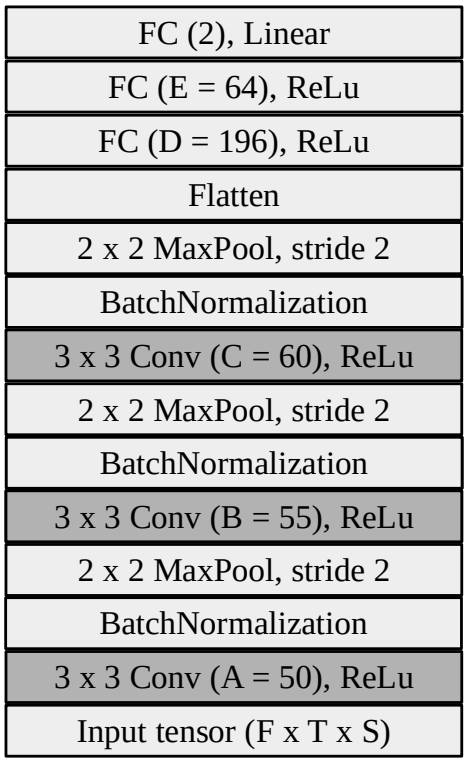

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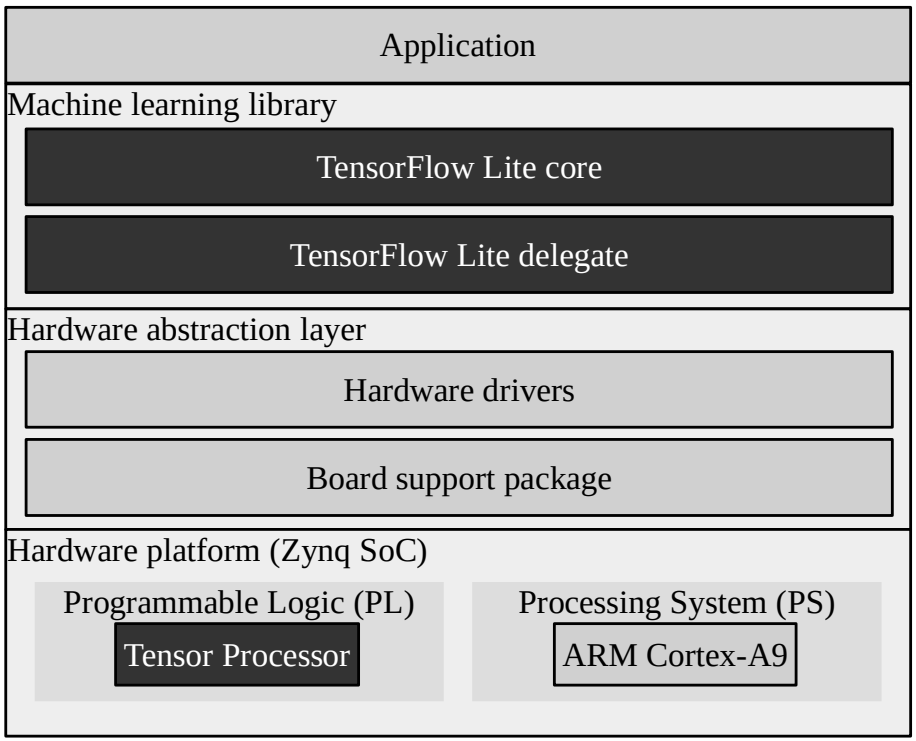

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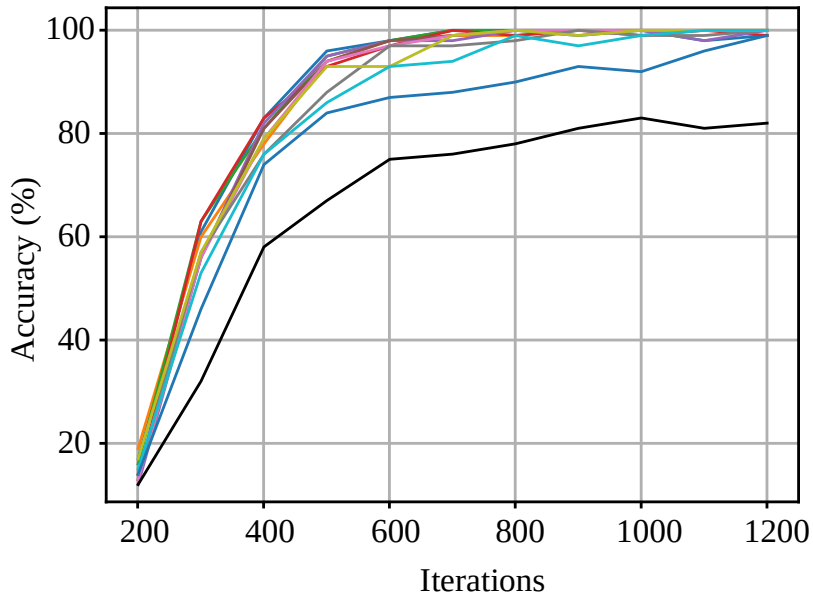
Iterative optimization



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Current state-of-the-art methods:

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Extreme quantization
Fails to adequately meet fundamental aspects, particularly in complex problems and mission-critical applications

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Current state-of-the-art methods:

Extreme quantization
Fails to adequately meet fundamental aspects, particularly in complex problems and mission-critical applications

Fixed precision
Fails to adequately adapt to the ongoing technological shift towards on-device training

Goal and Objectives

- **Goal**: To establish a future-proof neural network acceleration approach that supports inference and facilitates on-device training for TinyML applications.

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  - Conduct design exploration
  - Evaluate deployment, performance and impact

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  - Investigate optimizations for low-precision floating-point computation
  - Conduct design exploration
  - Evaluate deployment, performance and impact
  - Ensure cross-platform compatibility

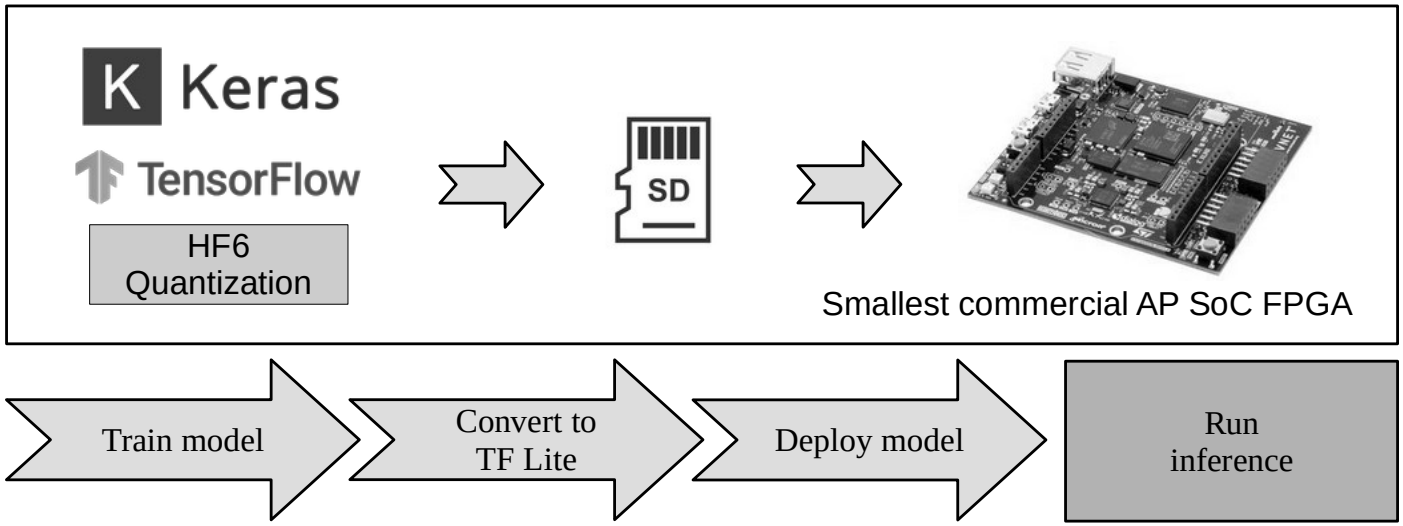
Outline

Trans-Precision Neural Network Deployment for Low-Power Embedded Systems

The methodology efficiently deploys and accelerates floating-point neural networks on embedded systems, optimizing performance, energy consumption, and hardware utilization.

Characteristics:

- Streamlined hardware architecture
- Custom floating-point arithmetic
- Neural network execution without quantization processes



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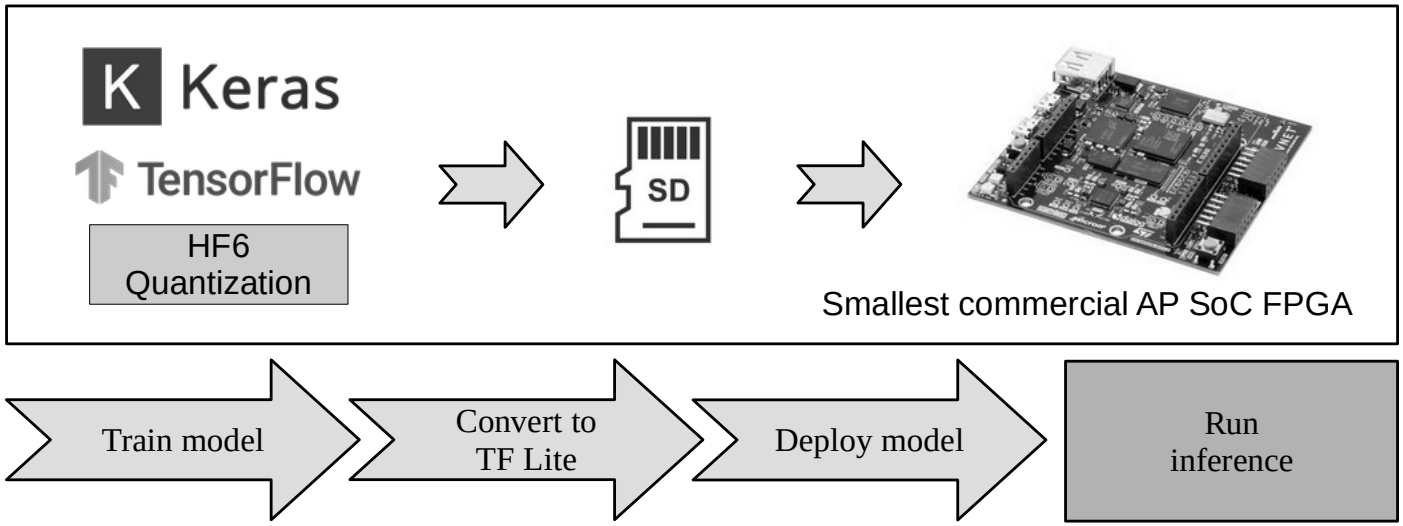

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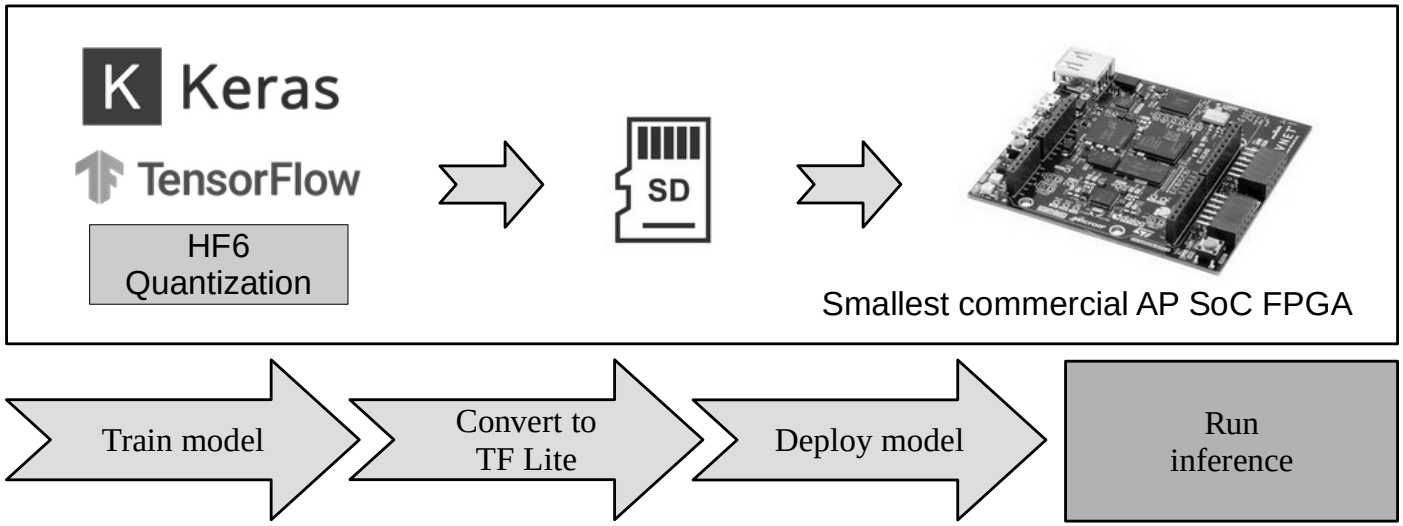

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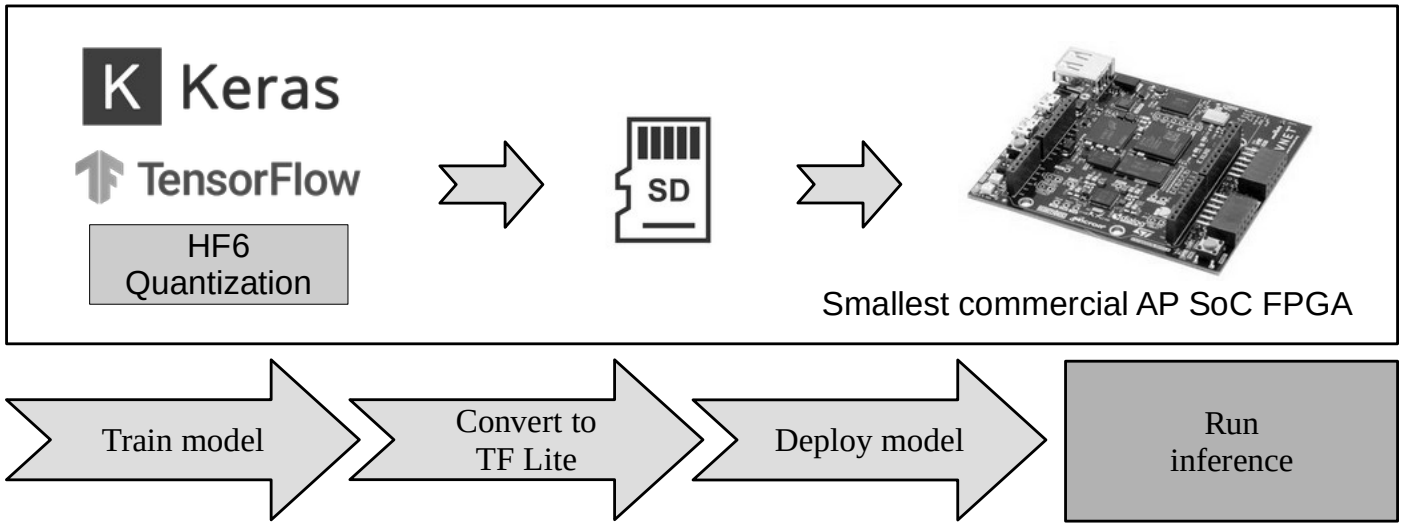

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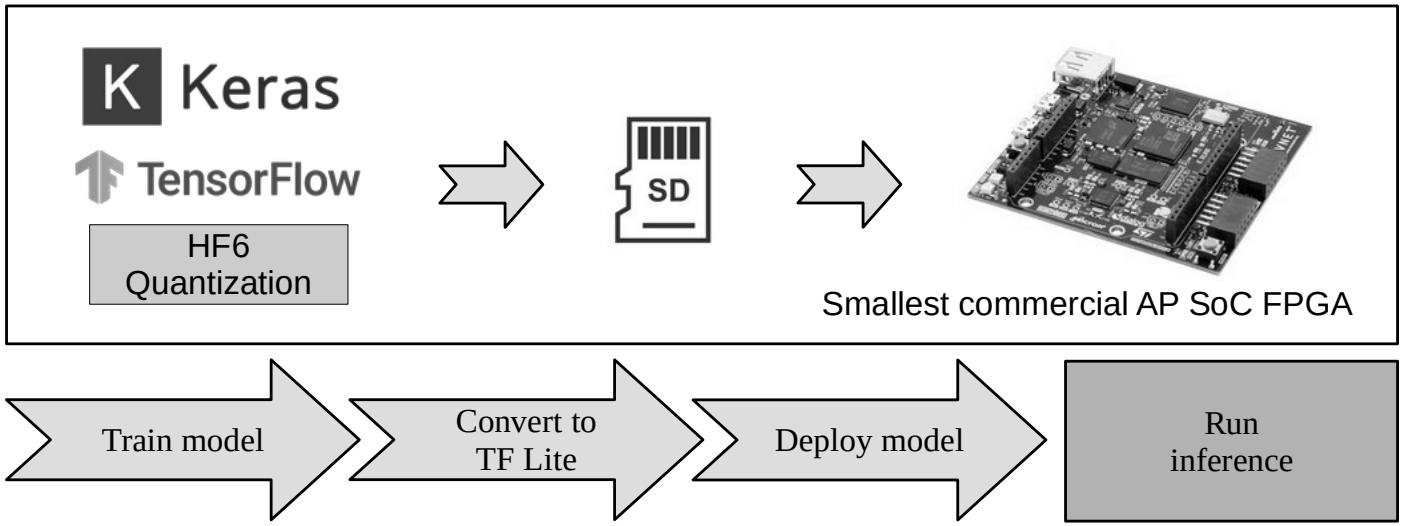

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Abstraction levels:

1. Model deployment
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3. Streamlined acceleration
4. Optimized processing

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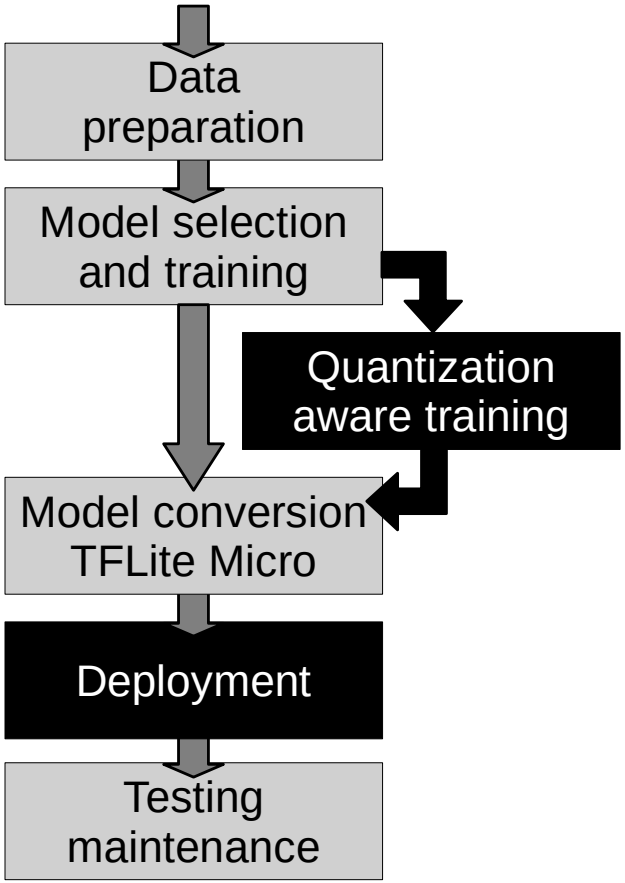

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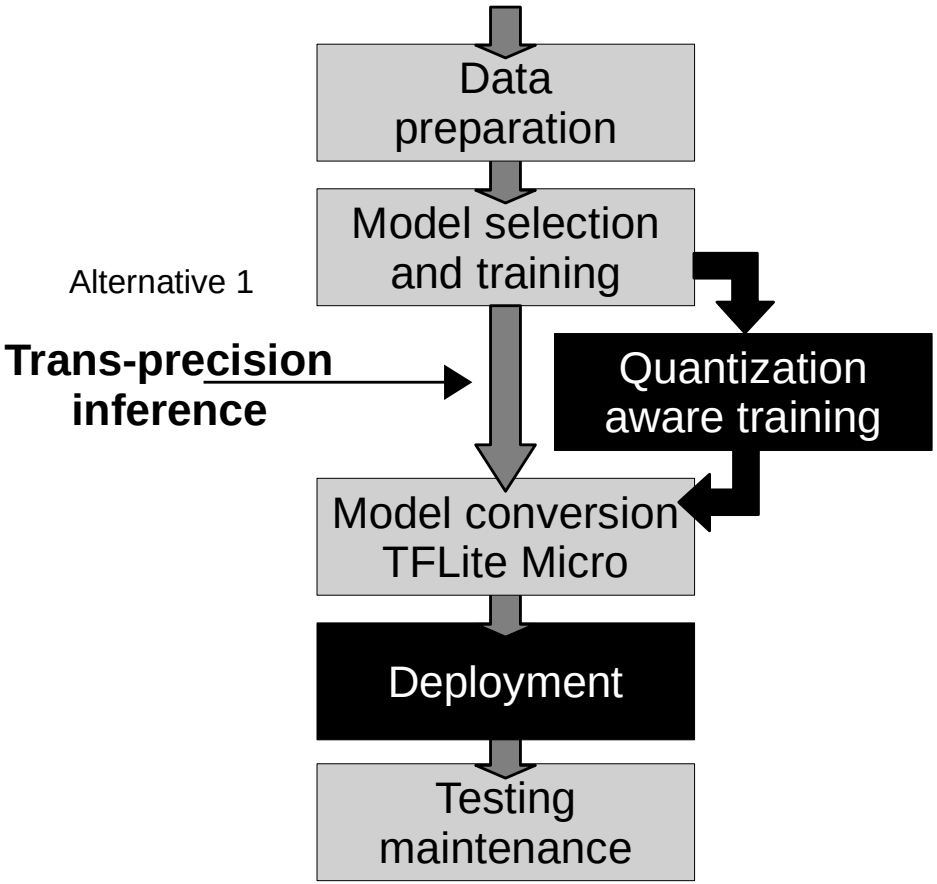

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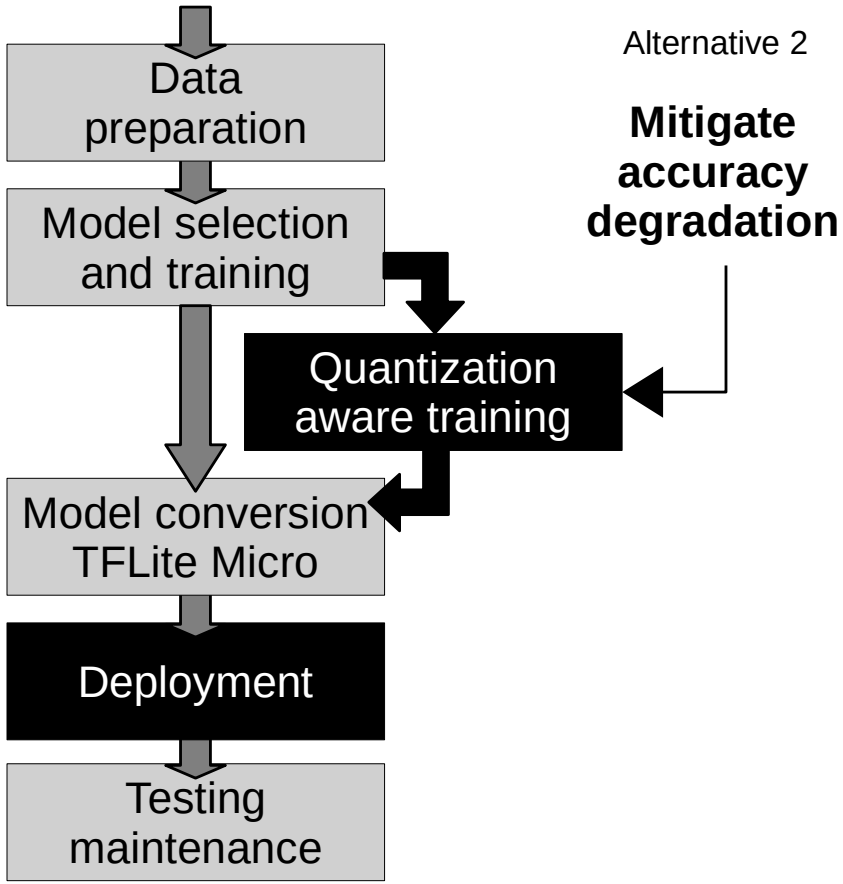

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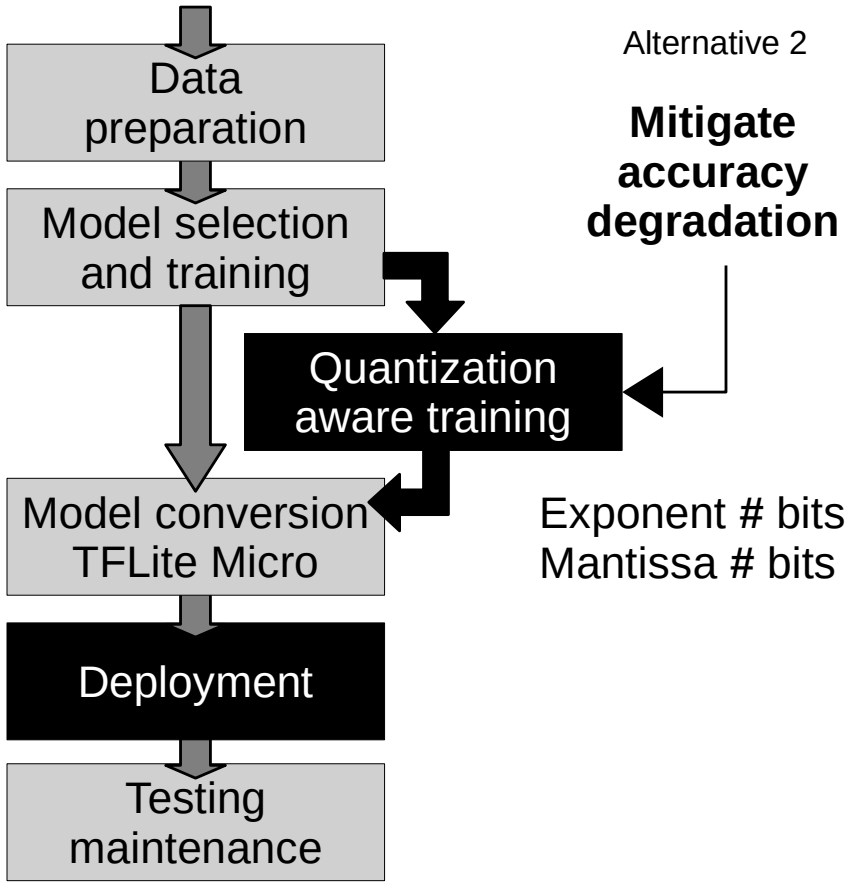

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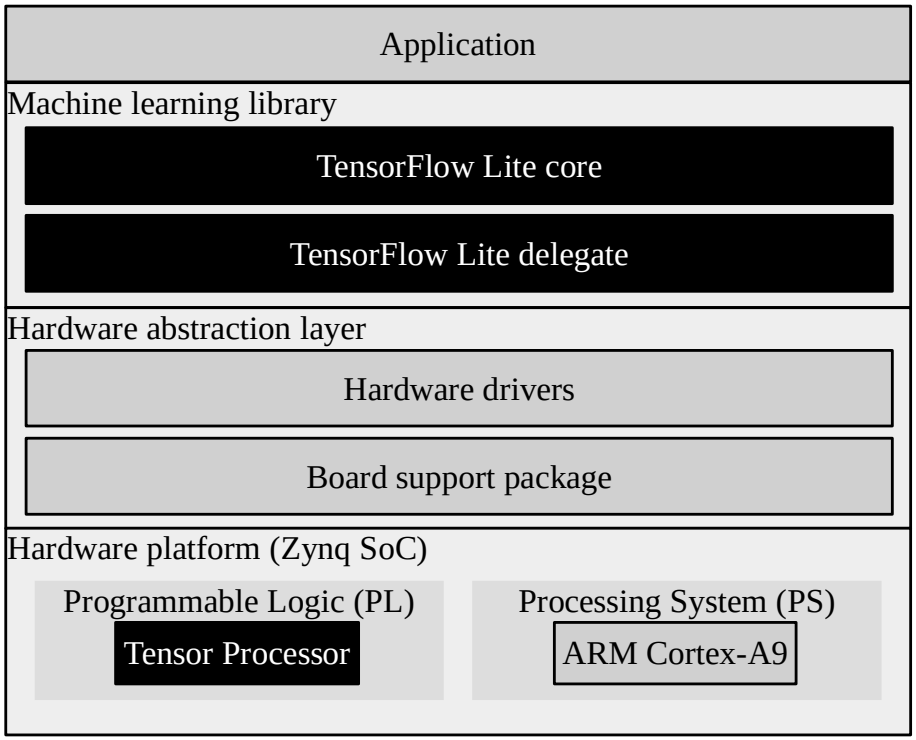

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Industry standard framework

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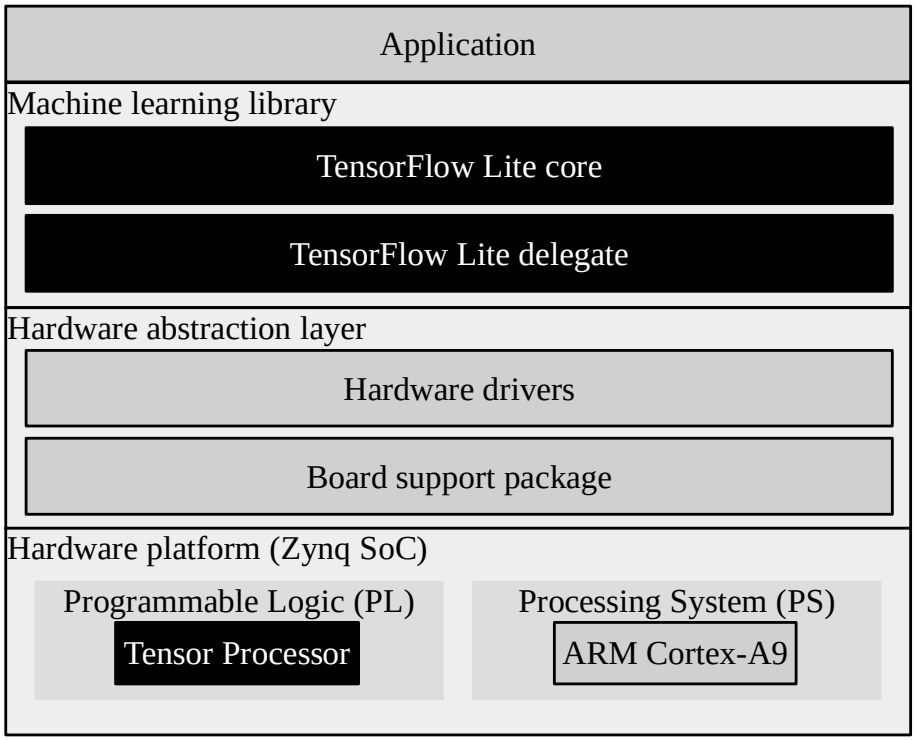

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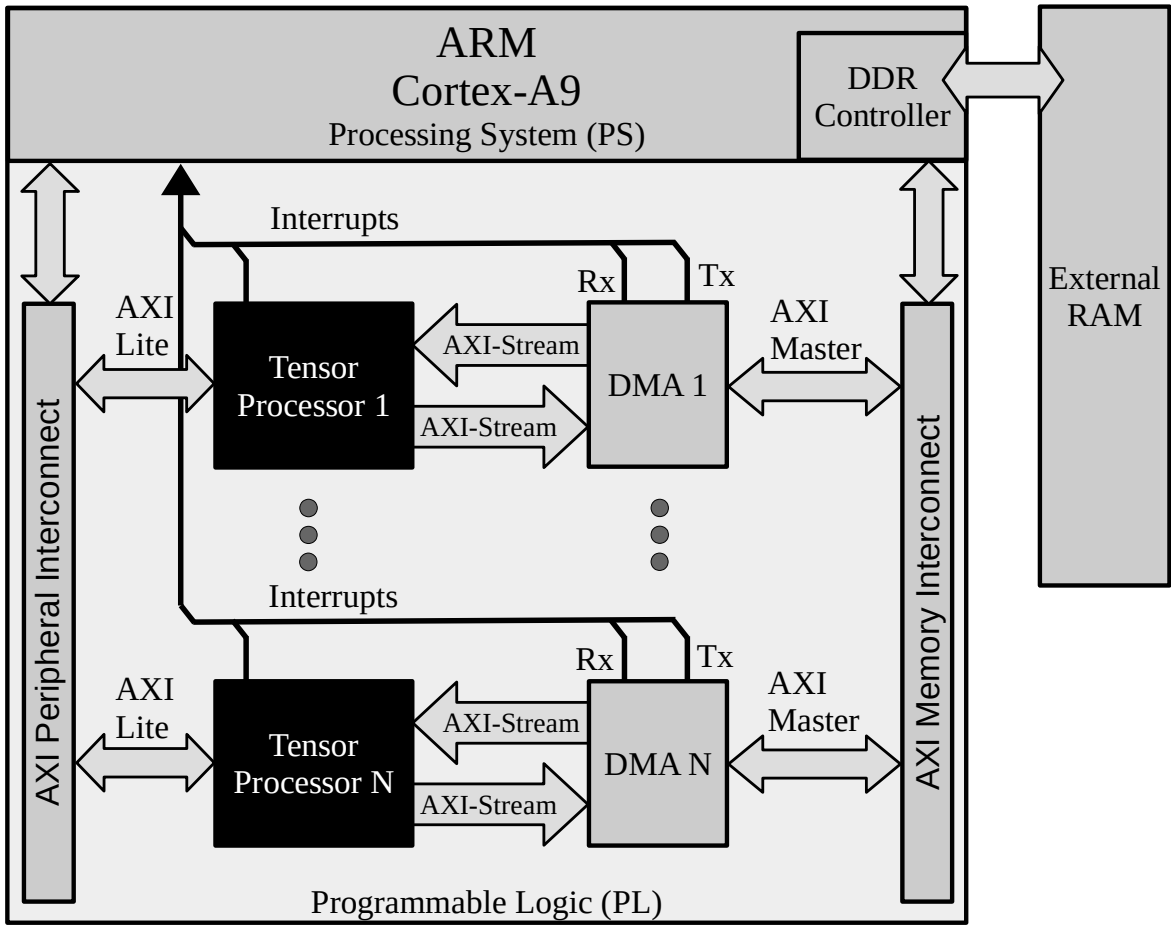

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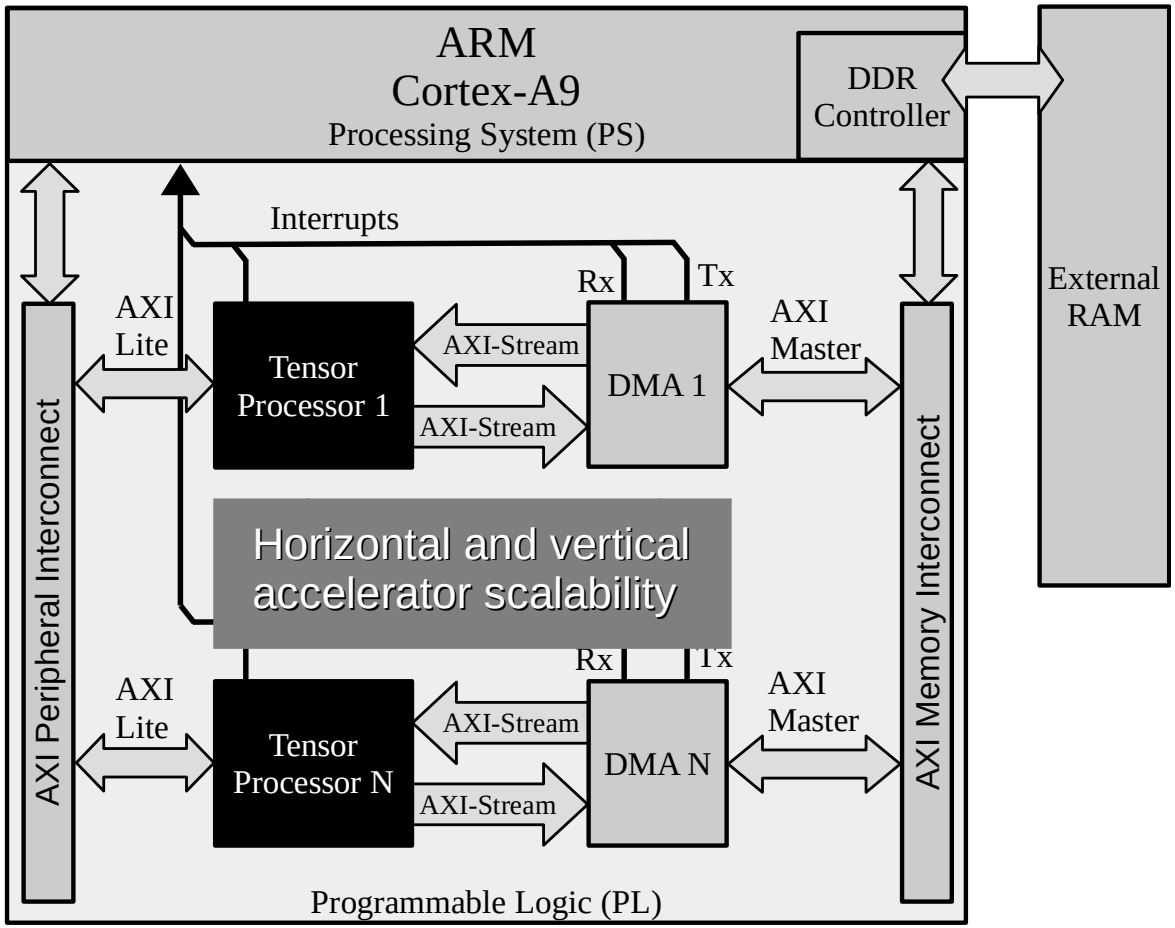

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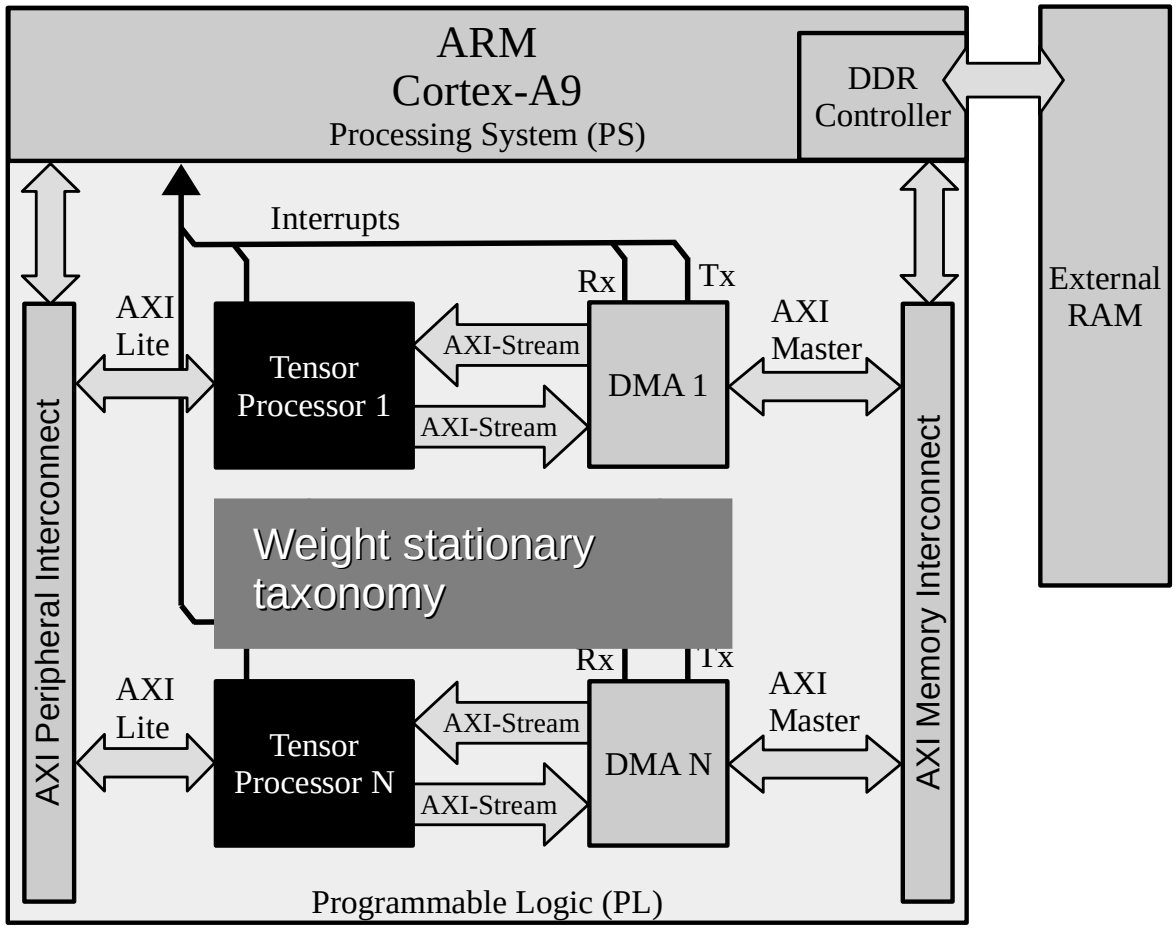

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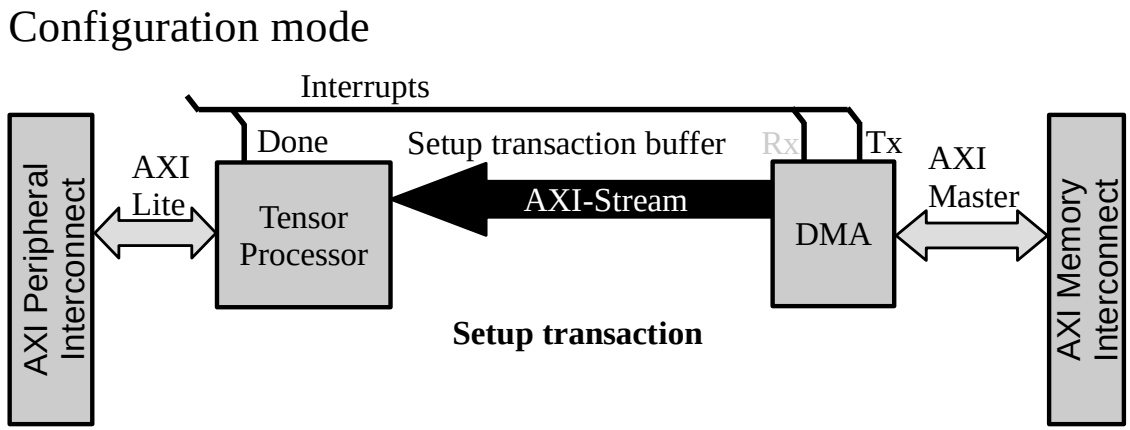

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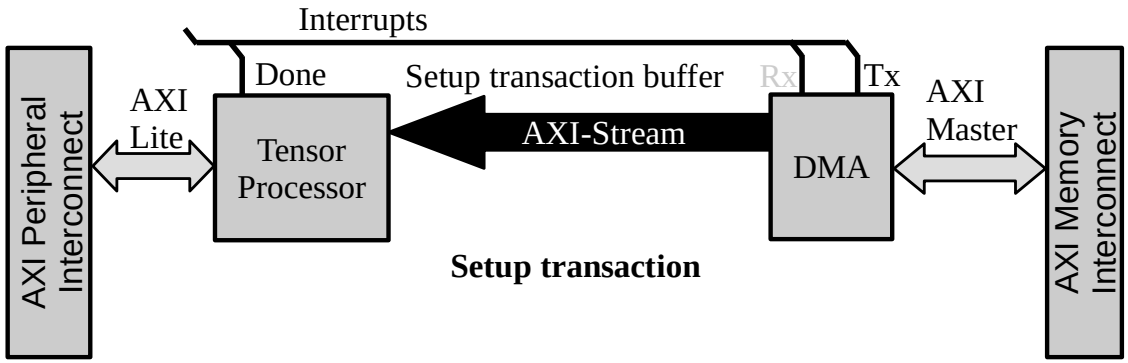
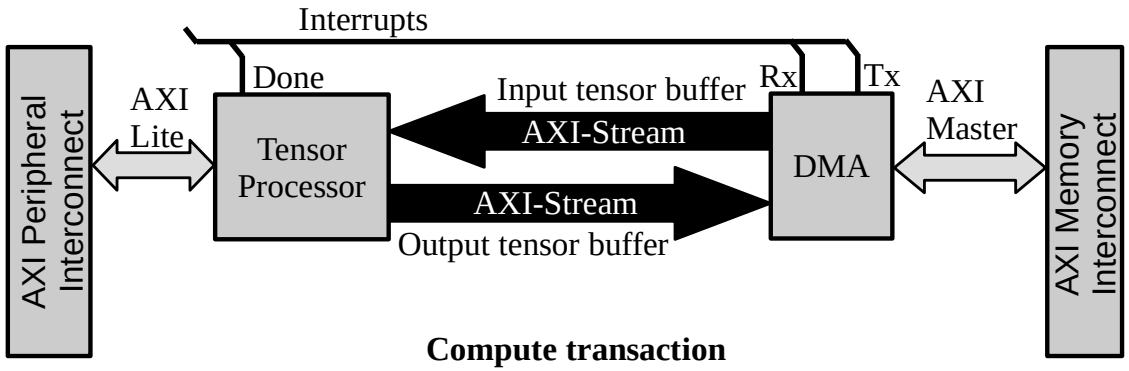


Execution mode



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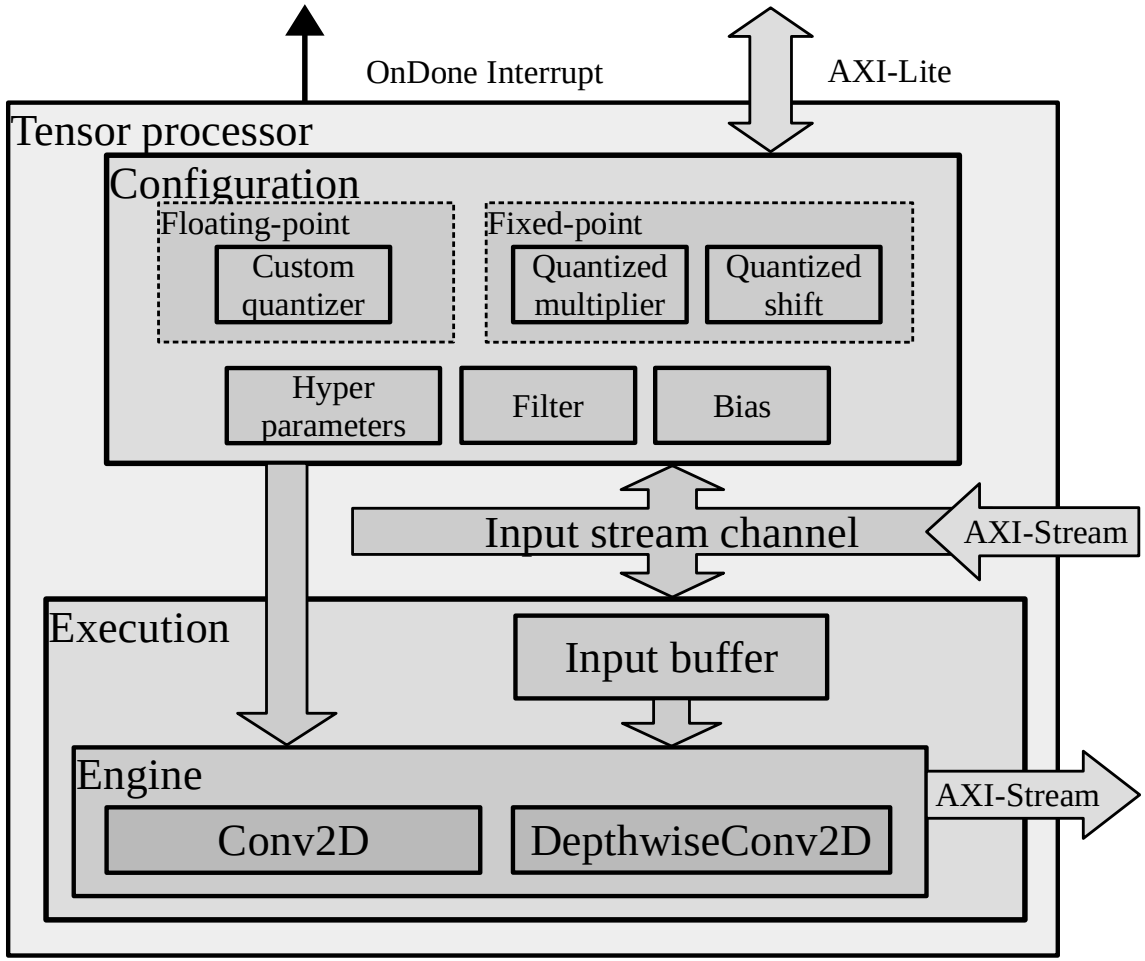

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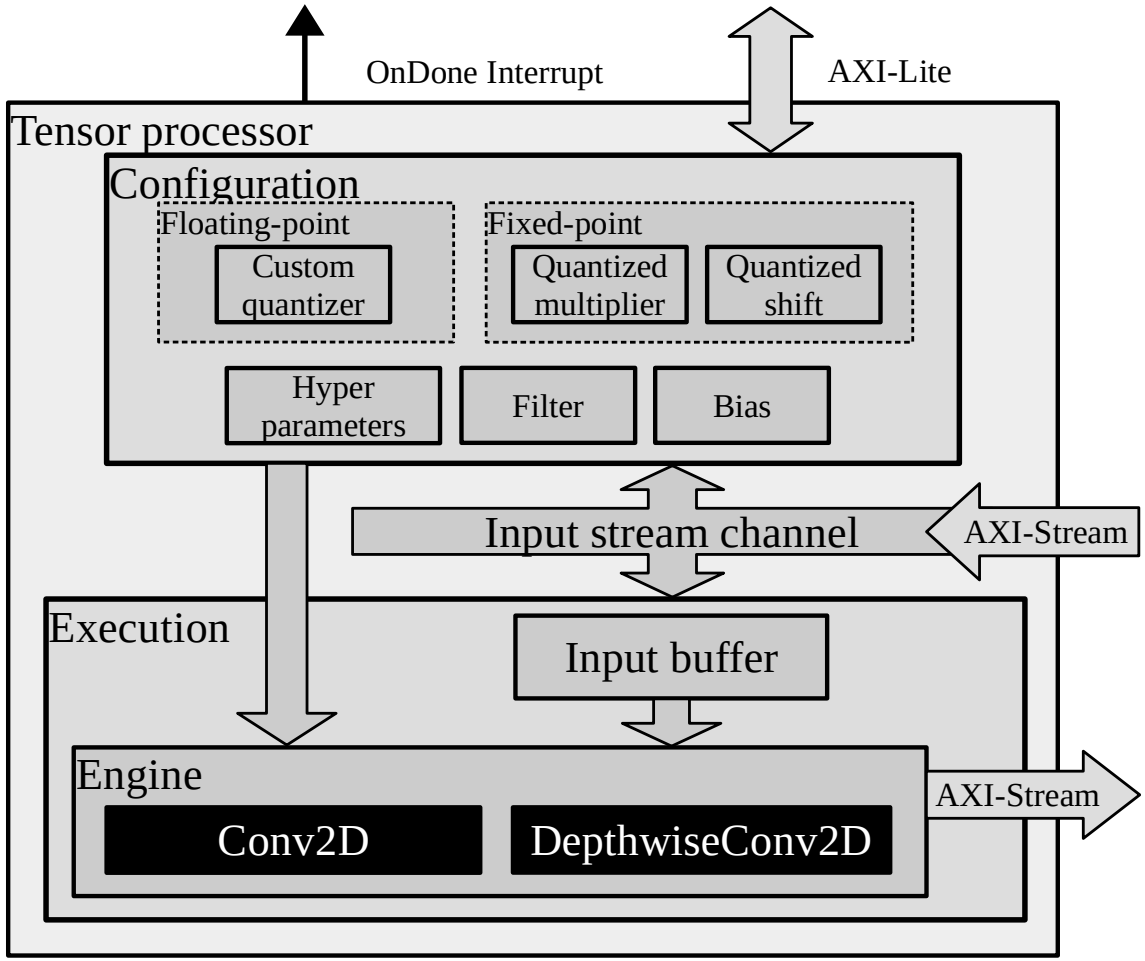

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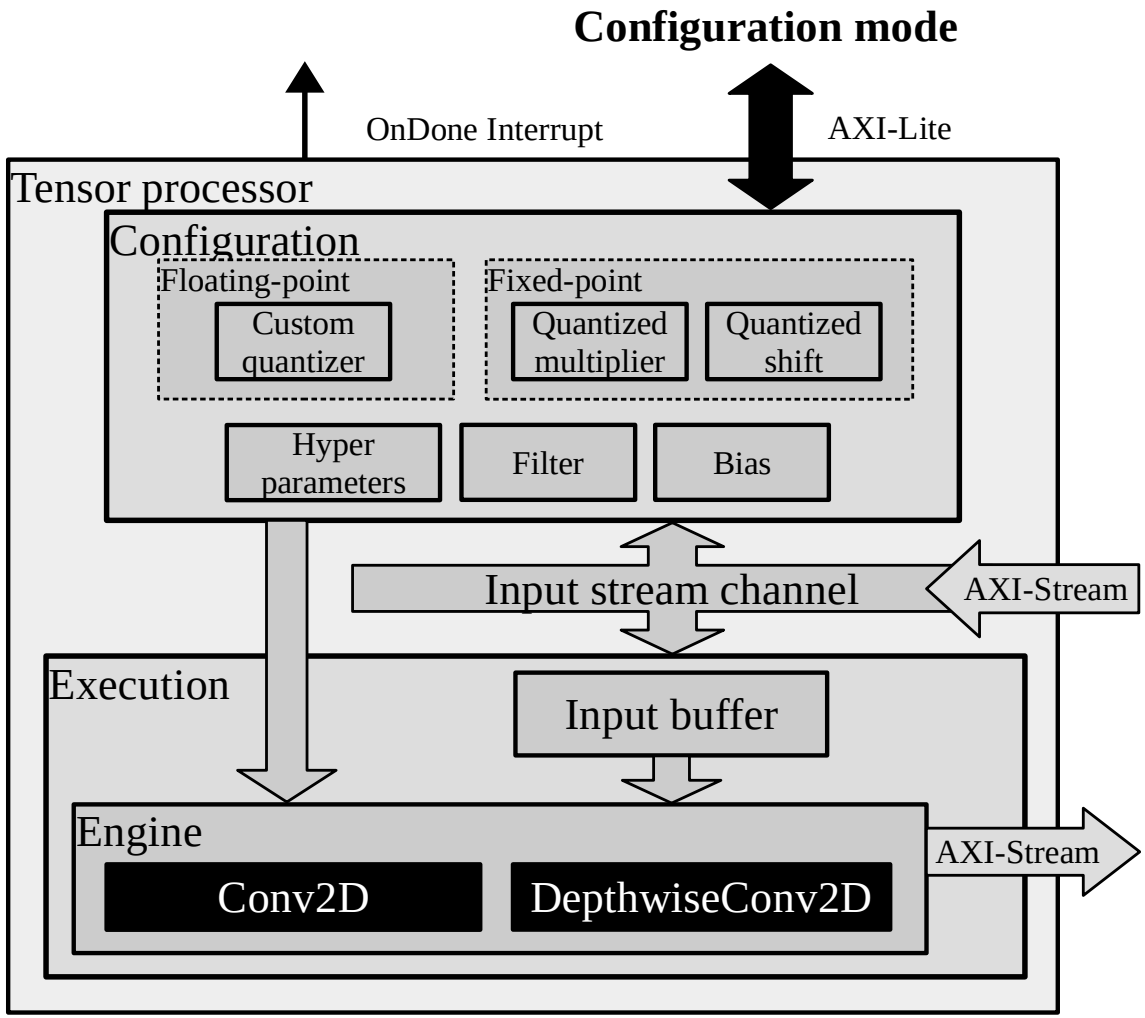

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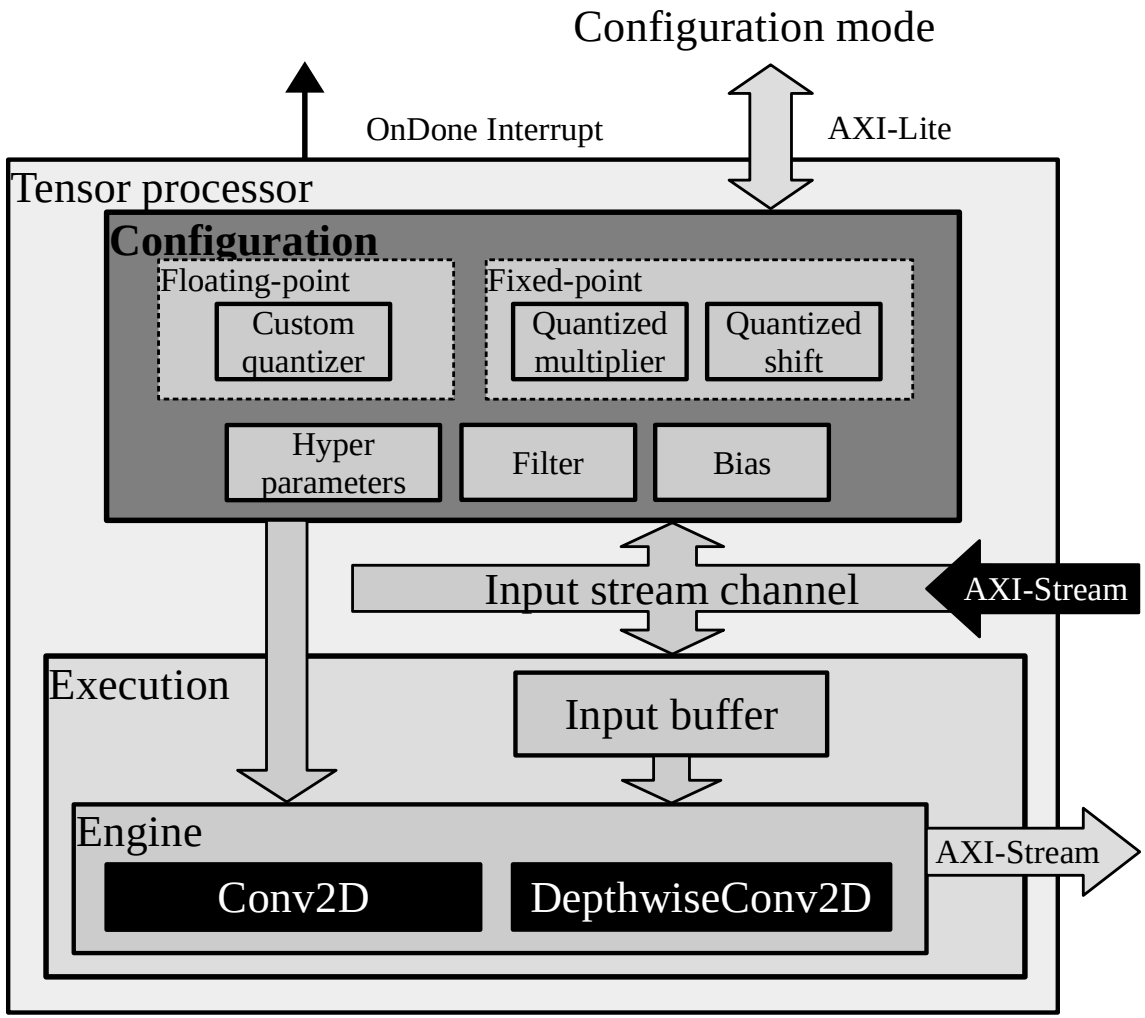

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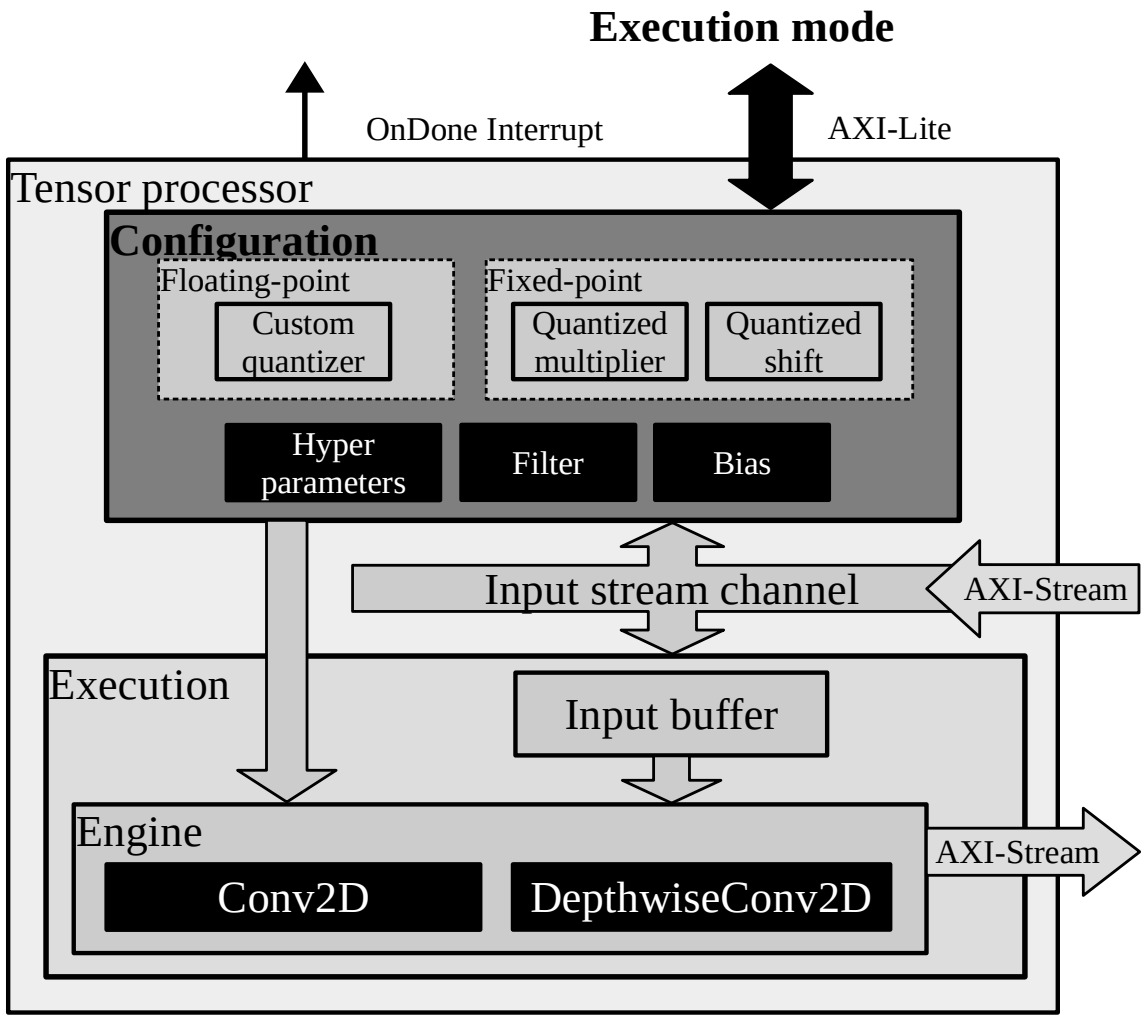

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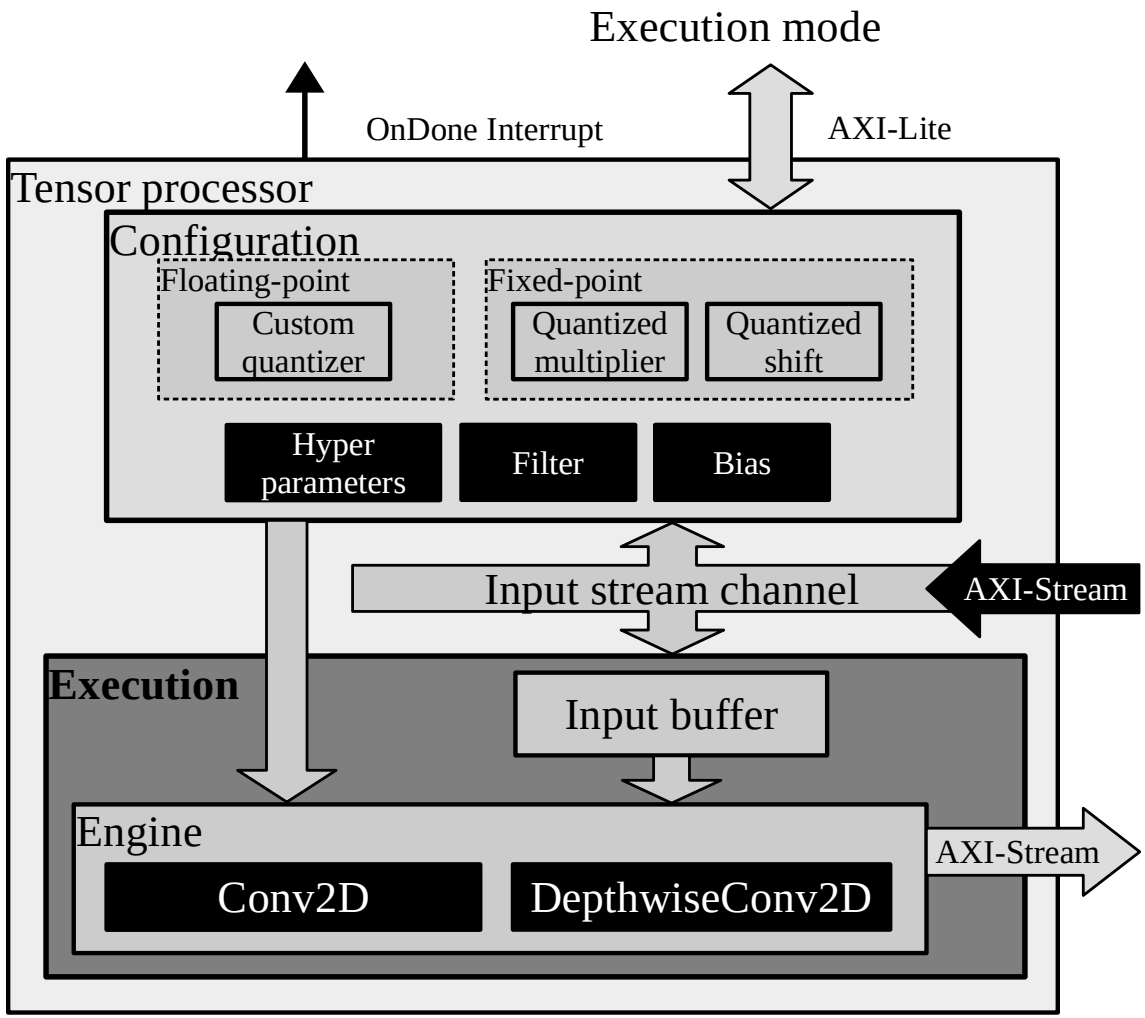

Trans-Precision Neural Network Deployment for Low-Power Embedded Systems

The methodology efficiently deploys and accelerates floating-point neural networks on embedded systems, optimizing performance, energy consumption, and hardware utilization.

Abstraction levels:

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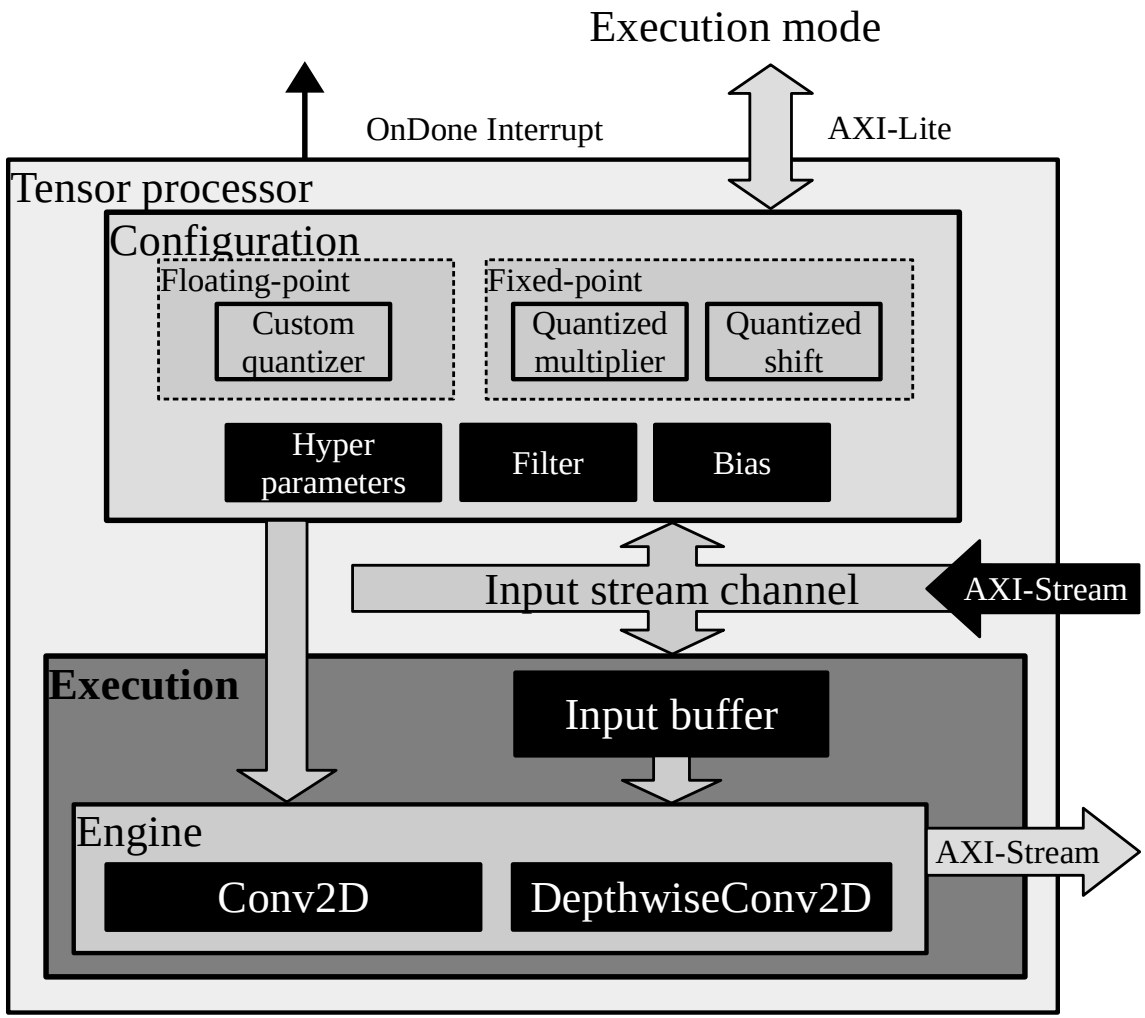

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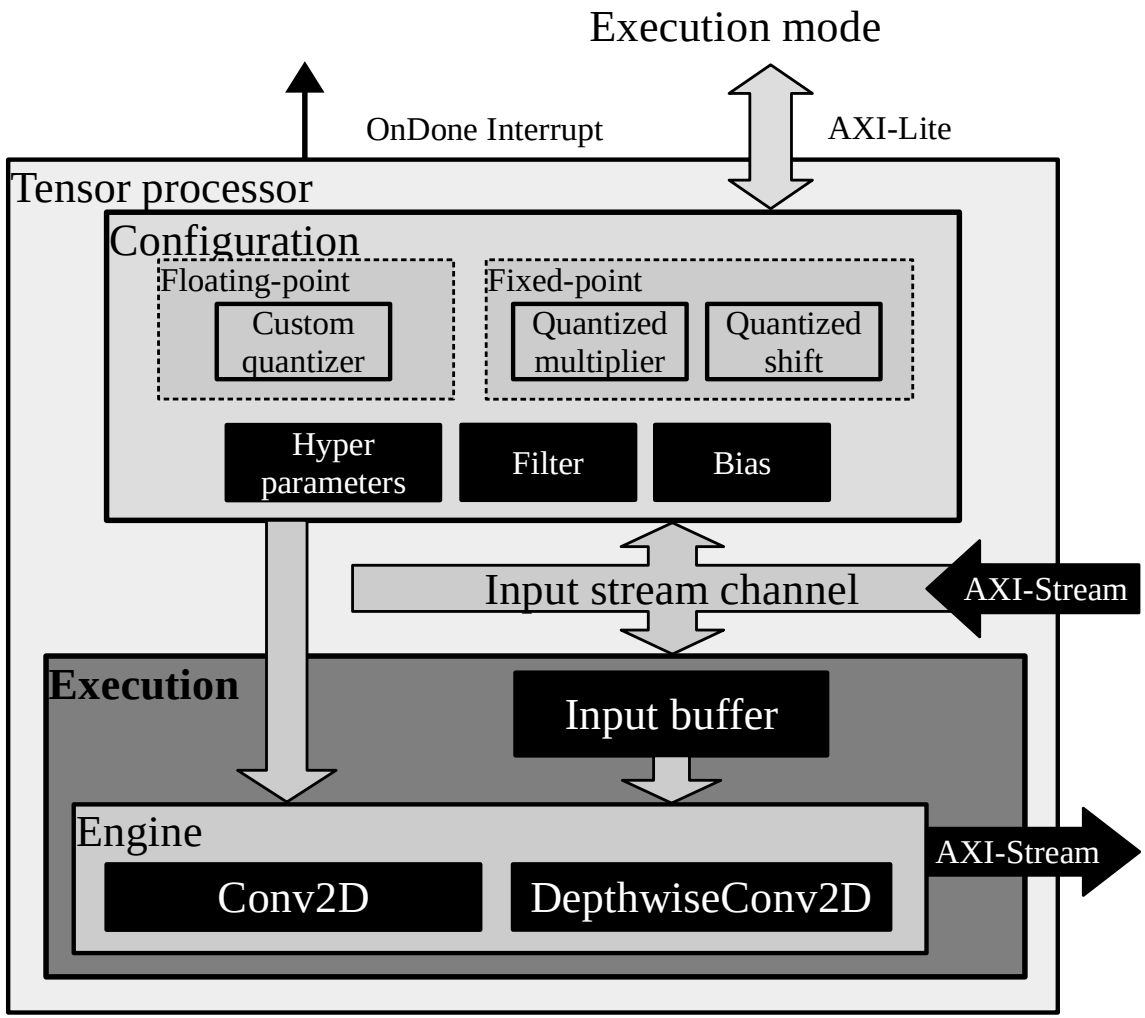

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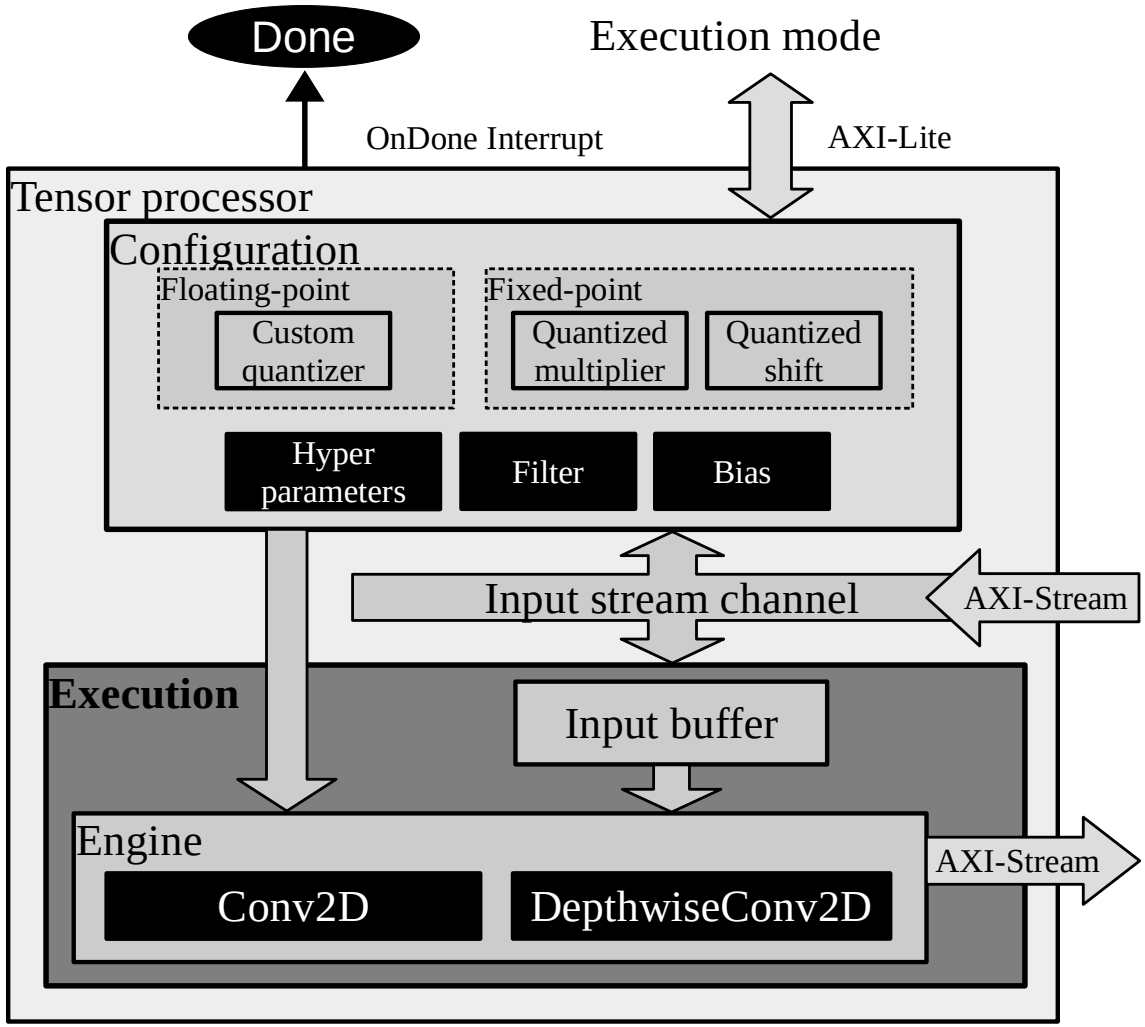

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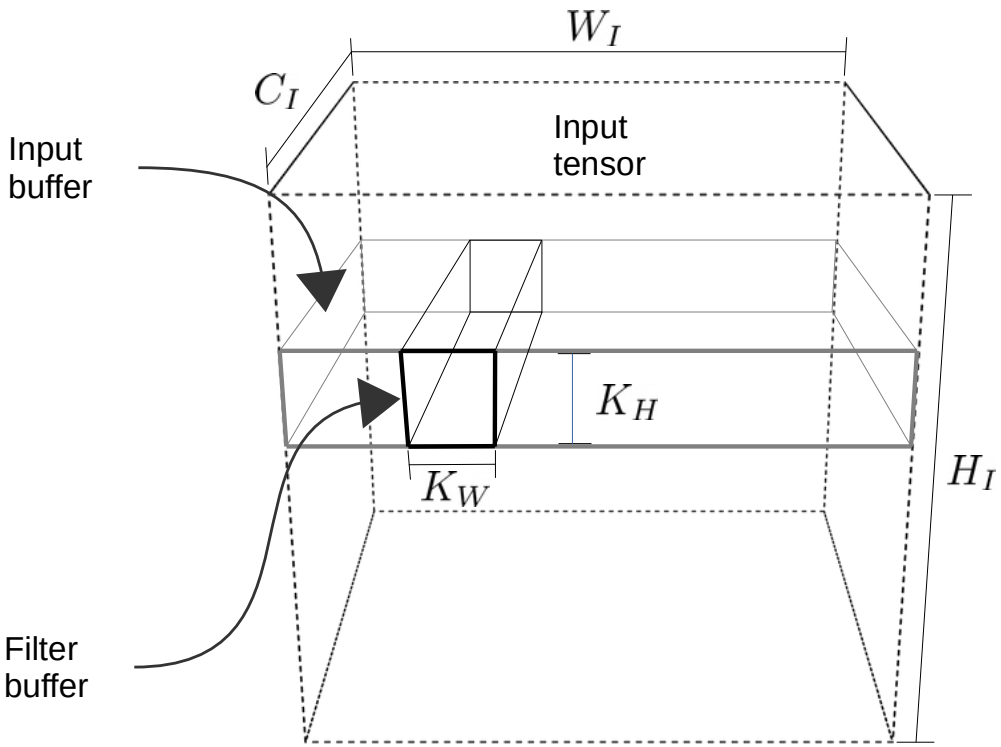

$$Conv2D\,(W,b,h)_{i,j,o} = \sum_{k,l,m}^{K,L,M} h_{(i+k,j+l,m)} W_{(o,k,l,m)} + b_o$$

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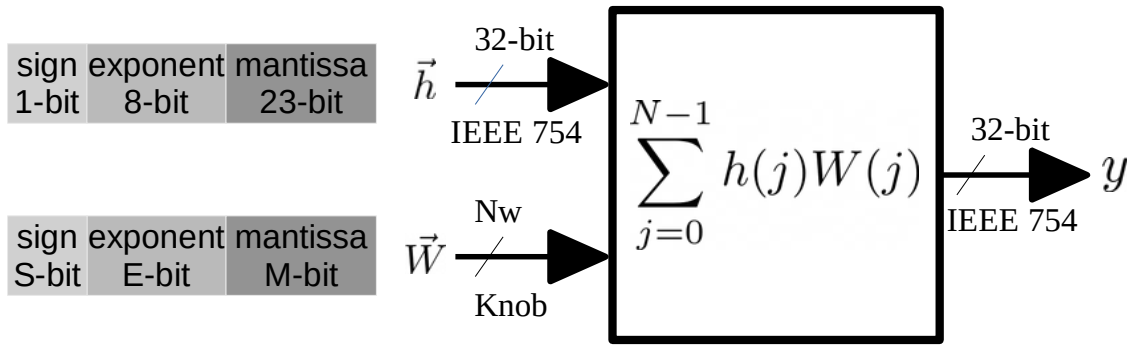
Multiply-Accumulate Unit
Hybrid Custom floating-point computation



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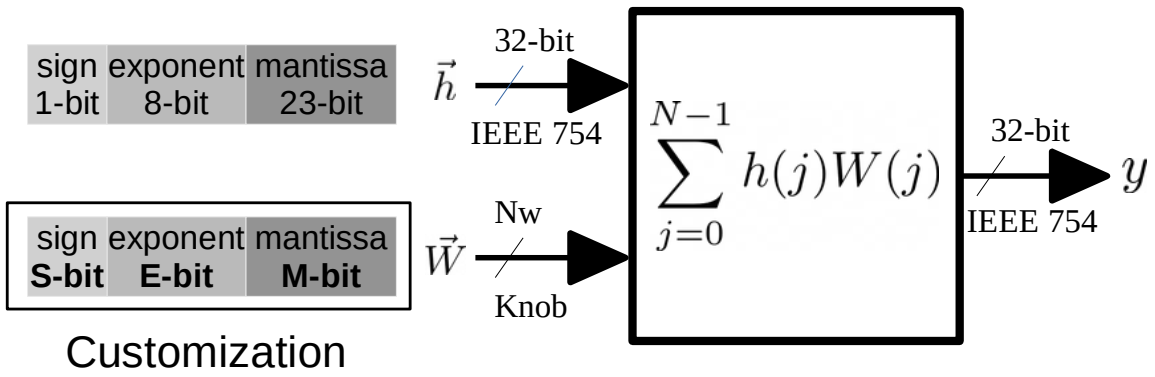

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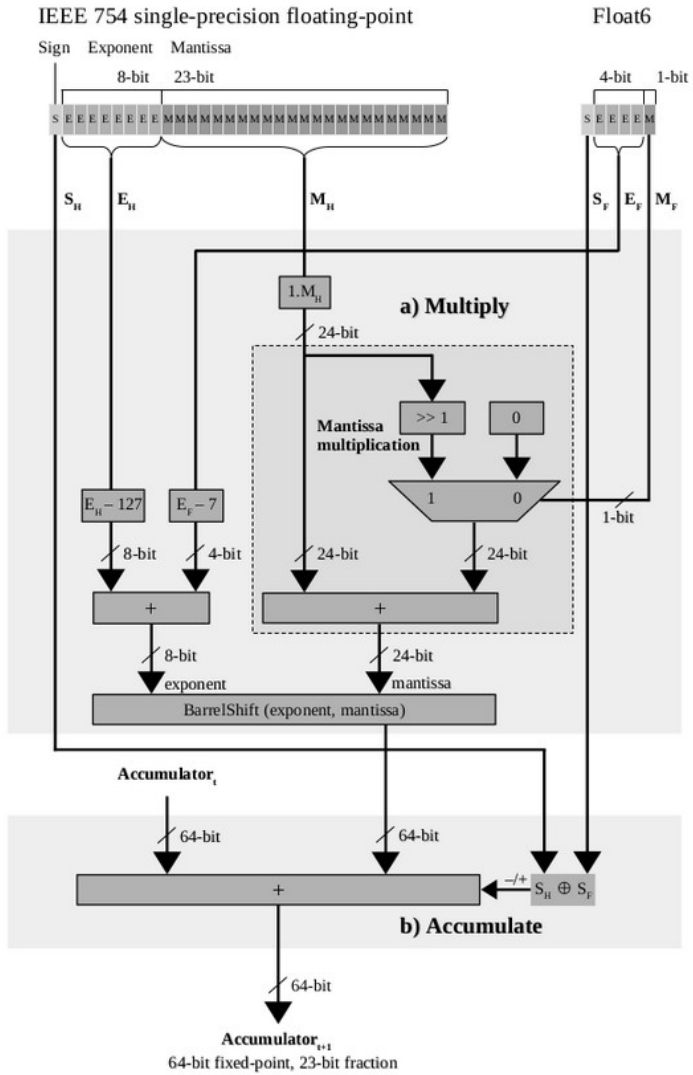
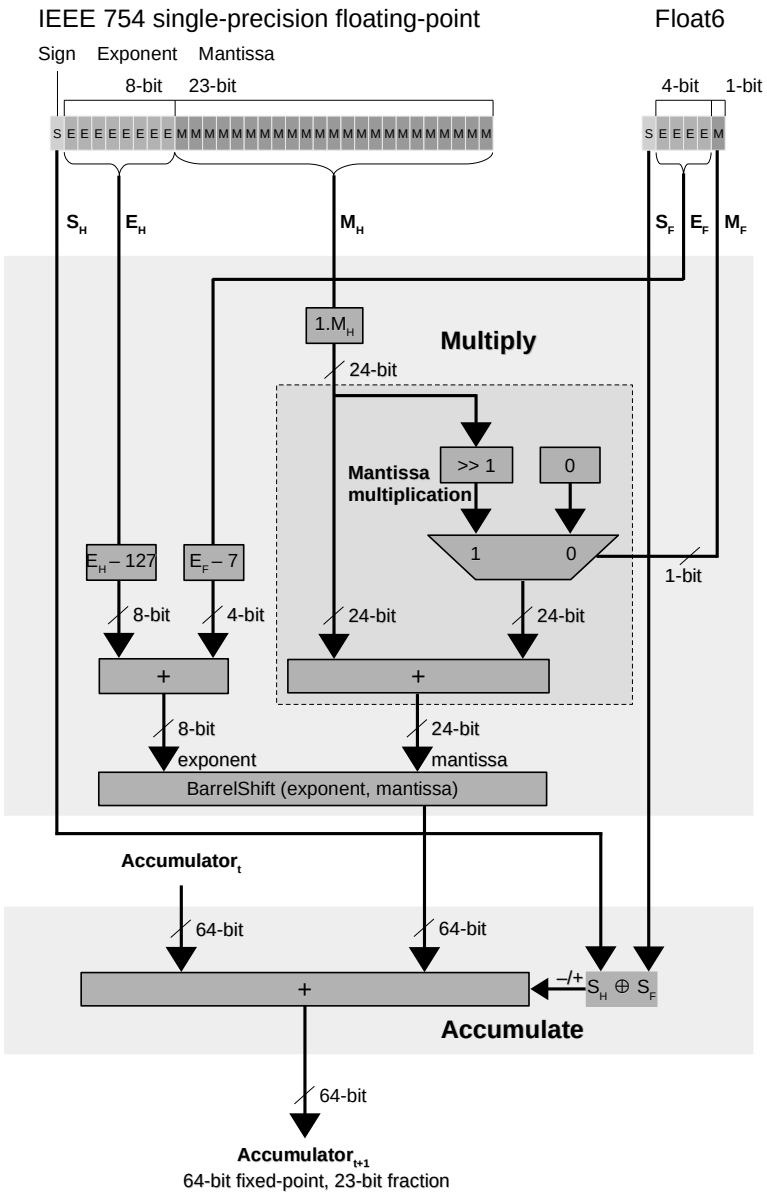


Hybrid Custom Floating-Point Multiply-Accumulate Unit

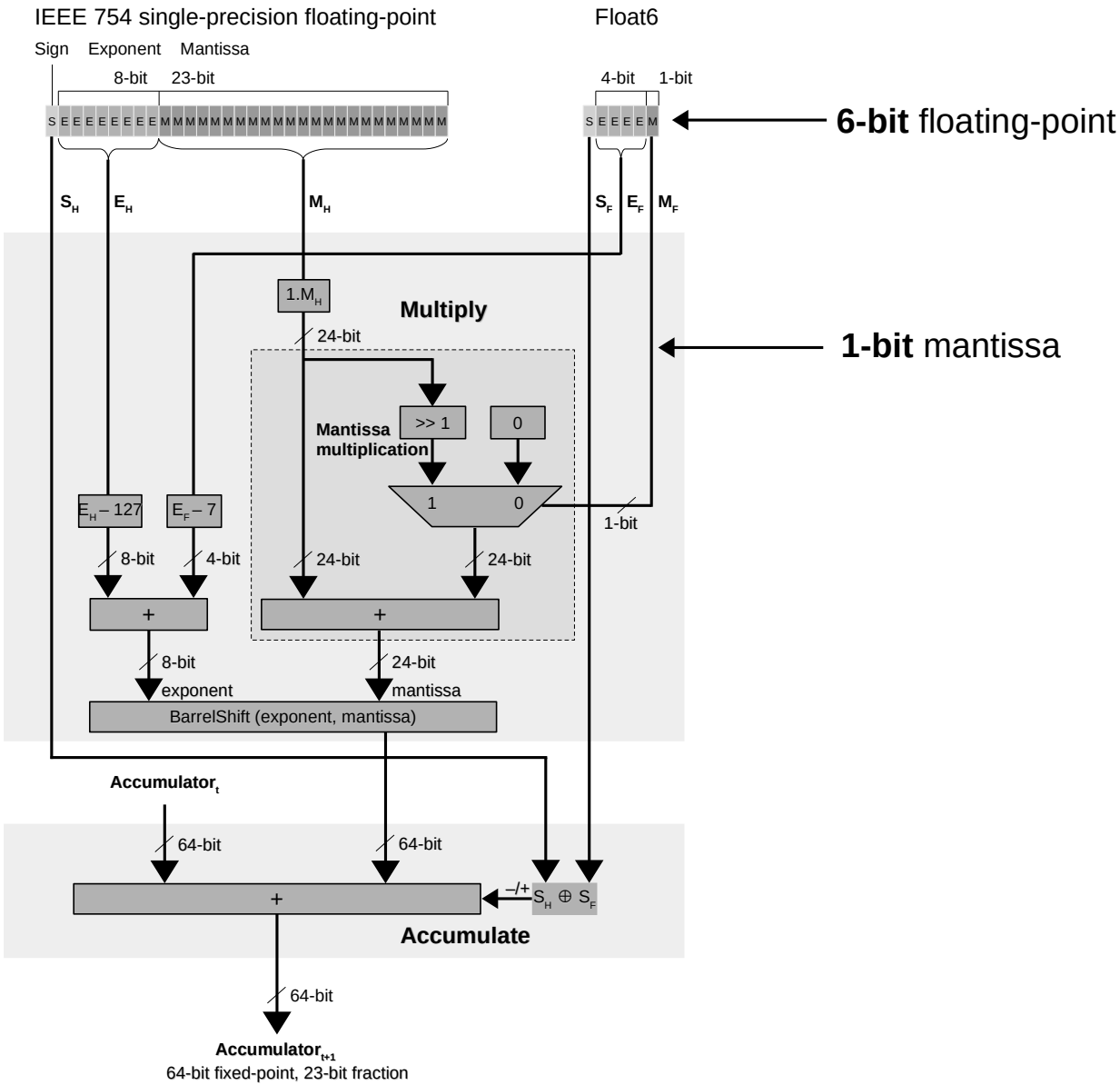


Custom Floating-Point MAC Designs

Hybrid Custom Floating-Point Multiply-Accumulate Unit

Vector dot-product:

- Multiplication
- Accumulation



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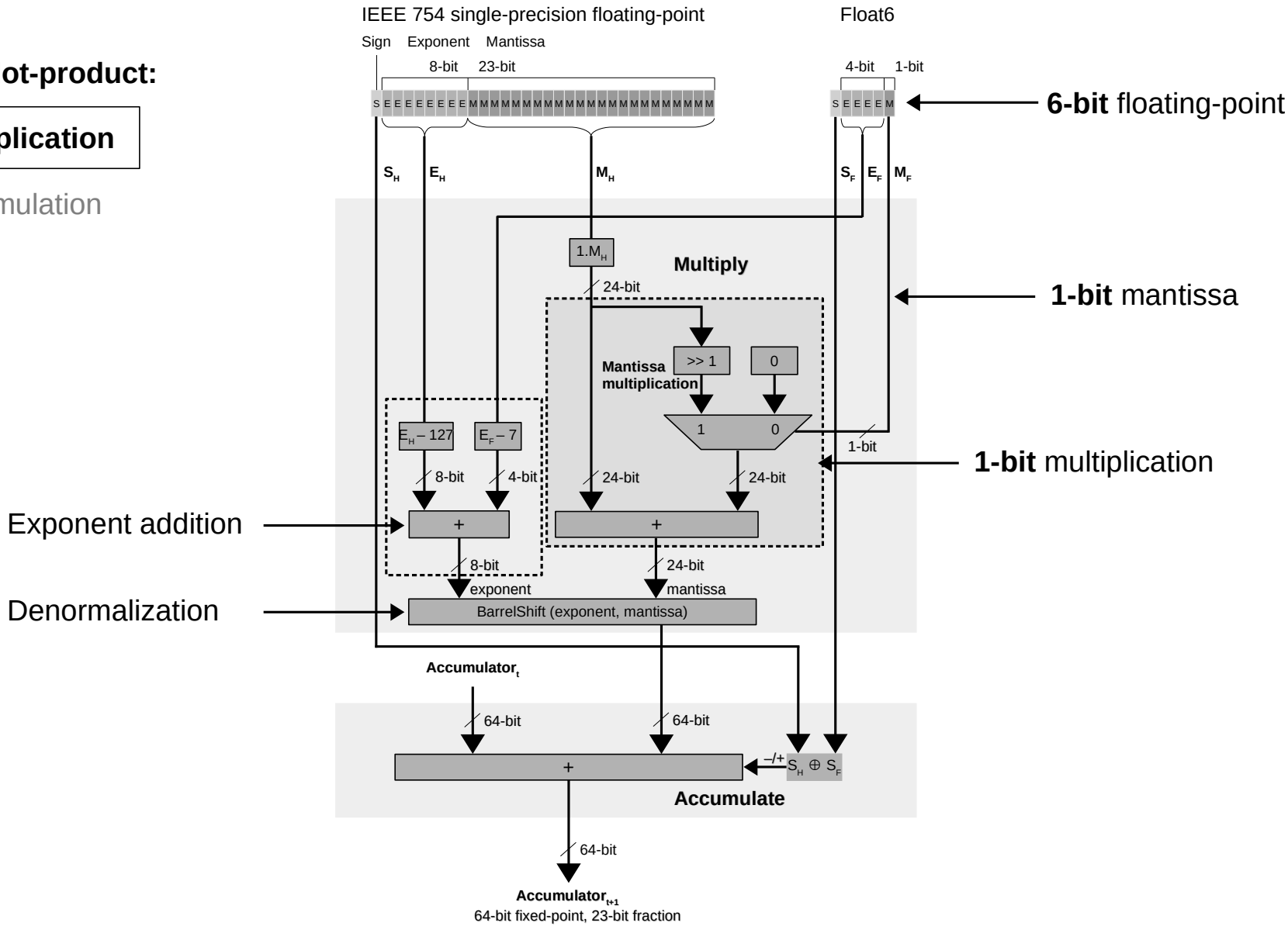

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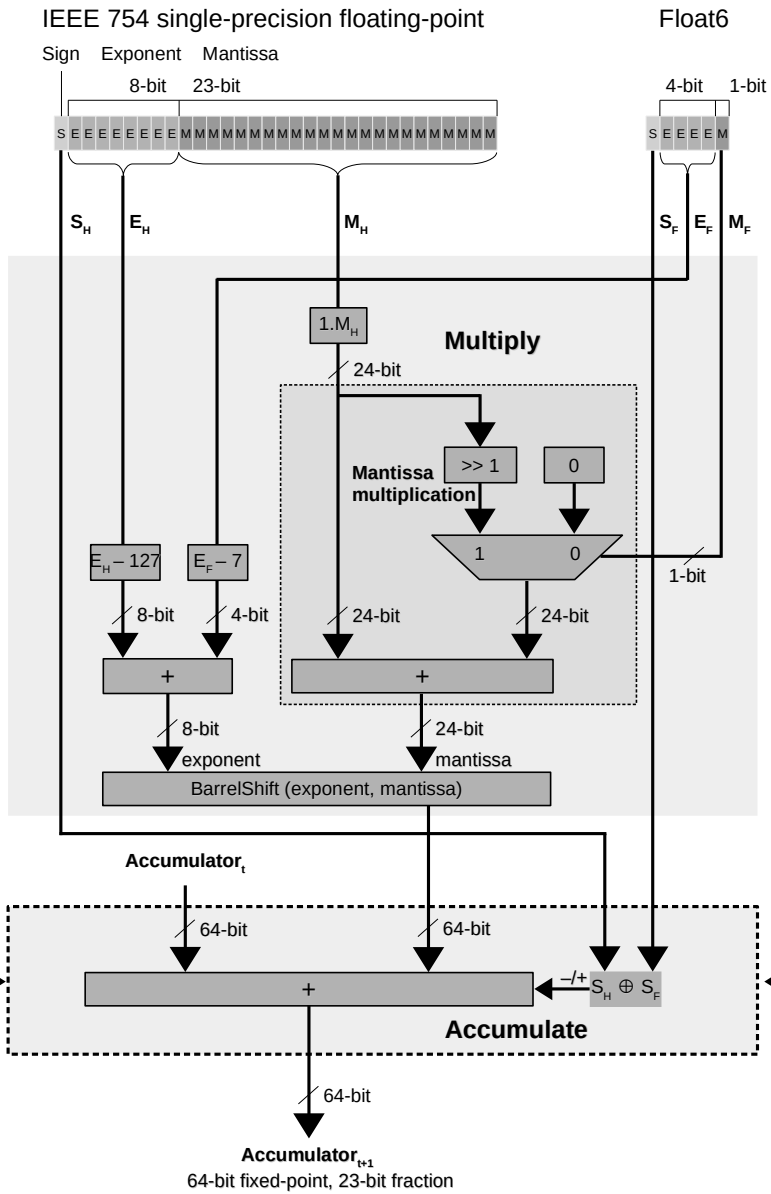

Denormalized accumulation →

← **64-bit** integer accumulation

Custom Floating-Point MAC Designs

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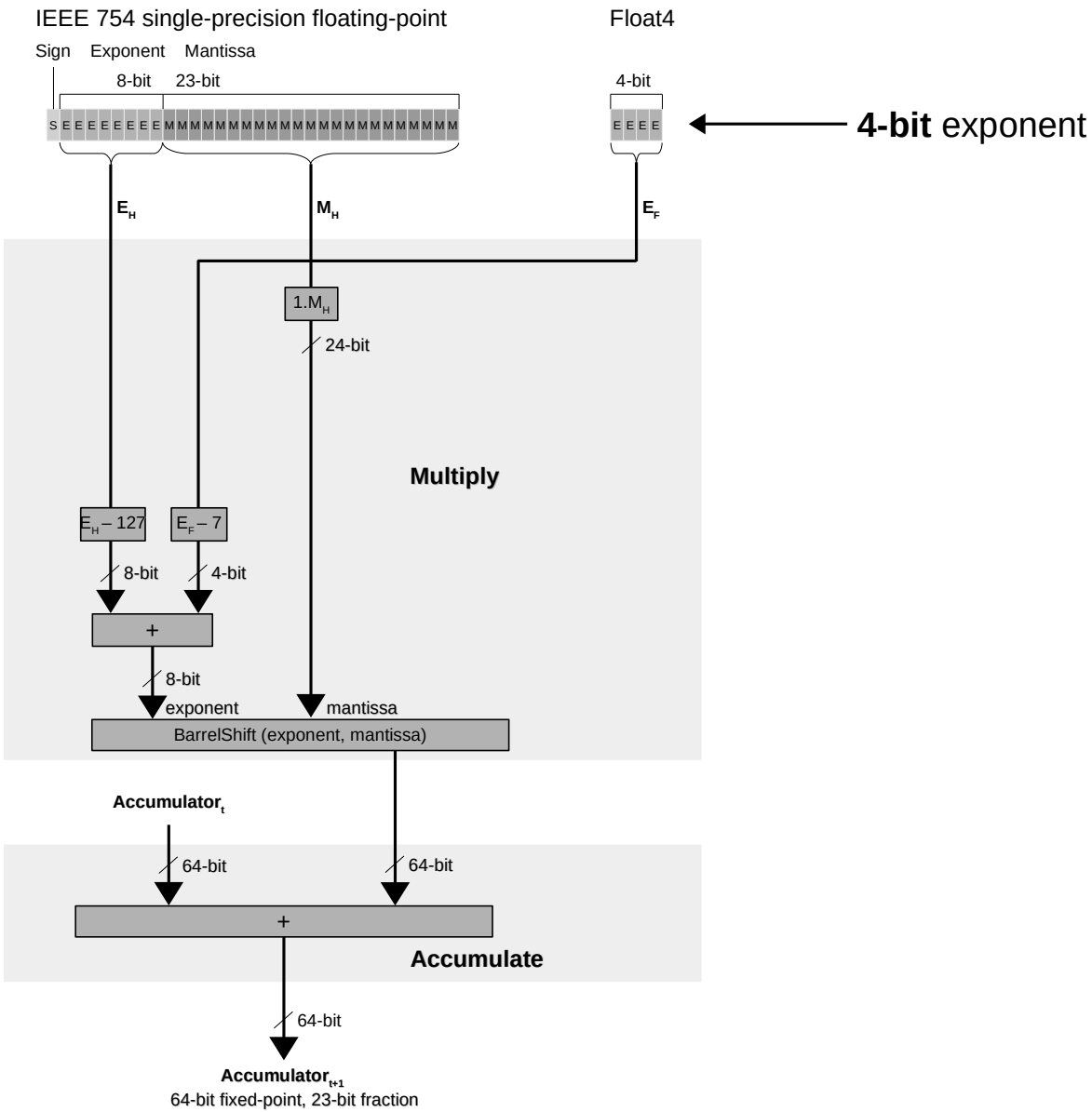


Custom Floating-Point MAC Designs

Hybrid Custom Floating-Point Multiply-Accumulate Unit

For **noise-robust applications** with **non-negativity constraints**.

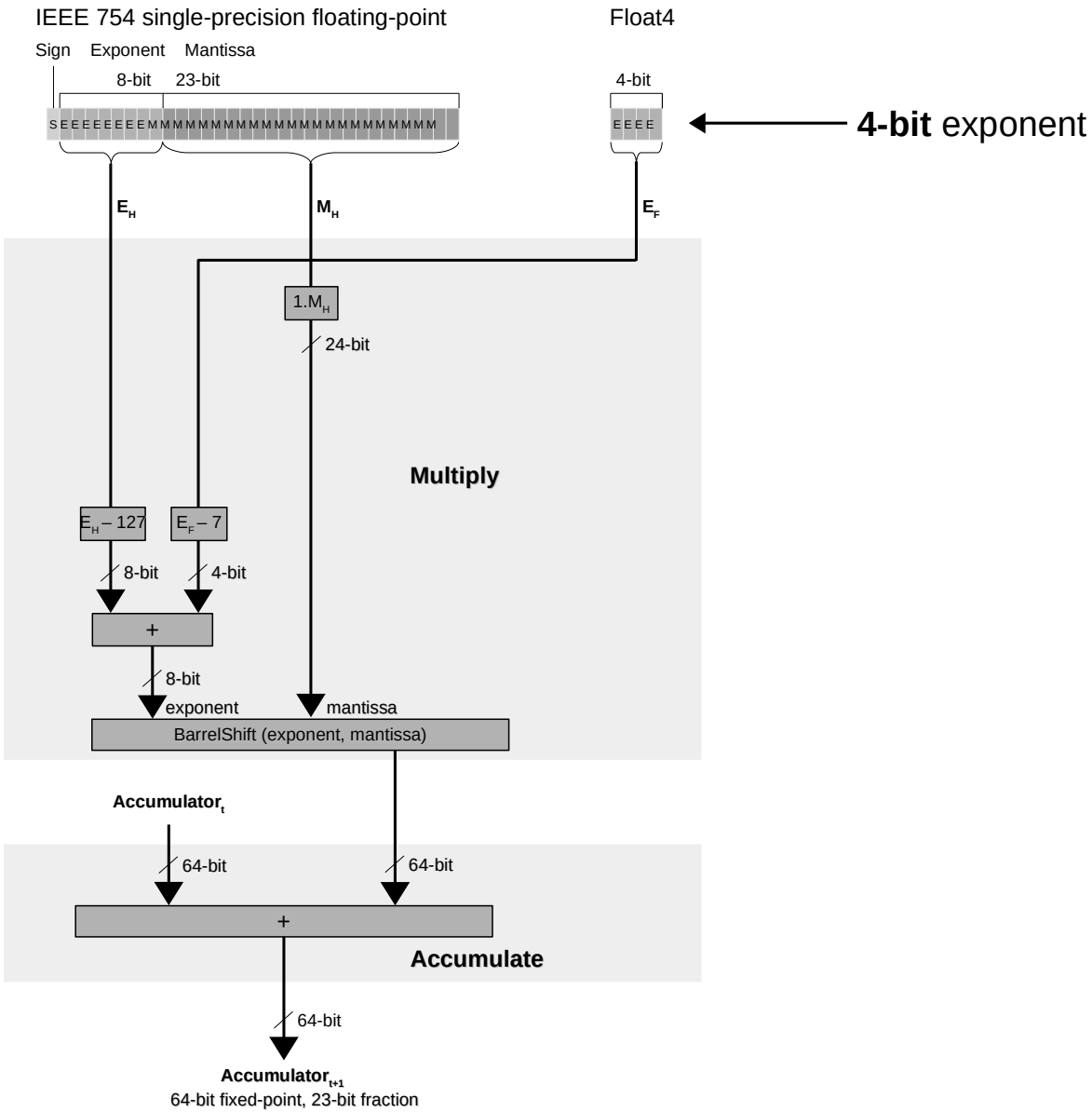
Non-negative Tensor Factorization

Non-negative Sparse Coding

Non-negative Matrix Factorization

Spike-by-Spike Neural Networks

Etc.



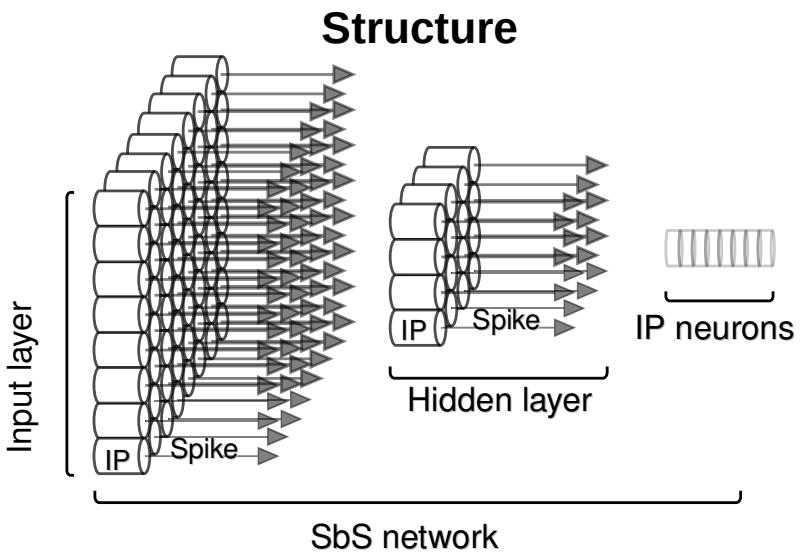
Custom Floating-Point Quantization

Algorithm 1: Custom floating-point quantization

Input: $MODEL$ as the CNN
Input: E_{size} as the target exponent bit size
Input: M_{size} as the target mantissa bits size
Input: $STDM_{size}$ as the IEEE 754 mantissa bit size
Output: $MODEL$ as the quantized CNN

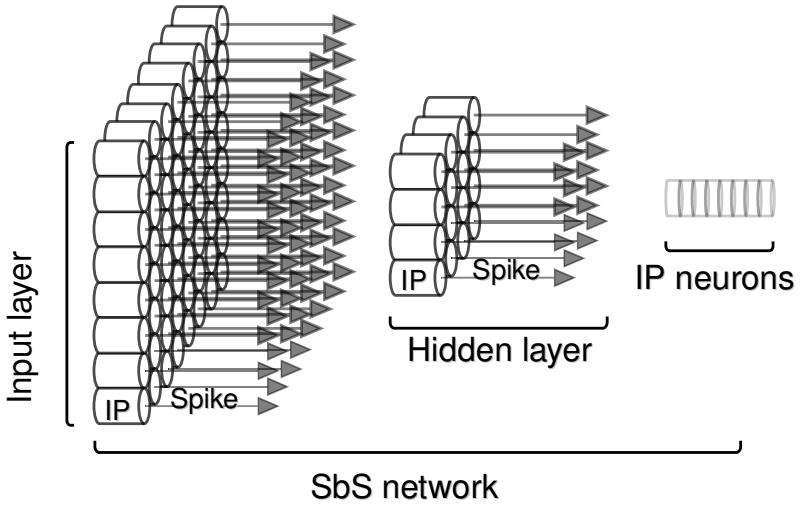
foreach *layer in* $MODEL$ **do**
  if *layer is* $Conv2D$ *or* $SeparableConv2D$ **then**
    $filter, bias \leftarrow GetWeights(layer)$
    foreach x *in* $filter$ *and* $bias$ **do**
      $sign \leftarrow GetSign(x)$
      $exp \leftarrow GetExponent(x)$
      $fullexp \leftarrow 2^{E_{size}-1} - 1$ `// Get full range value`
      $cman \leftarrow GetCustomMantissa(x, M_{size})$
      $leftman \leftarrow GetLeftoverMantissa(x, M_{size})$
      if $exp < -fullexp$ **then**
        $x \leftarrow 0$
      else
        if $exp > fullexp$ **then**
          $x \leftarrow (-1)^{sign} \cdot 2^{fullexp} \cdot (1 + (1 - 2^{-M_{size}}))$
        else
          if $2^{STDM_{size}-M_{size}-1} - 1 < leftman$ **then**
            $cman \leftarrow cman + 1$ `// Above halfway`
            if $2^{M_{size}} - 1 < cman$ **then**
              $cman \leftarrow 0$ `// Correct mantissa overflow`
              $exp \leftarrow exp + 1$
          $x \leftarrow (-1)^{sign} \cdot 2^{exp} \cdot (1 + cman \cdot 2^{-M_{size}})$
    $SetWeights(layer, filter, bias)$

Spike-by-Spike Neural Network

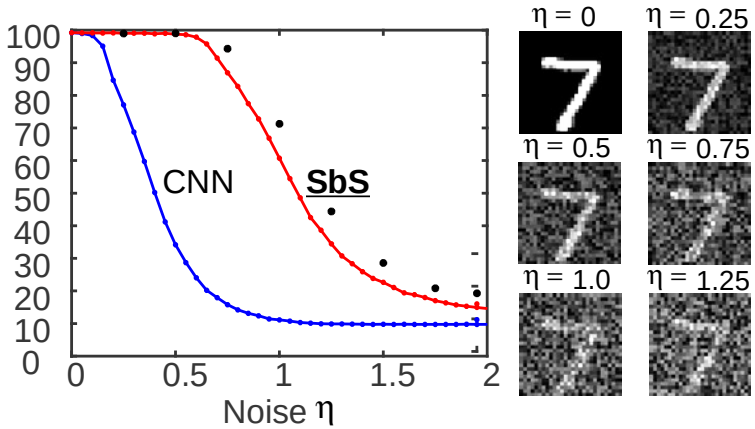


Spike-by-Spike Neural Network

Structure



Noise robustness



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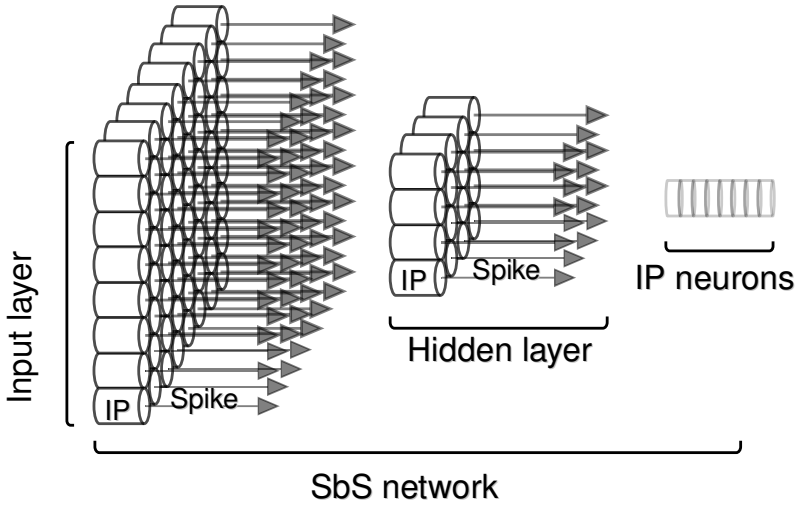

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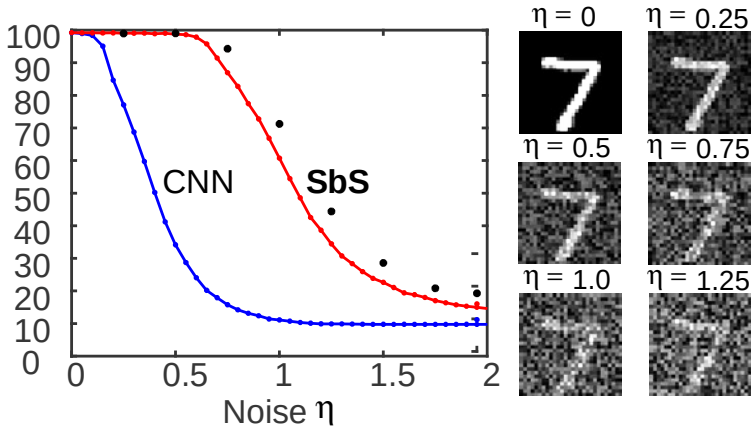

Neuron update

$$h_\mu^{new}(i) = \frac{1}{1+\epsilon}\left(h_\mu(i) + \epsilon \frac{h_\mu(i)W(s_t|i)}{\sum_j h_\mu(j)W(s_t|j)}\right)$$

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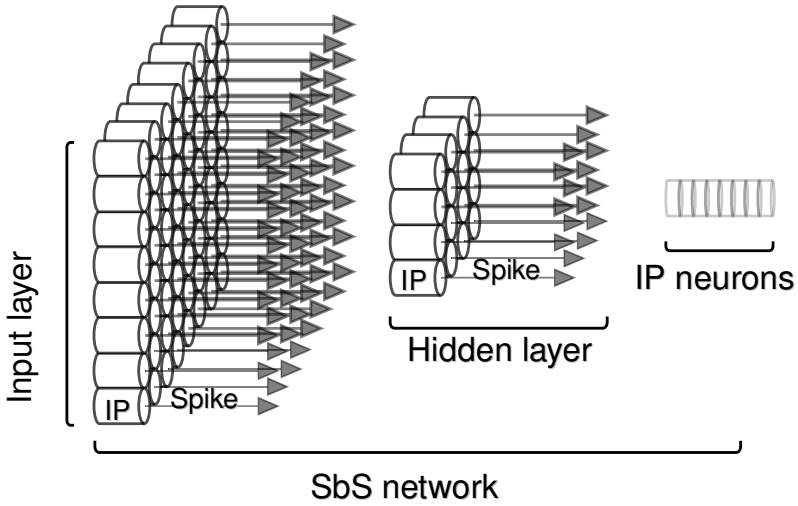

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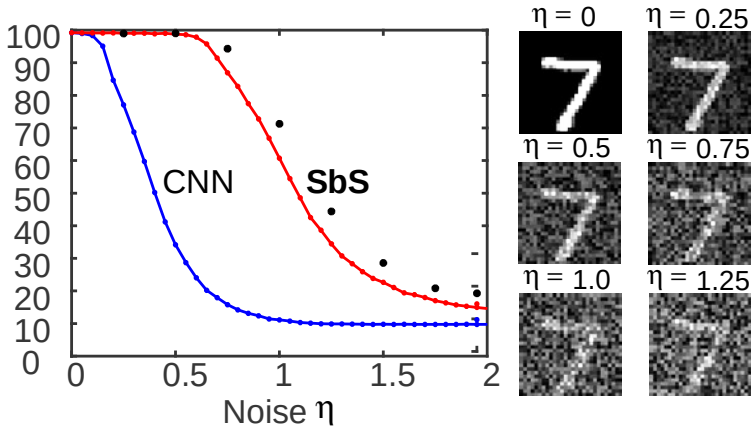

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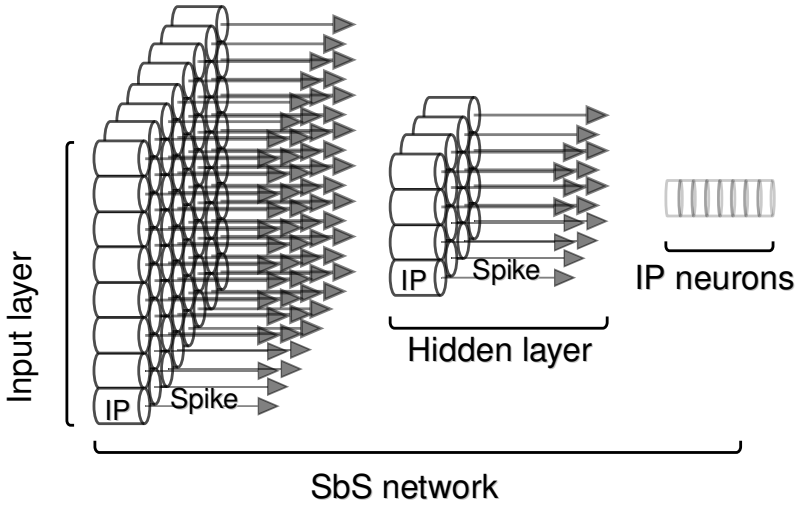

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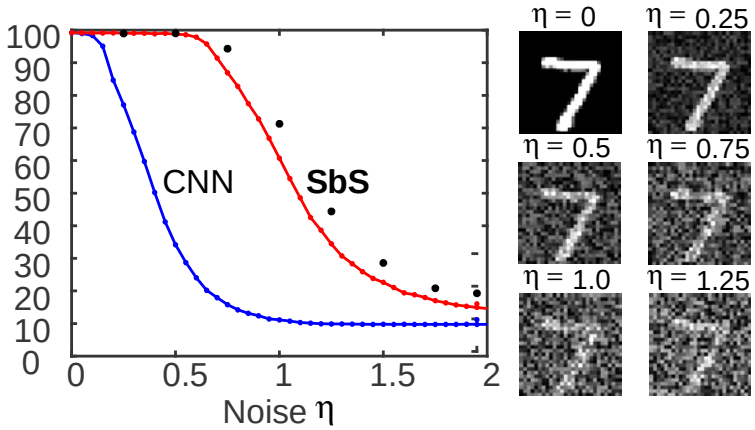

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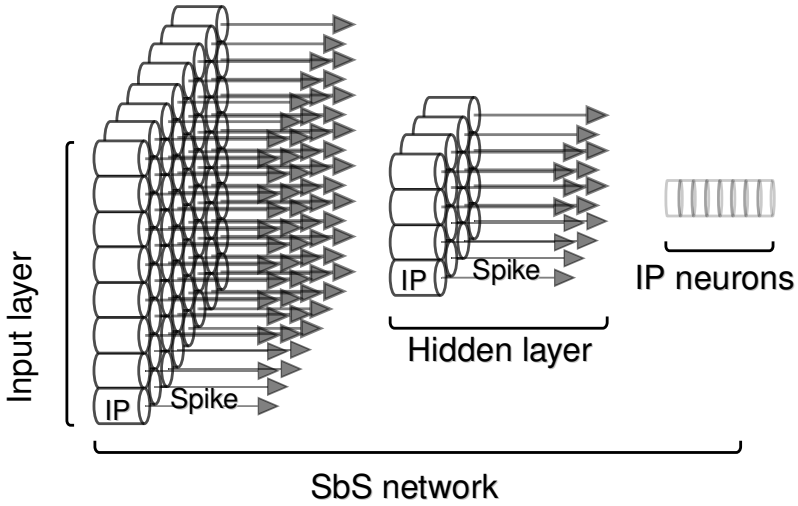

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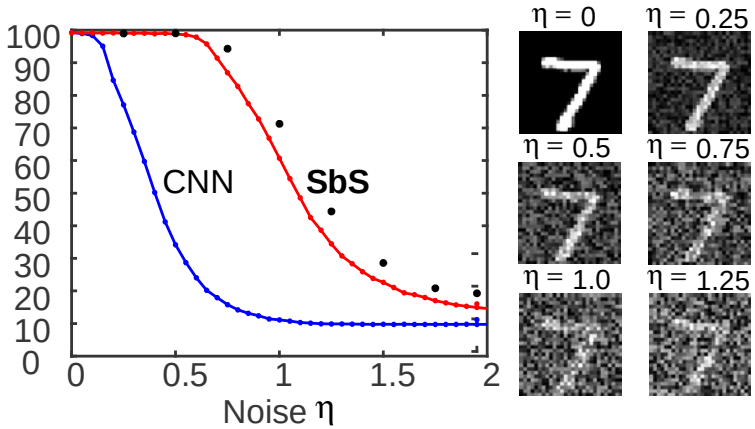

Properties:

- Noise robustness
- Iterative optimization
- No sign bit required
- Requires division
- Compute and memory intensive

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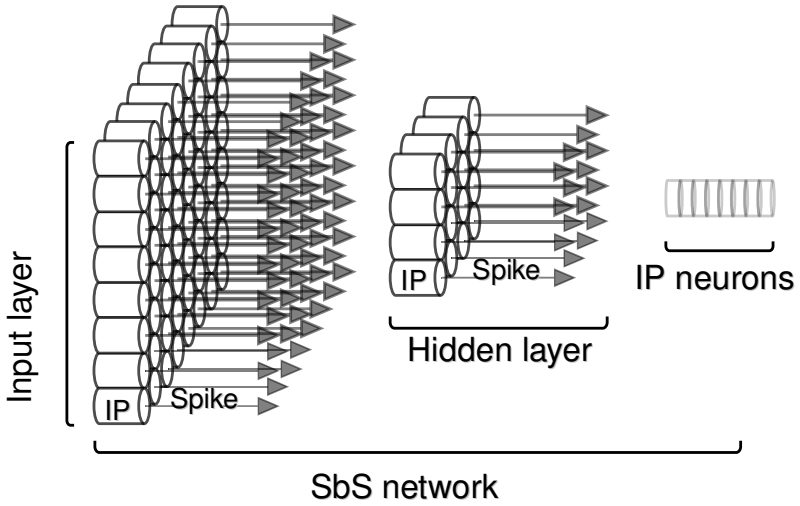

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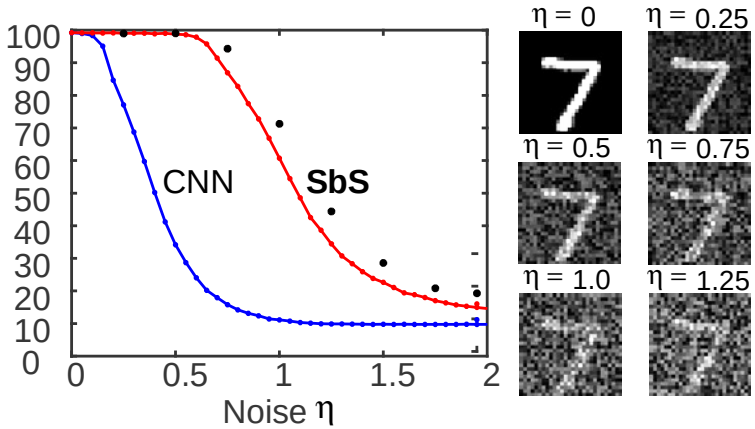

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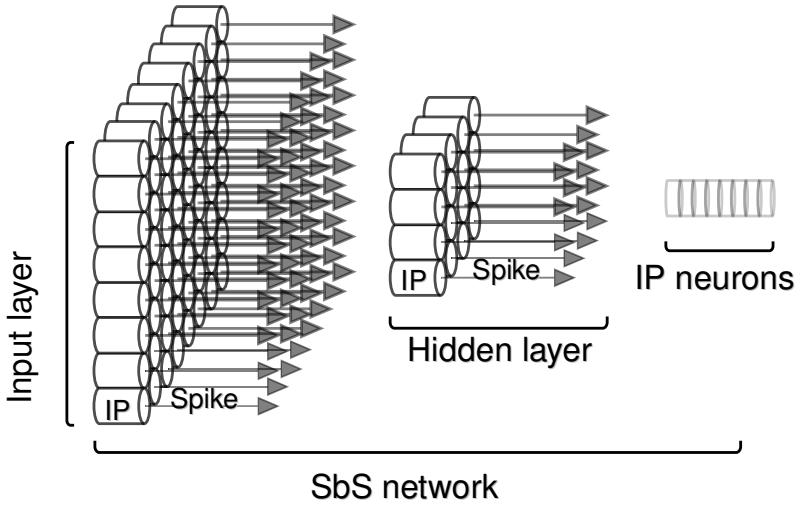

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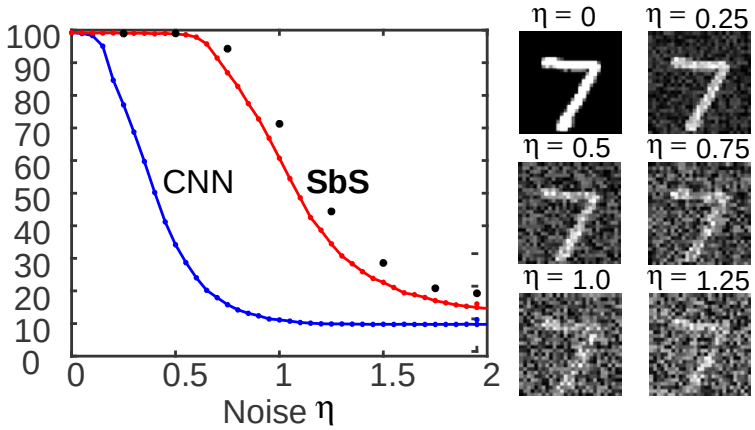

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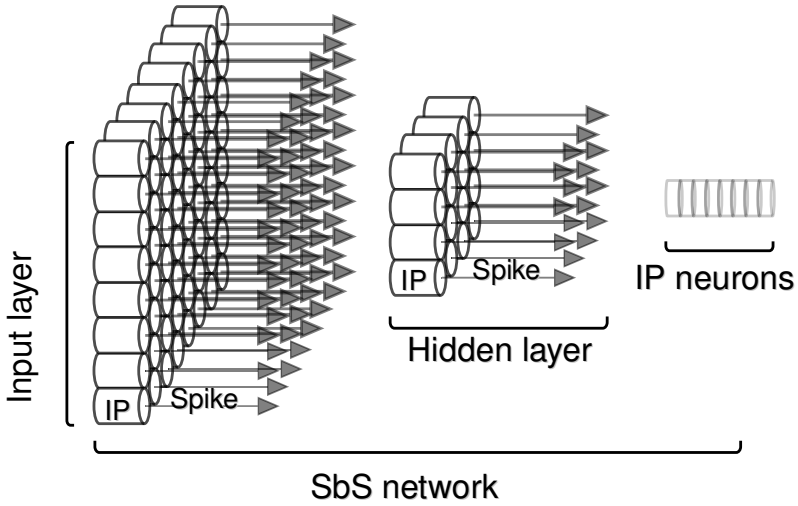

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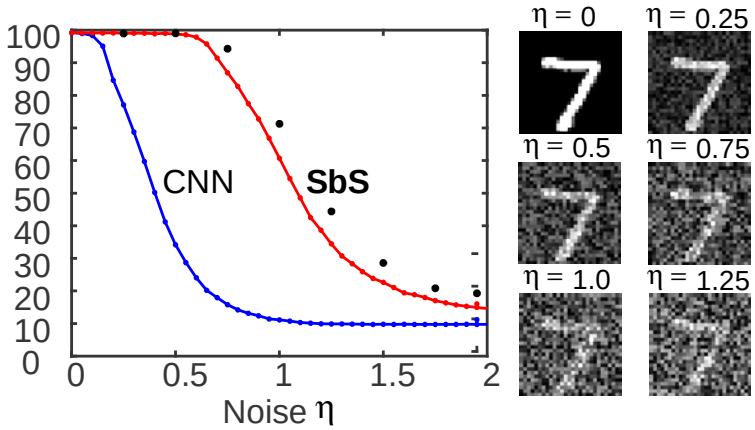

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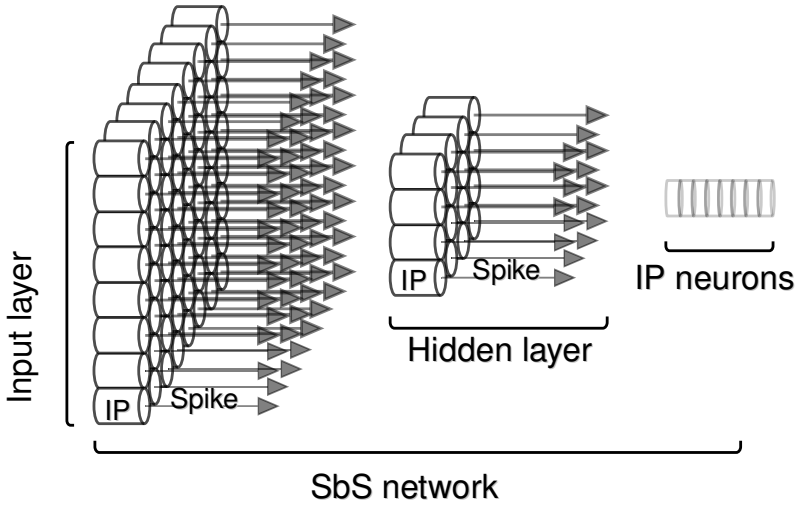

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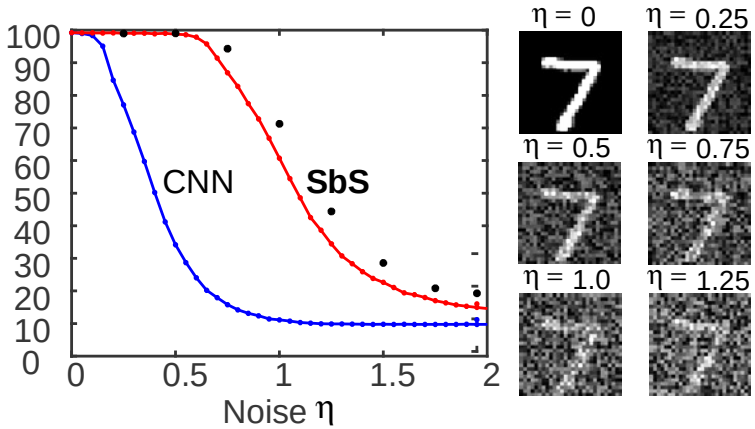

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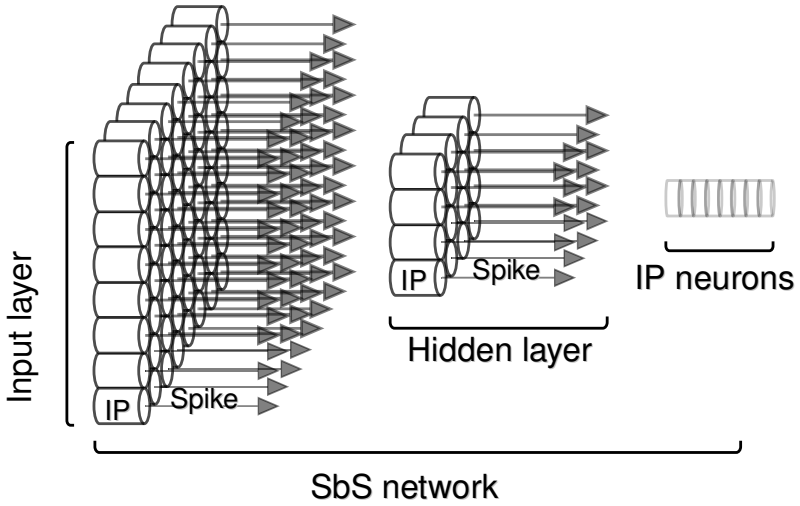

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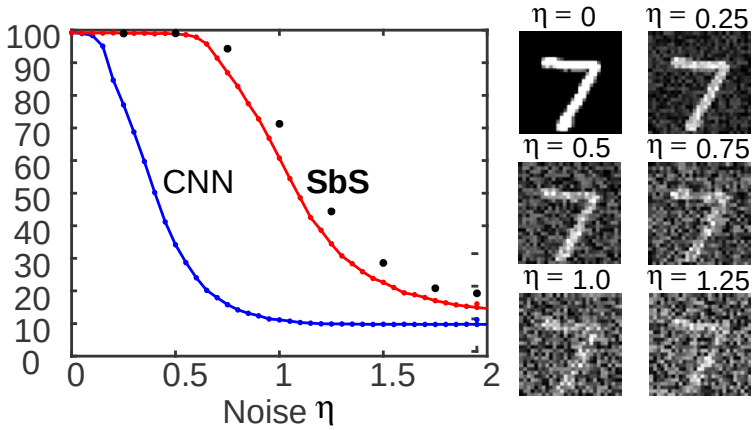

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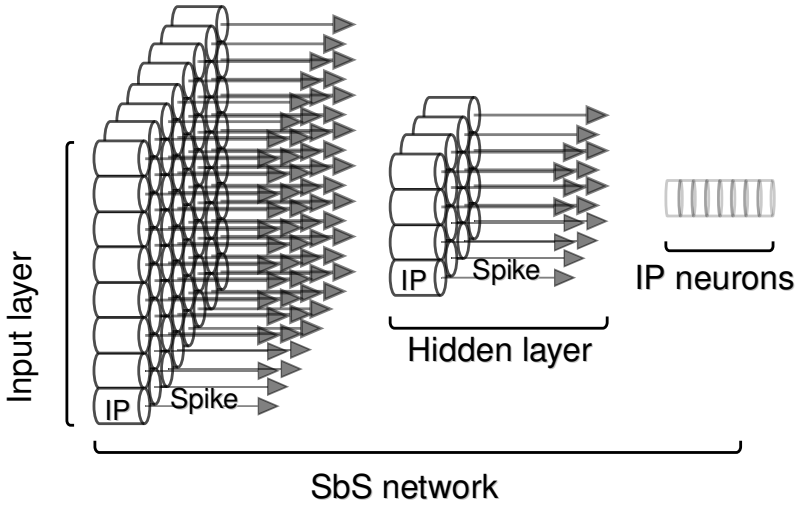
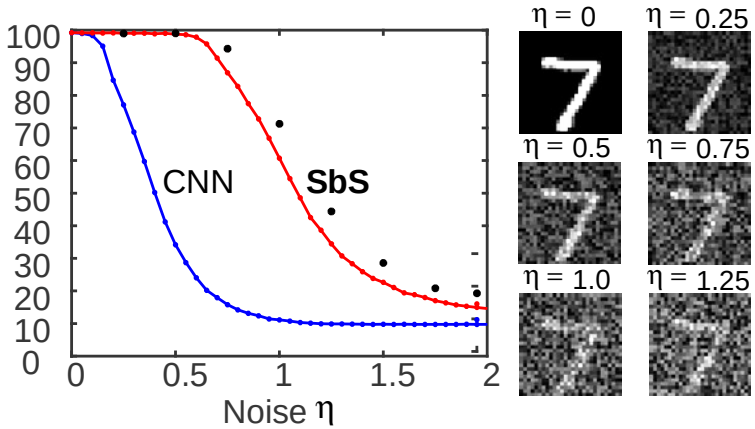
Spike-by-Spike Neural Network

Structure



Noise robustness



Properties:

- Noise robustness
- Iterative optimization
- No sign bit required
- Requires division
- Compute and memory intensive

Neuron update

$$h_\mu^{new}(i) = \frac{1}{1+\epsilon}\left(h_\mu(i) + \epsilon \frac{h_\mu(i)W(s_t|i)}{\sum_j h_\mu(j)W(s_t|j)}\right)$$

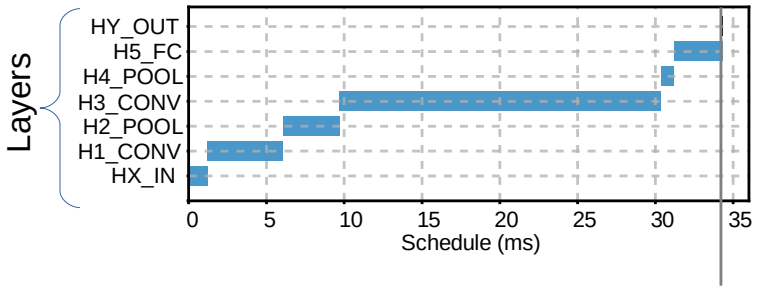
Non-negativity $0 \leq W(s_t|j) \leq 1$

Normalized $\sum_{s_t=0}^{M-1} W(s_t|j) = 1$

Deployment

Floating-point 32-bit

ARM Cortex A9 @ 666 MHz

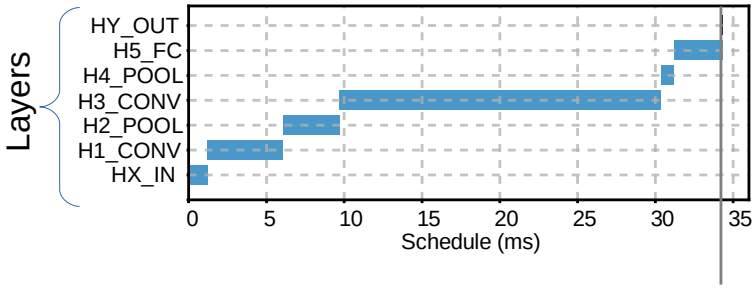


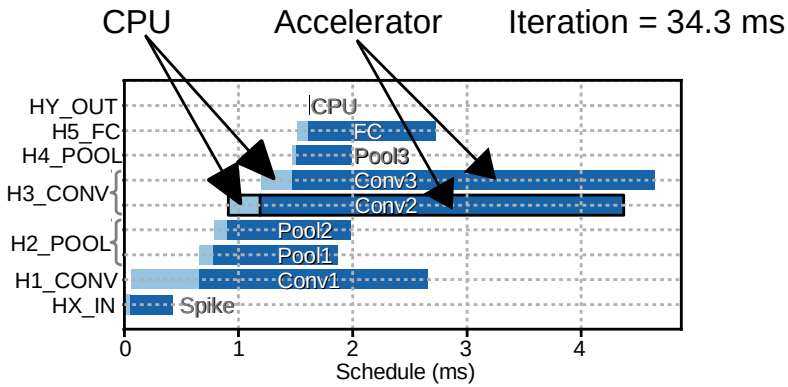
Iteration = 34.3 ms

Deployment

Floating-point 32-bit

ARM Cortex A9 @ 666 MHz

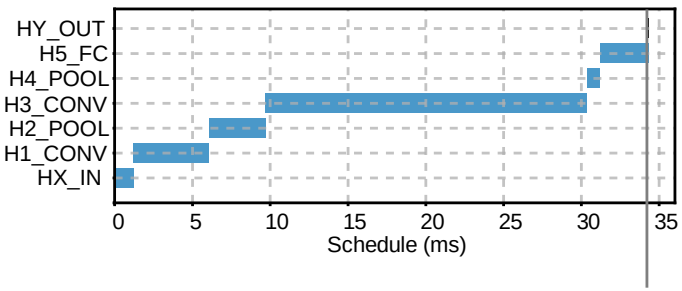


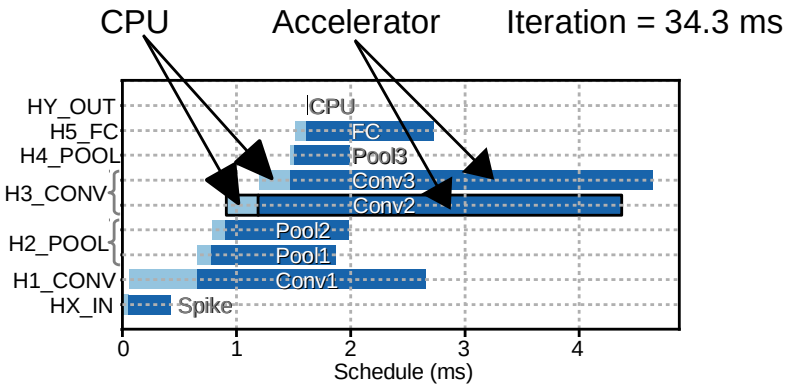


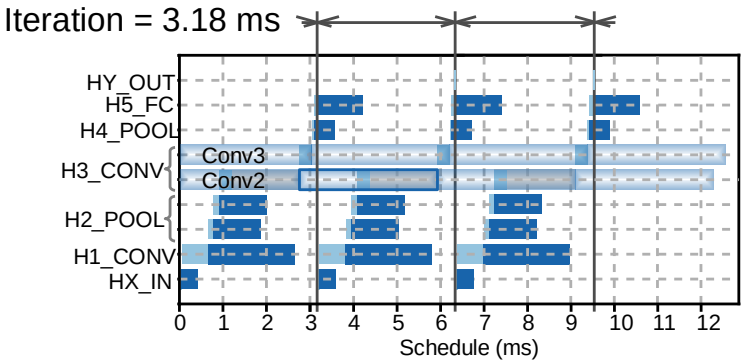
Deployment

Floating-point 32-bit

ARM Cortex A9 @ 666 MHz



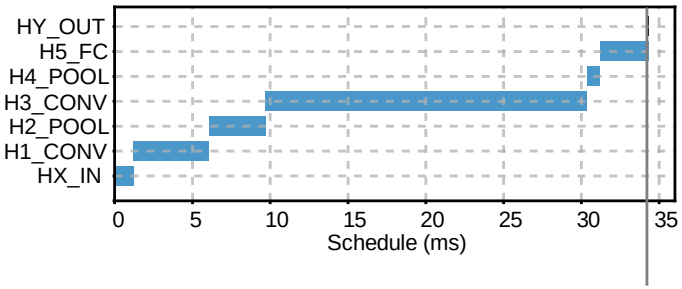


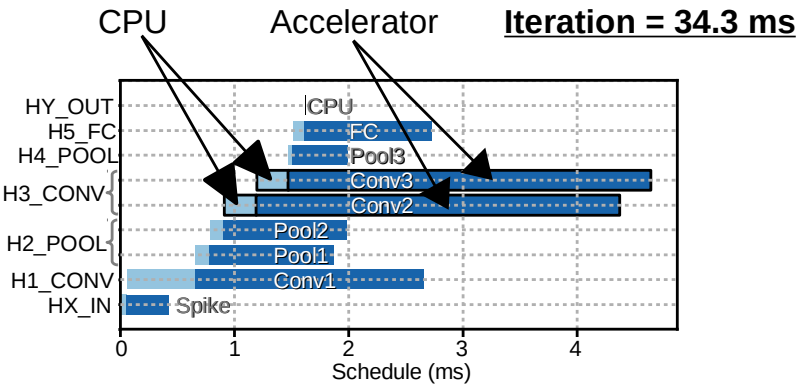


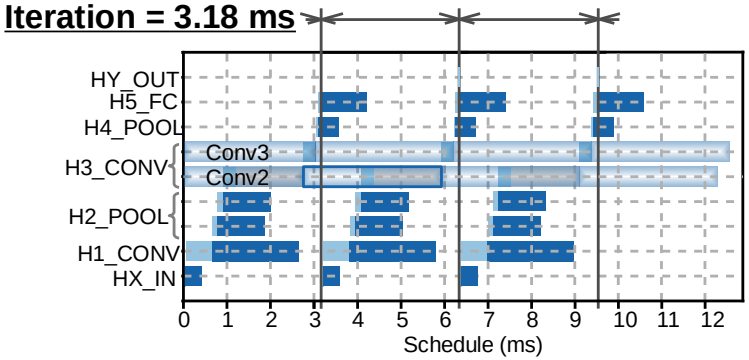
Deployment

Floating-point 32-bit

ARM Cortex A9 @ 666 MHz



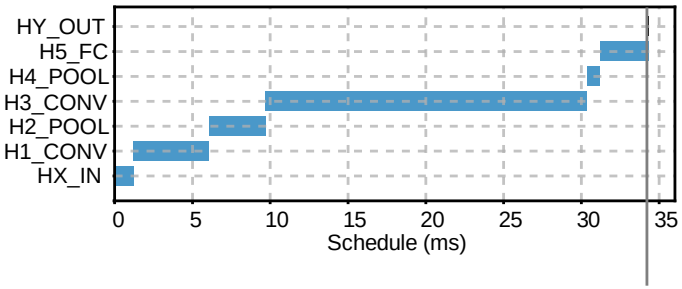


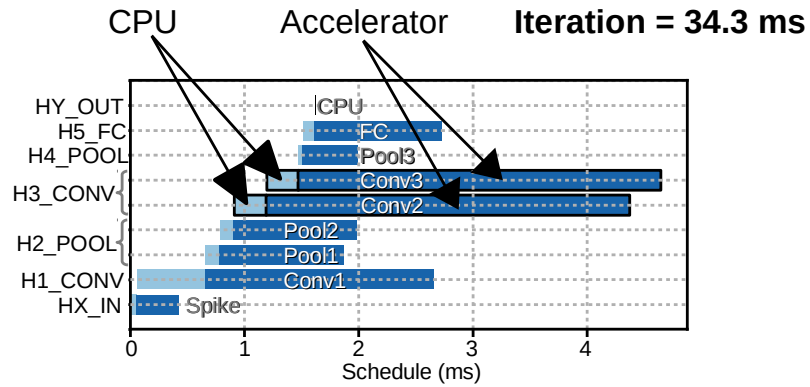


Deployment

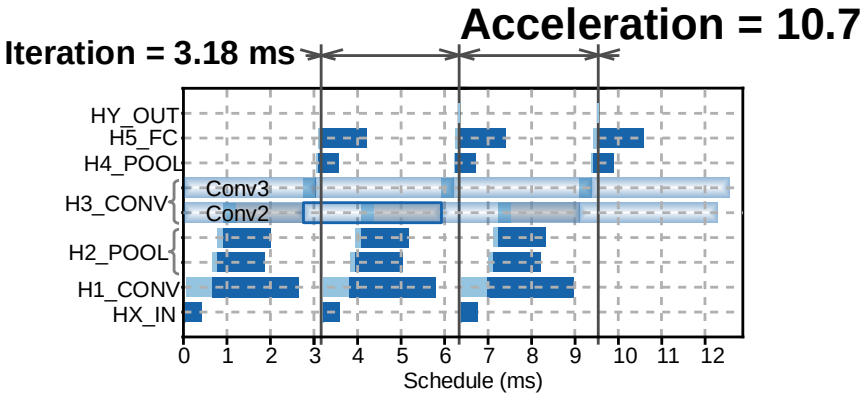
Floating-point 32-bit

ARM Cortex A9 @ 666 MHz





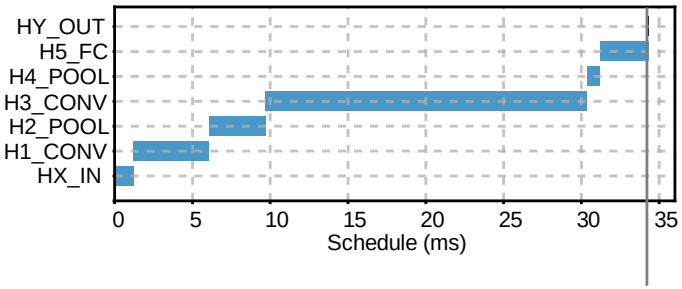
Acceleration = 10.7



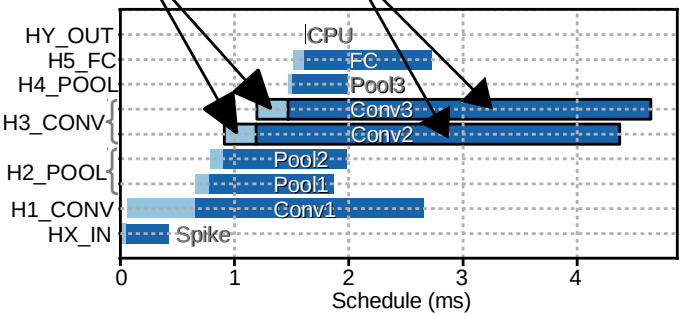
Deployment

Floating-point 32-bit

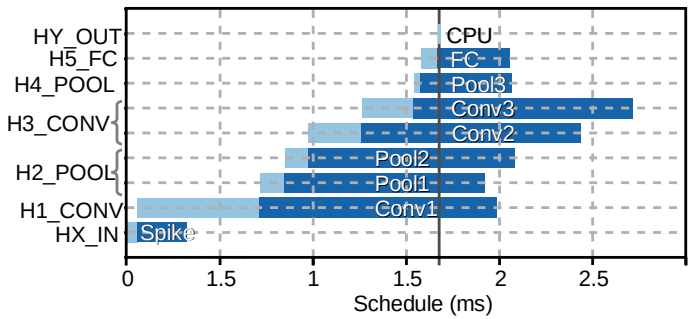
ARM Cortex A9 @ 666 MHz



CPU Accelerator **Iteration = 34.3 ms**

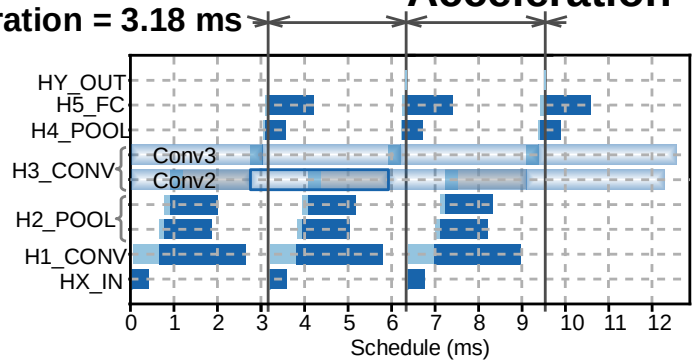


Hybrid logarithmic 4-bit

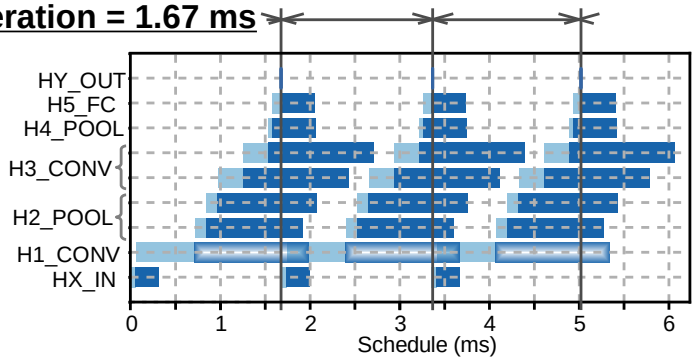


Acceleration = 10.7

Iteration = 3.18 ms



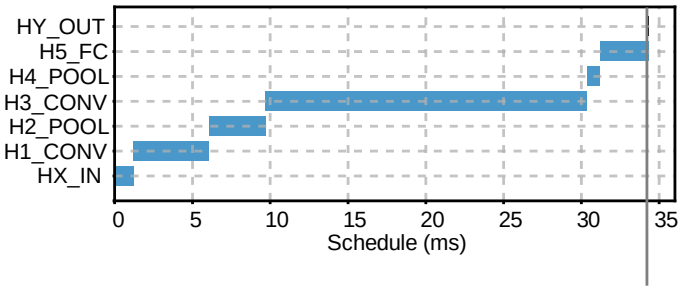
Iteration = 1.67 ms

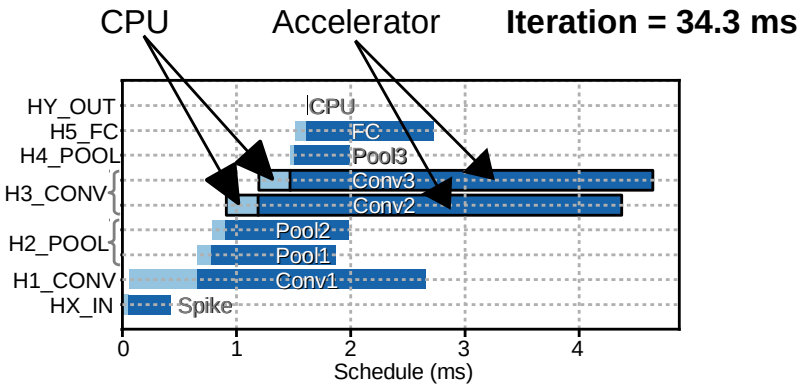


Deployment

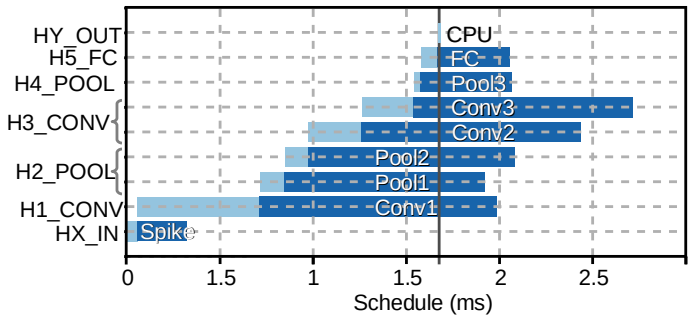
Floating-point 32-bit

ARM Cortex A9 @ 666 MHz

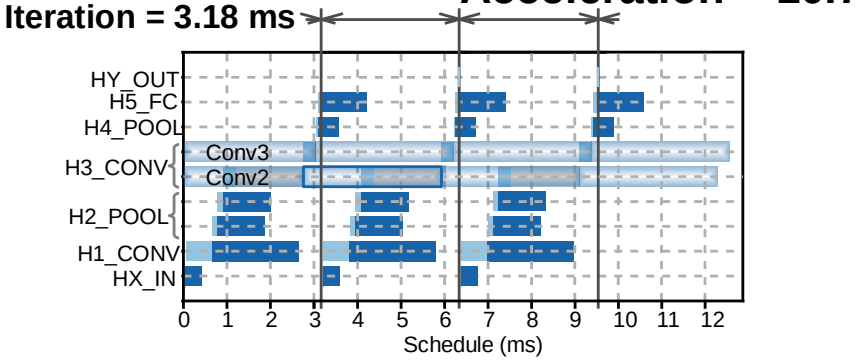




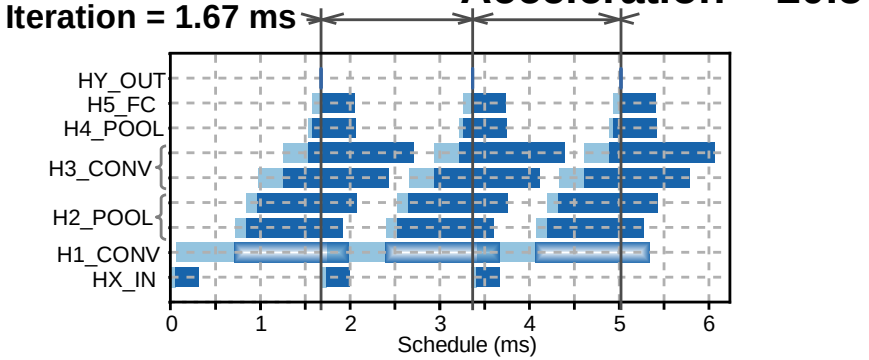
Hybrid logarithmic 4-bit



Acceleration = 10.7

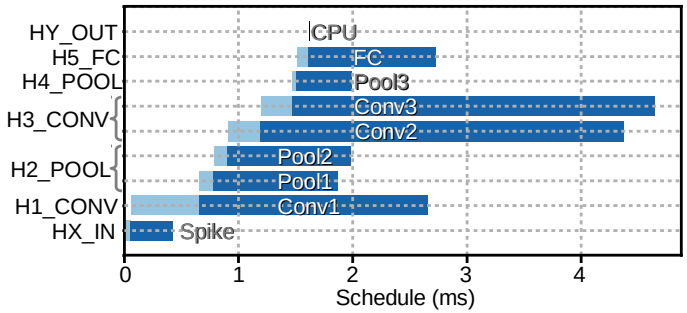


Acceleration = 20.5

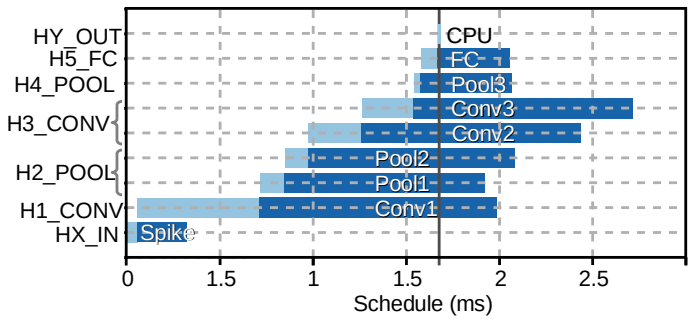


Deployment

Standard floating-point

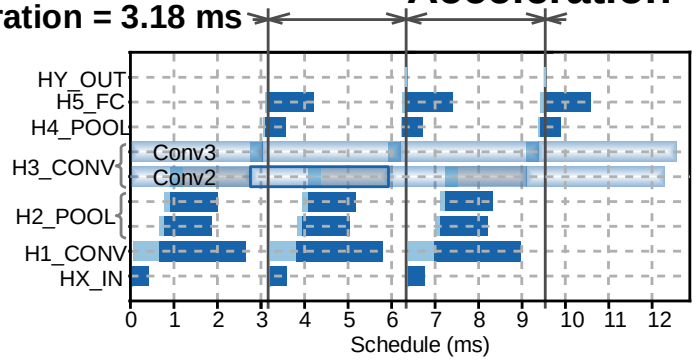


Hybrid logarithmic 4-bit



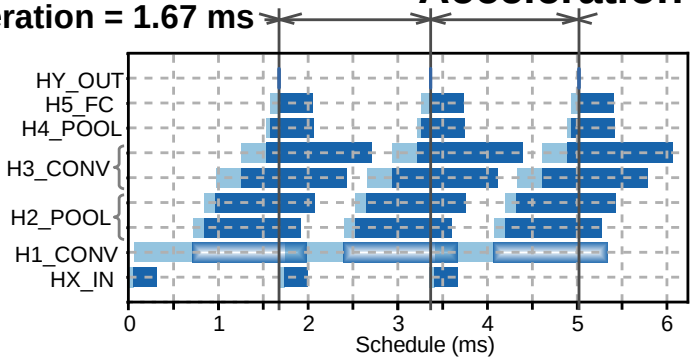
Acceleration = 10.7

Iteration = 3.18 ms



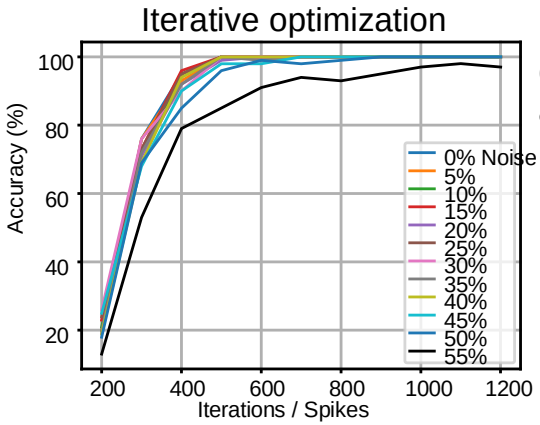
Acceleration = 20.5

Iteration = 1.67 ms

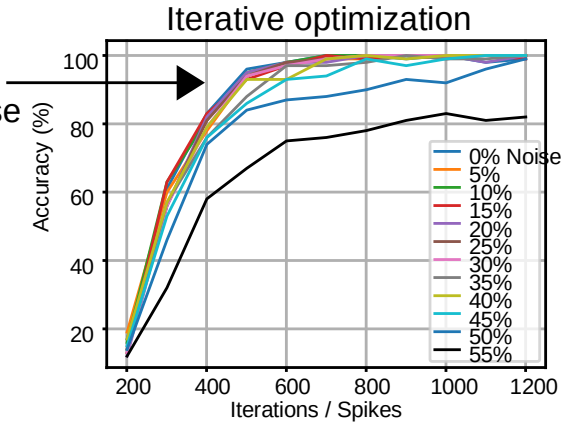


Accelerating Spike-by-Spike Neural Networks with Hybrid Logarithmic 4-bit

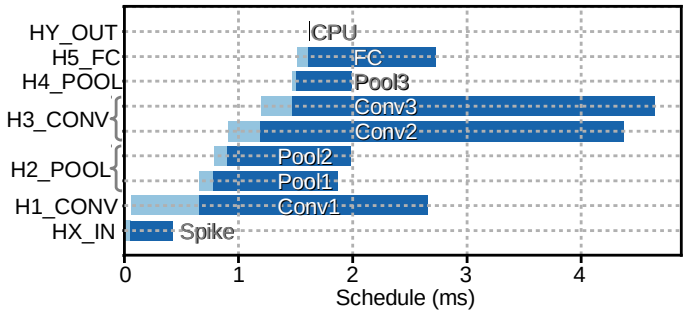
Deployment



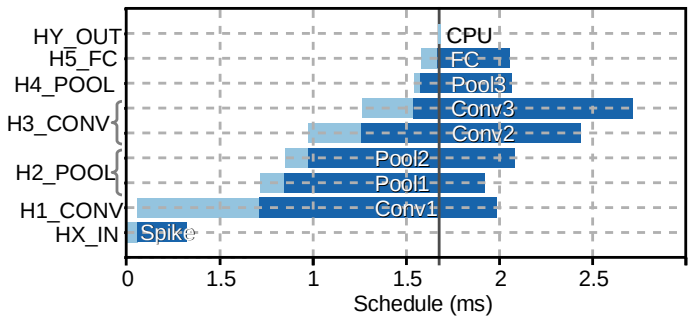
Good convergence
applying levels of noise



Standard floating-point

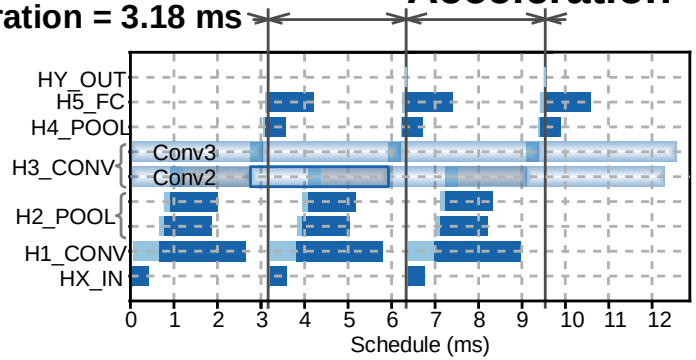


Hybrid logarithmic 4-bit



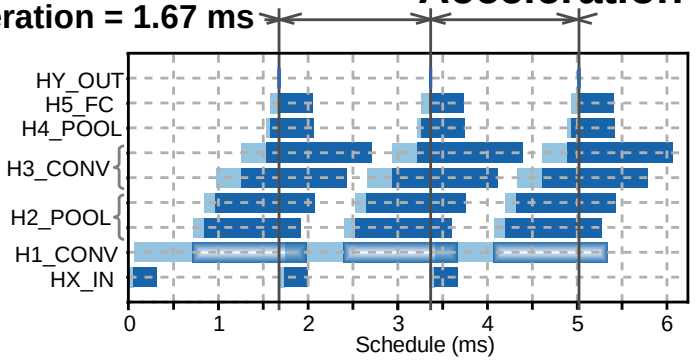
Acceleration = 10.7

Iteration = 3.18 ms



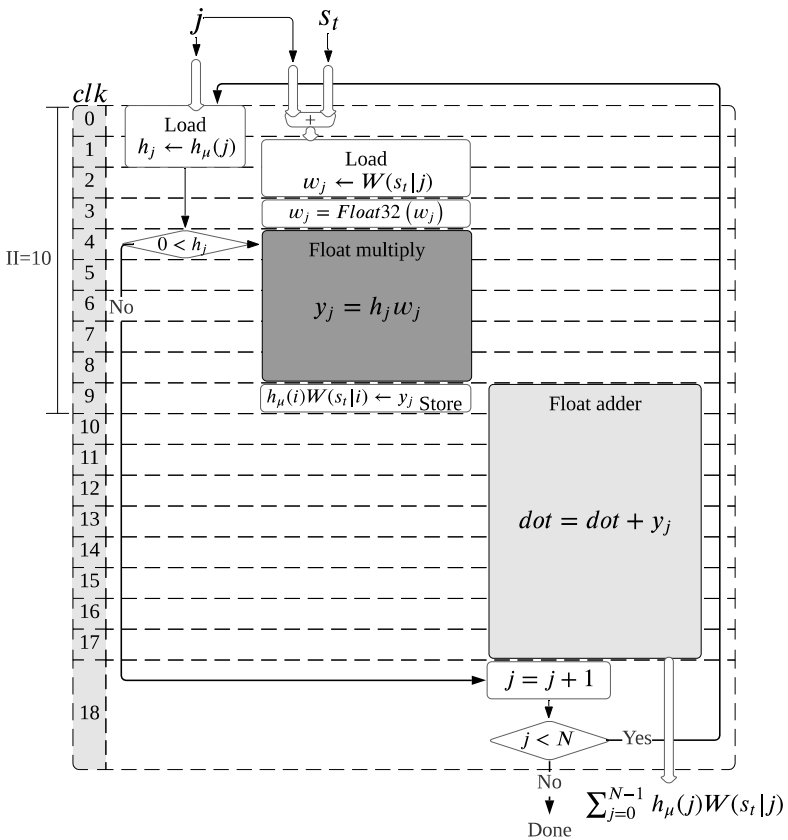
Acceleration = 20.5

Iteration = 1.67 ms

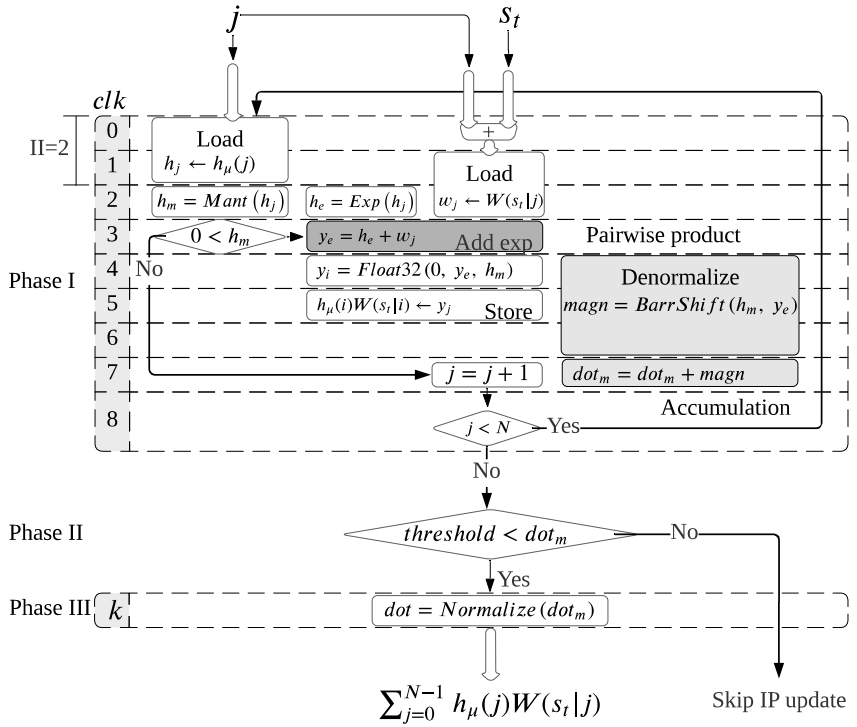


MAC Design: Standard Floating-Point vs. Hybrid Logarithmic 4-bit

Standard floating-point



Hybrid logarithmic 4-bit



MAC Design: Standard Floating-Point vs. Hybrid Logarithmic 4-bit

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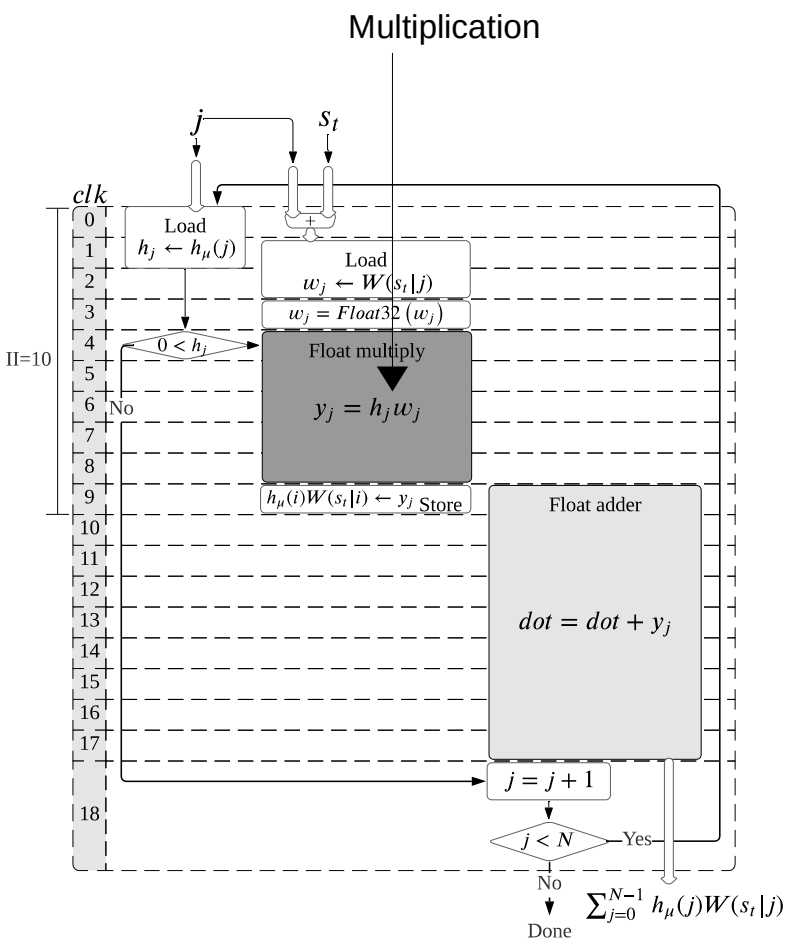
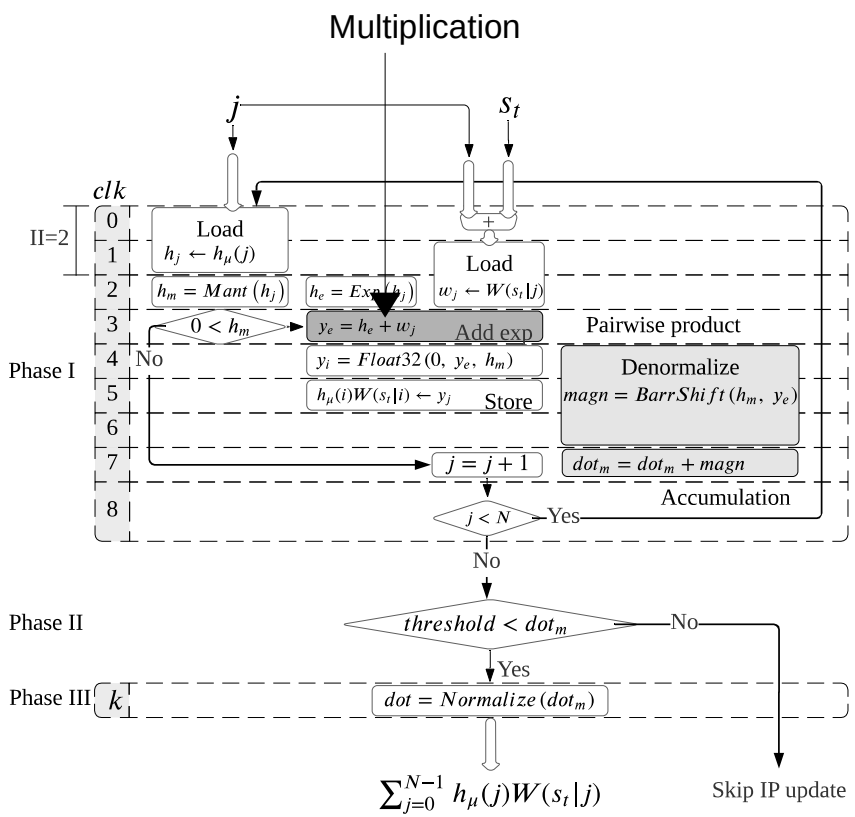
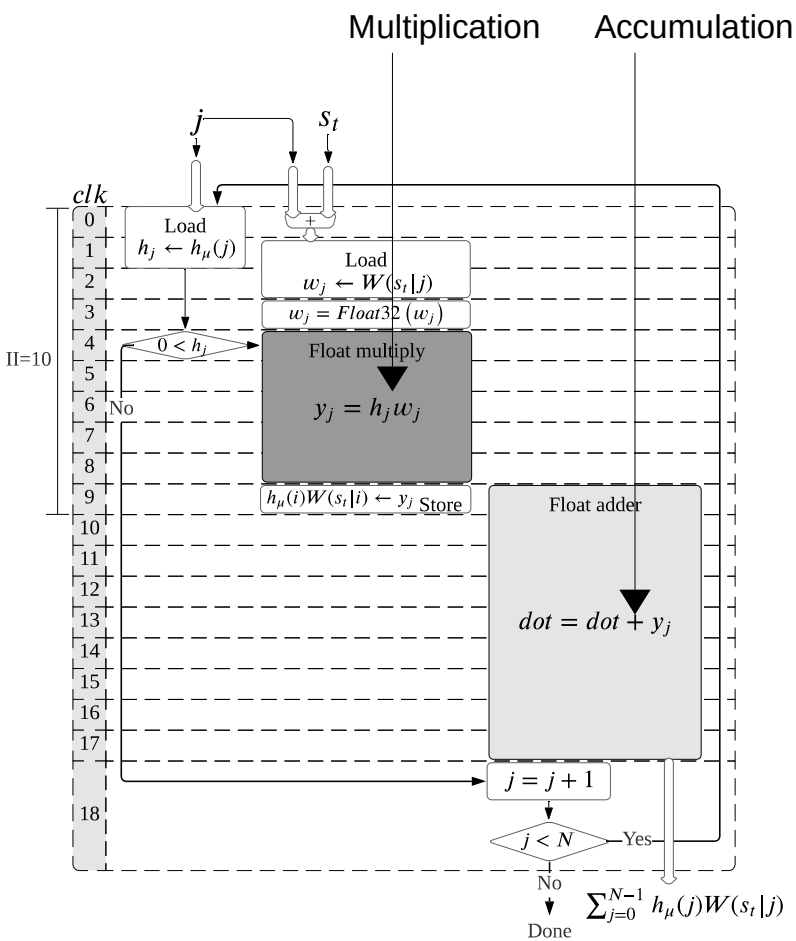


Hybrid logarithmic 4-bit

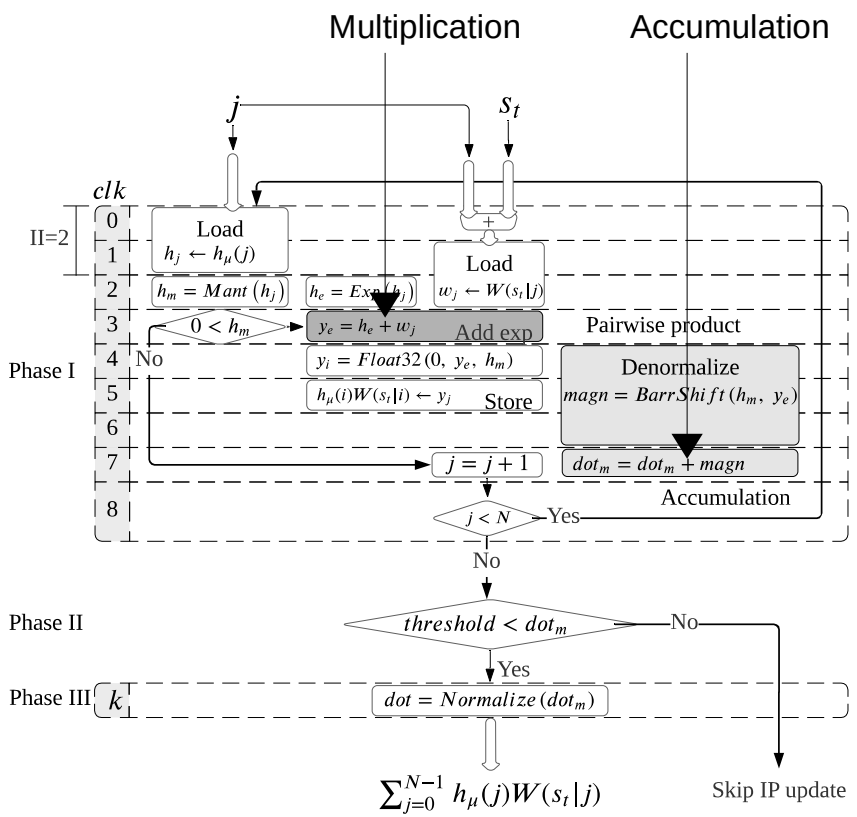


MAC Design: Standard Floating-Point vs. Hybrid Logarithmic 4-bit

Standard floating-point

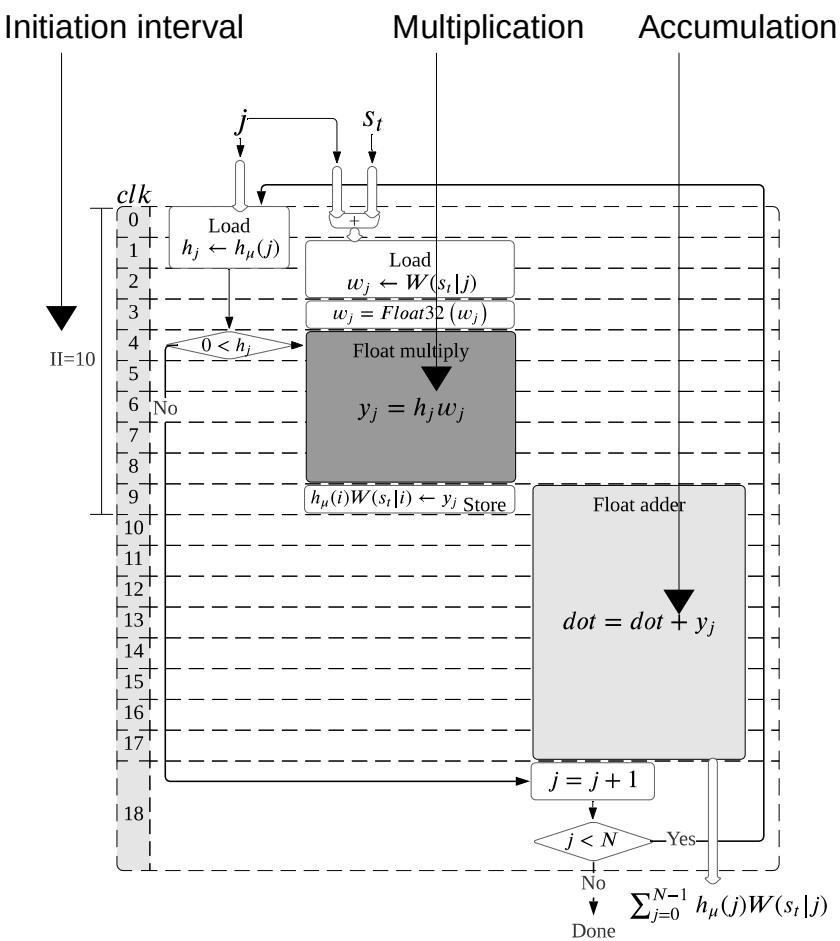


Hybrid logarithmic 4-bit

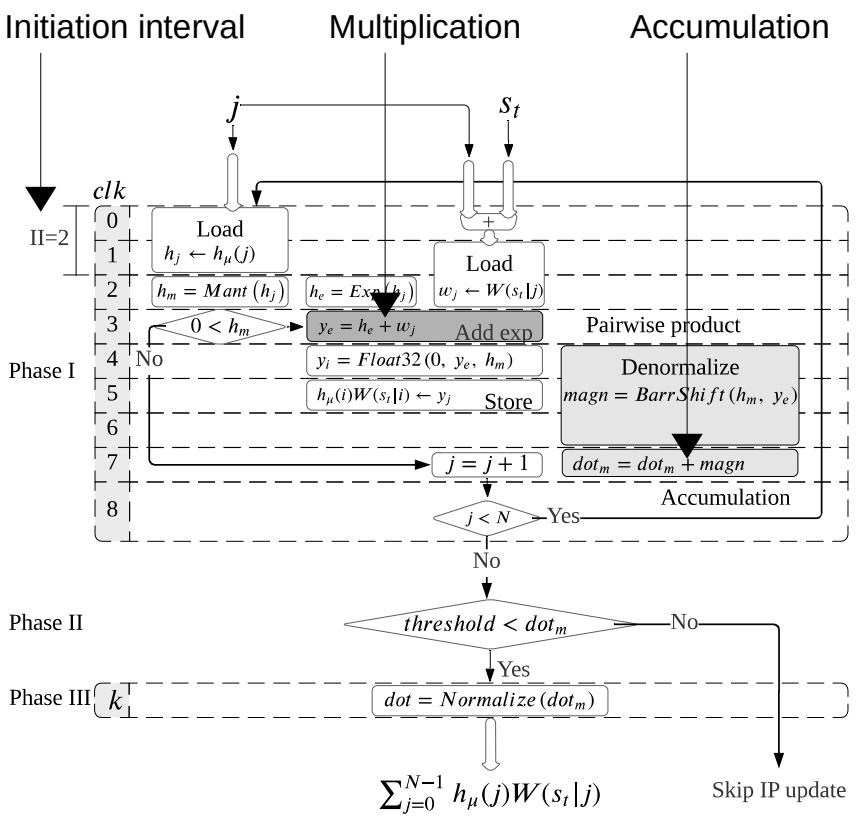


MAC Design: Standard Floating-Point vs. Hybrid Logarithmic 4-bit

Standard floating-point

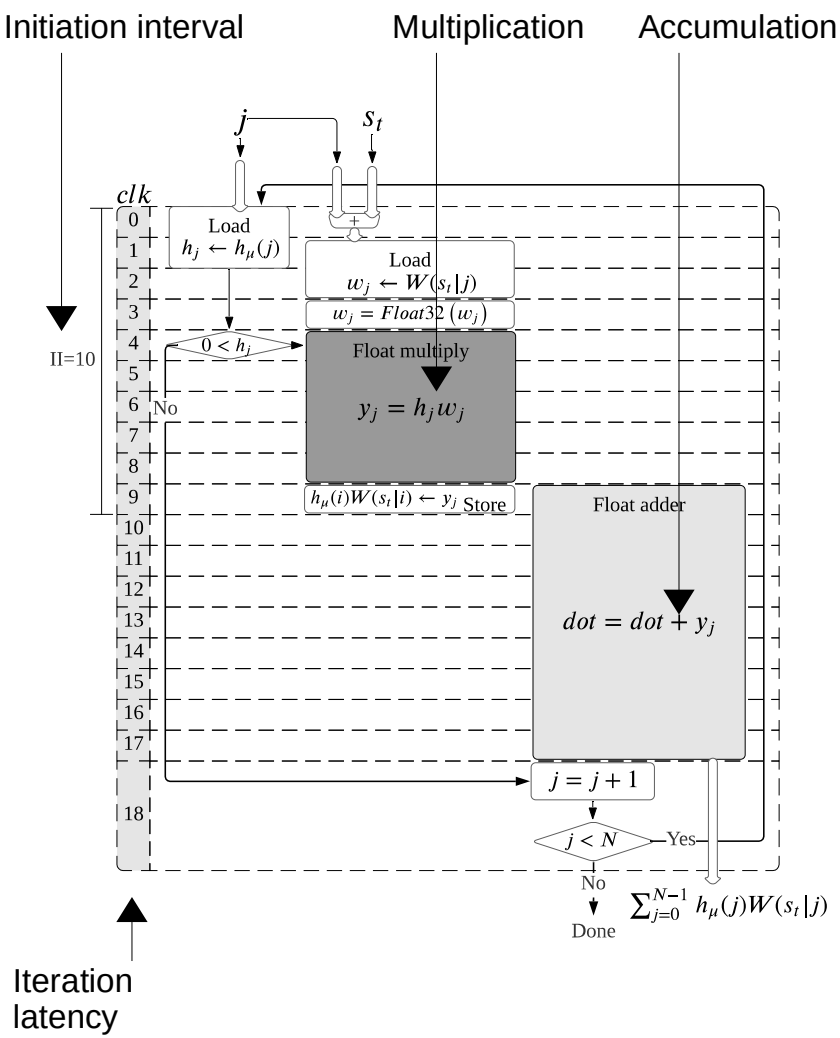


Hybrid logarithmic 4-bit

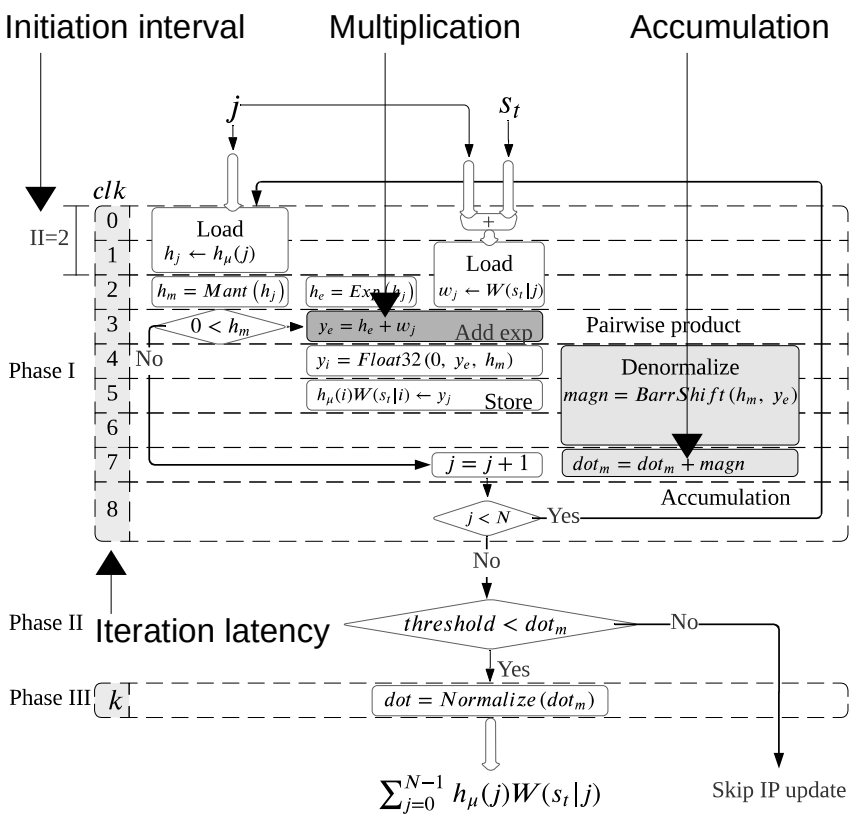


MAC Design: Standard Floating-Point vs. Hybrid Logarithmic 4-bit

Standard floating-point

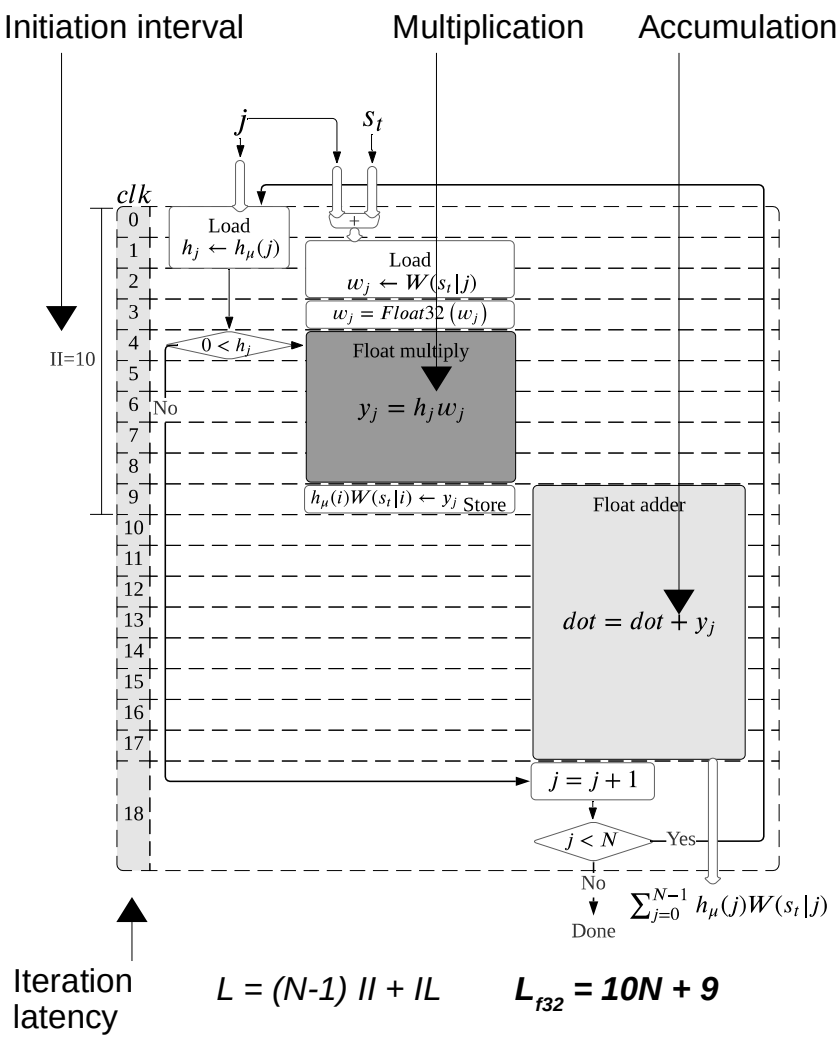


Hybrid logarithmic 4-bit



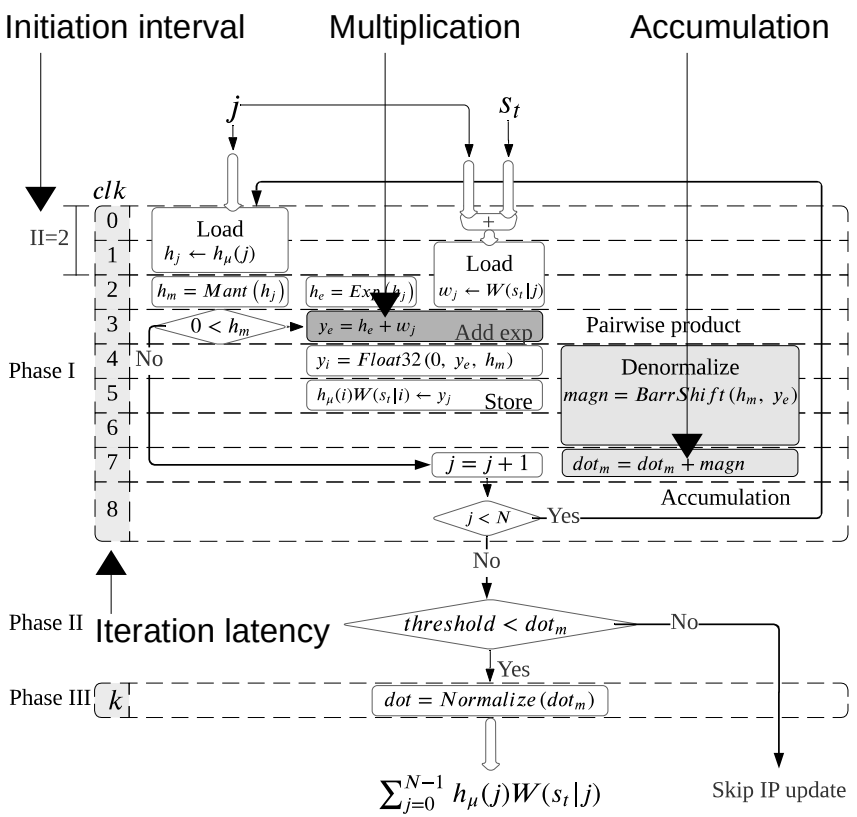
MAC Design: Standard Floating-Point vs. Hybrid Logarithmic 4-bit

Standard floating-point



$L = (N-1)\ II + IL$ $\quad L_{f32} = 10N + 9$

Hybrid logarithmic 4-bit

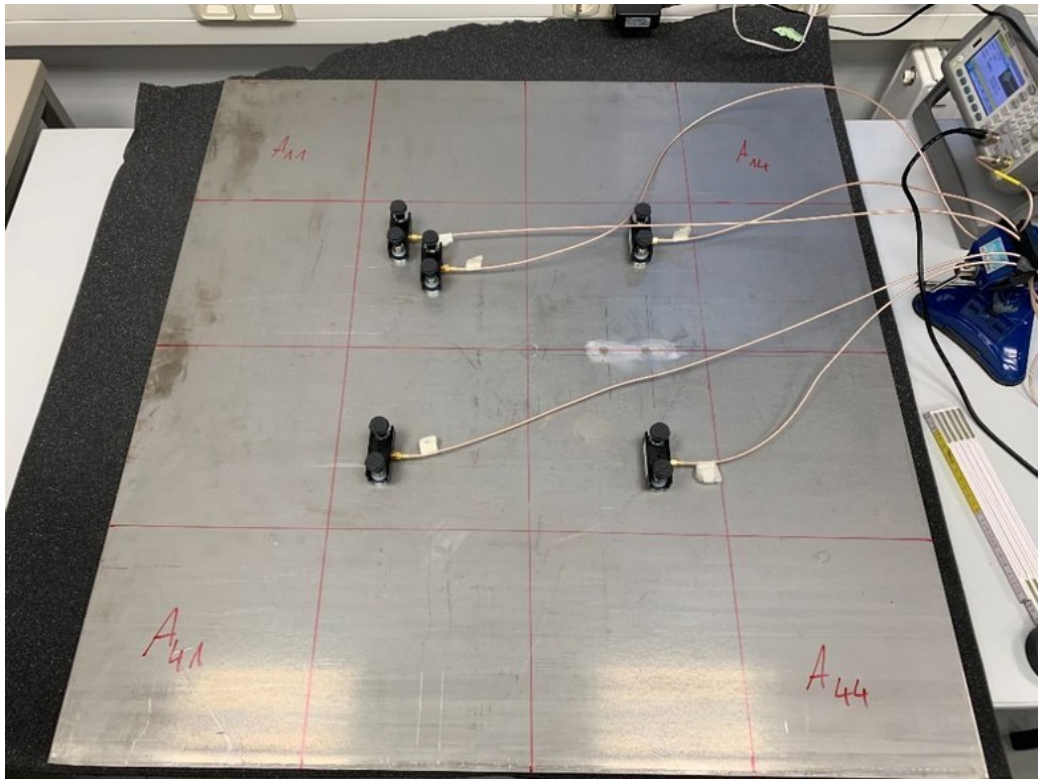


$L_{log} = 2N+7$

TinyML Application: CNN Sensor Analytics for Structural Health Monitoring

Experimental setup:

- Sensor and noise positions
- Training dataset
- Testing dataset
- Model architecture



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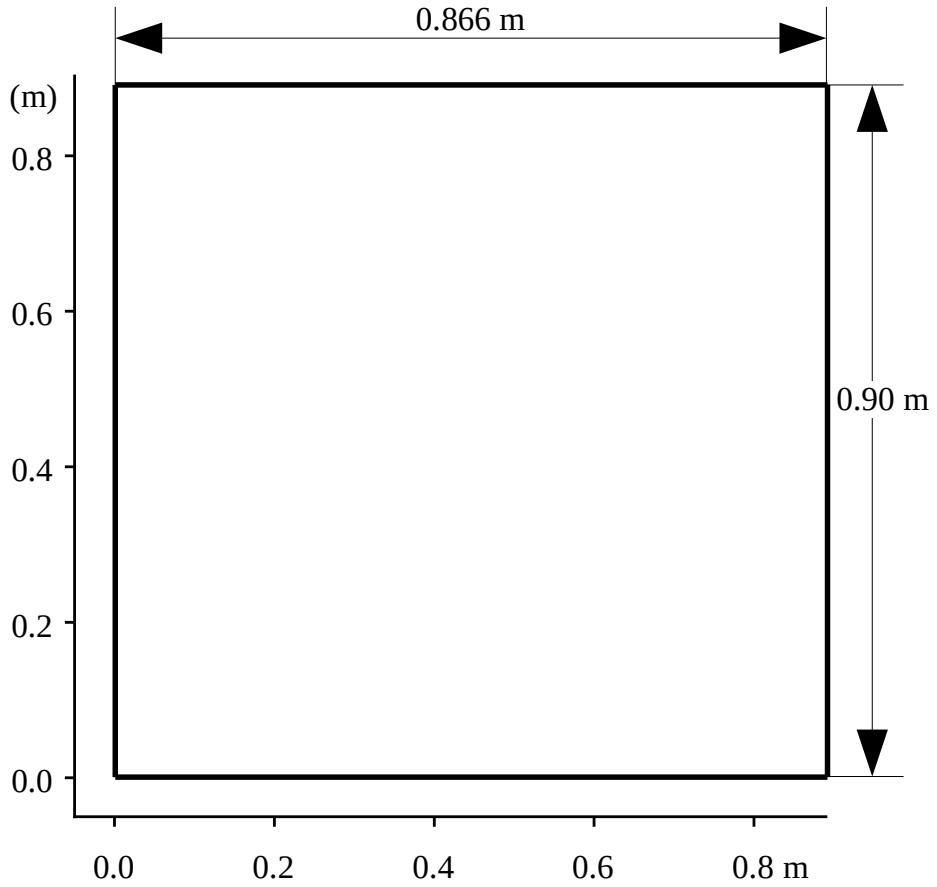

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- Testing dataset
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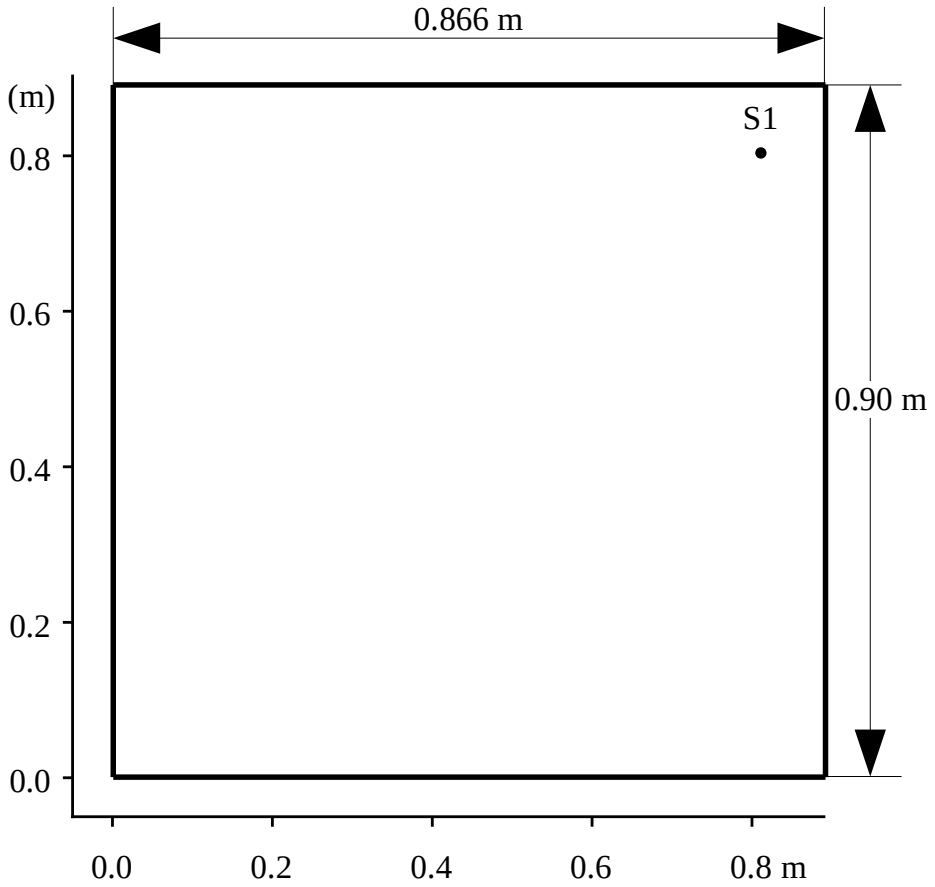

TinyML Application: CNN Sensor Analytics for Structural Health Monitoring

Experimental setup:

- **Sensor and noise positions**
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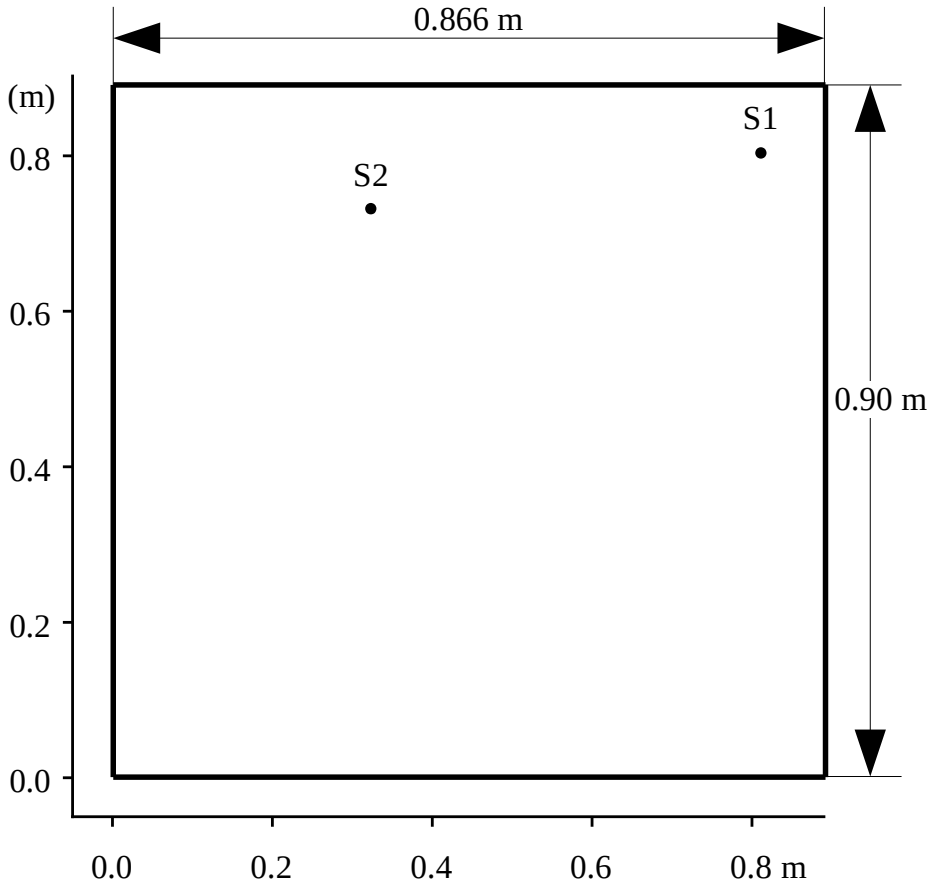

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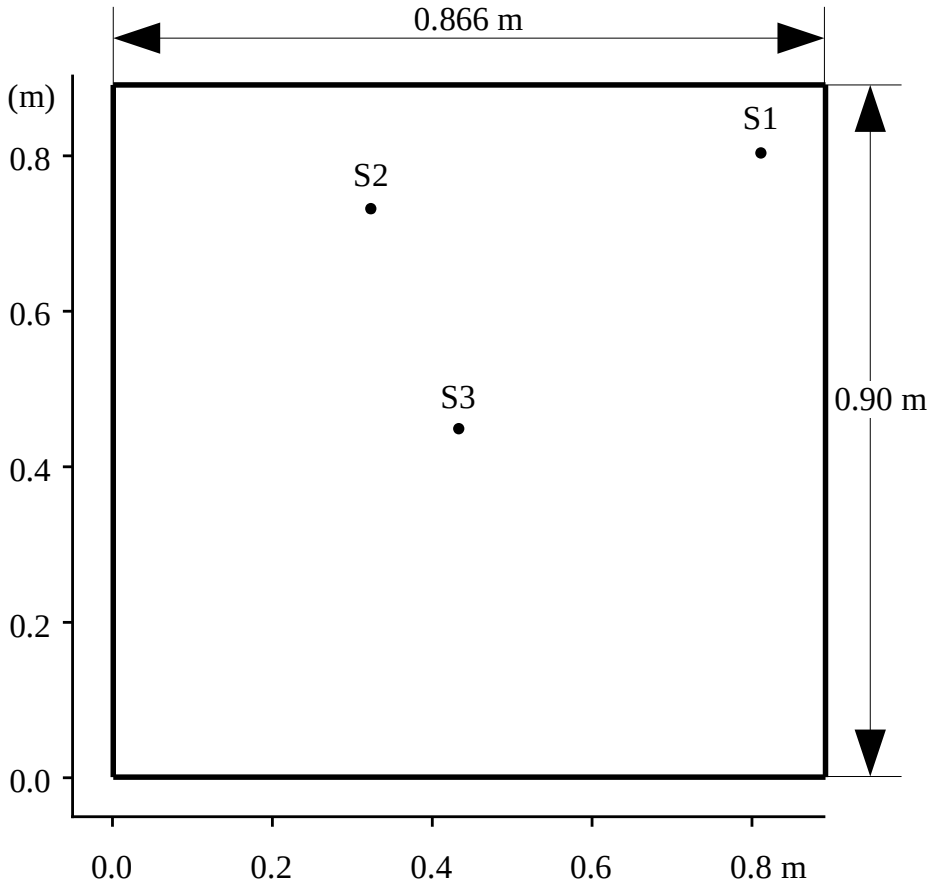

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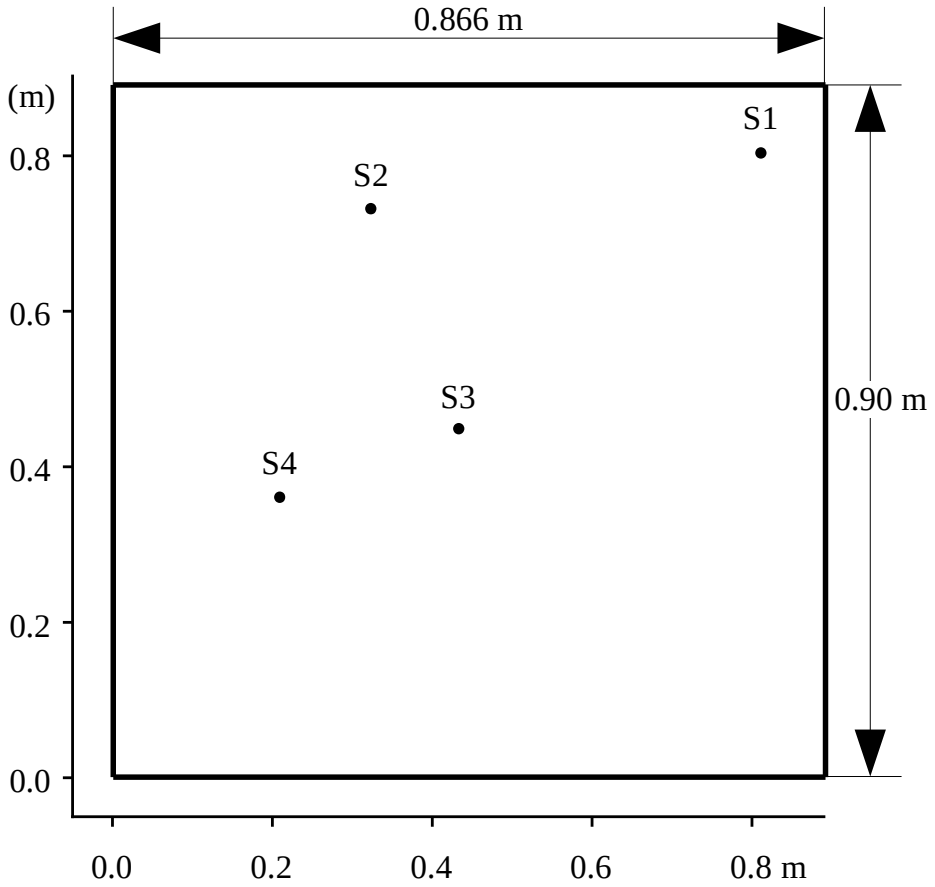

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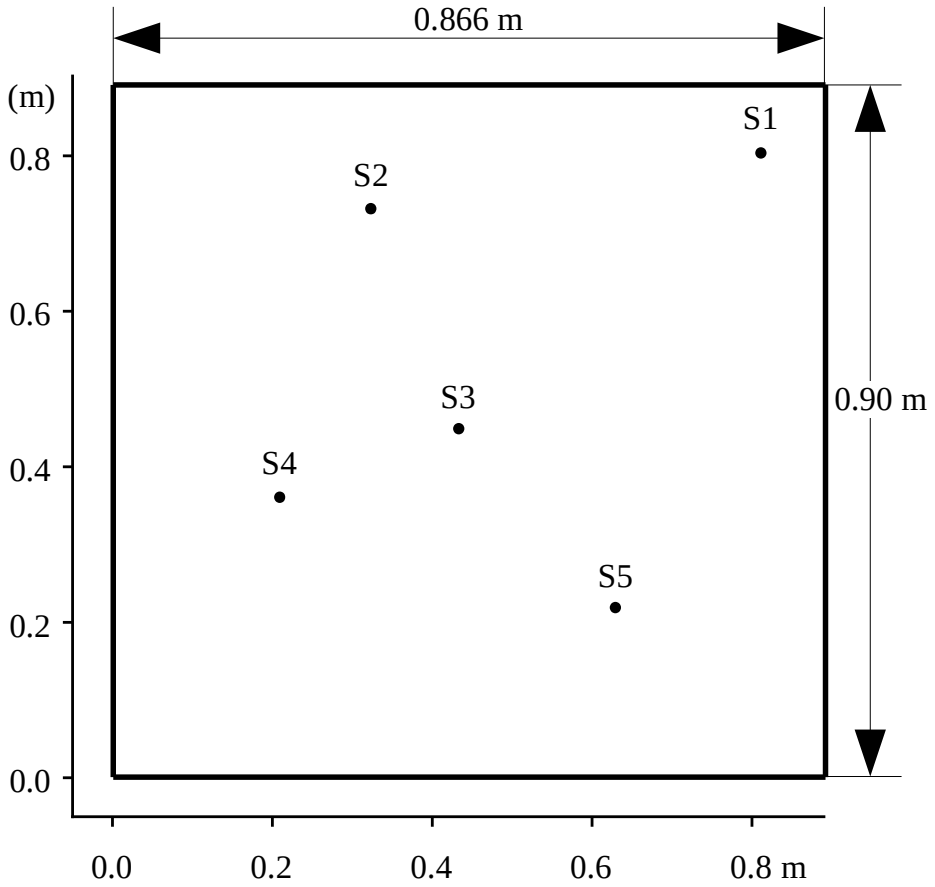

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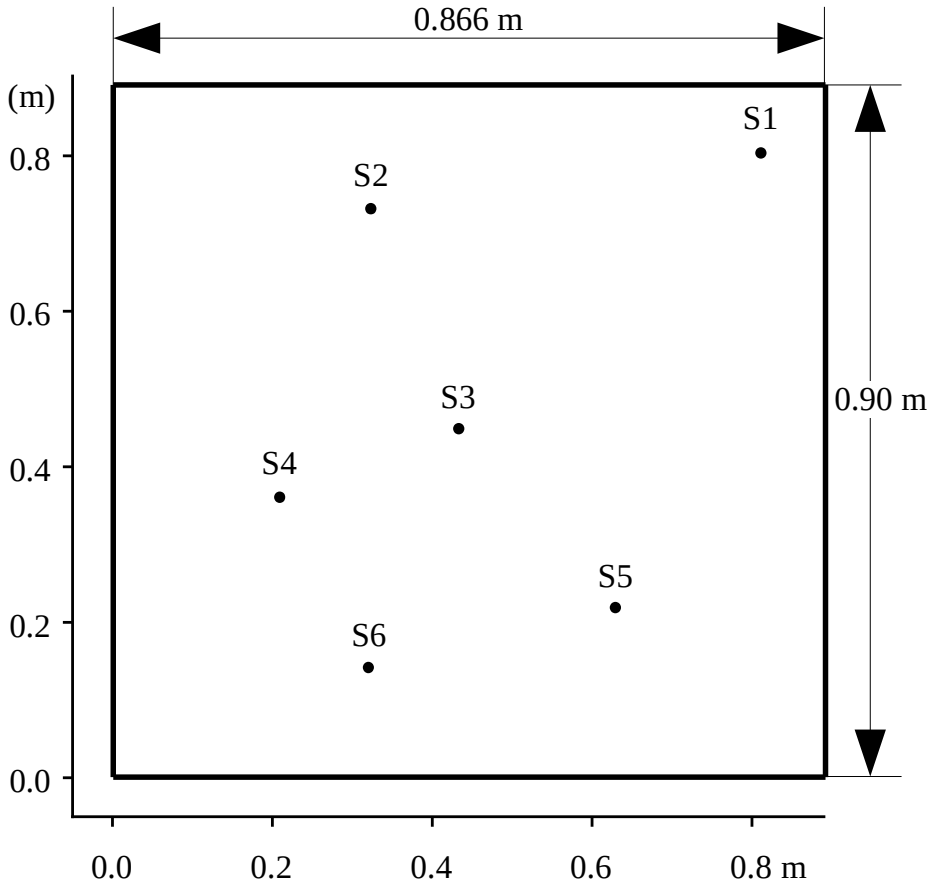

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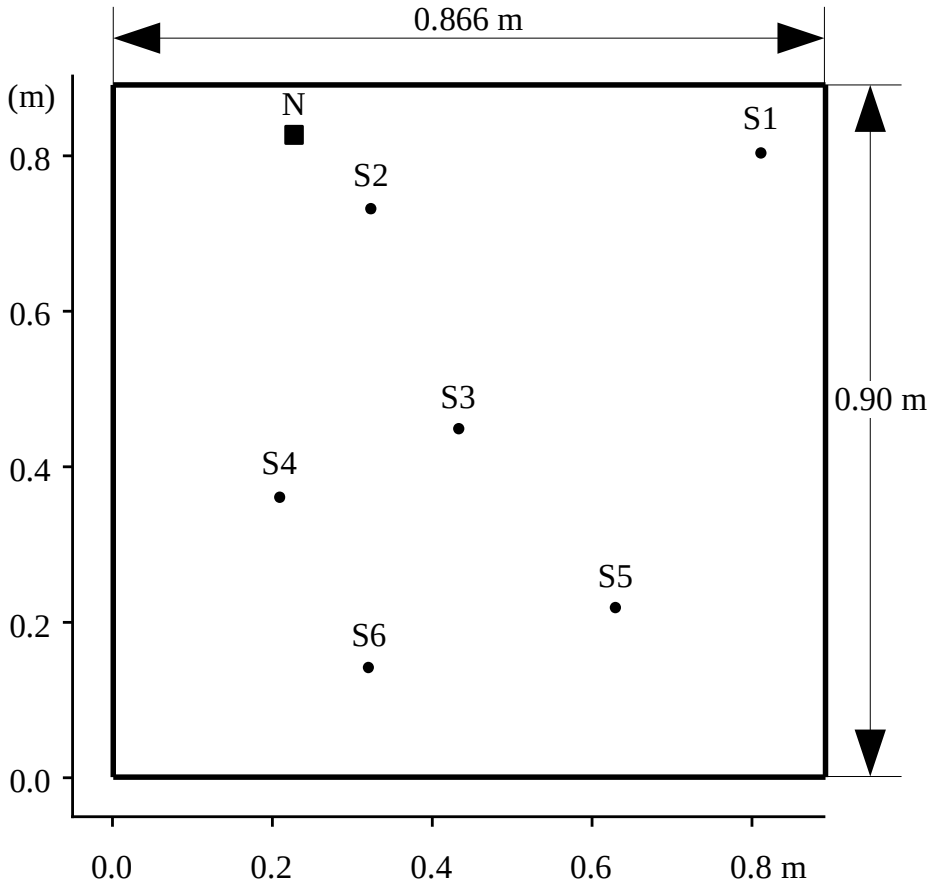

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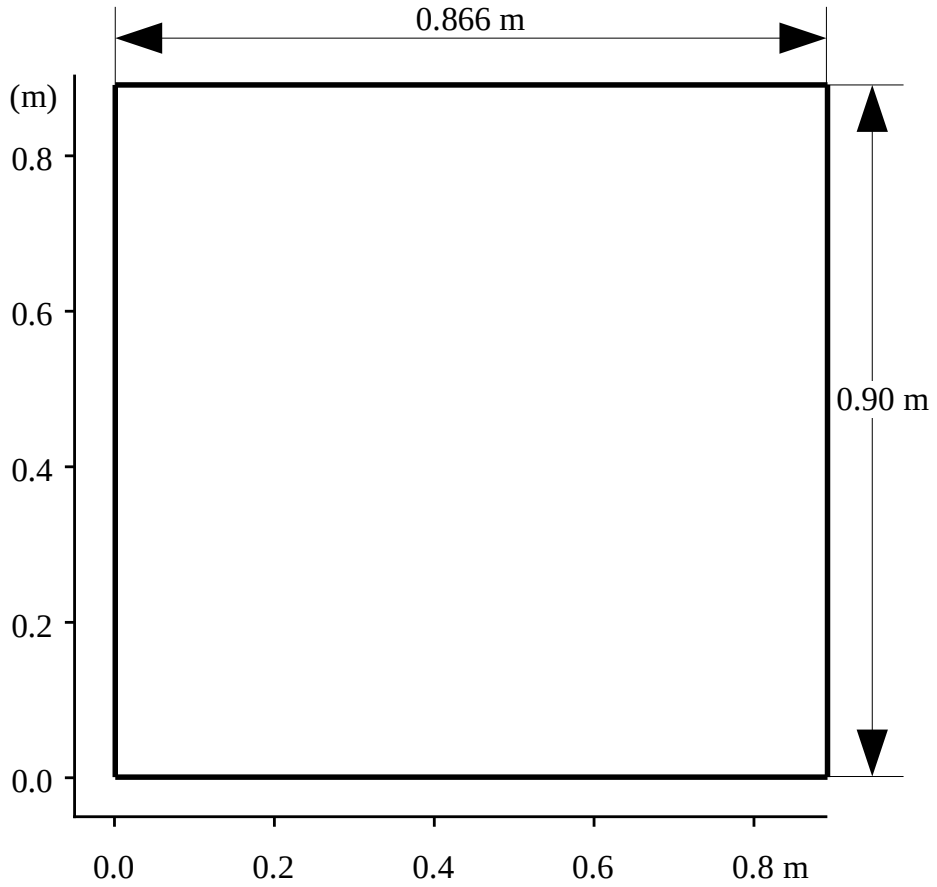

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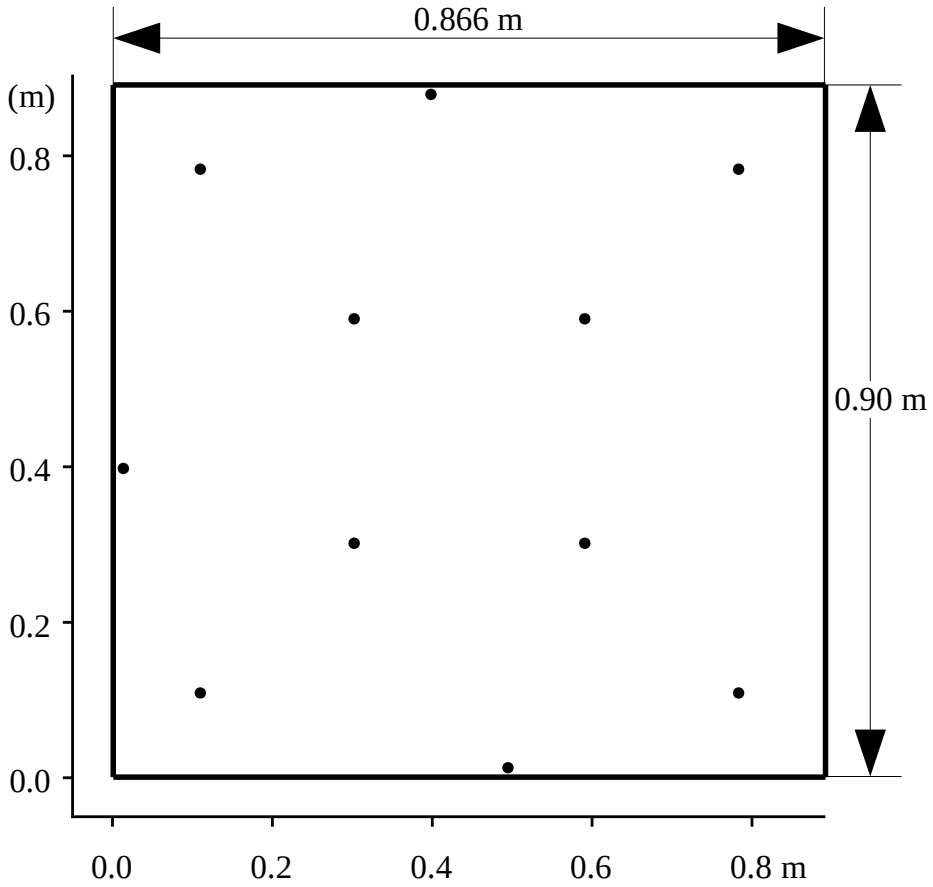

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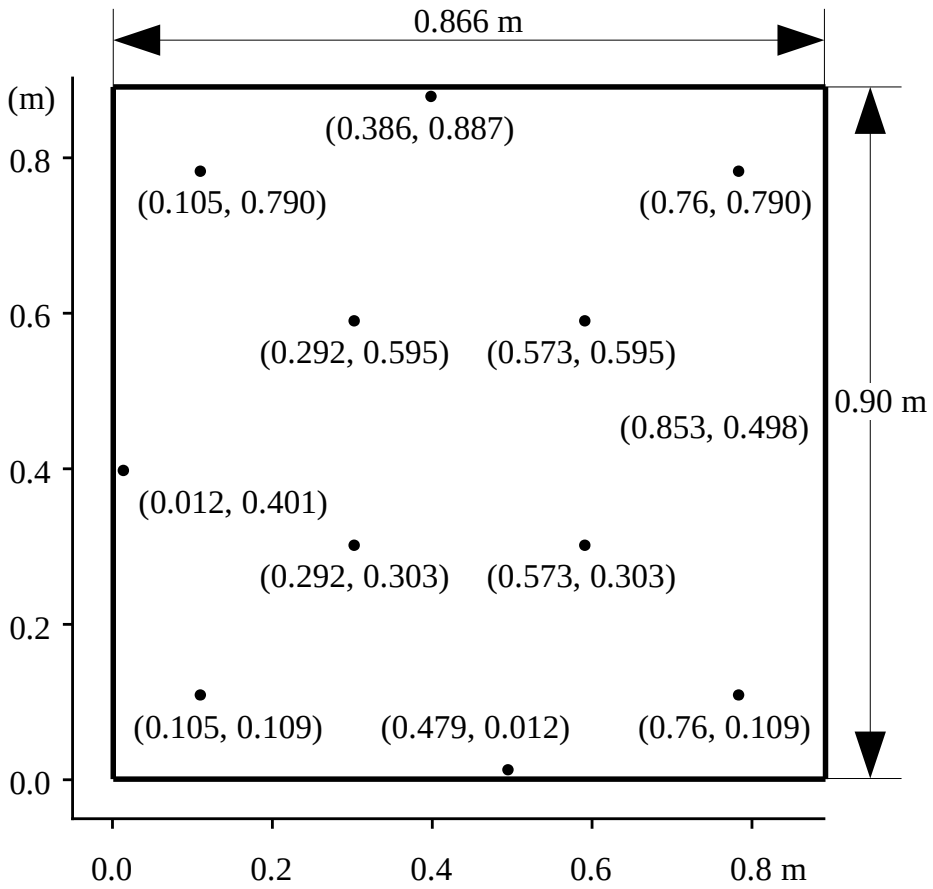

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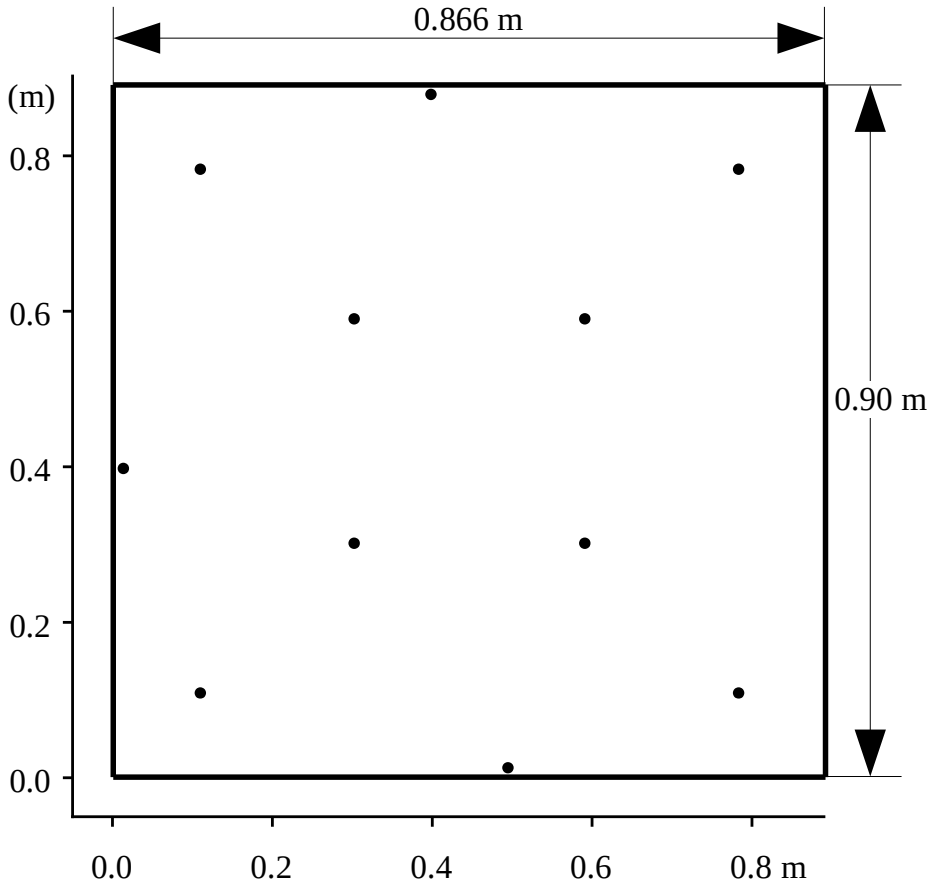

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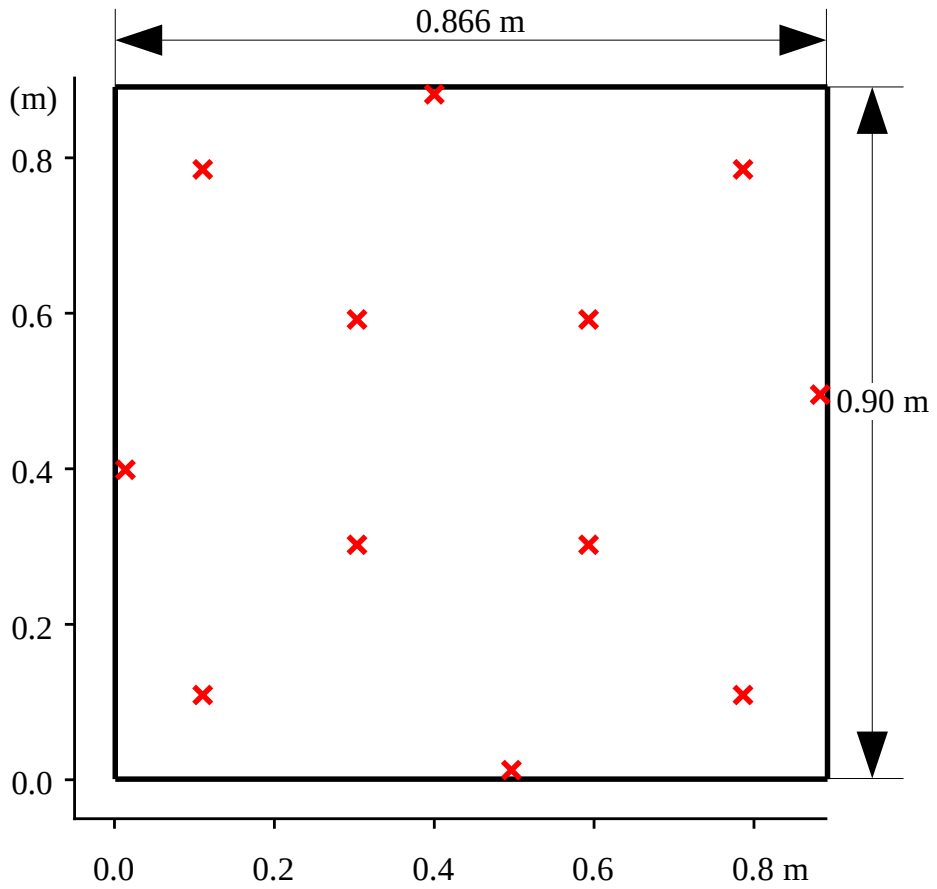

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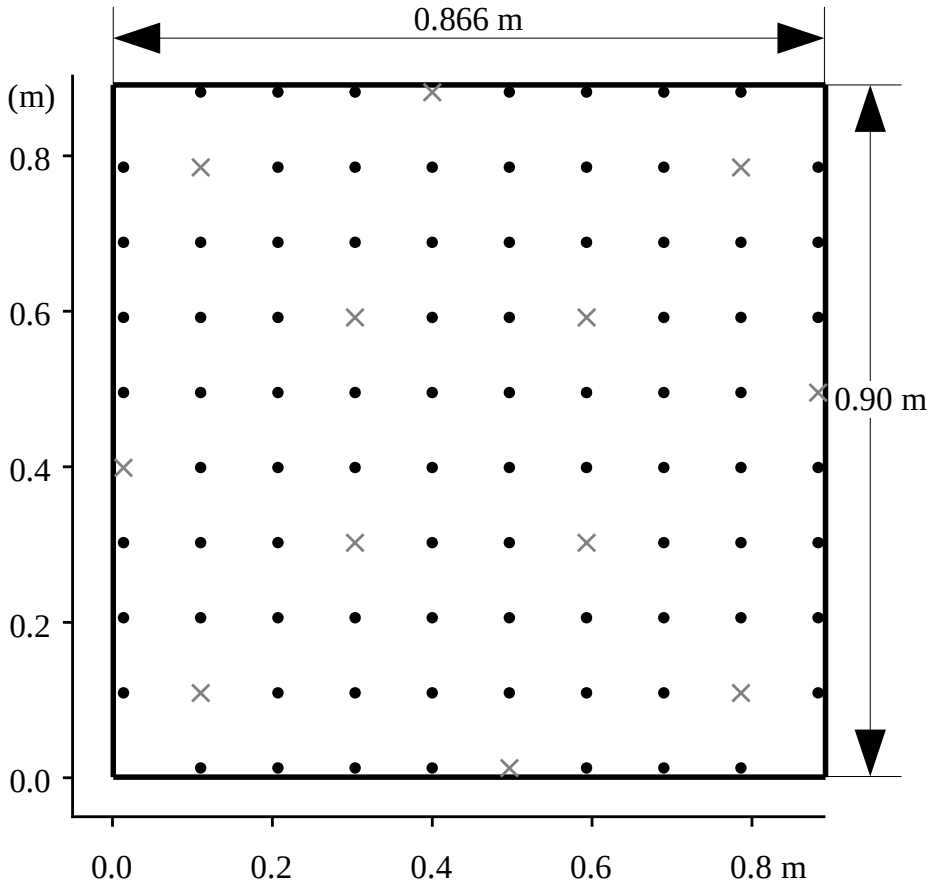

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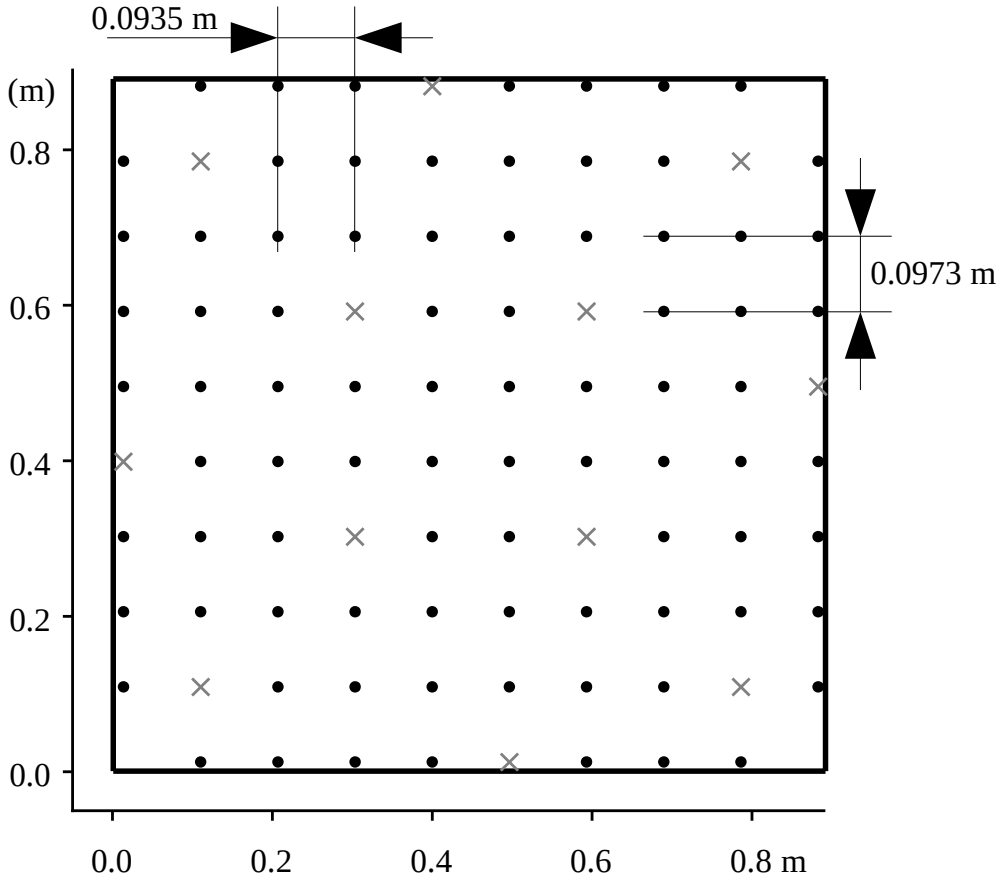

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Experimental setup:

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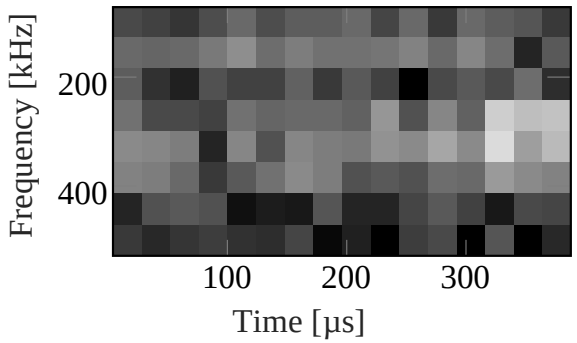
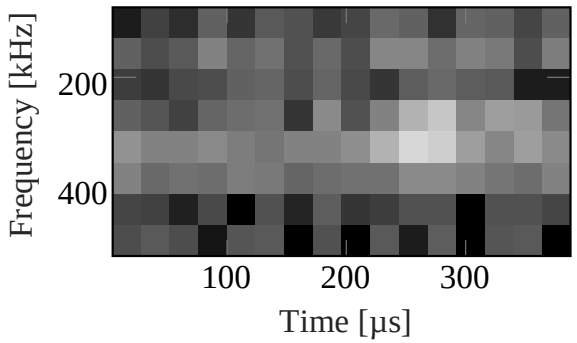
S1



S2

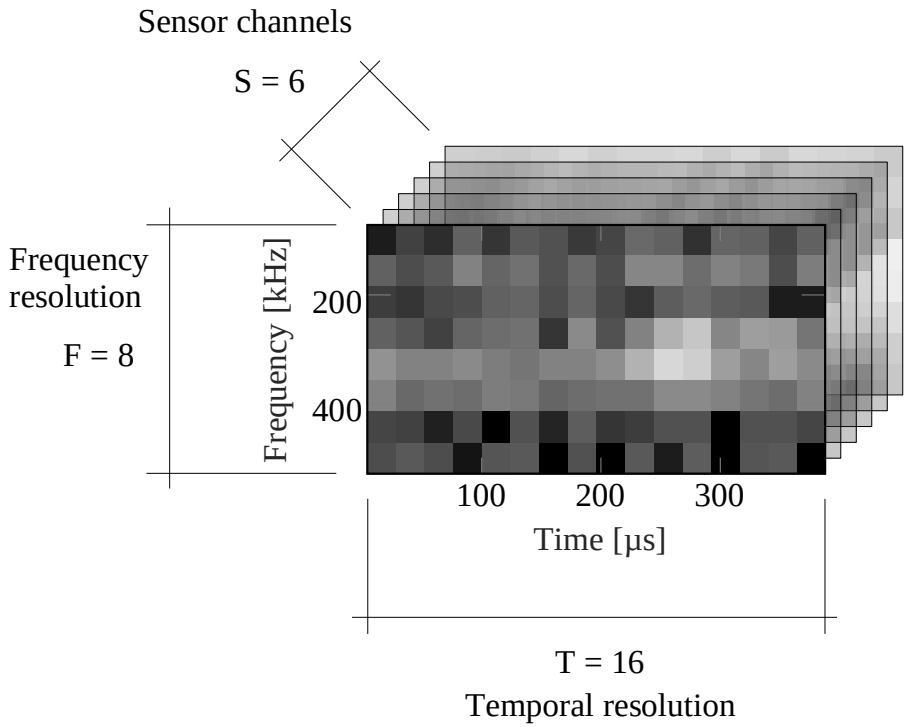


TinyML Application: CNN Sensor Analytics for Structural Health Monitoring

Experimental setup:

- Sensor and noise positions
- Training dataset
- Testing dataset
- **Model architecture**

Input tensor

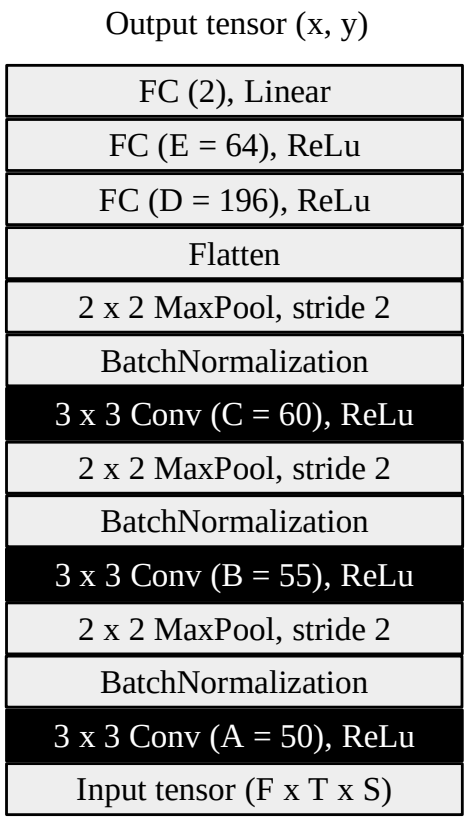


TinyML Application: CNN Sensor Analytics for Structural Health Monitoring

Experimental setup:

- Sensor and noise positions
- Training dataset
- Testing dataset
- **Model architecture**

CNN-regression model



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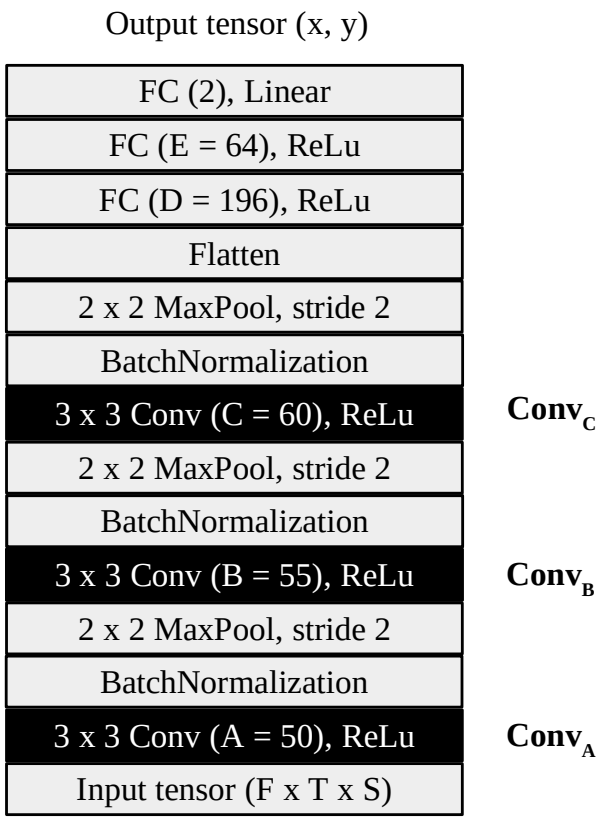

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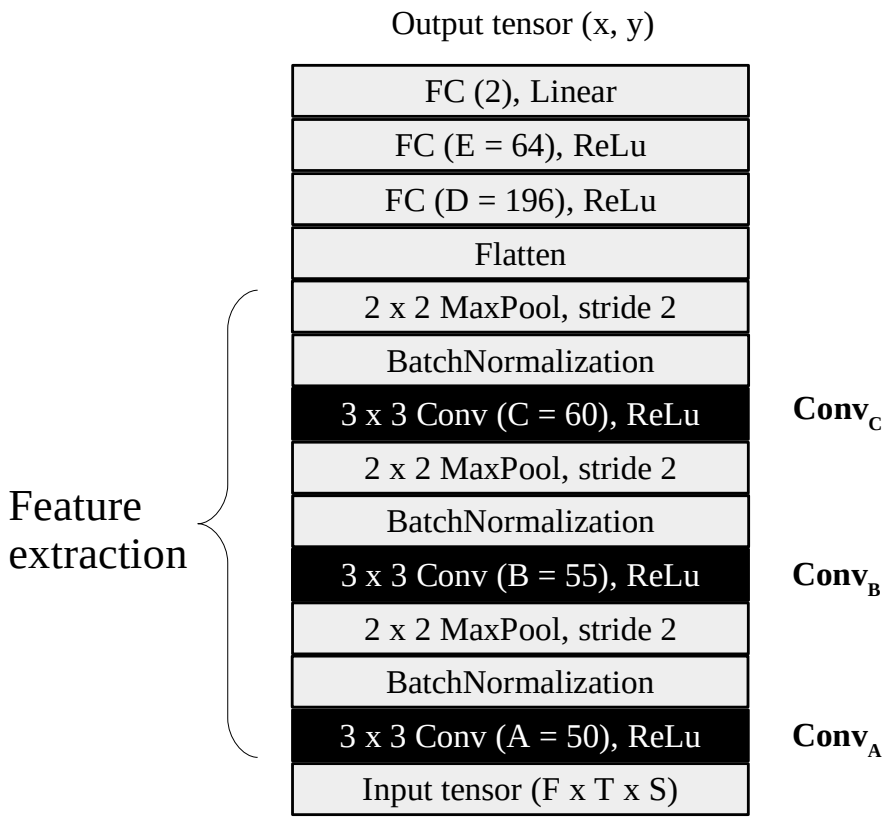

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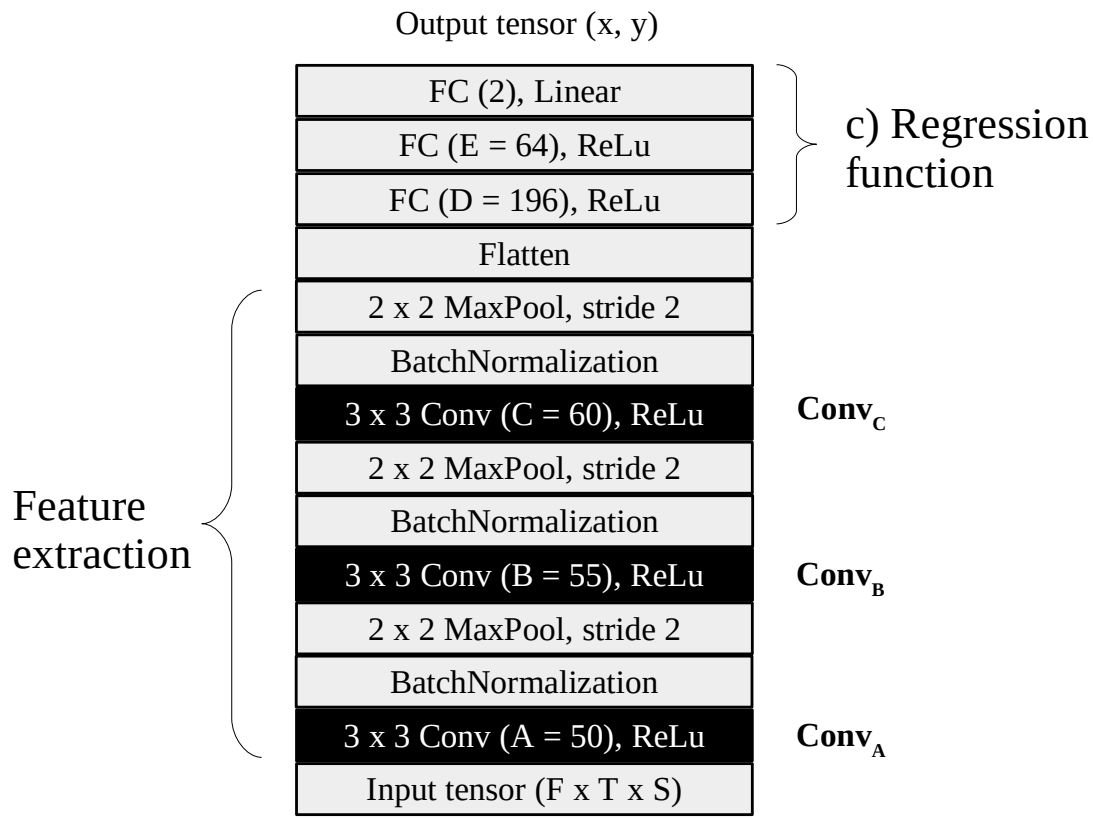

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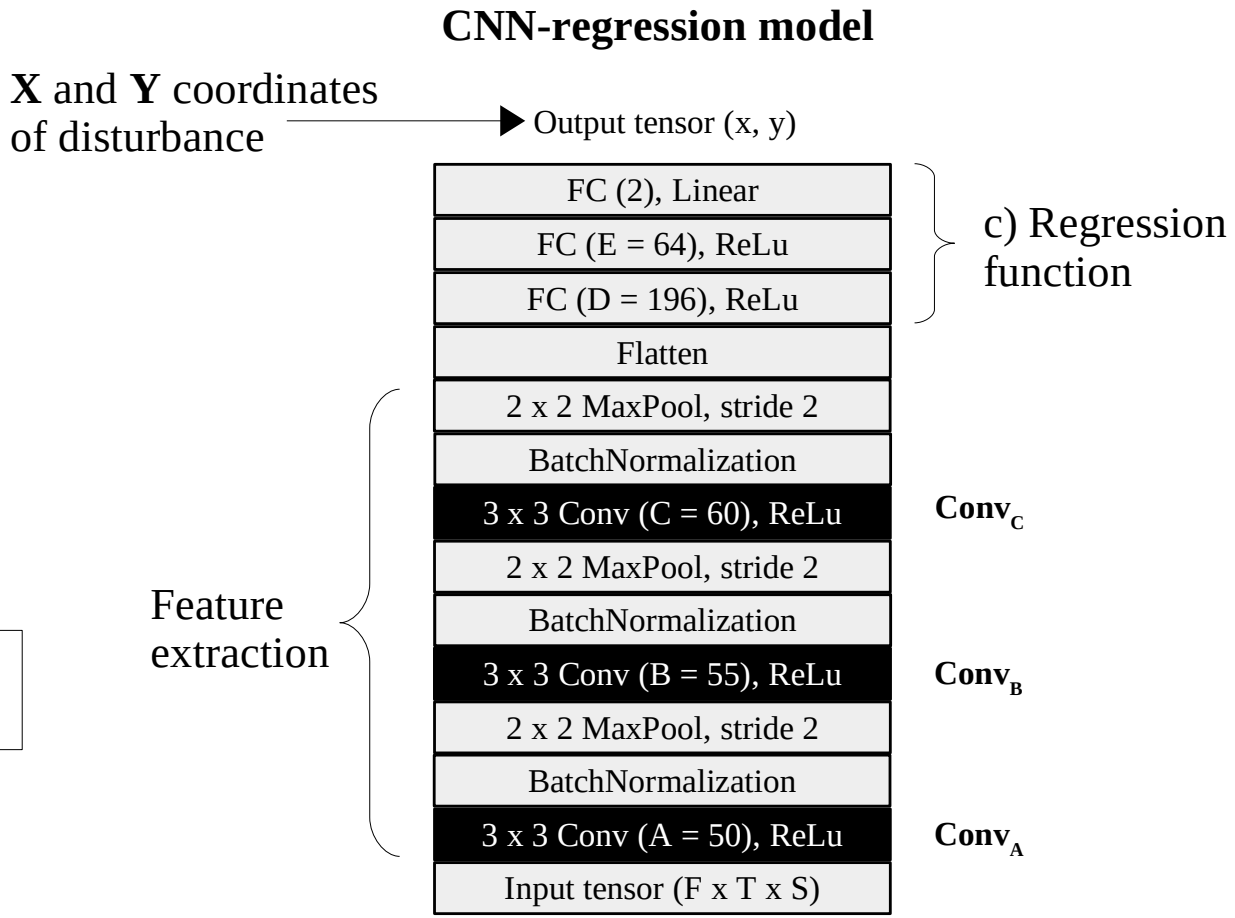
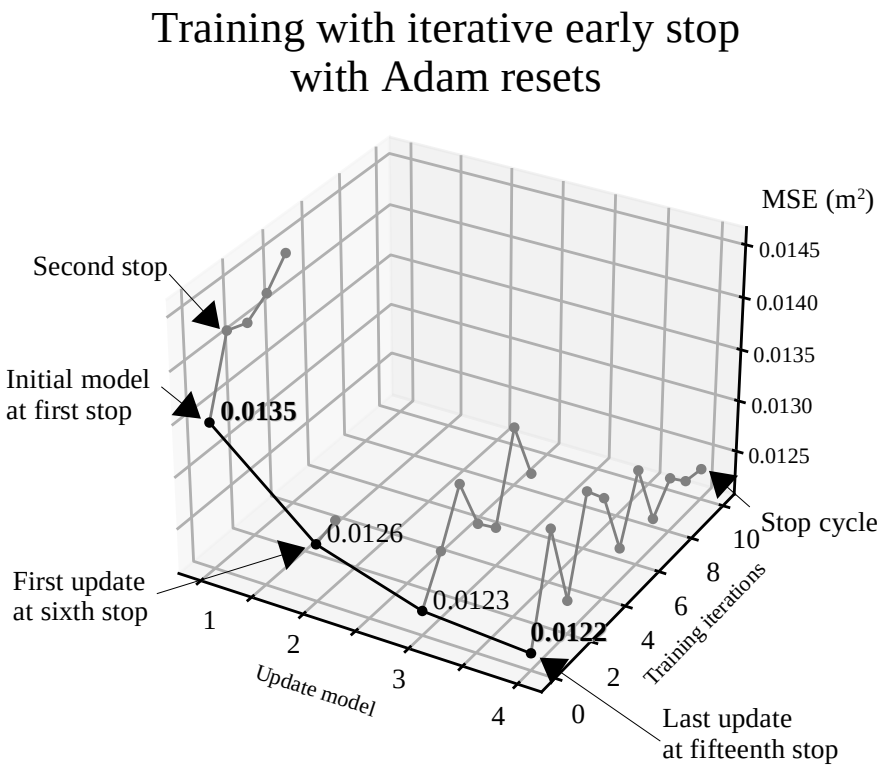
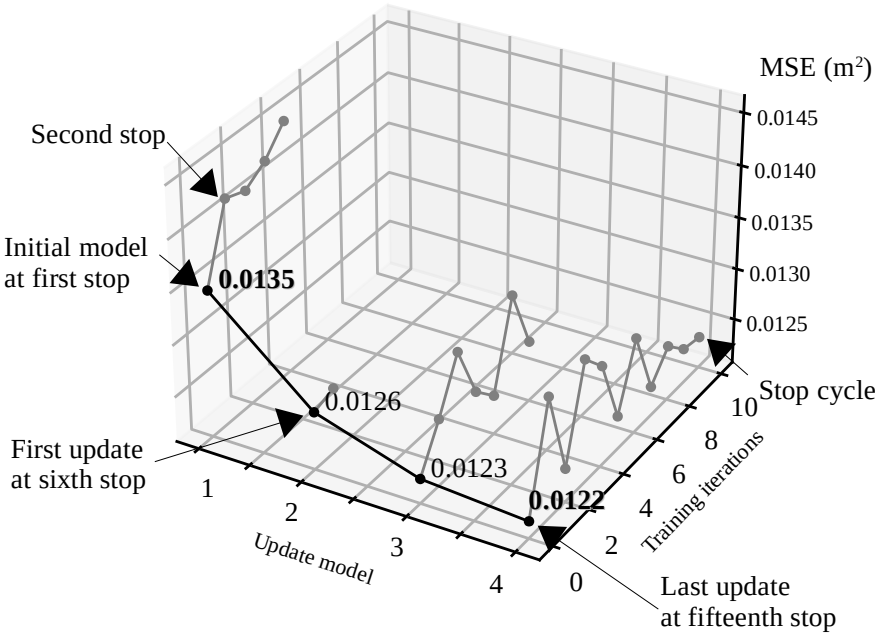


Multi-Phase Model Optimization

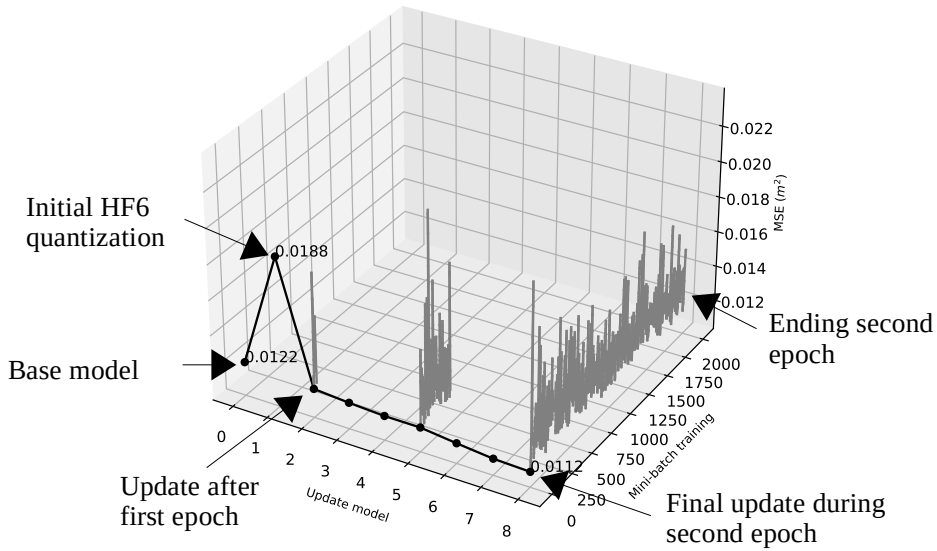


Multi-Phase Model Optimization

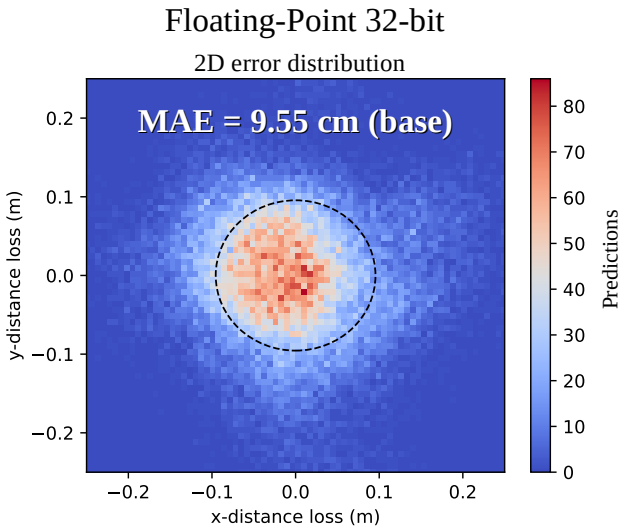
Training with iterative early stop with Adam resets



Quantization-aware training for hybrid floating-point 6-bit

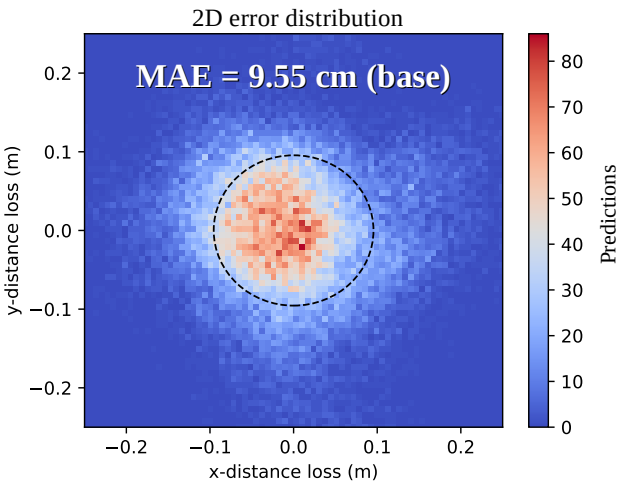


Assessing X and Y Coordinate Prediction Accuracy Across Multiple Quantization Strategies

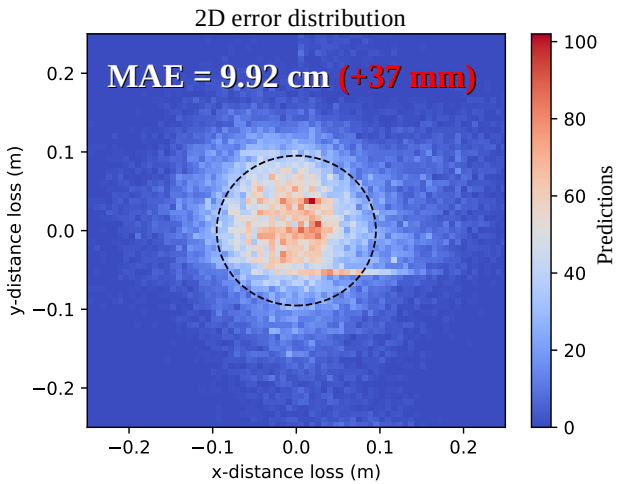


Assessing X and Y Coordinate Prediction Accuracy Across Multiple Quantization Strategies

Floating-Point 32-bit



Fixed-Point 8-bit



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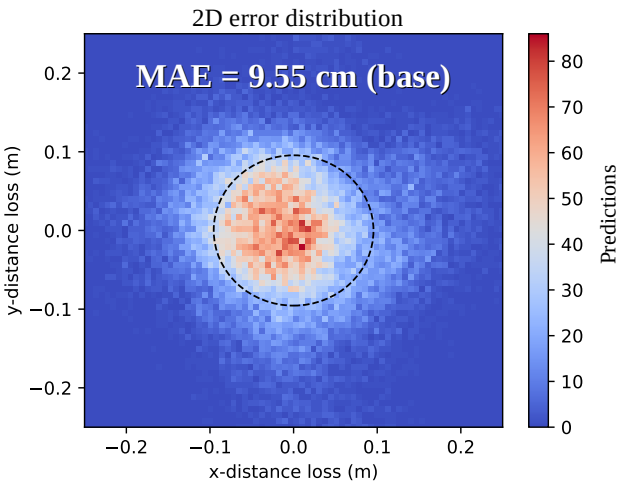

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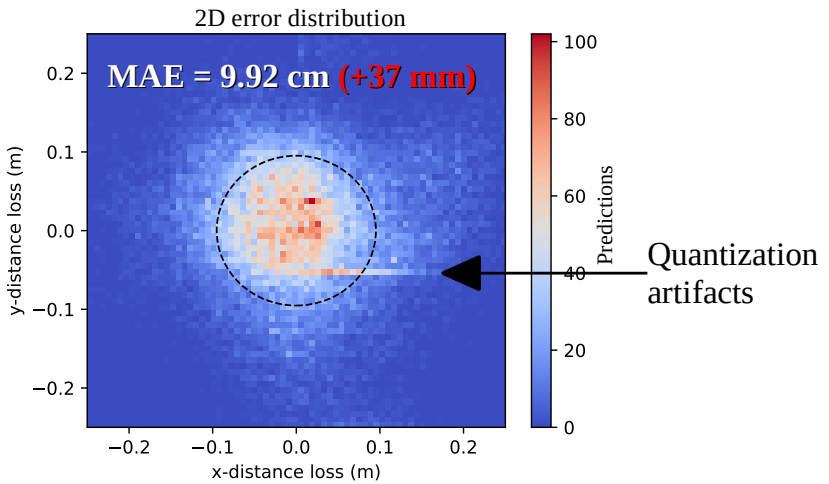

Boosting TinyML Performance with Hybrid Floating-Point 6-bit

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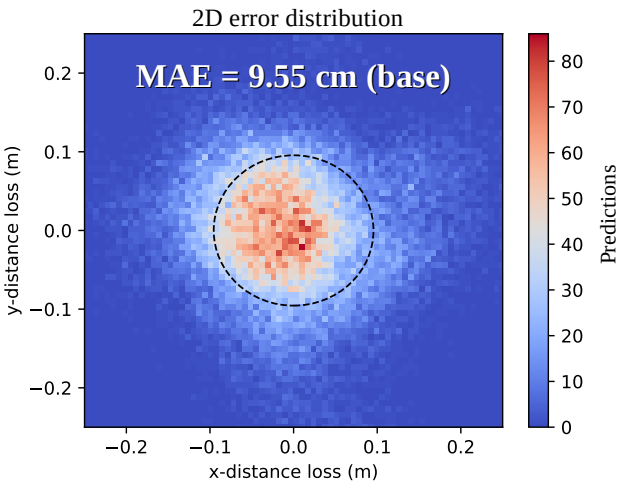
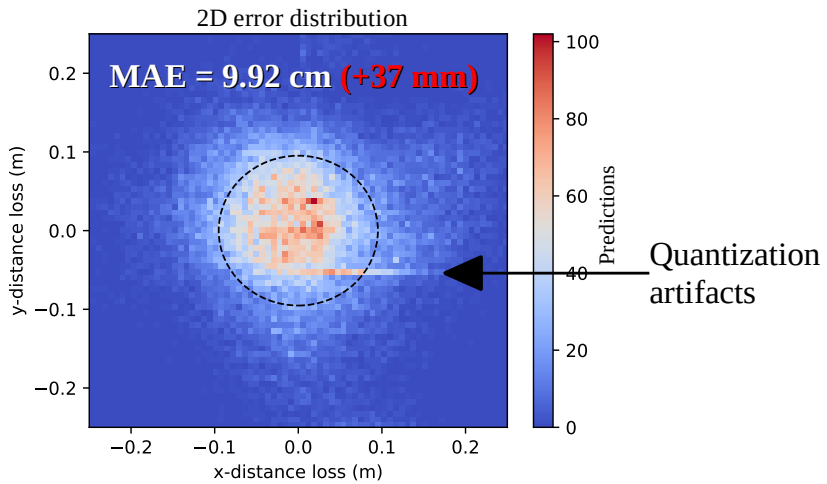
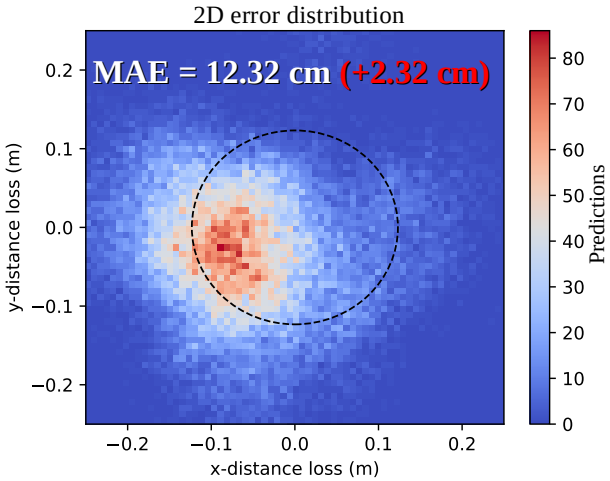
Floating-Point 32-bit



Fixed-Point 8-bit



Hybrid-Float6 (E4M1) without QAT



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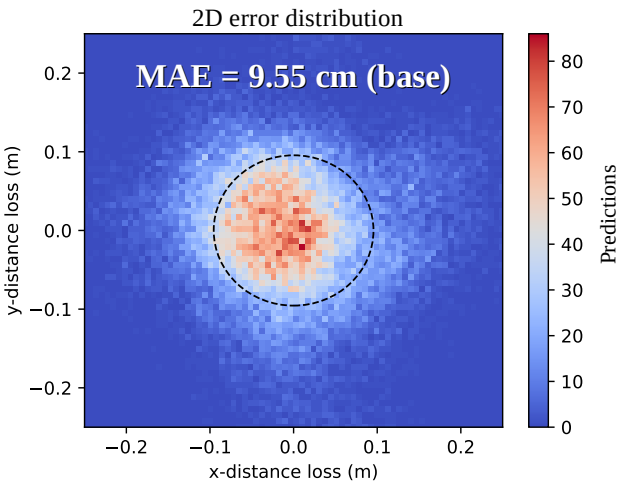

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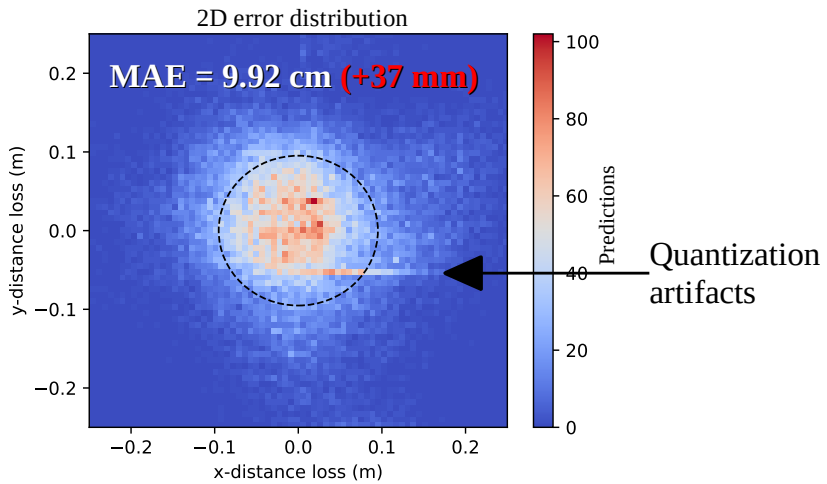

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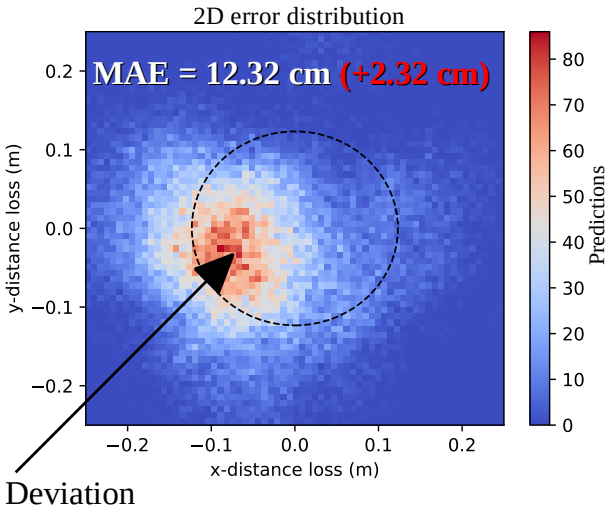

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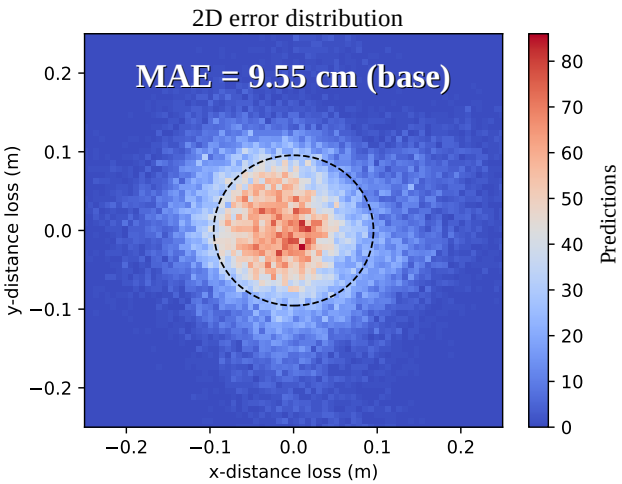

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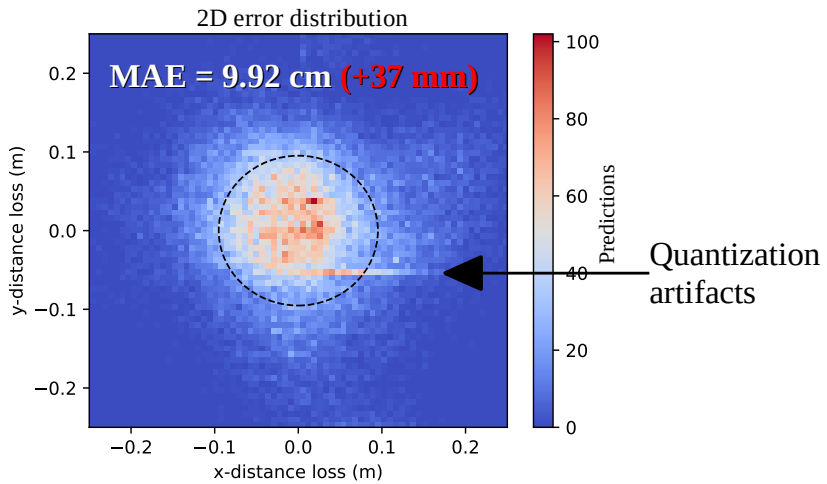

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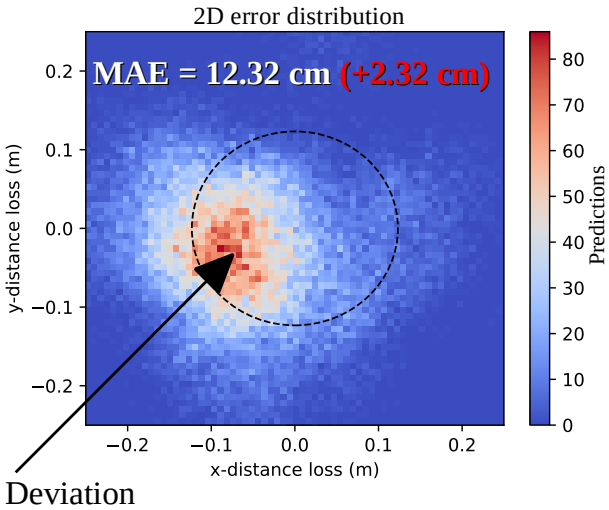

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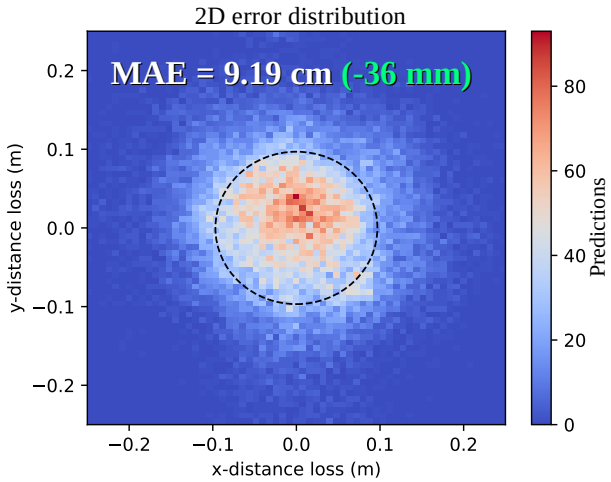

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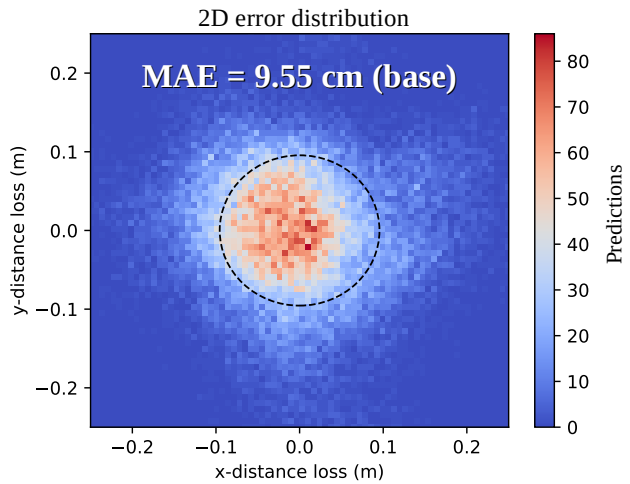
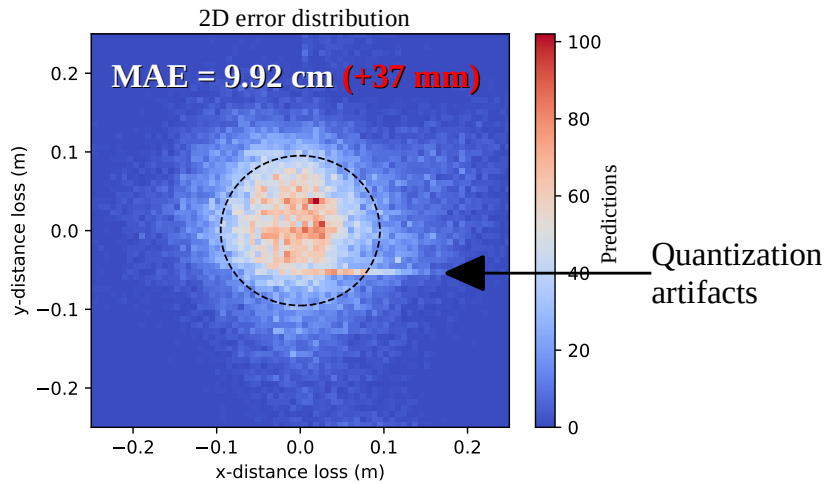


Fixed-Point 8-bit



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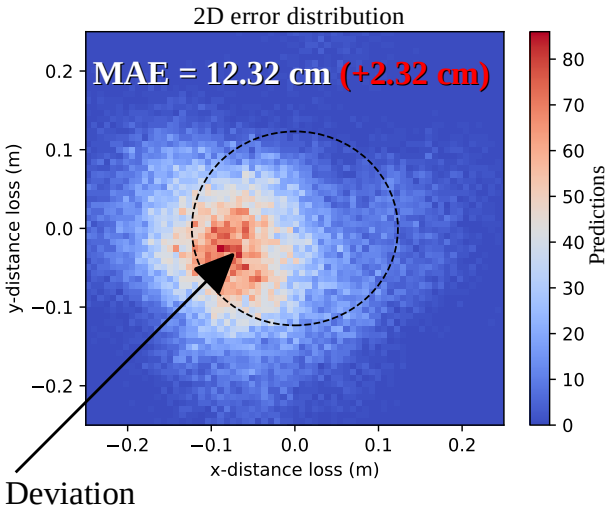

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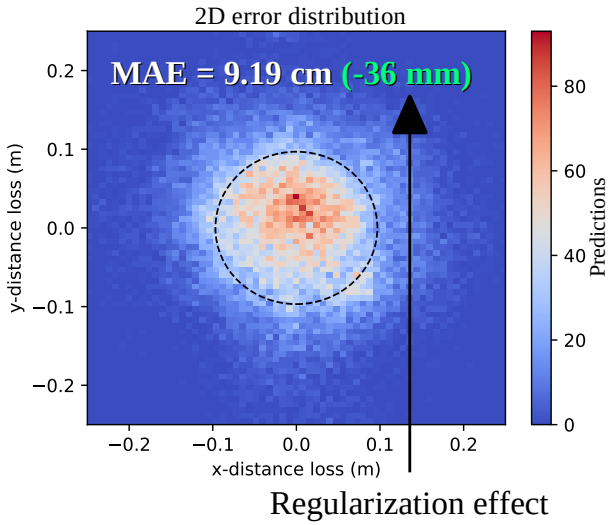

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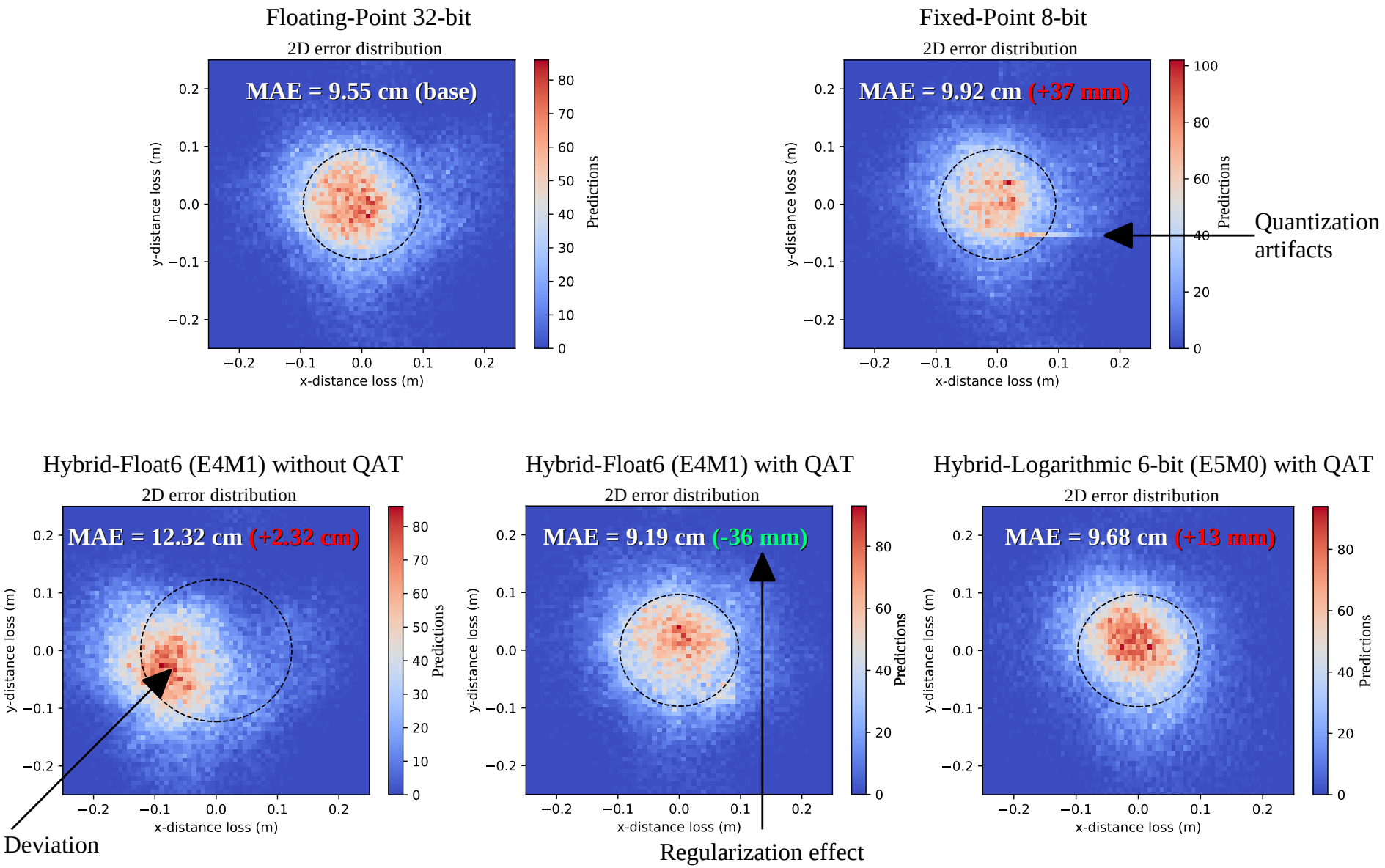
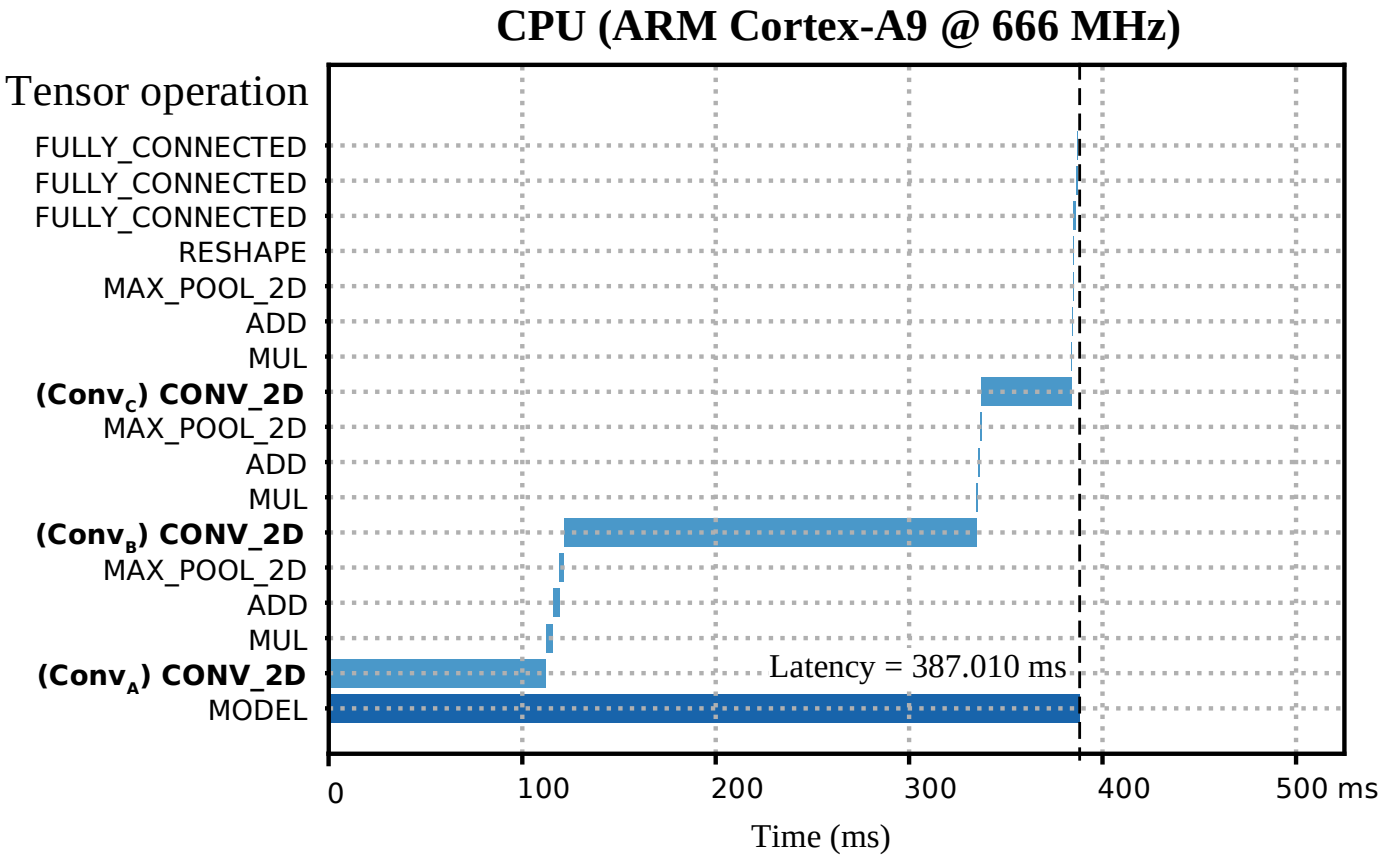


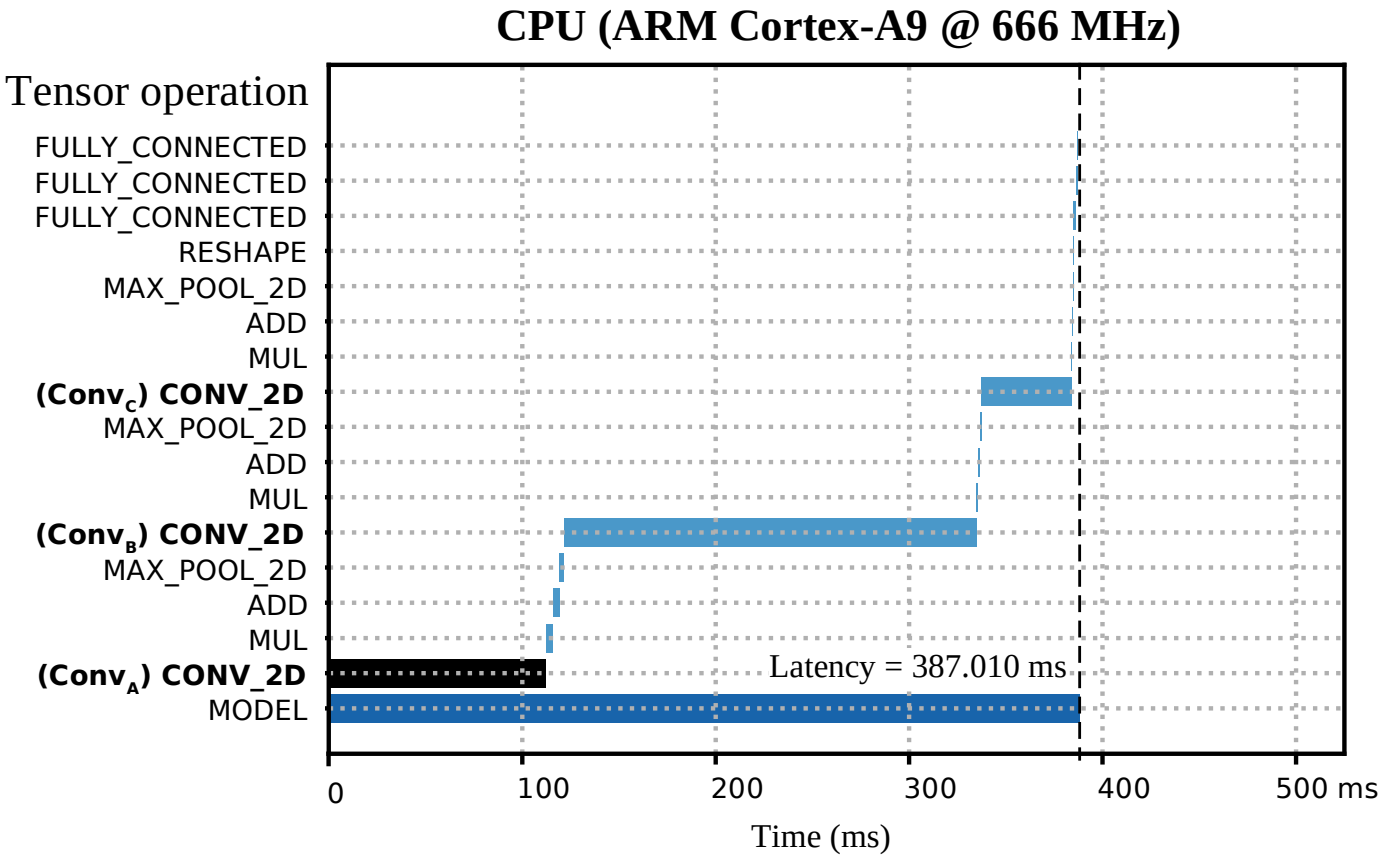
Runtime Profiling: Latencies and Scheduling on Floating-Point and Hybrid Float 6 Accelerators

Tensor Op	CPU (ms)	TP FP32 (ms)	Gain	**TP HF6 (ms)**	**Gain**
$Conv_A$					
$Conv_B$					
$Conv_C$					



Runtime Profiling: Latencies and Scheduling on Floating-Point and Hybrid Float 6 Accelerators

Tensor Op	CPU (ms)	TP FP32 (ms)	Gain	**TP HF6 (ms)**	**Gain**
$Conv_A$	112.24				
$Conv_B$					
$Conv_C$					



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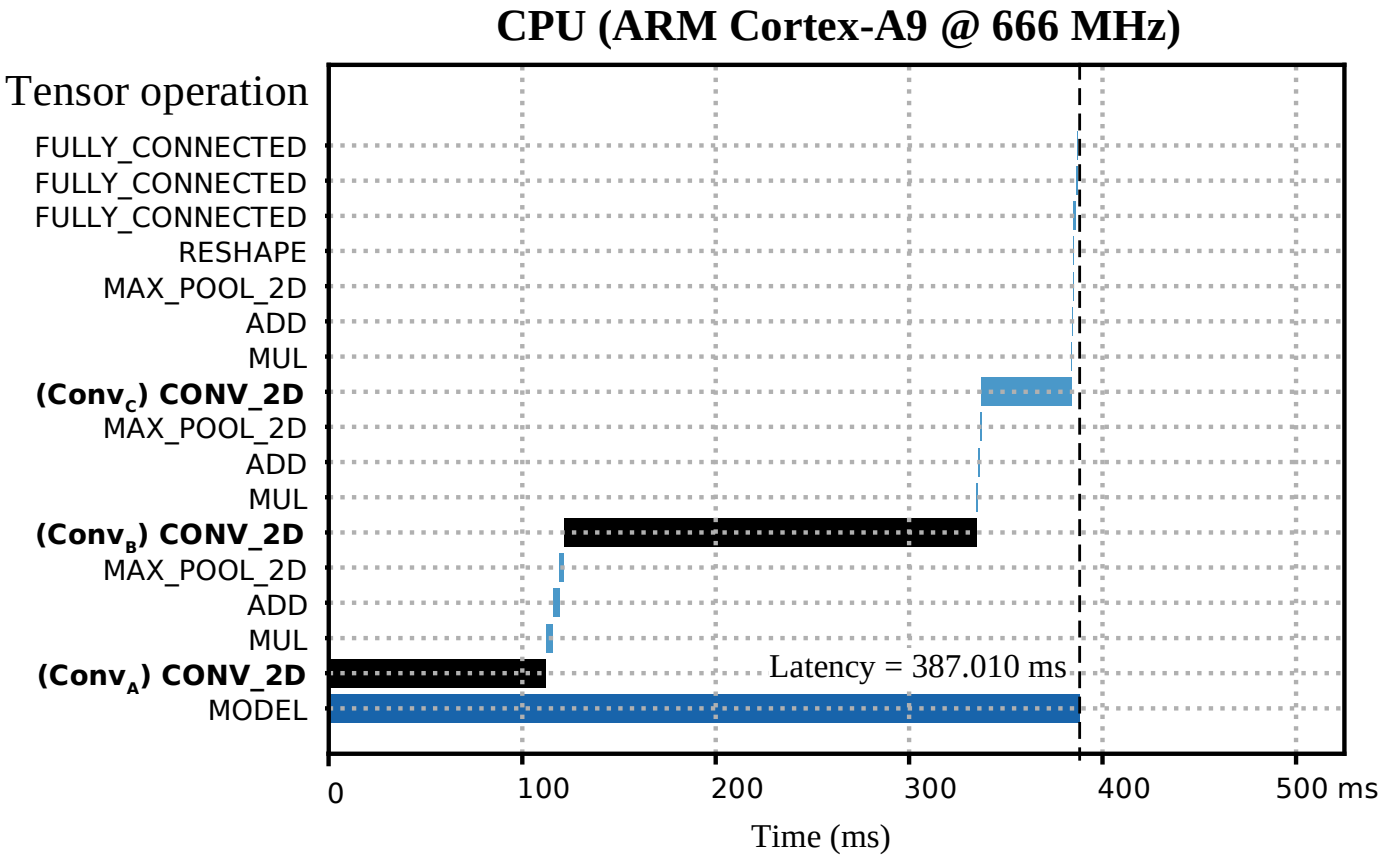

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Tensor Op	CPU (ms)	TP FP32 (ms)	Gain	**TP HF6 (ms)**	**Gain**
$Conv_A$	112.24				
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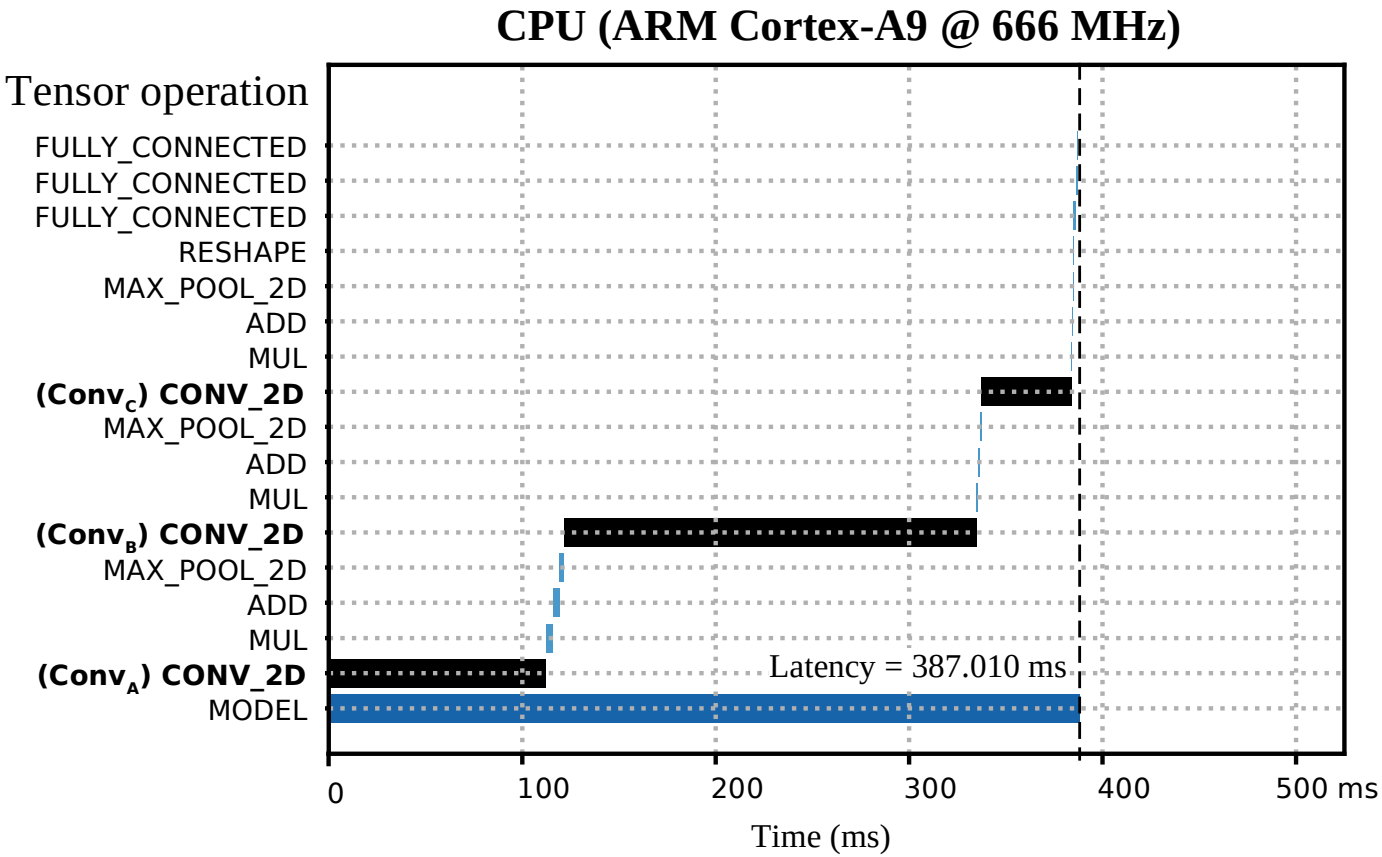

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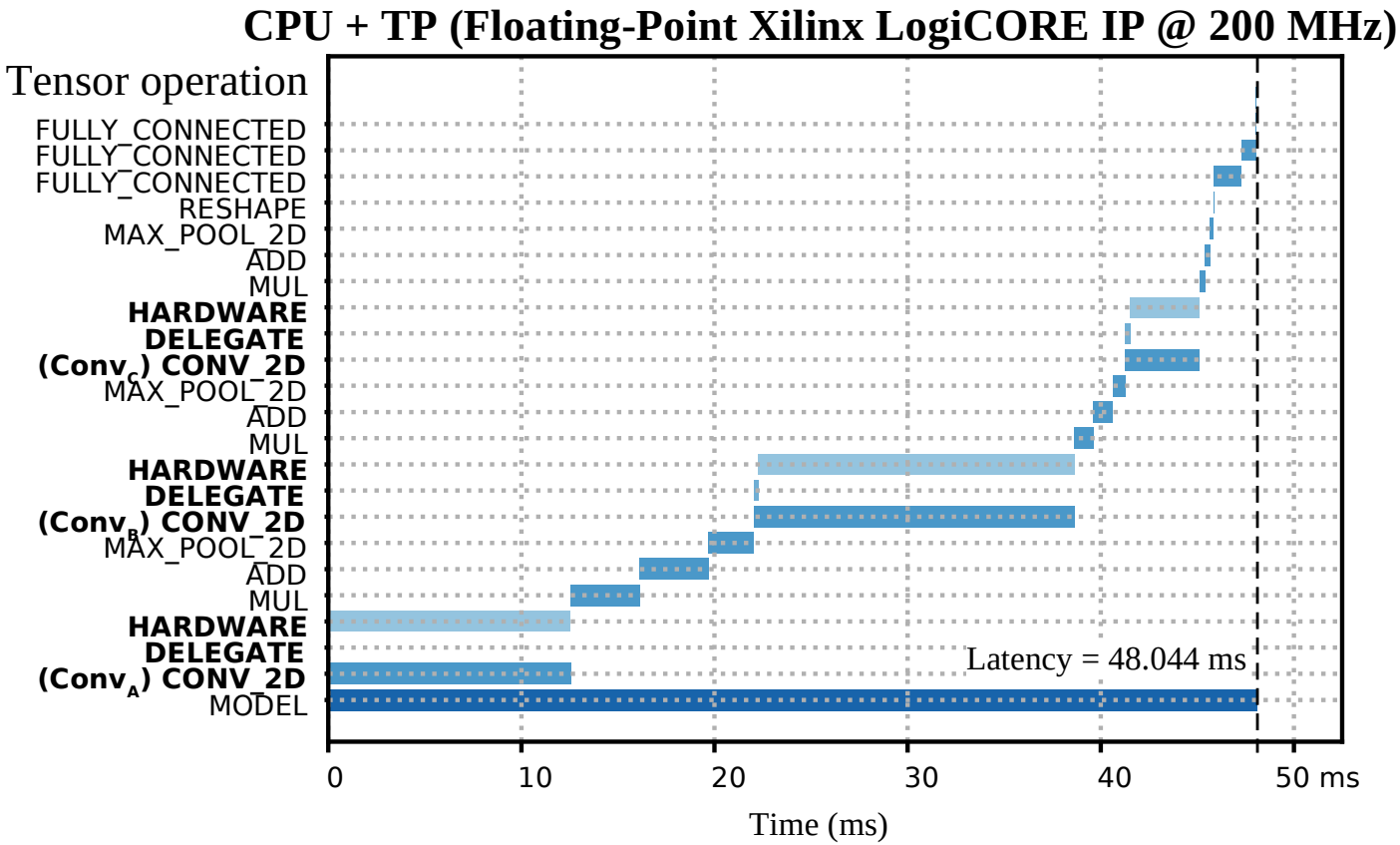

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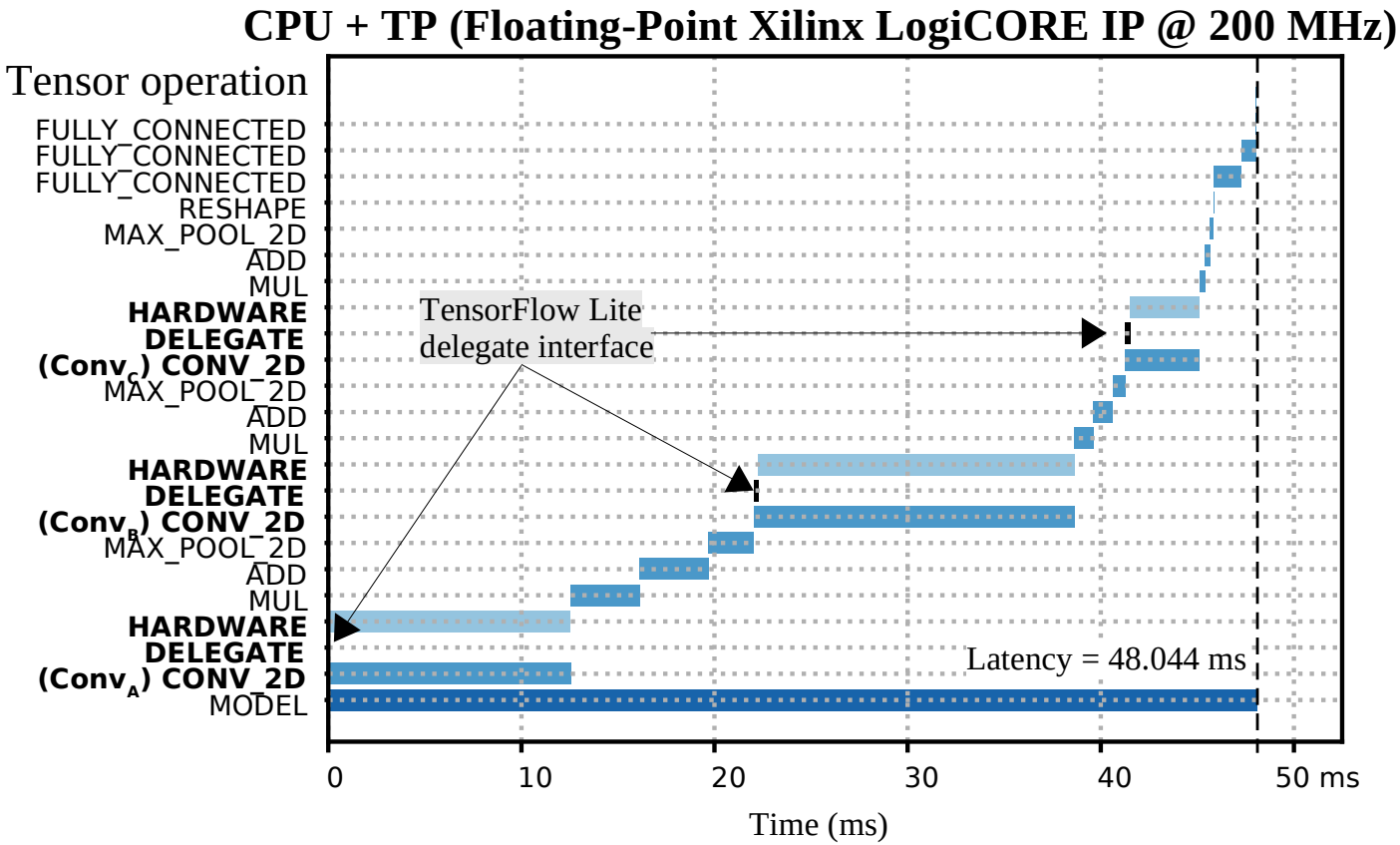

Runtime Profiling: Latencies and Scheduling on Floating-Point and Hybrid Float 6 Accelerators

Tensor Op	CPU (ms)	TP FP32 (ms)	Gain	**TP HF6 (ms)**	**Gain**
$Conv_A$	112.24	12.49	8.9		
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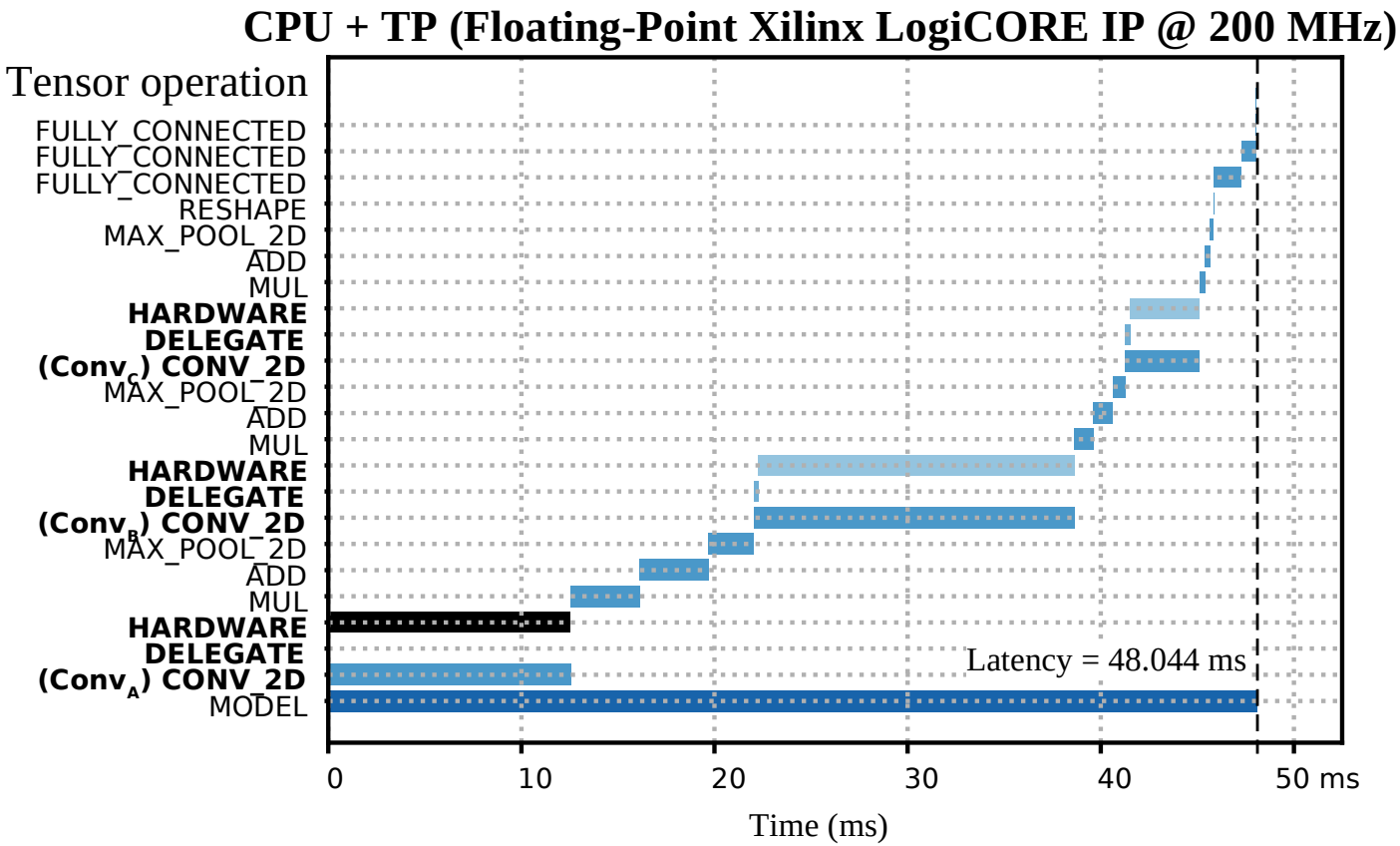

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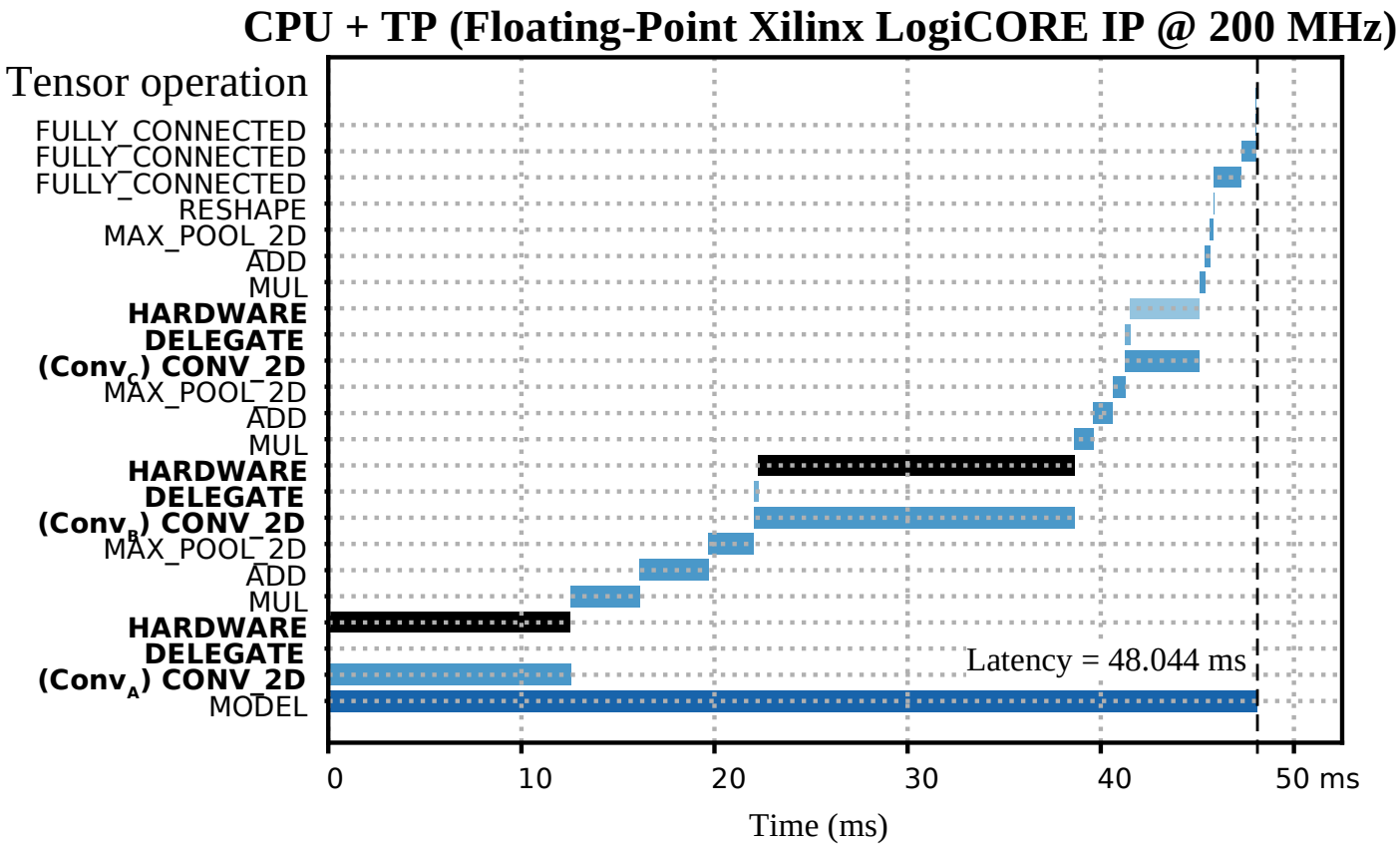
Tensor Op	CPU (ms)	TP FP32 (ms)	Gain	**TP HF6 (ms)**	**Gain**
$Conv_A$	112.24	12.49	8.9		
$Conv_B$	213.13	16.39	13.0		
$Conv_C$	46.59				



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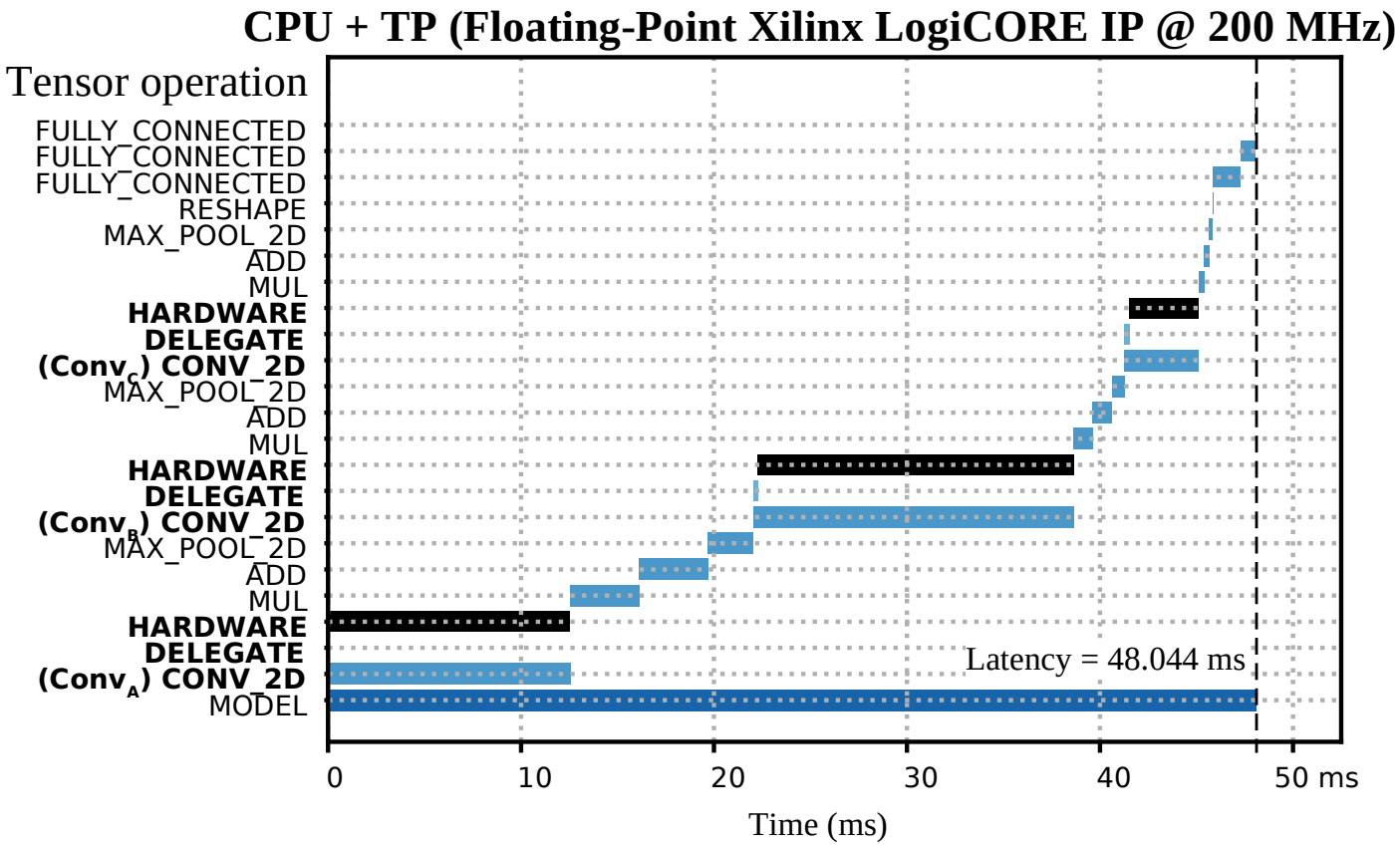

Runtime Profiling: Latencies and Scheduling on Floating-Point and Hybrid Float 6 Accelerators

Tensor Op	CPU (ms)	TP FP32 (ms)	Gain	**TP HF6 (ms)**	**Gain**
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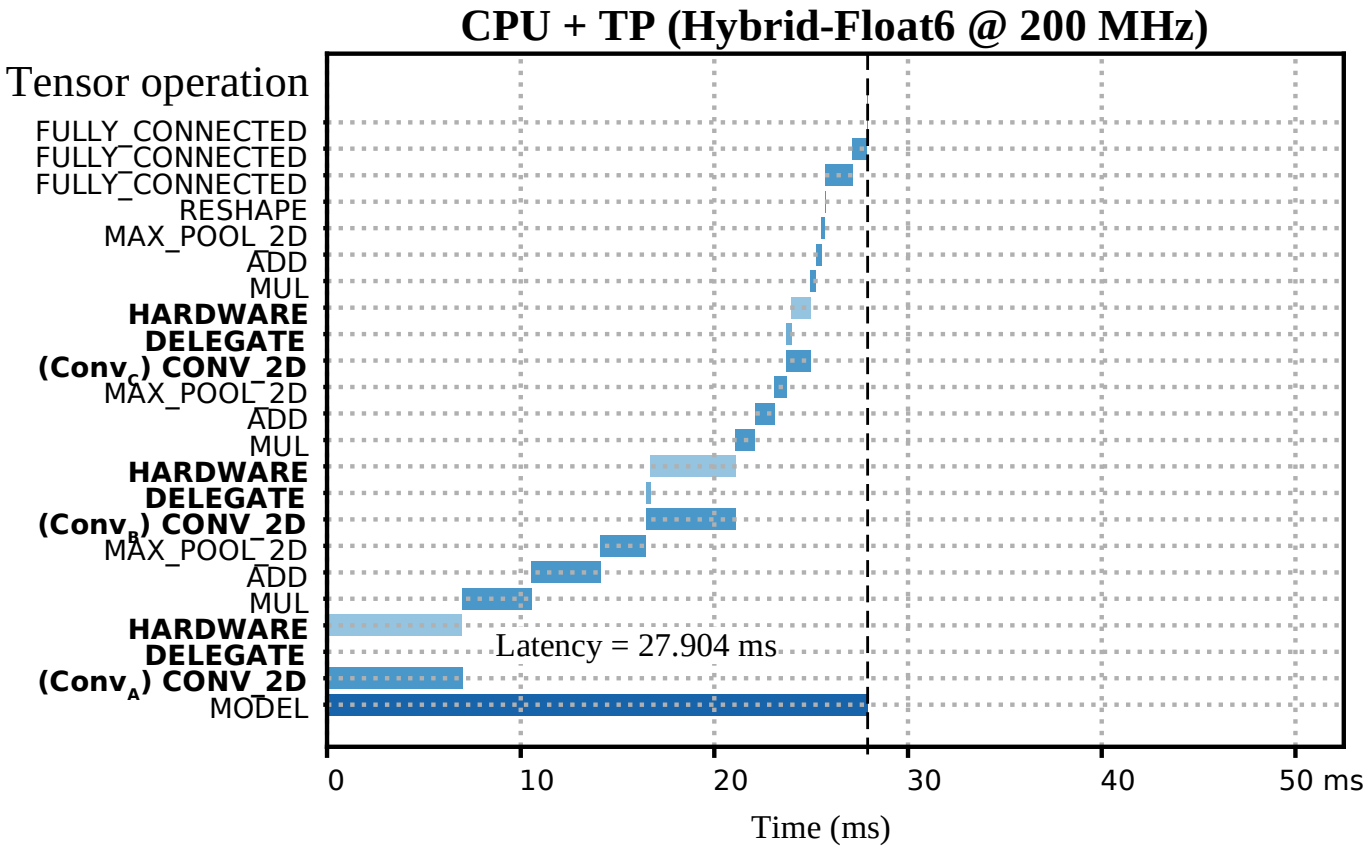
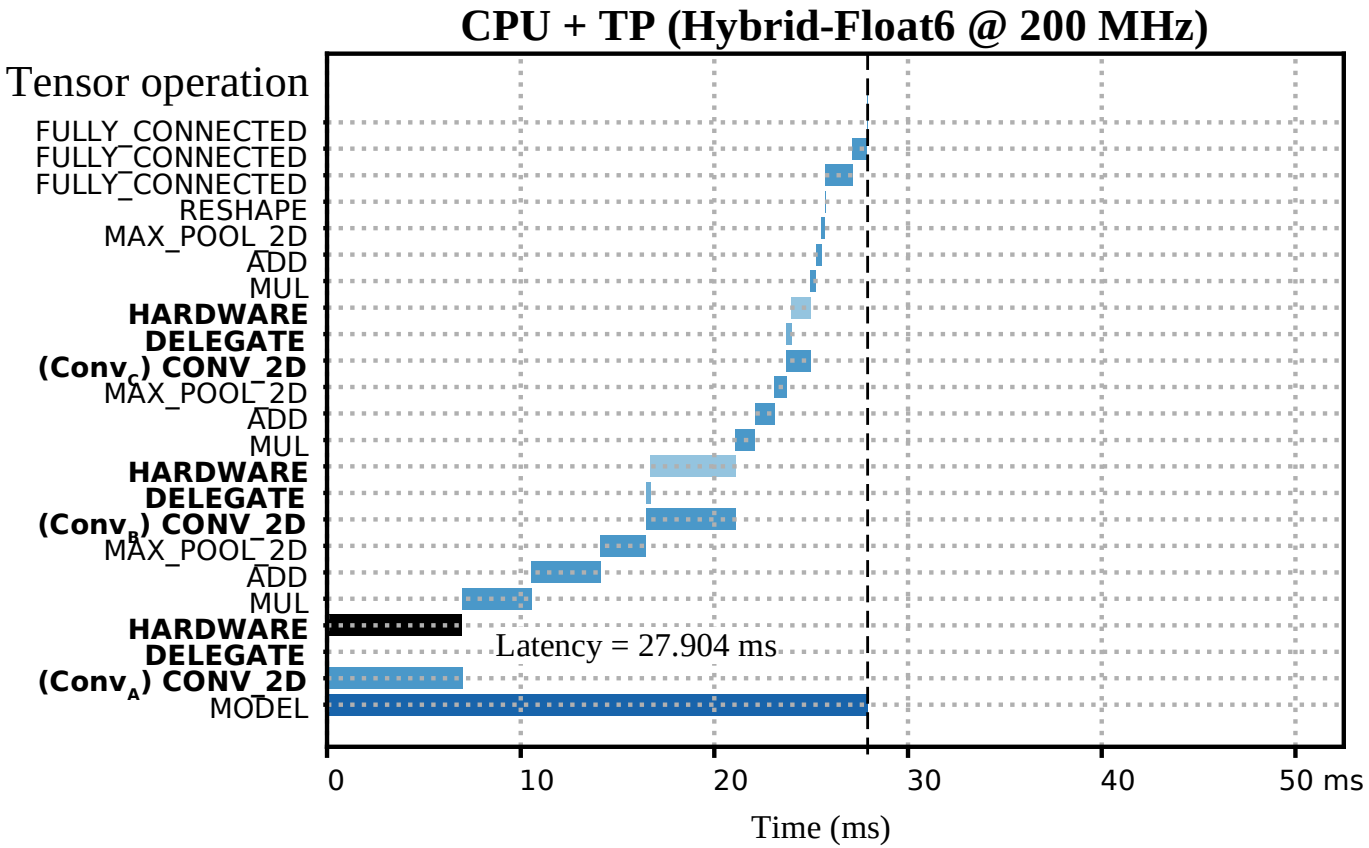


Runtime Profiling: Latencies and Scheduling on Floating-Point and Hybrid Float 6 Accelerators

Tensor Op	CPU (ms)	TP FP32 (ms)	Gain	**TP HF6 (ms)**	**Gain**
$Conv_A$	112.24	12.49	8.9	**6.92**	**16.2**
$Conv_B$	213.13	16.39	13.0		
$Conv_C$	46.59	3.59	12.9		



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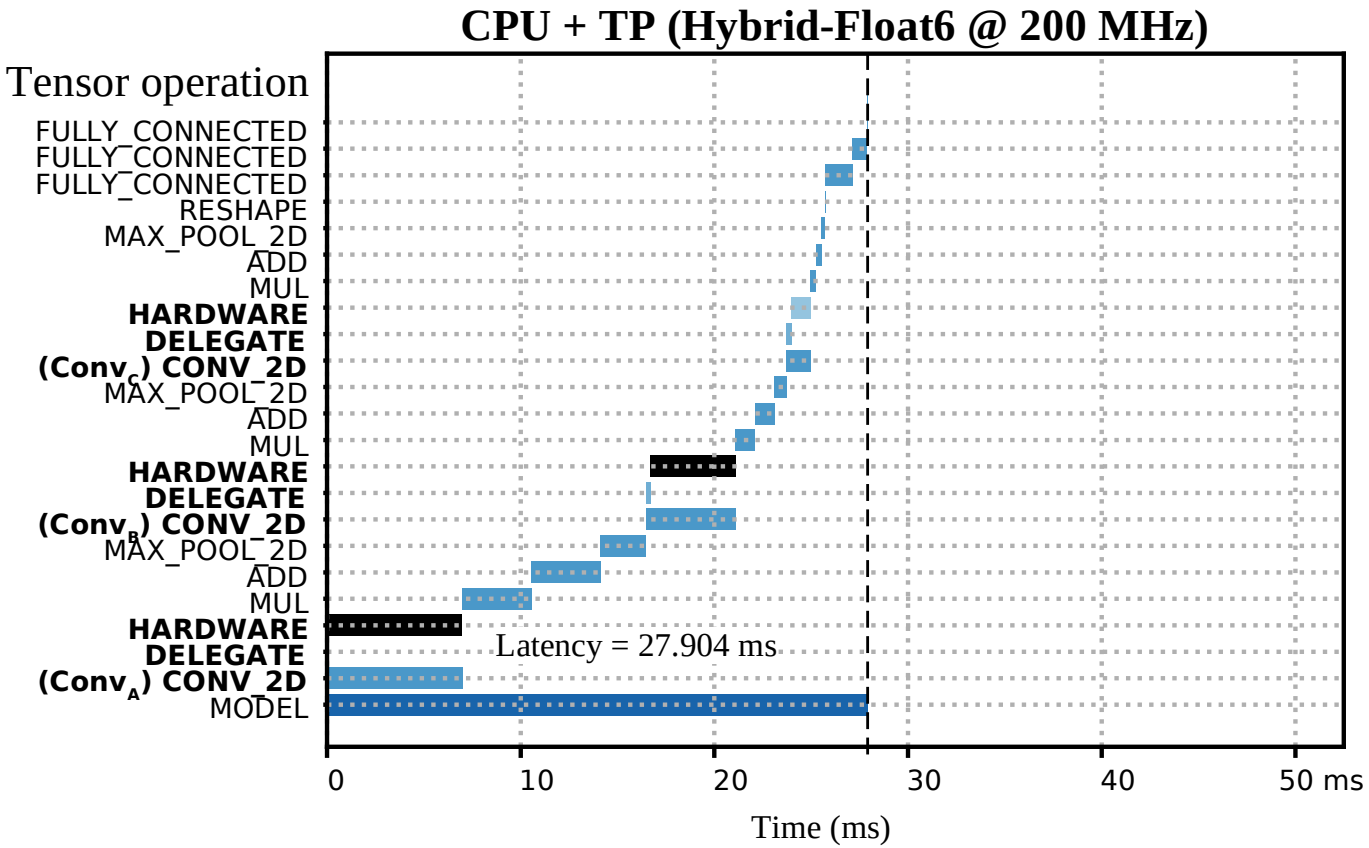
Tensor Op	CPU (ms)	TP FP32 (ms)	Gain	**TP HF6 (ms)**	**Gain**
$Conv_A$	112.24	12.49	8.9	**6.92**	**16.2**
$Conv_B$	213.13	16.39	13.0	**4.41**	**48.3**
$Conv_C$	46.59	3.59	12.9		



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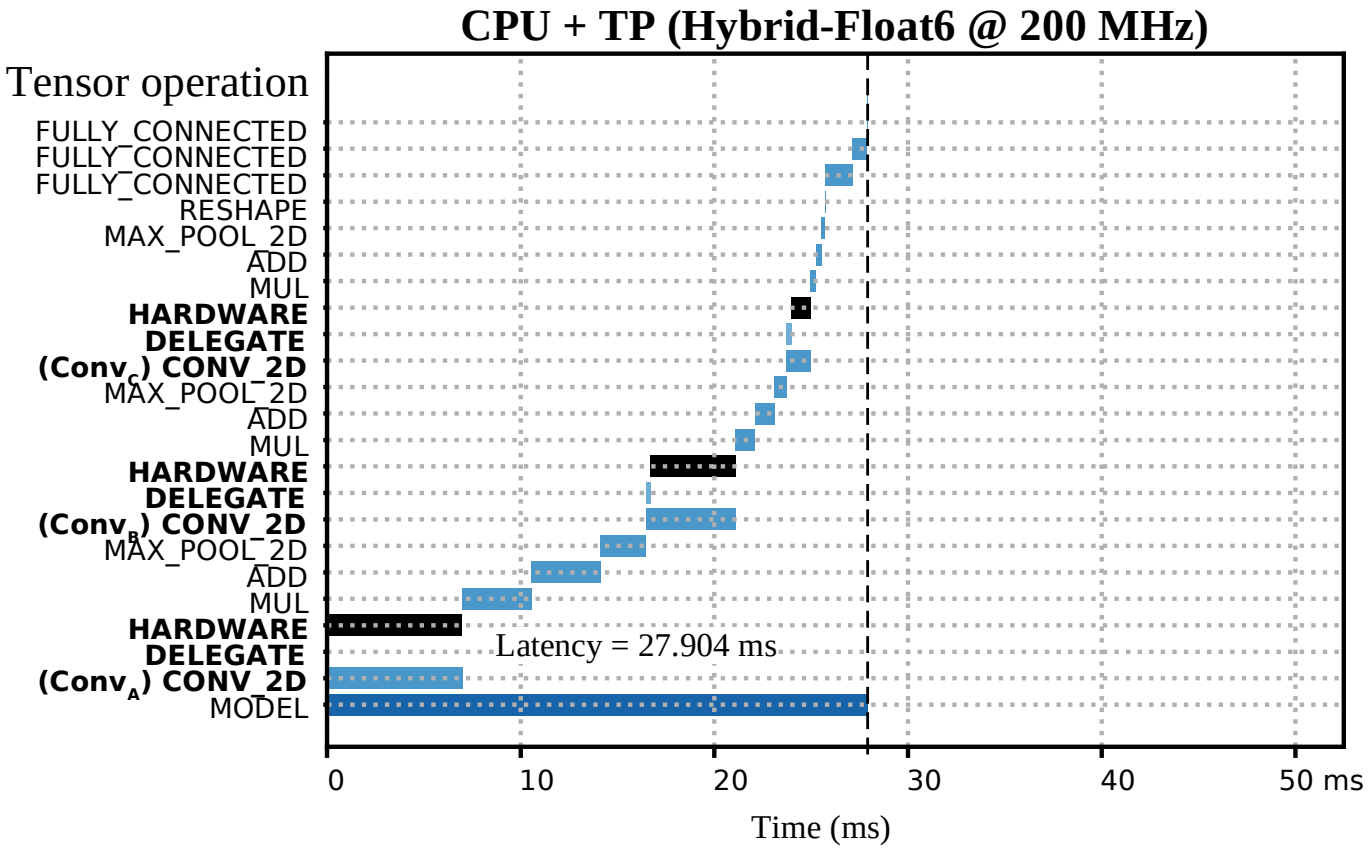
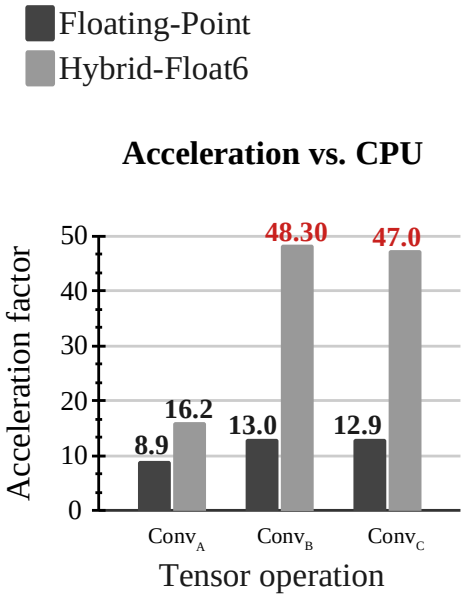


Final Benchmarking Insights: Accelerators vs. CPU in Performance and Power Efficiency



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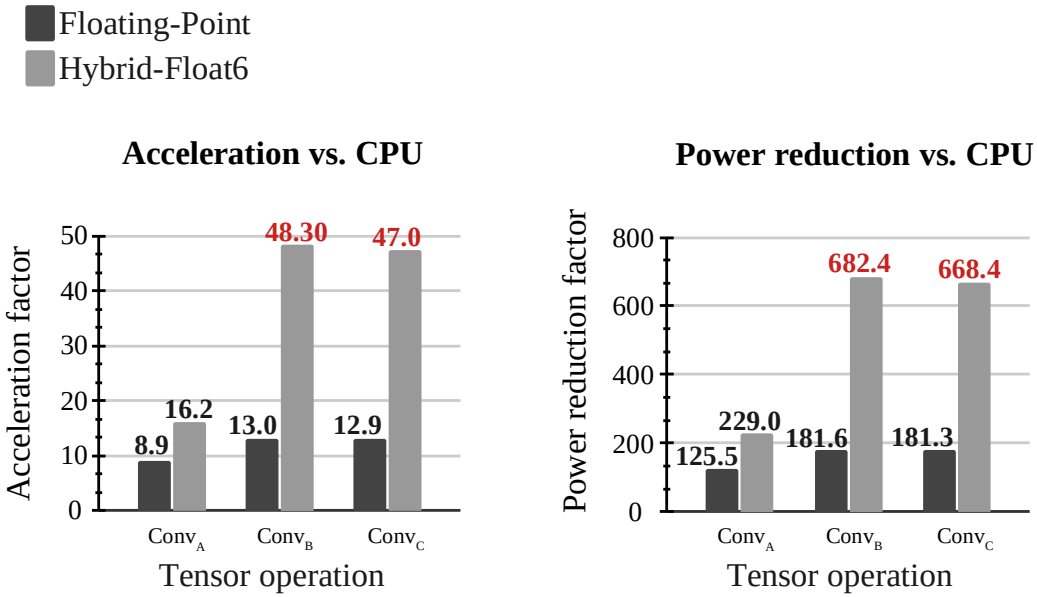

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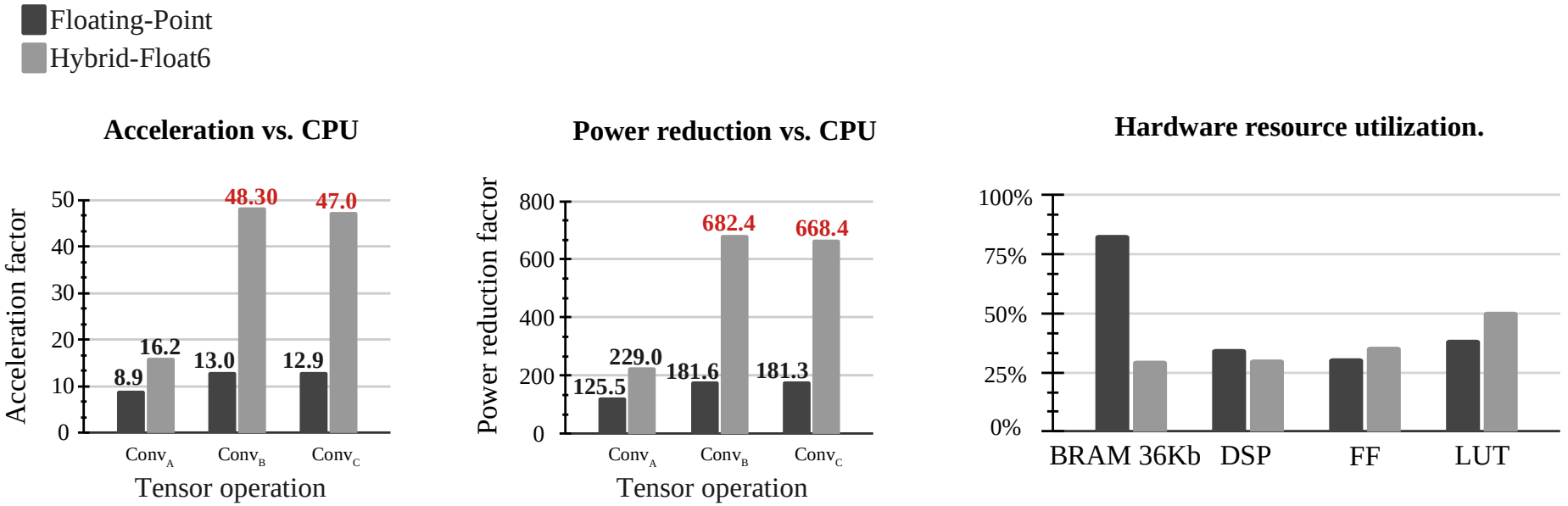

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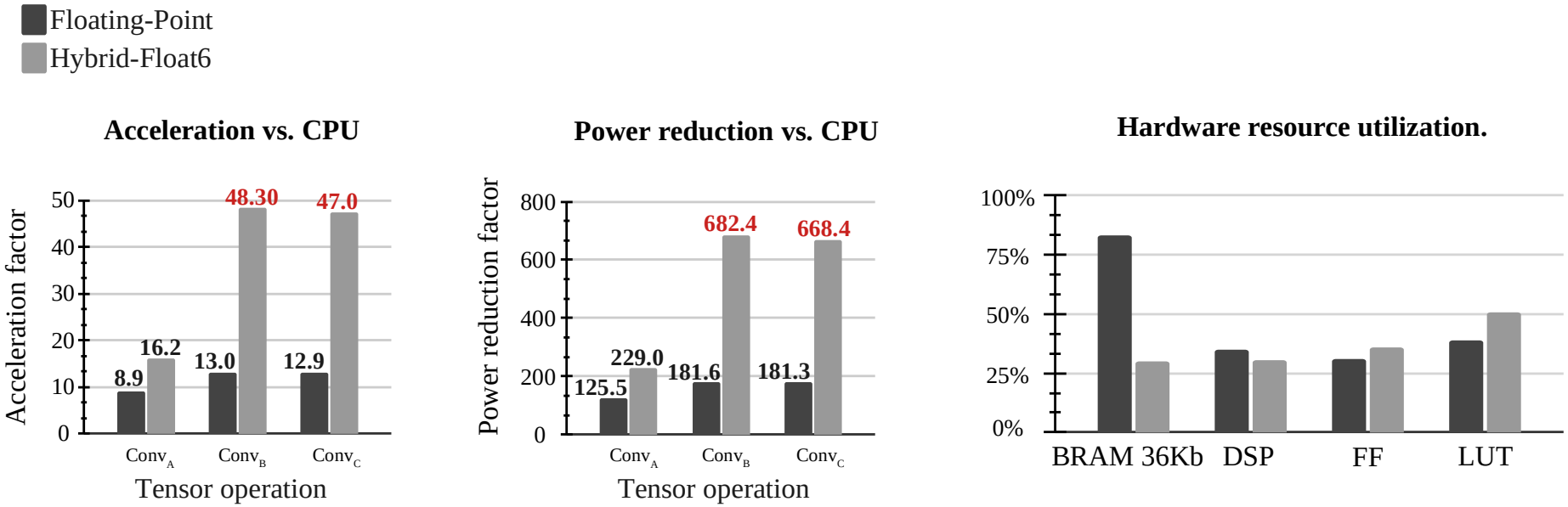
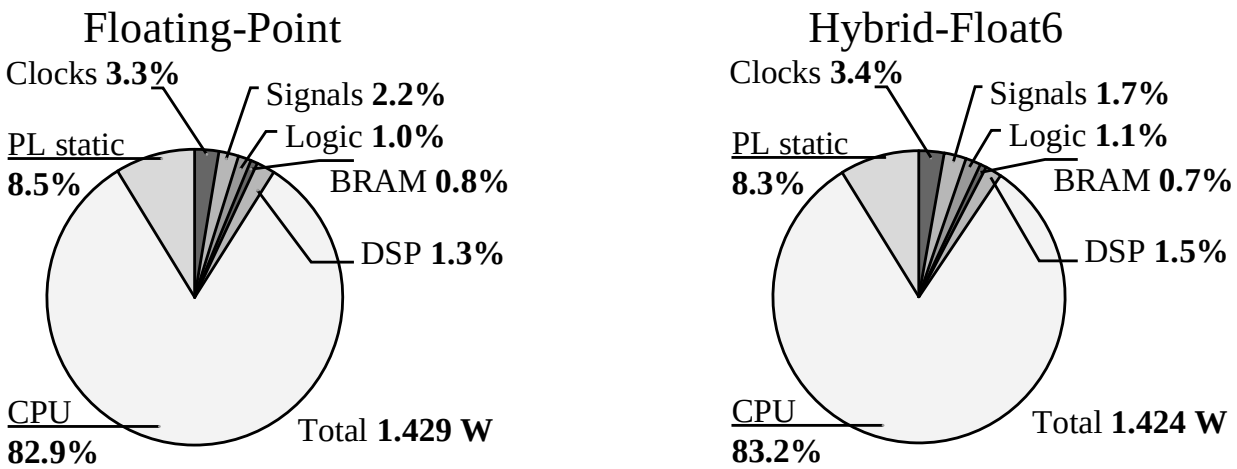


Estimated power dissipation on the Zynq-7007S AP SoC with PS at 666 MHz and PL at 200 MHz



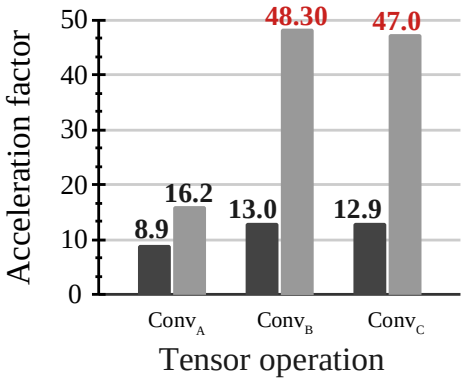
Boosting TinyML Performance with Hybrid Floating-Point 6-bit

Final Benchmarking Insights: Accelerators vs. CPU in Performance and Power Efficiency

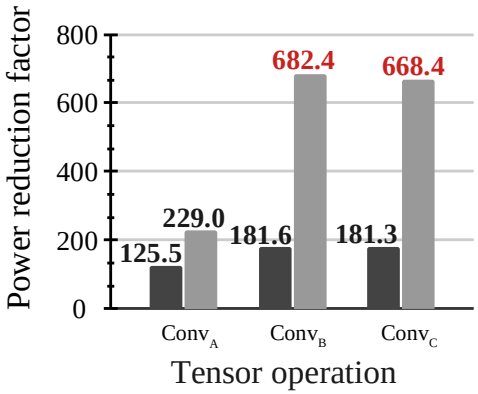
Floating-Point
Hybrid-Float6

Smallest CNN floating-point accelerator in the literature

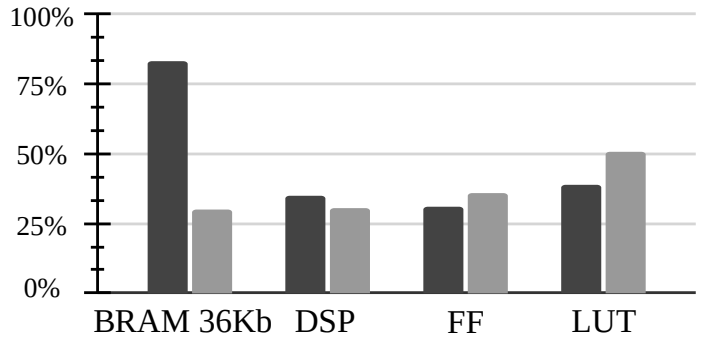
Acceleration vs. CPU



Power reduction vs. CPU



Hardware resource utilization.



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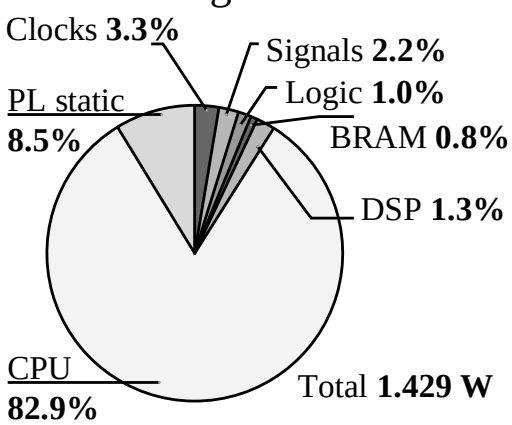
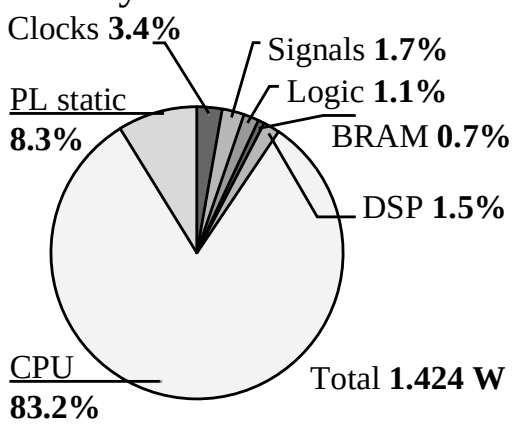
Floating-Point



Hybrid-Float6



1 Methodology

2 Custom Floating-Point MAC Designs and Quantization Techniques

3 Case Studies

4 Conclusions

Conclusion and Future Research

- **HW/SW Design Methodology for Low-Power Neural Network Acceleration with Hybrid Custom Floating-Point Arithmetic**

- **Technological Transformation**

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  - On-device iterative optimization with non-negativity constraints using 4-bit weights
- **Technological Transformation**
  - Inference was the beginning in TinyML. Low-precision floating-point is opening the door for a new generation of on-device training accelerators that are essential in the next phase of AI evolution.

Publications

Journal Articles

- **Yarib Nevarez**, David Rotermund, Klaus R Pawelzik, and Alberto Garcia-Ortiz, "Accelerating Spike-by-Spike Neural Networks on FPGA With Hybrid Custom Floating-Point and Logarithmic Dot-Product Approximation," *IEEE Access*, vol. 9, pp. 80603–80620, May 2021, doi: 10.1109/ACCESS.2021.3085216.
- **Yarib Nevarez**, Andreas Beering, Amir Najafi, Ardalan Najafi, Wanli Yu, Yizhi Chen, Karl-Ludwig Krieger, and Alberto Garcia-Ortiz, "CNN Sensor Analytics With Hybrid-Float6 Quantization on Low-Power Embedded FPGAs," *IEEE Access*, vol. 11, pp. 4852–4868, January 2023, doi: 10.1109/ACCESS.2023.3235866.

Conference Proceedings

- **Yarib Nevarez**, Alberto Garcia-Ortiz, David Rotermund, and Klaus R Pawelzik, "Accelerator framework of spike-by-spike neural networks for inference and incremental learning in embedded systems," 2020 9th International Conference on Modern Circuits and Systems Technologies (MOCAST), Bremen, 2020, pp. 1–5, doi: 10.1109/MOCAST49295.2020.9200288.
- Wanli Yu, Ardalan Najafi, **Yarib Nevarez**, Yanqiu Huang and Alberto Garcia-Ortiz, "TAAC: Task Allocation Meets Approximate Computing for Internet of Things," 2020 IEEE International Symposium on Circuits and Systems (ISCAS), Sevilla, 2020, pp. 1-5, doi: 10.1109/ISCAS45731.2020.9180895.

Publications

- Amir Najafi, Ardalan Najafi, **Yarib Nevarez** and Alberto Garcia-Ortiz, "Learning-Based On-Chip Parallel Interconnect Delay Estimation," 2022 11th International Conference on Modern Circuits and Systems Technologies (MOCAST), Bremen, 2022, pp. 1–5, doi: 10.1109/MOCAST49295.2020.9200288.
- Yizhi Chen, **Yarib Nevarez**, Zhonghai Lu, and Alberto Garcia-Ortiz, "Accelerating Non-Negative Matrix Factorization on Embedded FPGA with Hybrid Logarithmic Dot-Product Approximation," 2022 IEEE 15th International Symposium on Embedded Multicore/Many-core Systems-on-Chip (MCSoC), Malaysia, 2022, pp. 239–246, doi: 10.1109/MCSoC57363.2022.00070.
- Ardalan Najafi, Wanli Yu, **Yarib Nevarez**, Amir Najafi, Andreas Beering, Karl-Ludwig Krieger, and Alberto Garcia-Ortiz, "Acoustic Emission Source Localization using Approximate Discrete Wavelet Transform," 2023 12th International Conference on Modern Circuits and Systems Technologies (MOCAST), Bremen, 2023, pp. 1–5, doi: 10.1109/MOCAST57943.2023.10176952.

Thank You for Your Attention