

b) CPU + TP (Floating-Point Xilinx IP @ 200 MHz)

Tensor operation

FULLY_CONNECTED

FULLY_CONNECTED

FULLY_CONNECTED

RESHAPE

MAX_POOL_2D

ADD

MUL

HARDWARE

DELEGATE

(Conv_c) CONV_2D

MAX_POOL_2D

ADD

MUL

HARDWARE

DELEGATE

(Conv_b) CONV_2D

MAX_POOL_2D

ADD

MUL

HARDWARE

DELEGATE

(Conv_a) CONV_2D

MODEL

