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GENERAL CHAIR'S MESSAGE

Zhou Li
General Chair. 57th DAC

Dear Colleagues,

Welcome to the 57th Design Automation Conference, the first Virtual DAC.

For every great show, there is a great team behind it. The DAC Executive Committee consists of an amazing team of experts from the industry and academia, as well as MP Associates, Hall Erickson, and the DAC sponsor representatives from IEEE and ACM, along with the hundreds of volunteers who put the conference together. They collaborated in presenting you an excellent program with top quality research papers and Designer/IP/Embedded track presentations, great keynotes, SKY talks and invited talks, exciting panels, insightful tutorials, late breaking research outcome, work in progress update, and hundreds of posters from design practitioners, Ph.D. students, and young DAC fellows.

DAC 2020 sees a very healthy growth in all areas. On the research side, we have an impressive 20.7% increase in submissions compared to 2019. Out of 984 submitted research papers, 228 were accepted. The submissions in AI/ML architecture and systems category increased by an impressive 210%, but more importantly, we see healthy increased submissions across all areas - design, embedded systems and software, autonomous systems, IP, security as well as our foundation, traditional EDA. On the Designer/IP/Embedded track, we also received a record high number of submissions.

Over the last 57 years, DAC has grown from a small workshop with technical sessions to adding design, IP and now embedded tracks and an industry tradeshow where exhibitors have become a big part of the program. DAC has also grown from a conference with just a laser focus on EDA, to a conference that covers the whole eco system with topics like design, machine learning/AI, IP, embedded systems and software, security, autonomous systems, 5G and cloud. DAC is a unique event that brings together the entire design and design automation ecosystem from academic and industrial researchers to designers, developers, vendors, and educators. Going forward, I see great momentum for DAC to grow for another 50 years.

I hope you all enjoy Virtual DAC this week. Attend a presentation on a topic you don't know. Visit the virtual booths. Interact with live text chats or leave a message for the speakers to answer any questions or simply to introduce yourself. Attend our virtual happy hours and networking events and connect with old friends or make some new ones, even in the virtual setting.

We are going through a special time in history due to the COVID-19 pandemic. It is more important than ever to work as one big global community among the chip and EDA community, communications community, ML/AI community, security community, autonomous system community, etc. By working together, collaborating, sharing and exchanging ideas, great new ideas will come and all of us can contribute to our global society in a bigger way.

Please keep yourself and your family safe. Enjoy the #57thDAC!

Sincerely,
Zhuo Li

TECHNICAL PANEL ABSTRACTS

SESSION 22: Dead or Alive? The Fate of Formal Methods in Securing "Everyday" SoCs
THURSDAY July 23, 11:00AM – 12:00 PM
TRACK(S): HARDWARE SECURITY, SECURITY & PRIVACY, VERIFICATION/VALIDATION
TOPIC AREA(S): SECURITY, EDA

Moderator: Jason Fung - *Intel Corp., Hillsboro, OR*
Organizer: Jason Fung - *Intel Corp., Hillsboro, OR*
Carlos Rozas - *Intel Corp., Hillsboro, OR*

Whether we are at home, at work, or in the public, we are surrounded by more and more "smart" devices powered by SoCs big and small. While these everyday SoCs by themselves may not be as mission-critical as those that power flight control systems or cyber-physical systems, their broad installed based and how tightly they couple with end-users' everyday life can still cause serious impacts when they are compromised. For decades, the proliferation of formal verification techniques to improve secure-by-design of hardware systems has been limited mostly to critical components that power infrastructure with high reliability/resilience/safety requirements. Is it the ultimate fate of formal methods? Or is there still hope that these techniques can make into mainstream SoC product development practices within this decade? What are the key roadblocks that limit adoption? Is it a technology, policy, or economic challenge? What roles should academia, EDA vendors, SoC suppliers, and the government play? Would a concerted effort help and how would that look like?

Panelists:

Sharad Malik - *Princeton Univ., Princeton, NJ*
Ray Richards - *Defense Advanced Research Projects Agency, Washington, DC*
Tim Sherwood - *Univ. of California, Santa Barbara, CA*
Joseph Kiniry - *Galois, Inc., OR*

SESSION 32: Research Grants – Opportunities, Trends, and Implications
TUESDAY July 21, 3:30PM – 4:30 PM
TRACK(S): EDA, DESIGN
TOPIC AREA(S): ANY

Moderator: Yiran Chen - *Duke Univ., Durham, NC*
Organizer: Sankar Basu - *National Science Foundation, Washington, DC*

Research grants and their distribution mechanisms are critical to maintaining long-term competence and sustainability of academic research. Various goals and focuses of different funding sources ensure the diversity of research activities. The proposed panel will include representatives from both federal and industrial funding agencies in the electronic society, and address many topics that are of great interests to the community such as:

1. What are the new trends in funding strategies of different funding agencies?
2. How to resolve the competition between the big research centers and small individual awards
3. How do we initiate new and emerging research topics (e.g., AL/ML, security) within the scope of the society?
4. How to balance the focus and diversity of the funded topics from a funding agency's perspective?
5. Similarities, differences, challenges, and solutions, in research funding strategies from a regional and global perspective.
6. The importance of diversity and broader impact on proposal writing and evaluation.

Panelists:

Sankar Basu - *National Science Foundation, Washington, DC*
Serge Leef - *Defense Advanced Research Projects Agency, Washington, DC*
Robinson Pino - *United States Department of Energy, Washington, DC*
Victor Zhirnov - *Semiconductor Research Corp., Durham, NC*
Damian Dudek - *Deutsche Forschungsgemeinschaft, Bonn, Germany*

SESSION 43: Artificial Intelligence Comes to CAD: Where's the Data?
WEDNESDAY July 22, 2:00PM – 3:00 PM
TRACK(S): MACHINE LEARNING/AI, EDA
TOPIC AREA(S): ANY

Moderator: Marilyn Wolf - *Univ. of Nebraska, Lincoln, NE*
Organizer: Marilyn Wolf - *Univ. of Nebraska, Lincoln, NE*

Machine learning has received widespread attention in many fields including CAD. This panel will discuss and debate two main questions that must be solved before machine learning can be successfully applied to computer-aided design of electronic systems. First, at what levels of abstraction is machine learning applicable? Potential applications include device optimization, circuit synthesis, and optimization, logic synthesis, ESL, verification, and validation. The machine learning methods required at these different levels of abstraction will vary widely. The impact of machine learning at these levels of abstraction is up for debate. Given the large investments required to introduce machine learning-based approaches, targets of opportunity must be carefully evaluated and identified. Second, how do we manage the huge amounts of data required to apply machine learning? Does data need to be labeled; if so, who will provide labels? Can models be used to augment labeling? What intellectual property rights must be negotiated to obtain training data? Who will own the results of machine learning methods driven by outside data?

Panelists:

Thomas Andersen - *Synopsys, Inc., Mountain View, CA*
Paul Franzon - *North Carolina State Univ., Raleigh, NC*
Elias Fallon - *Cadence Design Systems, Inc., Pittsburgh, PA*
Raviv Gal - *IBM Research - Haifa, Israel*
Sachin Sapatnekar - *Univ. of Minnesota, Minneapolis, MN*

SESSION 53: Real-Time Machine Learning at the Edge: Digital or Analog Computing?
THURSDAY July 23, 2:00 PM – 3:00 PM
TRACK(S): EDA, MACHINE LEARNING/AI, EMBEDDED SYSTEMS & SOFTWARE (ESS)
TOPIC AREA(S): IOT, LOW POWER, ARCHITECTURE & SYSTEM DESIGN

Moderator: Krste Asanović - *Univ. of California, Berkeley, CA*
Organizer: Yingyan Lin - *Rice Univ., Houston, TX*

Recent advances in machine learning are fueling a growing demand for intelligent Internet of Things (IoT). Many applications of IoT computing, such as autonomous vehicles, robots, and healthcare wearables, require real-time and in-situ learning to be perceived as truly intelligent, i.e., the desired systems must proactively interpret and learn from new data, improve their own performance using what they have learned, and adapt to dynamic environments, all in real-time. However, the limited computing and energy resources available at the edge devices (e.g., mobile devices and sensors) stand at odds with the massive and growing cost of state-of-the-art machine learning training, posing a grand challenge for real-time machine learning (RTML) at the edge. To address the aforementioned challenge, recently developed digital accelerators have demonstrated a great promise. On the other hand, there has been a growing interest in leveraging analog computing especially processing-in-memory for realizing RTML, considering its advantageous energy efficiency in the low-SNR regime where machine learning operates. This panel, comprised of distinguished researchers from both industry and academia, is meant to debate the following controversy: what is the right path to achieve RTML at the edge – specifically, digital or analog computing?

Panelists:

Jason Cong - *Univ. of California, Los Angeles, CA*
Kailash Gopalakrishnan - *IBM T.J. Watson Research Center, Yorktown Heights, NY*
Boris Murmann - *Stanford Univ., Stanford, CA*
Aravind Dasu - *Intel Corp., San Jose, CA*

SESSION 64: From AI-Phoria to AI-Phobia: Is Security & Privacy the Achilles Verse of AI?
WEDNESDAY July 22, 3:30 PM – 4:30 PM
TRACK(S): SECURITY, MACHINE LEARNING/AI
TOPIC AREA(S): SECURITY & PRIVACY, EMERGING TECHNOLOGIES, SYSTEM SECURITY

Moderator: Ahmad-Reza Sadeghi - *Technische Univ. Darmstadt, Germany*

Today, we are witnessing an AI euphoria in the true sense of the word, and rapidly growing dependency of modern societies on AI to provide various services. While emerging technologies, such as IoT, demand AI support in particular on resource constraint devices, the IT giants require AI platforms with increasingly more computational power to feed their data-hungry neural networks on their cloud farms. However, as for many emerging technologies, key security and privacy aspects are often neglected in favor of economic merit, performance, and time-to-market which can have devastating consequences for AI users (privacy, safety, correctness) as well as for the AI providers (IP theft, DoS, or manipulation of services). The utopia of a world in which intelligent devices and services should ease human life can easily become a dystopia where the ownership of personal data and computation is completely lost. Adversarial AI provides a blooming landscape for attackers with different incentives, allowing them to compromise any AI-based system in a stealthy manner, or shut it down completely in a wide range of applications from voice assistants to automotive and financial systems. This panel discusses the state-of-the-art attack vectors on AI platforms and systems on whether we should put too much trust in AI, given that compromised AI threatens our privacy, security, and safety. The panel will also explore possible design principles for AI systems to guarantee the correctness, security, and privacy requirements that are imposed on these systems.

Panelists:
Helena Handschuh - *Rambus Cryptography Research Division, San Francisco, CA*
Florian Kerschbaum - *Univ. of Waterloo, ON, Canada*
Pamela Norton - *Borsetta, San Francisco, CA*
Azalia Mirhoseini - *Google, Inc., Mountain View, CA*
Bita Darvish - *Microsoft Corporation, Redmond, WA*

SESSION 75: Designing for Machine Intelligence: To Brain or Not to Brain?
FRIDAY July 24, 11:00AM – 12:00 PM
TRACK(S): MACHINE LEARNING/AI, DESIGN
TOPIC AREA(S): ARCHITECTURE & SYSTEM DESIGN, EMERGING TECHNOLOGIES SECURITY

Moderator: Dan Hammerstrom - *Portland State Univ., Portland, OR*
Organizer: Qinru Qiu - *Syracuse Univ., Syracuse, NY*

To design a machine that exhibits intelligence that is indistinguishable from a human being is the ultimate goal of hardware and software designers. The human brain, the biological computing engine of human intelligence, is fundamentally different from silicon-based computers, from molecular level to behavioral level. With the progress of neuroscience, the structure and behavior of the brain, which used to be a Blackbox, are gradually revealed. There is a surge of brain-inspired architecture and computing models emerging in recent years. However, is the brain a good model for machine intelligence? At what level should a system resemble the brain in order to have comparable efficiency, robustness, and adaptiveness for cognitive tasks? Should it be behavioral level, architectural level, or even device level? Is it possible to copy the brain onto silicon? Is it necessary? Are we already unintentionally evolving our hardware and software systems towards a brain-like architecture, as it is the result of natural selection over millions of years? In this panel, we invited five experts in hardware, software, application, and neuroscience to discuss their views in those questions.

Panelists:
Mike Davies - *Intel Corp., Calabasas, CA*
Emre Neftci - *Univ. of California, Irvine, CA*
Cliff Young - *Google, Inc., Mountain View, CA*
Yu Wang - *Tsinghua Univ., Beijing, China*
Mihai A. Petrovici - *Univ. of Bern, Bern, Switzerland*

SESSION 82: Design of Autonomous Systems: Engineering, Science, or Art?
FRIDAY July 24, 2:00PM – 3:00 PM
TRACK(S): AUTONOMOUS SYSTEMS, MACHINE LEARNING/AI
TOPIC AREA(S): AUTOMOTIVE, IOT, ARCHITECTURE & SYSTEM DESIGN

Moderator: Susmit Jha - *SRI International, Menlo Park, CA*
Organizer: Qi Zhu - *Northwestern Univ., Evanston, IL*
Wenchao Li - *Boston Univ., Boston, MA*

Autonomous systems such as self-driving cars and robots have shown great potential in societal and economical impact. However, designing these systems and making them practical still face tremendous challenges. In this panel, experts from industry and academia will discuss and debate some of the key questions facing autonomous systems designers: How much can the design process be automated with engineering tools, and how much does it depend on designer intuition and experience? How much of the autonomous systems can be effectively designed with engineering heuristics, and how much has to be based on rigorous theories? And finally, what application domains could see wide development and adoption of design automation tools, as in EDA?

Panelists:
Alessandro Pinto - *Raytheon Technologies Corp., Berkeley, CA*
Sanjit Seshia - *Univ. of California, Berkeley, CA*
Shaoshan Liu - *PerceptIn, San Francisco, CA*
Joerg Seitter - *Bosch Research, Stuttgart, Germany*

SESSION 90: High-Level Synthesis 1974 - 2020: The Meteoric Rise of a Hot Topic?
THURSDAY July 23, 3:30PM – 4:30 PM
TRACK(S): EDA
TOPIC AREA(S): ARCHITECTURE & SYSTEM DESIGN

Moderator: Marilyn Wolf - *Univ. of Nebraska, Lincoln, NE*
Organizer: Marilyn Wolf - *Univ. of Nebraska, Lincoln, NE*

This panel celebrates the success of high-level synthesis as an important tool in CAD. High-level synthesis originated with research in the 1970s; a steady stream of innovation from both academic and industrial researchers paved the way for today's successful HLS tools.

Panelists:

Deming Chen - *Univ. of Illinois at Urbana-Champaign, Urbana, IL*
Ahmed Jerraya - *CEA-LETI, Grenoble, France*
Pierre Paulin - *Synopsys, Inc., Mountain View, CA*
Bryan Bowyer - *Mentor, A Siemens Business, Wilsonville, OR*
Sean Dart - *Cadence Design Systems, Inc., San Jose, CA*
Kazutoshi Wakabayashi - *Univ. of Tokyo, Japan*
Shankar Krishnamoorthy - *Synopsys, Inc., Mountain View, CA*
Arun Subbiah - *Intel Corp., Hillsboro, OR*
Charles J. Alpert - *Cadence Design Systems, Inc., Austin, TX*

MONDAY KEYNOTE ADDRESS
July 20, 2020
9:20 AM

Semiconductor Technology: A System Perspective

Philip Wong - *Taiwan Semiconductor Manufacturing Co., Ltd., Hsinchu, Taiwan*

Abstract: Future electronic systems will continue to rely on, and increasingly benefit from, the advances in semiconductor technology as they have had for more than five decades. Since its inception, the semiconductor industry has used a physical dimension (minimum gate length of a transistor) as a means to gauge continuous technology advancement. This metric is all but obsolete today. Density is what drives the benefits of new device technologies for computation – the primary application driver for semiconductors. Going forward, we will use a three-prong metric that consists of logic density (DL), memory bit density (DM), and interconnect density between logic and memory (DC) as a means to capture how advances in semiconductor device technologies enable system level benefits. Because DL and DM will increase at a slower rate than the historical trends, technologies that address the connectivity will become primary drivers for technology advancement. This trend is already visible in HPC products that progressively leverage more capable packaging technologies including 3D chip stacking. Indeed, vertical interconnect density associated with advanced packaging featured about three orders of magnitude improvement in the last decade alone. Scaling vertical interconnect pitch to sub-100 nm would enable another four orders of magnitude improvement. As such, there is plenty of room for system-level advances based on 3D ICs. The distinction between on-die connectivity (vias and on-chip interconnect wires) and off-chip connectivity (e.g. TSVs and micro-bumps) will become increasingly blurred. Wafer-level monolithic integration technologies and packaging technologies will smoothly blend into one another. New design tools that optimally perform system partitioning will become indispensable.

Biography: H.-S. Philip Wong is the Willard R. and Inez Kerr Bell Professor in the School of Engineering at Stanford University. In 2018, he was on leave from Stanford and was the Vice President of Corporate Research at TSMC, the largest semiconductor foundry in the world. Since 2020, he has been the Chief Scientist of TSMC. He joined Stanford University as Professor of Electrical Engineering in September, 2004. From 1988 to 2004, he was with the IBM T.J. Watson Research Center. He is a Fellow of the IEEE and received the IEEE Electron Devices Society J.J. Ebers Award. He served as the Editor-in-Chief of the IEEE Transactions on Nanotechnology (2005 – 2006), sub-committee Chair of the ISSCC (2003 – 2004), General Chair of the IEDM (2007), and is currently the Chair of the IEEE Executive Committee of the Symposia of VLSI Technology and Circuits. He received the honorary doctorate degree from Institut Polytechnique de Grenoble, France. Professor Wong and his students have won best paper awards at premier conferences such as the International Solid-State Circuits Conference (ISSCC) and Symposia on VLSI. He is the faculty director of the Stanford Non-Volatile Memory Technology Research Initiative (NMTRI), and is the founding Faculty Co-Director of the Stanford SystemX Alliance – an industrial affiliate program focused on building systems.

MONDAY SKY TALK
July 20, 2020
12:30 PM

Succeeding with AI Today and Tomorrow

Toby Cappell - *IBM Corp., Austin, TX*

Abstract: Businesses and Functions are under increasing pressure to innovate, evolved and adapt to a changing environment and business climate. We are going to talk about the role AI plays is that change and how each of you can and should be thinking about the use of AI in your work, your function and your business(es).

Biography: Toby Cappello is the Vice President of Industry Architecture and Client Success within IBM's Data and AI business. In this executive leadership role, Toby is responsible for engaging our customers in discussion about industry use cases and proof points to better leverage the data they have for business value and differentiation. Done correctly, customers will unlock previously unattainable value from their Data Assets and Business Processes. Toby has focused on working with Customers to drive business value through enablement and building competencies around transformational and disruptive technologies. He has done this by aligning people, processes and technology ensuring organizations are prepared to realize value from technology investments and business transformation.

TUESDAY KEYNOTE ADDRESS
July 21, 2020
9:20 AM

RISC-V Revolution and Momentum

Calista Redmond - *RISC-V Foundation, San Francisco, CA*

Abstract: RISC-V has ushered in a profound shift in the technical and business models for microprocessors. Let's talk about the revolution and the many facets of engagement and strategic adoption around the world, across industries, and within existing and new domains. Learn more about RISC-V International's role in leading the revolution and disrupting the status quo.

Biography: Calista Redmond is the CEO of RISC-V International with a mission to expand and engage RISC-V stakeholders, compel industry adoption, and increase visibility and opportunity for RISC-V within and beyond RISC-V International. Prior to RISC-V International, Calista held a variety of roles at IBM, including Vice President of IBM Z Ecosystem where she led strategic relationships across software vendors, system integrators, business partners, developer communities, and broader engagement across the industry. Focus areas included execution of commercialization strategies, technical and business support for partners, and matchmaker to opportunities across the IBM Z and LinuxOne community. Calista's background includes building and leading strategic business models within IBM's Systems Group through open source initiatives including OpenPOWER, OpenDaylight, and Open Mainframe Project. For OpenPOWER, Calista was a leader in drafting the strategy, cultivating the foundation of partners, and nurturing strategic relationships to grow the org from zero to 300+ members. While at IBM, she also drove numerous acquisition and divestiture missions, and several strategic alliances. Prior to IBM, she was an entrepreneur in four successful start-ups in the IT industry. Calista holds degrees from the University of Michigan and Northwestern University.

TUESDAY SKY TALK
July 21, 2020
12:30 PM

If you want to be rich, get a lot of money: Theory and Systems for Weak Supervision

Christopher Ré - *Stanford Univ., Stanford, CA*

Abstract: If you want to build a high-quality machine learning product, build a large, high-quality training set. At first glance, this seems as useful as the statement “if you want to be rich, get a lot of money.” However, a key idea driving our work is that new theoretical and systems concepts including weak supervision, automatic data augmentation policies, and more, can enable engineers to build training sets more quickly and cost effectively. Along with state-of-the-art results on benchmarks, these concepts have allowed our group and collaborators to build a range of state-of-the-art applications including patient-care monitoring on electronic health records, automatic triage systems for radiologists, and enabling cardiologists to spot rare abnormalities in video MRI—along with widely used products from Apple and Google. This talk describes the theoretical and systems challenges that such applications create. On the machine-learning theory side, a key problem is estimating the quality and correlation of various sources of training data—but without ground truth labels. This problem connects to classical questions about estimating the covariance of latent variable models. We describe our new techniques that solve this case and can even improve fully supervised methods for estimating the structure of graphical models. On the machine-learning systems side, this theory opens up new ways to build machine-learning systems. Here, we describe our recent work on systems that help engineers build and maintain machine learning products—without writing low-level code in frameworks like TensorFlow. These systems draw on recent ideas in machine learning, e.g., zero-code deep learning systems, and twists on classical data management ideas, e.g., schemas to separate the model, the supervision, and down-stream serving code. Much of this work is open source and available at http://snorkel.org or my website.

Biography: Christopher (Chris) Ré is an associate professor in the Department of Computer Science at Stanford University. He is in the Stanford AI Lab and is affiliated with the Statistical Machine Learning Group. His recent work is to understand how software and hardware systems will change as a result of machine learning along with a continuing, petulant drive to work on math problems. Research from his group has been incorporated into scientific and humanitarian efforts, such as the fight against human trafficking, along with products from technology and enterprise companies. He cofounded a company, based on his research into machine learning systems, that was acquired by Apple in 2017. More recently, he cofounded SambaNova systems based, in part, on his work on accelerating machine learning. He received a SIGMOD Dissertation Award in 2010, an NSF CAREER Award in 2011, an Alfred P. Sloan Fellowship in 2013, a Moore Data Driven Investigator Award in 2014, the VLDB early Career Award in 2015, the MacArthur Foundation Fellowship in 2015, and an Okawa Research Grant in 2016. His research contributions have spanned database theory, database systems, and machine learning, and his work has won best paper at a premier venue in each area, respectively, at PODS 2012, SIGMOD 2014, and ICML 2016. Film.”

WEDNESDAY KEYNOTE ADDRESS
July 22, 2020
9:20 AM

A Massive Wafer-Scale Supercomputer for Deep Learning Acceleration: A Radically New Paradigm for Deep Learning Acceleration

Andrew Feldman - *Cerebras Systems Inc., Los Altos, CA*

Abstract: Deep learning has emerged as one of the most important silicon workloads of our time. Its computational demands are massive and ever-increasing: the requirements to train the largest deep learning models increased by 300,000x between 2012-2018. Traditional processors are not well-suited to meet this demand, mainly due to the overhead of bringing massive amounts of weight and training data to and from the processor. This makes the deep learning problem a prime candidate for custom ASIC hardware and innovative EDA software. Our startup company Cerebras has developed a new super computer system optimized for this deep learning task. This system is powered by the largest monolithic chip ever built: the Cerebras Wafer-Scale Engine (WSE). This is a single integrated 46,225 mm^2 silicon chip with a whopping 1,200 Billion transistors. Its array of 400,000 compute cores make the chip 56x larger than today's largest GPU, with 3,000x more on-chip memory and >10,000x memory bandwidth. The WSE delivers more compute, more memory, and more communication bandwidth to enable AI research at revolutionary speeds and scale. In this talk, we will first describe the general architecture of the systolic computer hardware, including the enclosure that can generate and absorb the over 15 kilowatts of energy. Next, we will dive into the technical complexities of the Cerebras compiler flow when mapping Tensorflow neural network computation graphs to the Cerebras WSE hardware This mapping problem is both different and also strangely similar to a traditional ASIC and FPGA design flows. In particular, we will highlight the unique technical challenges of the Cerebras place and route flow and compare/contrast the Cerebras compiler to other EDA tools in the ASIC and FPGA domains.

Biography: Andrew Feldman is co-founder and CEO of Cerebras Systems, a unicorn startup dedicated to accelerating Artificial intelligence (AI) compute. Cerebras is a team of pioneering computer architects, computer scientists, deep learning researchers, and engineers of all types who have come together to build a new class of computer optimized for AI work. Prior to Cerebras, Andrew was co-founder and CEO of SeaMicro the inventors of the microserver category and pioneers in energy efficient computation. SeaMicro was acquired by AMD for $357 million in 2012. Prior SeaMicro, Andrew was Vice President of Marketing and Product Management at Force10 Networks (acquired by Dell for $800 Million) and before that was Vice President of Corporate Marketing and Corporate Development for Riverstone Networks (NASDAQ: RSTN) from inception through IPO. Andrew is passionate about building teams that solve industry transforming problems. He is a sought-after advisor to startups, and currently serves on the board of directors at Natron Energy and on the advisory board of more than a dozen startups. Andrew is a frequent keynote speaker and guest lecturer at the Stanford Graduate School of Business. Andrew holds a bachelor's degree and an MBA from Stanford University.

WEDNESDAY SKY TALK
July 22, 2020
12:30 PM

Design and Manufacturing in 2030

Greg Yeric - *Arm, Ltd., Austin, TX*

Abstract: Looking out to 2030, our industry's underlying technology faces some "extreme" challenges. Will a 3rd generation EUV tool making 1.2nm CMOS nanowires be worth it? What disruptive opportunities may come forward in 10 years to help? There are many options to speculate about, but in every case it remains clear that the trend that started as Design for Manufacturing, and became Design Technology Co-Optimization, will need to continue to strengthen, and will need to adapt even more quickly to allow some of these disruptive opportunities to carry us to 2030 and beyond.

Biography: Greg Yeric earned his BSEE, MSEE, and PhD in Microelectronics at The University of Texas at Austin. He began his career at Motorola's Advanced Products Research and Development Laboratories in the area of process integration, subsequently working at TestChip Technologies, HPL Technologies, and Synopsys, in the areas of test structures and yield analysis. In this part of his career, he attended several Semicon West conventions. For the last 12 years, he has been at Arm. He is currently an ARM Fellow in the Research group, focusing on future technology and its interaction with design. At Arm he attended his first DAC, and made a point to visit the DAC's conveniently held in Austin. Outside of Arm, Greg serves on the TPC for IEEE's VLSI Technology Symposium and is currently the chair of the Microelectronics Exploratory Committee, a volunteer organization serving DARPA's MTO office.

THURSDAY KEYNOTE ADDRESS
July 23, 2020
9:20 AM

New Paradigms for 6G Wireless Communications

Andrea Goldsmith - *Stanford Univ., Stanford, CA*

Abstract: Wireless technology has enormous potential to change the way we live, work, and play over the next several decades. Future wireless networks will support 100 Gbps communication between people, devices, and the “Internet of Things,” with high reliability and uniform coverage indoors and out. New architectures including edge computing will drastically enhance efficient resource allocation while also reducing latency for real-time control. The shortage of spectrum will be alleviated by advances in massive MIMO and mmW technology, and breakthrough energy-efficiency architectures, algorithms and hardware will allow wireless networks to be powered by tiny batteries, energy-harvesting, or over-the-air power transfer. There are many technical challenges that must be overcome in order to make this vision a reality. This talk will describe our recent research addressing some of these challenges, including new modulation and detection techniques robust to rapidly time-varying channels, blind MIMO decoding strategies, machine learning equalization and source-channel coding, as well as “fog”-optimization of resource allocation in cellular systems.

Biography: Andrea Goldsmith is the Stephen Harris professor in the School of Engineering and a professor of Electrical Engineering at Stanford University. She co-founded and served as Chief Technical Officer of Plume WiFi and of Quantenna (QTNA), and she currently serves on the Board of Directors for Crown Castle (CCI) and Medtronic (MDT). She has also held industry positions at Maxim Technologies, Memorylink Corporation, and AT&T Bell Laboratories. Dr. Goldsmith is a member of the National Academy of Engineering and the American Academy of Arts and Sciences, a Fellow of the IEEE and of Stanford, and has received several awards for her work, including the IEEE Sumner Award, the ACM Athena Lecturer Award, the IEEE Comsoc Edwin H. Armstrong Achievement Award, the National Academy of Engineering Gilbreth Lecture Award, the Women in Communications Engineering Mentoring Award, and the Silicon Valley/San Jose Business Journal’s Women of Influence Award. She is author of the book ``Wireless Communications'' and co-author of the books ``MIMO Wireless Communications'' and “Principles of Cognitive Radio,” all published by Cambridge University Press, as well as an inventor on 29 patents. Her research interests are in information theory and communication theory, and their application to wireless communications and related fields. She received the B.S., M.S. and Ph.D. degrees in Electrical Engineering from U.C. Berkeley.

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REVIEWERS

A total of 984 manuscripts were submitted to the 57th DAC. The Technical Program Committee, together with the help of invited expert and external reviewers, selected 228 papers for presentation at the conference. The Conference Executive and Technical Program Committees wish to acknowledge the time and effort spent by the following people who reviewed these manuscripts. Many thanks to all of those who participated and contributed to the success of the conference.

Expert Reviewers (Topic Experts Invited by the TPC Subcommittee Chairs)

None provided by TPC chair

External Reviewers (Technical Volunteers Affiliated with DAC)

None provided by TPC Chair

AWARDS

2019 PHIL KAUFMAN AWARD FOR DISTINGUISHED CONTRIBUTIONS TO ESD
Mary Jane Irwin, Penn State University, University Park, PA
For her extensive contributions to EDA through technical efforts, community service, and leadership

2019 IEEE CEDA DISTINGUISHED SERVICE AWARD
Donatella Sciuto, Politecnico di Milano, Italy
For distinguished service to the EDA community and the IEEE Council on EDA

2019 IEEE CEDA DISTINGUISHED SERVICE AWARD
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For distinguished service to the EDA community and the IEEE Council on EDA

IEEE CEDA OUTSTANDING SERVICE RECOGNITION
Robert Aitken, Arm, Ltd., Sunnyvale, CA
For outstanding service to the EDA community as DAC General Chair in 2019

IEEE FELLOW
Maciej Ciesielski, University of Massachusetts, Amherst, MA
For contributions to logic synthesis and formal verification of arithmetic circuits

IEEE FELLOW
Partha Pratim Pande, Washington State University, Pullman, WA
For contributions to network-on-chip architectures for manycore computing

ACM SIGDA/IEEE CEDA A. RICHARD NEWTON TECHNICAL IMPACT AWARD IN ELECTRONIC DESIGN AUTOMATION
Luca Benini, ETH Zürich, Switzerland
Giovanni De Micheli, EPFL Lausanne, Switzerland
For the paper entitled, "Networks on Chips: A New SoC Paradigm"

2020 IEEE TRANSACTIONS ON COMPUTER-AIDED DESIGN OF INTEGRATED CIRCUITS AND SYSTEMS DONALD O. PEDERSON BEST PAPER
Alwin Zulehner, Johannes Kepler University Linz, Austria
Alexandru Paler, Johannes Kepler University Linz, Austria
Robert Wille, Johannes Kepler University Linz, Austria
For the paper entitled, "An Efficient Methodology for Mapping Quantum Circuits to the IBM QX Architectures"

IEEE COMPUTER SOCIETY 2020 EDWARD J. MCCLUSKEY TECHNICAL ACHIEVEMENT AWARD
Yuan Xie, University of California, Santa Barbara, CA
For contributions to technology-driven computer architecture and to tools for their implementation and evaluation

2020 ACM TODAES BEST PAPER AWARD
Bo-Yuan Huang, Princeton University, Princeton, NJ
Hongce Zhang, Princeton University, Princeton, NJ
Pramod Subramanyan, Indian Institute of Technology Kanpur, India
Yakir Vizel, Technion Israel Institute of Technology, Haifa, Israel
Aarti Gupta, Princeton University, Princeton, NJ
Sharad Malik, Princeton University, Princeton, NJ
For "Instruction-Level Abstraction (ILA): A Uniform Specification for System-on-Chip (SoC) Verification," Vol. 24, Issue 1, Jan. 2019

2020 ACM TRETS BEST PAPER AWARD
Michaela Blott, Xilinx Research Labs, Saggart, Ireland
Thomas B. Preußer, Xilinx Research Labs, Saggart, Ireland
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Yaman Umuroglu, Xilinx Research Labs, Saggart, Ireland
Miriam Leeser, Northeastern University, Boston, MA
Kees Vissers, Xilinx Research, San Jose, CA
For "FINN-R: An End-to-End Deep-Learning Framework for Fast Exploration of Quantized Neural Networks," Vol. 11, No. 3, Dec. 2018

ACM SIGDA DISTNGUISHED SERVICE AWARD
Sri Parameswaran, University of New South Wales, Australia
For leadership and distinguished service to the EDA community

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For a junior faculty member early in her or his academic career who demonstrates outstanding potential as an educator and/or researcher in the field of electronic design automation

ACM SIGDA OUTSTANDING PH.D. DISSERTATION AWARD
Gengjie Chen, Chinese University of Hong Kong, China
For "VLSI Routing: Seeing Nano Tree in Giga Forest"
Advisor: Evangeline F. Y. Young

ACM FELLOW
Diana Marculescu, University of Texas Austin, TX
For contributions to design and optimization of energy-aware computing systems

ACM FELLOW
Yuan Xie, University of California, Santa Barbara, CA
For contributions to the design techniques and tools for the implementation and evaluation of computer architectures

DESIGN AUTOMATION CONFERENCE UNDER-40 INNOVATORS AWARD
Kris Breen, Mentor, a Siemens Business, San Jose, CA
Shimeng Yu, Georgia Institute of Technology, Atlanta, GA
Jianyi Meng, Alibaba Group, Hangzhou, China

2020 MARIE R. PISTILLI WOMEN IN ENGINEERING ACHIEVEMENT AWARD
Alessandra Nardi, Cadence Design Systems, Inc., Berkeley, CA
This annual award, named for Marie R. Pistilli, the former organizer of DAC, recognizes individuals who have visibly helped advance women in Electronica Design.

P.O. PISTILLI UNDERGRADUATE SCHOLARSHIP FOR ADVANCEMENT IN COMPUTER SCIENCE AND ELECTRICAL ENGINEERING
Anthony Villegas
Will be attending UC Berkeley in the fall

57th DAC Best Paper Candidates

Fourteen research papers were nominated by the Technical Program Committee as DAC Best Paper Candidates. Final decisions will be made after the papers are presented at the conference.

Research:

20.1 - FLOPS: Efficient On-Chip Learning for Optical Neural Networks Through Stochastic Zeroth-Order Optimization
Jiaqi Gu - *Univ. of Texas at Austin, TX*
Zheng Zhao - *Univ. of Texas at Austin, TX*
Chenghao Feng - *Univ. of Texas at Austin, TX*
Wuxi Li - *Xilinx Inc., San Jose, CA*
Ray T. Chen - *Univ. of Texas at Austin, TX*
David Z. Pan - *Univ. of Texas at Austin, TX*

30.5 - Algorithm-Hardware Co-Design of Adaptive Floating-Point Encodings for Resilient Deep Learning Inference
Thierry Tambe - *Harvard Univ., Cambridge, MA*
En-Yu Yang - *Harvard Univ., Cambridge, MA*
Zishen Wan - *Harvard Univ., Cambridge, MA*
Yuntian Deng - *Harvard Univ., Cambridge, MA*
Vijay Janapa Reddi - *Harvard Univ., Cambridge, MA*
Alexander Rush - *Cornell Univ., New York, NY*
David Brooks - *Harvard Univ., Cambridge, MA*
Gu-Yeon Wei - *Harvard Univ., Cambridge, MA*

34.6 - TP-GNN: A Graph Neural Network Framework for Tier Partitioning in Monolithic 3D ICs
Yi-Chen Lu - *Georgia Institute of Technology, Atlanta, GA*
Sai Surya Kiran Pentapati - *Georgia Institute of Technology, Atlanta, GA*
Lingjun Zhu - *Georgia Institute of Technology, Atlanta, GA*
Kambiz Samadi - *Qualcomm Technologies, Inc., San Diego, CA*
Sung Kyu Lim - *Georgia Institute of Technology, Atlanta, GA*

35.1 - COEXE: An Efficient Co-Execution Architecture for Real-Time Neural Network Services
Liu Chubo - *Hunan Univ., China*
Kenli Li - *Hunan Univ., China*
Mingcong Song - *Univ. of Florida, Gainesville, FL*
Jiechen Zhao - *Univ. of Florida, Gainesville, FL*
Keqin Li - *State Univ. of New York, New Paltz, NY*
Tao Li - *Univ. of Florida, Gainesville, FL*
Zihao Zeng - *Hunan Univ., China*

67.5 - ATUNs: Modular and Scalable Support for Atomic Operations in a Shared Memory Multiprocessor
Andreas Kurth - *ETH Zurich, Switzerland*
Samuel Riedel - *ETH Zurich, Switzerland*
Florian Zaruba - *ETH Zurich, Switzerland*
Torsten Hoefler - *ETH Zurich, Switzerland*
Luca Benini - *ETH Zurich & Univ. of Bologna, Switzerland*

69.1 - A Two-Way SRAM Array Based Accelerator for Deep Neural Network On-Chip Training
Hongwu Jiang - *Georgia Institute of Technology, Atlanta, GA*
Shanshi Huang - *Georgia Institute of Technology, Atlanta, GA*
Xiaochen Peng - *Georgia Institute of Technology, Atlanta, GA*
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Yen-Chi Chou - *National Tsing Hua Univ., Taiwan*
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Ta-Wei Liu - *National Tsing Hua Univ., Taiwan*
Ruhui Liu - *National Tsing Hua Univ., Taiwan*
Meng-Fan Chang - *National Tsing Hua Univ., Hsinchu, Taiwan*
Shimeng Yu - *Georgia Institute of Technology, Atlanta, GA*

DESIGN AUTOMATION CONFERENCE 2020 PROCEEDINGS

10.1 - An Efficient Asynchronous Batch Bayesian Optimization Approach for Analog Circuit Synthesis
Shuhan Zhang, Fan Yang, Dian Zhou, Xuan Zeng

10.2 - GUI-Enhanced Layout Generation of FFE SST TXs for Fast High-Speed Serial Link Design
Seungho Han, Sungyu Jeong, Chanho Kim, Hong-June Park, Byungsub Kim

10.3 - Bit Parallel 6T SRAM In-Memory Computing with Reconfigurable Bit-Precision
Kyeongho Lee, Jinho Jeong, SungSoo Cheon, Woong Choi, Jongsun Park

10.4 - Factored Radix-8 Systolic Array for Tensor Processing
Inayat Ullah, Kashif Inayat, Joon-Sung Yang, Jaeyong Chung

11.1 - StatSAT: A Boolean Satisfiability Based Attack on Logic-Locked Probabilistic Circuits
Ankit Mondal, Michael Zuzak, Ankur Srivastava

11.2 - DECOY: DEflection-Driven HLS-Based Computation Partitioning for Obfuscating Intellectual PropertY
Jianqi Chen, Monir Zaman, Yiorgos Makris, R. D. Shawn Blanton, Subhasish Mitra, Benjamin Carrion Schaefer

11.3 - RELIC-FUN: Logic Identification through Functional Signal Comparisons
James Geist, Travis Meade, Shaojie Zhang, Yier Jin

11.4 - Flashmark: Watermarking of NOR Flash Memories for Counterfeit Detection
Prawar Poudel, Biswajit Ray, Aleksandar Milenkovic

13.1 - AI Utopia or Dystopia: On Securing AI Platforms
Patrick Jauernig, Emmanuel Stapf, Ghada Dessouky, Nele Mentens, Ahmad-Reza Sadeghi

13.2 - Unified Architectural Support for Secure and Robust Deep Learning
Mojan Javaheripi, Huili Chen, Farinaz Koushanfar

13.3 - Developing Privacy-preserving AI Systems: The Lessons Learned
Fabian Boemer, Rosario Cammarota, Huili Chen, Siam Umar Hussain, Ahmad-Reza Sadeghi , Emmanuel Stapf , Farinaz Koushanfar

14.1 - Time-Division Multiplexing Based System-Level FPGA Routing for Logic Verification
Peng Zou, Zhifeng Lin, Xiao Shi, Yingjie Wu, Jianli Chen, Jun Yu, Yao-Wen Chang

14.2 - Symbolic Computer Algebra and SAT Based Information Forwarding for Fully Automatic Divider Verification
Christoph Scholl, Alexander Konrad

14.3 - A-QED Verification of Hardware Accelerators
Eshan Singh, Florian Lonsing, Saranyu Chattopadhyay, Max Strange, Peng Wei, Xiaofan Zhang, Yuan Zhou, Jason Cong, Deming Chen, Zhiru Zhang, Priyanka Raina, Clark Barrett, Subhasish Mitra

14.4 - Circuit Learning for Logic Regression on High Dimensional Boolean Space
Pei-Wei Chen, Yu-Ching Huang, Cheng-Lin Lee, Jie-Hong Roland Jiang

DESIGN AUTOMATION CONFERENCE 2020 PROCEEDINGS

15.1 - Enabling a B+-Tree-Based Data Management Scheme for Key-Value Store Over SMR-Based SSHD
Yu-Pei Liang, Tseng-Yi Chen, Ching-Ho Chi, Hsin-Wen Wei, Wei-kuan Shih

15.2 - S-CDA: A Smart Cloud Disk Allocation Approach in Cloud Block Storage System
Hua Wang, Yang Yang, Ping Huang, Yu Zhang, Ke Zhou, Mengling Tao, Bin Cheng

15.3 - Content Sifting Storage: Achieving Fast Read for Large-Scale Image Dataset Analysis
Yu Liu, Hong Jiang, Yangtao Wang, Ke Zhou, Yifei Liu, Li Liu

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