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# Accelerating Spike-by-Spike Neural Networks on FPGA with Hybrid Custom Floating-Point and Logarithmic Dot-Product Approximation

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**ABSTRACT** Spiking neural networks (SNNs) represent a promising alternative to conventional neural networks. In particular, the so called Spike-by-Spike (SbS) neural networks provide an exceptional noise robustness and a reduced complexity. However, deep SbS networks require a memory footprint and a computational cost unsuitable for embedded applications. To address this problem, this work exploits the intrinsic error resilience of neural networks to improve performance and to reduce the hardware complexity. More precisely, we design a dot-product hardware unit based on approximate computing with configurable quality using hybrid custom floating-point and logarithmic number representation. This approach reduces computational latency, memory footprint, and power dissipation while preserving inference accuracy. To demonstrate our approach, we address a design exploration flow using high-level synthesis and a Xilinx SoC-FPGA. The proposed design reduces 20.5× computational latency and 8× weight memory footprint, with less than 0.5% of accuracy degradation on a handwritten digit recognition task.

**INDEX TERMS** Artificial intelligence, spiking neural networks, approximate computing, logarithmic, parameterisable floating-point, optimization, hardware accelerator, embedded systems, FPGA

## I. INTRODUCTION

THE exponential improvement in computing performance and the availability of large amounts of data are boosting the use of artificial intelligence (AI) applications in our daily lives. Among the various algorithms developed over the years, neural networks (NNs) have demonstrated remarkable performance in a variety of image, video, audio, and text analytics tasks [1], [2]. Historically, artificial neural networks (ANNs) can be classified into three different generations [3]: the first one is represented by the classical McCulloch and Pitts neuron model using discrete binary values as outputs; the second one is represented by more complex architectures as multi-layer perceptrons (MLPs) and convolutional neural networks (CNNs) using continuous activation functions; while the third generation is represented by spiking neural

networks using spikes as means for information exchange between groups of neurons. Although the AI research is currently dominated by deep neural networks (DNNs) from the second generation, the SNNs belonging to the third generation are receiving considerable attention [3]–[6].

SNNs offer advantageous robustness and the potential to achieve a power efficiency closer to that of the human brain. SNNs operate reliably using stochastic elements that are inherently non-reliable mechanisms [7]. This provides superior resistance against adversary attacks [5], [8]. Beside robustness, SNNs have further advantages like the possibility of a more efficient asynchronous parallelization and higher energy efficiency than DNNs. For example, Loihi [9], a SNN developed by Intel, can solve LASSO optimization problems with an over three orders of magnitude better

energy-delay product than conventional approaches. These advantages are motivating large research programs by major companies (e.g., Intel [9] and IBM [10]) as well as pan-european projects in the domain of spiking networks [4].

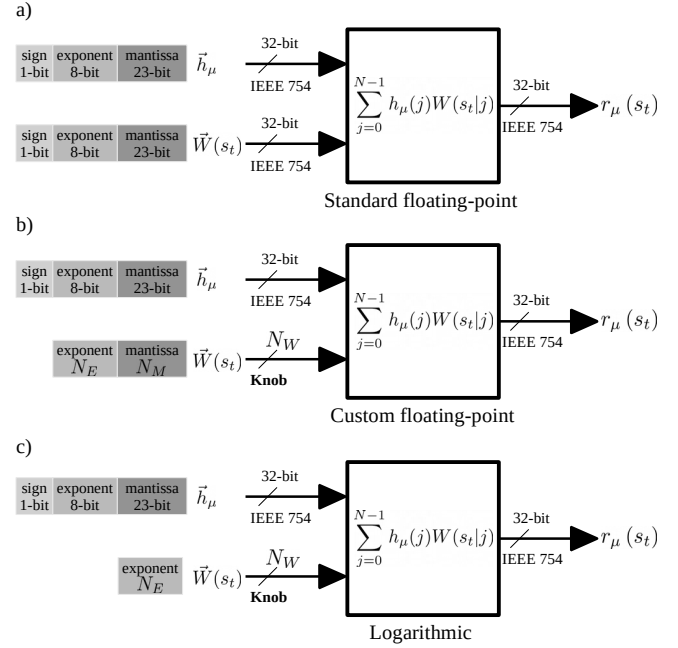
SNNs emulate the real behavior of neurons in different levels of detail. The more detailed the biological part is emulated, the greater the computational complexity [11], [12]. Most of today's SNNs use a very detailed model (e.g., Leaky Integrate-and-Fire (LIF)).

Alternatively, the Spike-by-Spike (SbS) neural network is a remarkable model for its reduced complexity, which is on the less realistic side of the SNN scale of biological realism [5], [13]. Consequently, the hardware complexity of SbS network implementations is greatly reduced [14], [15]. In spite of this, SbS still uses stochastic spikes as a means of transmitting information between populations of neurons and thus retains the advantageous robustness of SNNs.

The conceptual model in SbS (see Sec. III-A for a short review) differs fundamentally from conventional ANNs since (a) the building blocks of the network are inference populations (IP) which are an optimized generative representation with non-negative values, (b) time progresses from one spike to the next, preserving the property of stochastically firing neurons, and (c) a network has only a small number of parameters, which is an advantageous noise-robust stochastic version of Non-Negative Matrix Factorization (NNMF). The SbS network is placed between non-spiking NN and stochastically spiking NN, which offers advantages from both structures [13]. On one hand, the SbS model incorporates the inherent robustness of SNNs, which provide the possibility of more efficient asynchronous parallelization and superior resilience against disturbances based on the synaptic stochasticity; on the other hand, the SbS model incorporates the regular flow of information from CNNs, which are expressed on explicit vector operations.

As computational demanding algorithms, ANNs and SNNs in particular, must be addressed by specialized hardware architectures. A significant research effort has been performed in SNN accelerators, see e.g. Ref. [4], [9], [10], [16]–[18]. However, hardware accelerators that focus on SbS have only been partially investigated so far [14], [15]. Enhanced SbS accelerators will have a double impact. From an engineering point of view, they will contribute to the deployment of robust neural networks in small embedded systems [14]; from a scientific point of view, they will facilitate fundamental research for neuroscience [5], [19], [20].

A central point that can be optimized in current SbS accelerators is the use of approximation techniques. Most SbS models use floating-point numerical representation, which imposes high complexity of the required circuits for the floating-point operations. Model quantization has the potential to improve computational performance; however, this solution is often accompanied by quantization-aware training methods that, in some cases, are problematic or even inaccessible, particularly in deep SNN algorithms [21]. As



**FIGURE 1.** Dot-product hardware module with (a) standard floating-point (IEEE 754) arithmetic, (b) hybrid custom floating-point approximation, and (c) hybrid logarithmic approximation.

an alternative, based on the relaxed need for fully precise or deterministic computation of neural networks, approximate computing techniques allow substantial enhancement in processing efficiency with moderated accuracy degradation. Some research papers have shown the feasibility of applying approximate computing to the inference stage of neural networks [22]–[25]. Such techniques usually demonstrated small inference accuracy degradation, but significant enhancement in computational performance, resource utilization, and energy consumption. Hence, by taking advantage of the intrinsic error-tolerance of neural networks, approximate computing is positioned as a promising approach for inference on resource-limited devices.

In this paper, we accelerate SbS neural networks with a dot-product hardware design based on approximate computing with hybrid custom floating-point and logarithmic number representation. This hardware unit has a quality configurable scheme based on the bit truncation of the synaptic-weight vector. **Fig. 1** illustrates the dot-product hardware module with standard floating-point (IEEE 754) arithmetic, and our approach with hybrid custom floating-point as well as logarithmic approximation. As a design parameter, the mantissa bit-width of the weight vector provides a tunable knob to trade-off between efficiency and quality of result (QoR) [26], [27]. Since the lower-order bits have smaller significance than the higher-order bits, truncating them may have only a minor impact on QoR [28], [29]. Further on, we can remove completely the mantissa bits in order to use only the exponent of a floating-point representation. Therefore, the most efficient setup and yet the worst-case quality configuration becomes a logarithmic representation,

which consequently leads to significant architectural-level optimizations using only adders and shifters for dot-product approximation in hardware. Moreover, since approximations and noise have qualitatively the same effect [30], we apply noise tolerance plots as an intuitive visual measure to provide insights into the quality degradation of SbS networks under approximate processing effects.

Our main contributions are as follows:

- We develop a hardware component for dot-product approximation. To perform the sum of pairwise products of two vectors, this hardware module has the following three design features: (1) the pairwise product is approximated by adding integer exponents and multiplying truncated mantissas, and the sum of products is done by accumulating denormalized integer products with barrel shifters, which increases computational throughput; (2) the synaptic weight vector uses either reduced custom floating-point or logarithmic representation, which reduces memory footprint; and (3) the neuron vector uses either standard or custom floating-point representation, which preserves QoR and overall inference accuracy.
- We address a design exploration with the proposed dot-product approximation using synaptic weight vectors with custom floating-point and logarithmic representation as shown in Fig. 1. We evaluate inference latency, accuracy degradation, resource utilization and power dissipation. Experimental results demonstrate  $20.5\times$  latency enhancement versus embedded CPU (ARM Cortex-A9 at 666MHz), and less than 0.5% of accuracy degradation on a handwritten digit recognition task (MNIST). This machine learning task simply provides a proof of concept to demonstrate the feasibility of our approximation technique for SbS neural network accelerators.
- We propose a noise tolerance plot as quality monitor, which serves as an intuitive visual model to provide insights into the accuracy degradation of SbS networks under approximate processing effects.
- Our proposed design for dot-product approximation is adaptable as a building block for other error resilient applications (e.g., image/video processing).

The rest of the paper is organized as follows. Section II covers the related work; Section III introduces the background to SbS networks; Section IV describes the system design and the approximate dot-product hardware module; Section V presents the experimental results thorough a design exploration flow; Section VI concludes the paper.

To promote the research on SbS networks, our design exploration framework is made available to the public as an open-source project at <http://www.ids.uni-bremen.de/sbs-framework.html>

## II. RELATED WORK

### A. APPROXIMATE COMPUTING IN NEURAL NETWORKS

Approximate computing has been used in a wide range of applications to increase the computational efficiency in

hardware [27]. For neural network applications, two main approximation strategies are used, namely network compression and classical approximate computing [17].

#### 1) Network compression

Researchers focusing on embedded applications started lowering the precision of weights and activation maps to shrink the memory footprint of the large number of parameters representing ANNs, a method known as network compression or quantization. This practice takes advantage of the intrinsic error-tolerance of neural networks, as well as their ability to compensate for approximation while training. In this way, reduced bit precision causes a small accuracy loss [31]–[34].

In hardware development, weight quantization (WQ) has shown up to  $2\times$  improvement in energy consumption with an accuracy degradation of less than 1% [35], [36]. Some advanced quantization methods yield to binary neural networks (BNNs) allowing the use of XNORs instead of the conventional costly multiply-accumulate circuits (MACs) [34]. In [37], Sun et al. report an accuracy of 98.43% on handwritten digit classification (MNIST) with a simple BNN. Hence, quantization is a powerful tool for improving the energy efficiency and memory requirements of ANN accelerators, with limited accuracy degradation.

In addition to quantization, network pruning reduces the model size by removing structural portions of the parameters and its associated computations [38], [39]. This method has been identified as an effective technique to improve the efficiency of DNN for applications with limited computational budget [40]–[42].

These methods can be used for SNNs as well. In [43], Rathi et al. report up to  $3.1\times$  improvement in energy consumption with an accuracy loss of around 3%. Weight quantization allows the designer to realize a trade-off between the accuracy of the SNN application and efficiency of resources. Approximate computing can also be applied at the neuron level, where irrelevant units are deactivated to reduce the computation cost of the SNNs [44]. This computation skipping can be applied randomly on synapses, training ANNs with stochastic synapses improves generalization, resulting in a better accuracy [45], [46]. Such methods are compatible with SNNs and have been tested both during training [47], [48] and operation [49], and even to define the connectivity between layers [50], [51]. Implementations of spiking neuromorphic systems in FPGA [52] and hardware [53] demonstrated that synaptic stochasticity allows to increase the final accuracy of the networks while reducing memory footprint.

Quantization is therefore a powerful technique to improve energy efficiency and memory requirements of ANN and SNN accelerators, with small accuracy degradation. However, this approach requires quantization-aware training methods that, in some cases, are problematic or even inaccessible, particularly in emerging deep SNN algorithms [21].



## 2) Classical approximate computing

This approach consists of designing processing elements that approximate their computation by employing modified algorithmic logic units [27]. In [54], Kim et al. have shown SNNs using carry skip adders achieving  $2.4\times$  latency enhancement and 43% more energy efficiency, with an accuracy degradation of 0.97% on a handwritten digit classification task (MNIST). Therefore, approximate computing provides important enhancement in energy efficiency and processing speed.

However, as the complexity of the dataset increases, as well as the depth of the network topology, such as ResNet [55] on ImageNet [56], the accuracy degradation becomes more important and may not be negligible anymore [34], especially for critical applications such as autonomous driving. Therefore, it is not certain that network compression techniques and approximate computing are suitable for all applications.

## B. SPIKE-BY-SPIKE NEURAL NETWORKS ACCELERATORS

Recently, Rotermund et al. demonstrated the feasibility of a neuromorphic SbS IP on a Xilinx Virtex 6 FPGA [15]. It provides a massively parallel architecture, optimized to reduce memory access and suitable for ASIC implementations. Nonetheless, this design is considerably resource-demanding if implemented as a full SbS network in today's embedded technology.

In Ref. [14], we presented a cross-platform accelerator framework for design exploration and testing of fully functional SbS network models in embedded systems. As a hardware/software (HW/SW) co-design solution, this framework offers a comprehensive high level embedded software API that allows the construction of scalable sequential SbS networks with configurable hardware acceleration. However, this design works entirely with standard floating-point arithmetic (IEEE 754). This represents a large memory footprint and inadequate computational cost for error resilient applications on resource-limited devices. In this article, we will use this design exploration framework to investigate approximate computing for efficient deployment of deep SbS networks on resource-limited devices.

## III. BACKGROUND

### A. SPIKE-BY-SPIKE NEURAL NETWORKS

Technically, SbS is a spiking neural network approach based on a generative probabilistic model. It iteratively finds an estimate of its input probability distribution  $p(s)$  (i.e. the probability of input node  $s$  to stochastically send a spike) by its latent variables via  $r(s) = \sum_i h(i)W(s|i)$ . where  $\vec{h}$  is an inference population composed of a group of neurons that compete with each other. An inference population sees only the spikes  $s_t$  (i.e. the index identifying the input neuron  $s$  which generated that spike at time  $t$ ) produced by its input neurons, not the underlying input probability distribution  $p(s)$  itself. By counting the spikes arriving at a group of SbS

neurons,  $p(s)$  is estimated by  $\hat{p}(s) = 1/T \sum_t \delta_{s,s_t}$  after  $T$  spikes have been observed in total. The goal is to generate an internal representation  $r(s)$  from the string of incoming spikes  $s_t$  such that the negative logarithm of the likelihood  $L = C - \sum_\mu \sum_s \hat{p}_\mu(s) \log(r_\mu(s))$  is minimized.  $C$  is a constant which is independent of the internal representation  $r_\mu(s)$  and  $\mu$  denotes one input pattern from an ensemble of input patterns. Applying a multiplicative gradient descent method on  $L$ , an algorithm for iteratively updating  $h_\mu(i)$  with every observed input spike  $s_t$  could be derived [5]

$$h_\mu^{new}(i) = \frac{1}{1+\epsilon} \left( h_\mu(i) + \epsilon \frac{h_\mu(i)W(s_t|i)}{\sum_j h_\mu(j)W(s_t|j)} \right) \quad (1)$$

where  $\epsilon$  is a parameter that also controls the strength of sparseness of the distribution of latent variables  $h_\mu(i)$ . Furthermore,  $L$  can also be used to derive online and batch learning rules for optimizing the weights  $W(s|i)$ . The interested reader is referred to [5] for a more detailed exposition.

From a practical point of view, SbS provides a mechanism to obtain a sparse representation of input patterns. Given a set of training samples  $\{x_\eta\}$ , it learns weights ( $W$ ), that allow to express the input patterns as a linear sparse non-negative combination of features. During inference, it provides a mechanism for expressing each test input  $x_\mu$  as  $x_\mu \approx W h_\mu$  where all entries are non-negative.

The inference procedure consists in generating indices  $s_t$  distributed according to a categorical distribution of the input pattern  $s_t \sim \text{Categorical}(x_\mu(0), x_\mu(1), \dots, x_\mu(N-1))$ . Starting with a random  $h$  and executing iteratively Eq. (1) the SbS algorithm finds  $h_\mu$ . The fundamental concept of SbS can be extended from vector to matrix inputs. In this case, the linear operation  $W h_\mu$  can be replaced by a convolution to obtain a convolutional SbS layer. A detailed description of the SbS algorithm is presented in the supplementary material of this paper.

### B. BASIC NETWORK OVERVIEW

SbS network models can be constructed in sequential layered structures [13]. Each layer consists of many inference populations or IPs (represented by  $\vec{h}$ ), while the communication between them is organized by a low bandwidth signal – the spikes.

The SbS layer update is summarized in **Algorithm 1**. This is an iterative algorithm, where we denote the number of spikes ( $N_{Spk}$ ) as the number of iterations. As a generative model, each iteration updates the internal representation ( $H$ ) based on the input spikes ( $S_t^{in}$ ). A basic SbS network architecture for handwritten digit classification (MNIST) is shown in **Fig. 2** and **Tab. 1**. Each IP is an independent computational entity, this allows to design specialized hardware architectures that can be massively parallelized (see **Fig. 3**).

### C. COMPUTATIONAL COST

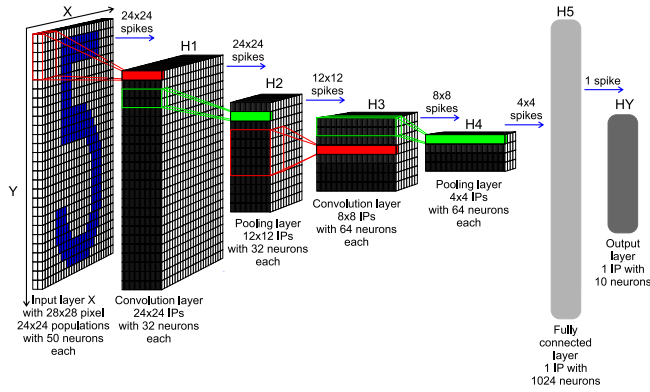
The number of multiply-accumulate (MAC) operations required for inference of an SbS layer is defined by

**Algorithm 1:** SbS layer update.

```

1: for  $t \leftarrow 0$  to  $N_{Spk} - 1$  do
2:   for  $x \leftarrow 0, y \leftarrow 0$  to  $N_X - 1, N_Y - 1$  do
3:      $S_t^{out}(x, y) \sim \text{Categorical}(H(x, y, :))$ 
4:     for  $\Delta_X \leftarrow 0, \Delta_Y \leftarrow 0$  to  $K_X - 1, K_Y - 1$  do
5:        $spk \leftarrow S_t^{in}(x + \Delta_X, y + \Delta_Y)$ 
6:       for  $i \leftarrow 0$  to  $N_H - 1$  do
7:          $\Delta h(i) \leftarrow H(x, y, i) \cdot W(\Delta_X, \Delta_Y, spk, i)$ 
8:          $r \leftarrow r + \Delta h(i)$ 
9:       end for
10:      for  $i \leftarrow 0$  to  $N_H - 1$  do
11:         $H^{new}(x, y, i) \leftarrow \frac{1}{1+\epsilon} (H(x, y, i) + \frac{\epsilon}{r} \Delta h(i))$ 
12:      end for
13:    end for
14:  end for
15: end for

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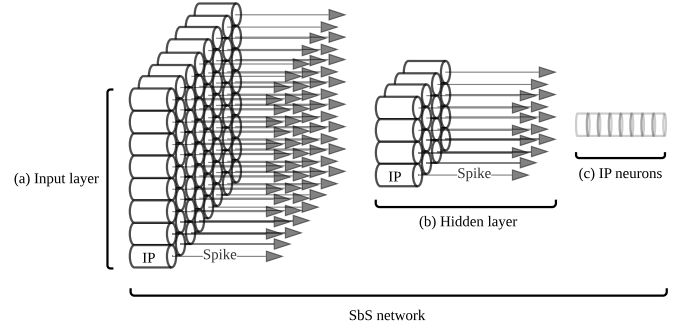
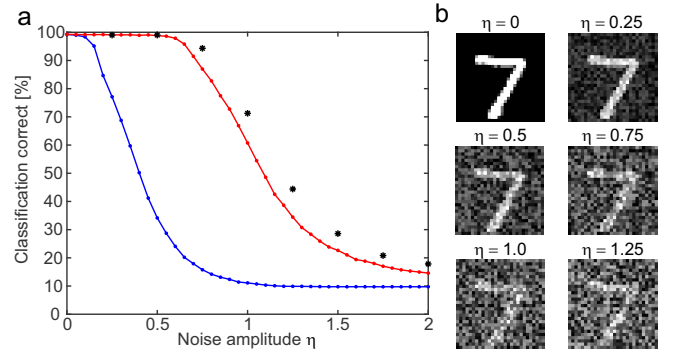
**FIGURE 2.** SbS network architecture for handwritten digit classification task.**TABLE 1.** SbS network architecture for handwritten digit classification task.

Layer ( $H^l$ )	Layer size			Kernel size	
	$N_X$	$N_Y$	$N_H$	$K_X$	$K_Y$
Input ( $HX$ )	28	28	2	-	-
Convolution ( $H1$ )	24	24	32	5	5
Pooling ( $H2$ )	12	12	32	2	2
Convolution ( $H3$ )	8	8	64	5	5
Pooling ( $H4$ )	4	4	64	2	2
Fully connected ( $H5$ )	1	1	1024	4	4
Output ( $HY$ )	1	1	10	1	1

$NOPS_{MAC} = N_{Spk} N_X N_Y K_X K_Y (3N_H + 2)$ , where  $N_{Spk}$  is the number of spikes (iterations),  $N_X N_Y$  is the size of the layer,  $K_X K_Y$  is the size of the kernel for convolution/pooling, and  $N_H$  is the length of  $\vec{h}$ . The computational cost of SbS network models is higher compared to equivalent CNN models and lower compared to regular SNN models (e.g., LIF) [11].

**D. ERROR RESILIENCE**

To illustrate the error resilience of SbS networks, we present a classification performance under positive additive uniformly distributed noise as external disturbance. **Fig. 4**

**FIGURE 3.** SbS IPs as independent computational entities, (a) illustrates an input layer with a massive amount of IPs operating as independent computational entities, (b) shows a hidden layer with an arbitrary amount of IPs as independent computational entities, (c) exhibits a set of neurons grouped in an IP.**FIGURE 4.** (a) Performance classification of SbS NN versus equivalent CNN, and (b) example of the first pattern in the MNIST test data set with different amounts of positive additive uniformly distributed noise.

presents a comparison of the classification performance of an SbS network and a standard CNN, with the same amount of neurons per layer as well as the same layer structure. We trained both neural networks for handwritten digit classification on MNIST dataset [57] (see [13] for details). The figure shows the correctness for the MNIST test set with its 10000 patterns in dependency of the noise level for positive additive uniformly distributed noise. The blue curve shows the performance for the CNN, while the red curve shows the performance for the SbS network with 1200 spikes (iterations). Beginning with a noise level of 0.1, the respective performances are different with a p - level of at least  $10^{-6}$  (tested with the Fisher exact test). Increasing the number of spikes per SbS population to 6000 (performance values shown as black stars), shows that more spikes can improve the performance under noise even more.

**IV. SYSTEM DESIGN**

In this section, we revise the system design of **Ref. [14]** where we presented a scalable hardware architecture composed of generic homogeneous accelerator units (AUs). This design works entirely with standard floating-point arithmetic (IEEE 754), which represents an unnecessary overhead for error resilient applications. Furthermore, this architecture

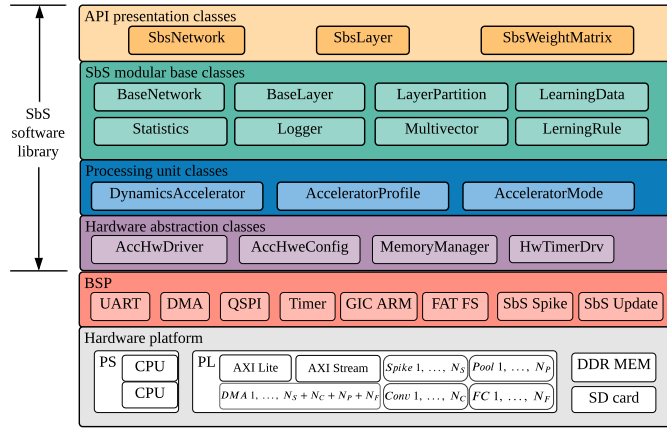


FIGURE 5. System-level overview of the embedded software architecture.

does not implement stationary synaptic weight matrices in the hardware AUs, resulting in heavy data movement, longer computational latency, and higher power consumption.

In this publication, we present an enhanced hardware architecture composed of specialized heterogeneous processing units (PUs) with hybrid custom floating-point and logarithmic dot-product approximation. This approach represents an advantageous design for error resilient applications in resource-constrained devices due to the reduced computational costs and memory footprint. Furthermore, the proposed approach allows the implementation of stationary synaptic weight matrices. These novelties result in an improved overall system design.

Regarding the software architecture, this is structured as a layered object-oriented application framework written in the C programming language. This offers a comprehensive high level embedded software application programming interface (API) that allows the construction of scalable sequential SbS networks with configurable hardware acceleration. Conceptually this design is modular, reusable, and extensible. The overall structure is depicted in Fig. 5.

### A. HARDWARE ARCHITECTURE

As a hardware/software co-design, the system architecture is an embedded CPU+FPGA-based platform, where the acceleration of SbS network computation is based on asynchronous<sup>1</sup> execution in parallel heterogeneous processing units: *Spike* (input layer), *Conv* (convolution), *Pool* (pooling), and *FC* (fully connected). Fig. 6 illustrates the system hardware architecture as a scalable structure. For hyperparameter configuration, each PU uses AXI-Lite interface. For data transfer, each PU uses AXI-Stream interfaces via Direct Memory Access (DMA) allowing data movement with high transfer rate. Each PU asserts an interrupt flag once the job or transaction is complete. This interrupt event is handled by the embedded CPU to collect results and start a new transaction.

<sup>1</sup>The system is synchronous at the circuit level, but the execution is asynchronous in terms of jobs.

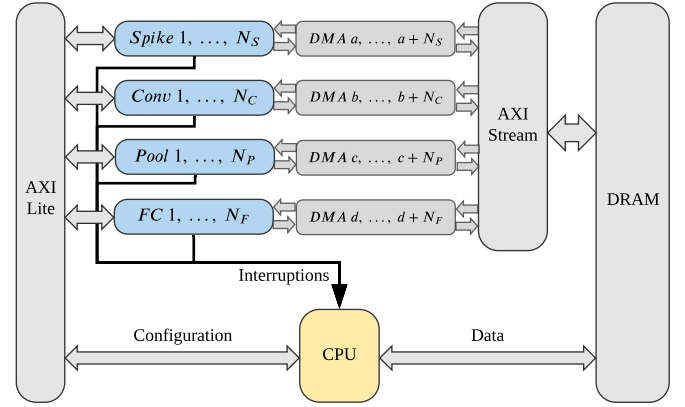


FIGURE 6. System-level hardware architecture with scalable number of heterogeneous PUs: *Spike*, *Conv*, *Pool*, and *FC*

The hardware architecture can resize its resource utilization by changing the number of PUs instances prior to the hardware synthesis, this provides scalability with a good trade-off between area and throughput. The dedicated PUs for *Conv* and *FC* implement the proposed dot-product approximation as a system component. The PUs are written in C using Vivado HLS (High-Level Synthesis) tool. In this publication, we illustrate the integration of the approximate dot-product component on the *Conv* processing unit.

### B. CONV PROCESSING UNIT

This hardware module computes the IP dynamics defined by Eq. (1) and offers two modes of operation: *configuration* and *computation*.

#### 1) Configuration mode

In this mode of operation, the PU receives and stores in on-chip memory (BRAM) the hyperparameters to compute the IP dynamics:  $\epsilon$  as the epsilon,  $N$  as the length of  $\tilde{h}_\mu \in \mathbb{R}^N$ ,  $K \in \mathbb{N}$  as the size of the convolution kernel, and  $H \in \mathbb{N}$  as the number of IPs to process per transaction.  $H$  is the number of IPs forming a layer or a partition.

Additionally, the processing unit also stores in on-chip memory (BRAM) the synaptic weight matrix using a number representation with a reduced memory footprint. Fundamentally, the synaptic weight matrix is defined by  $W \in \mathbb{R}^{K \times K \times M \times N}$  with  $0 \leq W(s_t|j) \leq 1$  and  $\sum_{s_t=0}^{M-1} W(s_t|j) = 1$  [13]. Hence,  $W$  employs only positive normalized real numbers. Therefore,  $W$  is deployed using a reduced floating-point or logarithmic representation as follows:

- Custom floating-point representation. In this case,  $W$  is deployed with a reduced floating-point representation using the user defined bit-width for the exponent and for the mantissa. For example, 4-bit exponent, 1-bit mantissa; as a result: 5-bit custom floating-point. The methodology to determine the required bit-width is described in Section IV-C.

- **Logarithmic representation.** In this case, the synaptic weight matrix is  $W \in \mathbb{N}^{K \times K \times M \times N}$  with positive natural numbers. Since  $0 \leq W(s_t|j) \leq 1$  and  $\sum_{s_t=0}^{M-1} W(s_t|j) = 1$ ,  $W$  has only negative values in the logarithmic domain. Hence, the sign bit is omitted, and the values are represented in its positive form. Therefore,  $W$  is deployed with a representation using the necessary bit-width for the exponent according to the given application. For example, 4-bit exponent. The methodology to determine the required bit-width is described in Section IV-C.

In order to deploy different SbS network models, the *Conv* processing units can be configured with different synaptic weight matrices and hyperparameters as required through the embedded software.

## 2) Computation mode

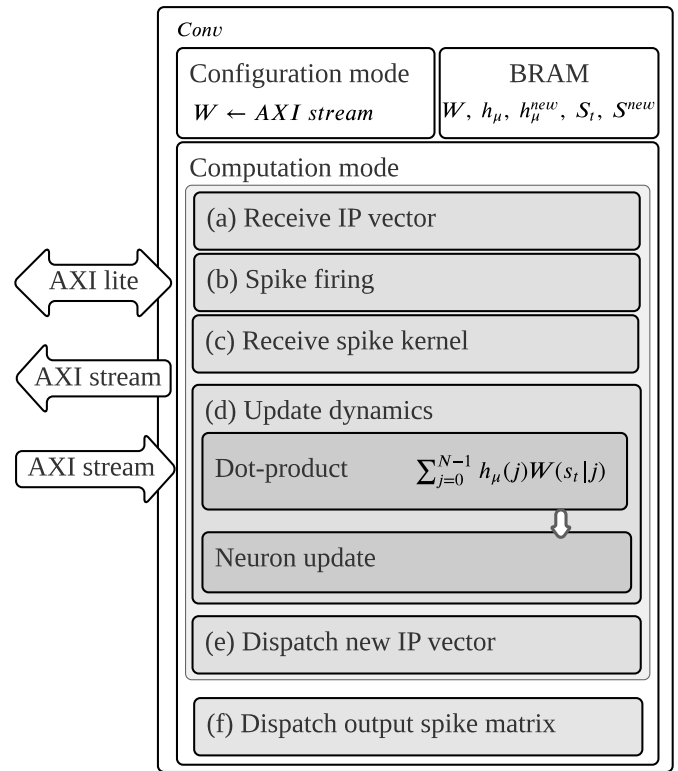
In this mode of operation, the PU executes a transaction to process a group of IPs using the previously given hyperparameters and synaptic weight matrix. This process operates in six stages as shown in **Fig. 7**. In the first two stages, the PU receives  $\vec{h}_\mu \in \mathbb{R}^N$ , then the PU calculates the emitted spike, and stores it in  $S^{new} \in \mathbb{N}^H$  (output spike vector). From the third to the fifth stage, the PU receives  $S_t \in \mathbb{N}^{K \times K}$  (input spike matrix), then it computes the update dynamics, and then it dispatches  $\vec{h}_\mu^{new} \in \mathbb{R}^N$  (updated IP). This process repeats for  $H$  number of loops (for each IP of the layer or partition). Finally, the  $S^{new}$  is dispatched.

The computation of the update dynamics (see **Fig. 7(d)**) operates in two modular stages: *dot-product* and *neuron update*. First, the *dot-product* module calculates the sum of pairwise products of  $\vec{h}_\mu$  and  $\vec{W}(s_t)$ , each pairwise product is stored as intermediate results. Subsequently, the *neuron update* module calculates **Eq. (1)** reusing previous results and parameters.

The calculation of the dot-product of **Eq. (1)** represents a considerable computational cost using standard floating-point in non-quantized network models. Fortunately, the pair product of  $h_\mu(j)$  and  $W(s_t|j)$  was defined by us as an approximable factor in the dot-product of **Eq. (1)**. In the following section, we focus on an optimized dot-product hardware design based on approximate computing.

## C. DOT-PRODUCT HARDWARE MODULE

This dot-product hardware module is part of an application-specific architecture optimized to approximate the dot-product of arbitrary length, see **Eq. (2)**. For quality configurability, we parameterized the mantissa bit-width of  $\vec{W}(s_t)$ , which provides a tunable trade-off between resource utilization and QoR. Since the lower-order bits have smaller significance than the higher-order bits, removing them may have only a minor impact on QoR. We designate this as hybrid custom floating-point approximation (see **Fig. 8(a)**).



**FIGURE 7.** The *Conv* processing unit and its six stages: (a) receive IP vector, (b) spike firing, (c) receive spike kernel, (d) update dynamics, (e) dispatch new IP vector, (f) dispatch output spike matrix.

$$r_\mu(s_t) = \sum_{j=0}^{N-1} h_\mu(j)W(s_t|j) \quad (2)$$

Further on, we remove the mantissa bits completely in order to use only the exponent of a floating-point representation. Hence, the worst-case quality and yet the most efficient configuration becomes a logarithmic representation. Consequently, this structure leads to advantageous architectural optimizations using only adders and barrel shifters for dot-product approximation in hardware. We designate this as hybrid logarithmic approximation (see **Fig. 8(b)**).

In order to determine the required bit-width for the number representation, we use **Eq. (3)**, **Eq. (4)**, and **Eq. (5)**.

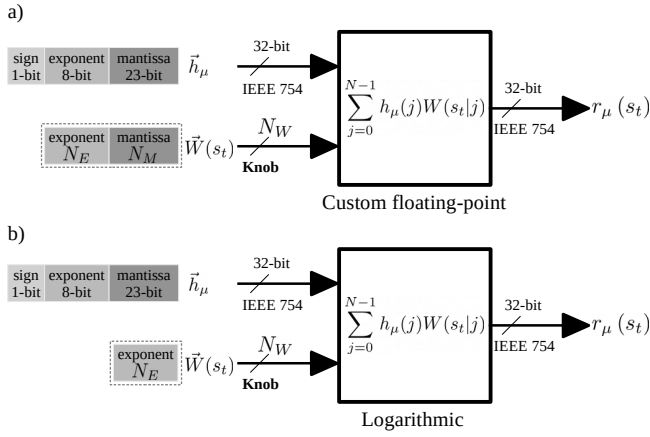
$$E_{\min} = \log_2(\min_{\forall i}(W(i))) \quad (3)$$

$$N_E = \lceil \log_2(|E_{\min}|) \rceil \quad (4)$$

$$N_W = N_E + N_M \quad (5)$$

The **Eq. (3)** obtains the exponent of the minimum entry value in the synaptic weight matrix. Since  $0 \leq W(s_t|j) \leq 1$  and  $\sum_{s_t=0}^{M-1} W(s_t|j) = 1$ ,  $W$  has only negative values in





**FIGURE 8.** Dot-product hardware module with (a) hybrid custom floating-point approximation, and (b) hybrid logarithmic approximation.

the logarithmic domain; hence, by searching for the smallest value, we obtain the biggest negative exponent ( $E_{\min}$ ). Then, the Eq. (4) obtains the necessary bit-width to represent the exponent ( $N_E$ ). Finally, we obtain the total bit-width by incorporating both exponent and mantissa bit-widths in Eq. (5).  $N_M$  denotes the mantissa bit-width, this is a knob parameter that is tuned by the designer to trade-off between resource utilization and QoR. The bit-width concept is illustrated in Fig. 8.

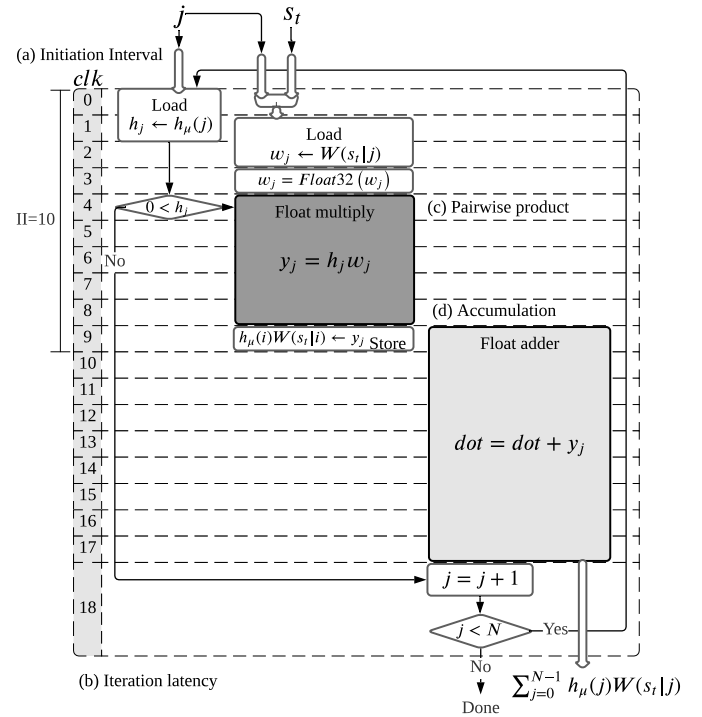
In this section, we will present three pipelined hardware modules with standard floating-point (IEEE 754) computation, hybrid custom floating-point approximation, and hybrid logarithmic approximation.

#### 1) Dot-product with standard floating-point computation

The hardware module to calculate the dot-product with standard floating-point computation is shown in Fig. 9. This diagram presents the hardware blocks and their clock cycle schedule. This module loads both  $h_\mu(j)$  and  $W(s_t|j)$  from BRAM, then the PU executes the pairwise product (Fig. 9(c)) and accumulation (Fig. 9(d)). The intermediate results of  $h_\mu(j)W(s_t|j)$  are stored in BRAM for reuse in the neuron update. The latency in clock cycles of this hardware module is defined by Eq. (6), where  $N$  is the dot-product length. This latency equation is obtained from the general pipelined hardware latency formula:  $L = (N - 1)II + IL$ , where  $II$  is the initiation interval (Fig. 9(a)), and  $IL$  is the iteration latency (Fig. 9(b)). Both  $II$  and  $IL$  are obtained from the high-level synthesis analysis. The equation for the latency with standard 32-bit floating-point is:

$$L_{f32} = 10N + 9 \quad (6)$$

In this design, the high-level synthesis tool infers computational blocks with considerable latency cost for standard floating-point. In the case of floating-point multiplication (Fig. 9(c)), the synthesis infers a hardware block with a latency cost of 5 clock cycles. Theoretically, this block would handle exponents addition, mantissas multiplication,



**FIGURE 9.** Dot-product hardware module with standard floating-point (IEEE 754) computation, (a) exhibits the initiation interval of 10 clock cycles, (b) presents the iteration latency of 19 clock cycles, (c) shows the pairwise product block in dark-gray, and (d) illustrates the accumulation block in light-gray.

and mantissa correction if needed. Moreover, in the case of floating-point addition (Fig. 9(d)), the synthesis infers a hardware block with a latency cost of 9 clock cycles. Seemingly, this block would handle mantissas alignment, addition, and correction if needed. Therefore, the use of standard floating-point in high-level synthesis results in high computational cost, which represents unnecessary overhead in error tolerant applications.

#### 2) Dot-product with hybrid custom floating-point and logarithmic approximation

The hardware module to calculate dot-product with hybrid custom floating-point approximation is shown in Fig. 10. In this design,  $h_\mu(j)$  uses standard 32-bit floating-point number representation, and  $W(s_t|j)$  uses a positive reduced custom floating-point number representation, where the mantissa bit width is the quality configurability knob. This parameter is tuned by the designer to trade-off between QoR and resource utilization, thus, energy consumption.

As the most efficient setup and yet the worst-case quality configuration, by completely truncating the mantissa of  $W(s_t|j)$  leads to a slightly different hardware architecture using only adders and shifters, which computes the dot-product with hybrid logarithmic approximation. This is shown in Fig. 11.

Additionally, the exponent bit-width of  $W(s_t|j)$  is a design parameter for efficient resource utilization and it is defined based on the application or deployment needs.

The hybrid custom floating-point and logarithmic approximation designs work in three phases: *Computation*, *Threshold-test*, and *Result normalization*.

- Phase I, *Computation*:

This phase approximates the magnitude of the dot-product in a denormalized representation. This is calculated in two iterative steps over each vector element: *pairwise product* and *accumulation*, where *pairwise product* is executed either in hybrid custom floating-point or hybrid logarithmic approximation described below.

- Pairwise product.

- Hybrid custom floating-point approximation. As shown in Fig. 10(c) in dark-gray, the pairwise product is approximated by adding exponents and multiplying mantissas of both  $W(s|i)$  and  $h_\mu(i)$ . If the mantissa multiplication results in an overflow, then it is corrected by increasing the exponent and shifting the resulting mantissa by one position to the right. Then we get  $h_\mu(j)W(s_t|j)$  as an intermediate result which is stored for future reuse in the neuron update calculation. In this design the pairwise product has a latency of 5 clock cycles.

- Hybrid logarithmic approximation. As shown in Fig. 11(c) in dark-gray, the pairwise product is approximated by adding  $W(s|i)$  to the exponent of  $h_\mu(i)$ , since  $W(s|j)$  values are represented in the logarithmic domain and  $h_\mu(j)$  in standard floating-point. In this design the pairwise product has a latency of one clock cycle.

- Accumulation. As shown in both Fig. 10(d) and Fig. 11(d) in light-gray, first, it is obtained the denormalized representation of  $h_\mu(j)W(s_t|j)$  by shifting its mantissa using its exponent as shifting parameter (barrel shifter). Then, this denormalized representation is accumulated to obtain the approximated magnitude of the dot-product.

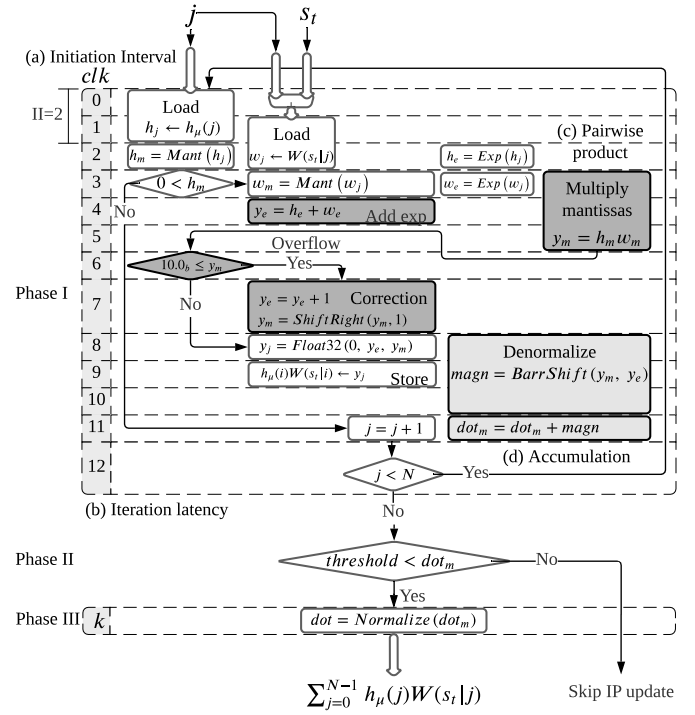
The process of pairwise product and accumulation iterates over each element of the vectors. The computation latency is given by Eq. (7) for hybrid custom floating-point, and Eq. (8) for hybrid logarithmic, where  $N$  is the length of the vectors. Both pipelined hardware modules have the same throughput, since both have two clock cycles as initiation interval.

$$L_{custom} = 2N + 11 \quad (7)$$

$$L_{log} = 2N + 7 \quad (8)$$

- Phase II, *Threshold-test*:

The accumulated denormalized magnitude is tested to be above of a predefined threshold, it must be above zero, since the dot-product is the denominator in Eq. (1). If passing the threshold, then the next phase is executed.



**FIGURE 10.** Dot-product hardware module with hybrid custom floating-point approximation. (a) exhibits the initiation interval of 2 clock cycles, (b) presents the iteration latency of 13 clock cycles, (c) shows the pairwise product blocks in dark-gray, and (d) illustrates the accumulation blocks in light-gray.

Otherwise the rest of update dynamics is skipped. The threshold-test takes one clock cycle.

- Phase III, *Result-normalization*:

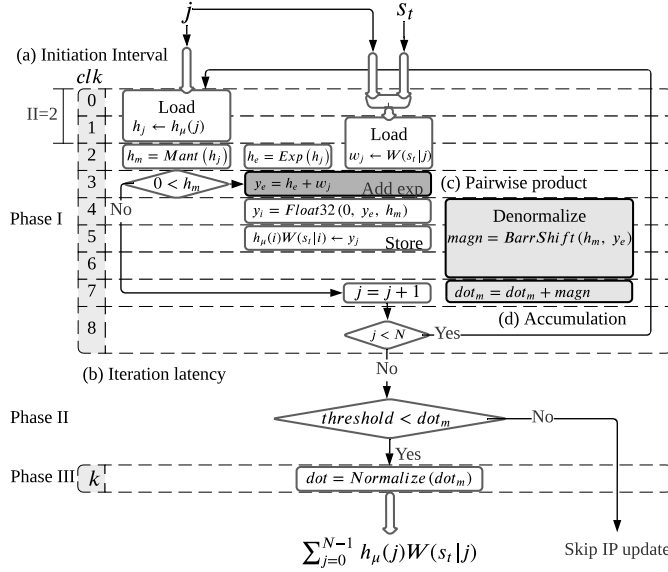
In this phase, the dot-product is normalized to obtain the exponent and mantissa in order to convert it to standard floating-point for later use in the neuron update. The normalization is obtained by shifting the approximated dot-product magnitude in a loop until it is in the form of a normalized mantissa where the iteration count represents the exponent of the dot-product. Each iteration takes one clock cycle.

The total latency of the hardware module with hybrid custom floating-point and hybrid logarithmic approximation is the accumulated latency of the three phases.

The proposed architectures with approximation approach exceeds the performance of the design with standard floating-point. This performance enhancement is achieved by decomposing the floating-point computation into an advantageous handling of exponent and mantissa using intermediate accumulation in a denormalized representation and only one final normalization.

## V. EXPERIMENTAL RESULTS

The proposed architecture is demonstrated on a Xilinx Zynq-7020. This device integrates a dual ARM Cortex-A9 based processing system (PS) and programmable logic (PL) equivalent to Xilinx Artix-7 (FPGA) in a single chip [58]. The Zynq-7020 architecture conveniently maps the custom logic



**FIGURE 11.** Dot-product hardware module with hybrid logarithmic approximation, (a) exhibits the initiation interval of 2 clock cycles, (b) presents the iteration latency of 9 clock cycles, (c) shows the pairwise product block in dark-gray, and (d) illustrates the accumulation blocks in light-gray.

and software in the PL and PS respectively as an embedded system.

In this platform, we implement the proposed hardware architecture to deploy the SbS network structure shown in **Fig. 2** for handwritten digit classification task using MNIST data set. The SbS model is trained in Matlab without any quantization method, using standard floating-point. The resulting synaptic weight matrices are deployed on the embedded system. There, the SbS network is built as a sequential model using the API from the SbS embedded software framework [14]. This API allows to configure the computational workload of the neural network, which can be distributed among the hardware processing units and the embedded CPU.

For the evaluation of our approach, we address a design exploration by reviewing the computational latency, inference accuracy, resource utilization, and power dissipation. First, we benchmark the performance of SbS network simulation on the embedded CPU, and then repeat the measurements on hardware processing units with standard floating-point computation. Afterwards, we evaluate our dot-product architecture, addressing a design exploration with hybrid custom floating-point approximation, as well as the hybrid logarithmic approximation. Finally, we present a discussion of the presented results.

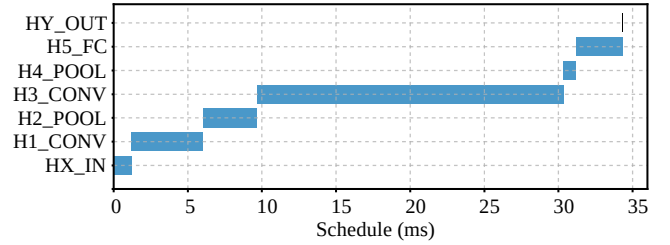
## A. PERFORMANCE BENCHMARK

### 1) Benchmark on embedded CPU

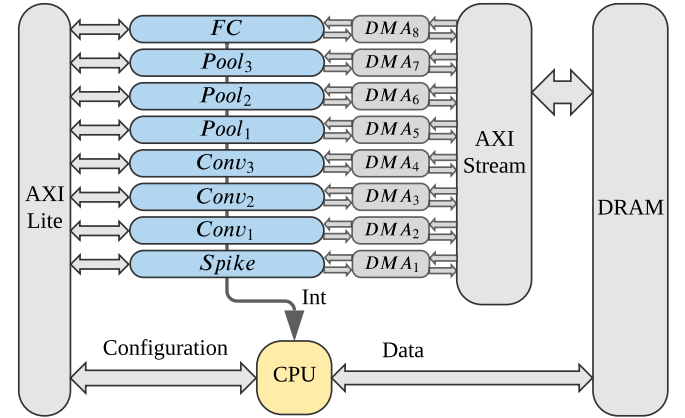
We examine the performance of the CPU for SbS network simulation with no hardware coprocessing. In this case, the embedded software builds the SbS network as a sequential model mapping the entire computation to the CPU (ARM

**TABLE 2.** Computation on embedded CPU.

Layer	Latency (ms)
HX_IN	1.184
H1_CONV	4.865
H2_POOL	3.656
H3_CONV	20.643
H4_POOL	0.828
H5_FC	3.099
HY_OUT	0.004
TOTAL	34.279



**FIGURE 12.** Computation on embedded CPU.



**FIGURE 13.** System overview of the top-level architecture with 8 processing units.

Cortex-A9) at 666 MHz and a power dissipation of 1.658W.

The SbS network computation on the CPU achieves a latency of 34.28ms per spike with an accuracy of 99.3% correct classification on the 10,000 image test set with 1000 spikes. The latency and schedule of the SbS network computation are displayed in **Tab. 2** and **Fig. 12** respectively.

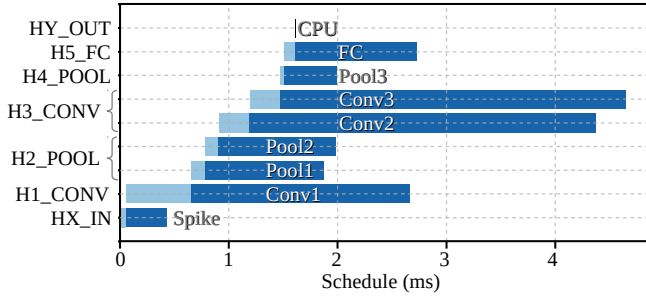
### 2) Benchmark on processing units with standard floating-point computation

To benchmark the computation on hardware PUs with standard floating-point, we implement the system architecture shown in **Fig. 13**. In this case, the embedded software builds the SbS network as a sequential model mapping the network computation to the hardware processing units at 200 MHz as clock frequency.

The layers of the neural network with the most neurons are partitioned for asynchronous parallel processing. Since H2\_POOL and H3\_CONV are the layers with the most neu-

**TABLE 3.** Performance of processing units with standard floating-point (IEEE 754) computation.

Hardware mapping		Computation schedule (ms)			
Layer	PU	$t_s$	$t_{CPU}$	$t_{PU}$	$t_f$
HX_IN	Spike	0	0.056	0.370	0.426
H1_CONV	Conv1	0.058	0.598	2.002	2.658
H2_POOL	Pool1	0.658	0.126	1.091	1.875
H2_POOL	Pool2	0.785	0.125	1.075	1.985
H3_CONV	Conv2	0.911	0.280	3.183	4.374
H3_CONV	Conv3	1.193	0.279	3.176	4.648
H4_POOL	Pool3	1.473	0.037	0.481	1.991
H5_FC	FC	1.512	0.101	1.118	2.731
HY_OUT	CPU	1.615	0.004	0	1.619

**FIGURE 14.** Performance of processing units with standard floating-point (IEEE 754) computation.

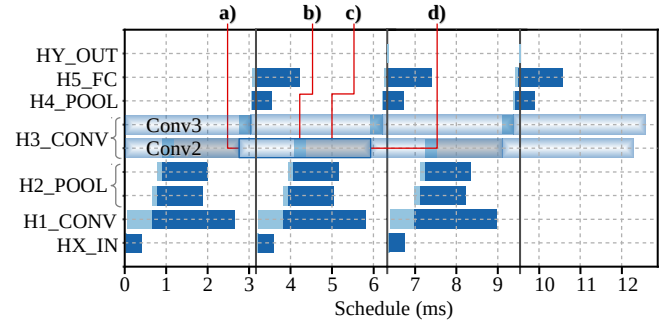
rons, the computational workload is distributed between two PUs for each one of these layers. The output layer *HY\_OUT* is fully processed by the CPU, since it is the layer with fewest neurons. The hardware mapping and the computation schedule of this deployment are displayed in **Tab. 3** and **Fig. 14**.

In the computation schedule, the following terms are defined as follows:  $t_s(n)$  as the start time for the processing of the neural network layer (as a compute node)  $n \in L$  where  $L$  represents the set of layers;  $t_{CPU}(n)$  as the CPU preprocessing time;  $t_{PU}(n)$  as the PU latency; and  $t_f(n)$  as the finish time. For data preparation, the  $t_{CPU}(n)$  is the duration in which the CPU writes a DRAM buffer with  $\vec{h}_\mu$  (vector of neuron latent variables) of the current processing layer and  $S_t$  (input spike matrix) from its preceding layer. This buffer is streamed to the PU via DMA.

The total execution time of the CPU is defined by **Eq. (9)**. In a cyclic spiking inference, the execution time of the network computation is the longest path among the processing units including the CPU. This is denoted as the latency of an spike cycle and it is defined by **Eq. (11)**. The total execution time of the network computation is the last finish time ( $t_f$ ) in the schedule defined by **Eq. (12)**.

$$T_{CPU} = \sum_{n \in L} t_{CPU}(n) \quad (9)$$

$$T_{PU} = \max_{n \in L} (t_{PU}(n)) \quad (10)$$

**FIGURE 15.** Performance bottleneck of cyclic computation on processing units with standard floating-point (IEEE 754) arithmetic, (a) exhibits the starting of  $t_{PU}$  of *Conv2* on a previous computation cycle, (b) presents  $t_{CPU}$  of *Conv2* on the current computation cycle, (c) shows the CPU waiting time (in gray color) for *Conv2* as a busy resource (awaiting for *Conv2* interruption), and (d) illustrates the  $t_f$  from the previous computation cycle, the starting of  $t_{PU}$  on the current computation cycle (*Conv2* interruption on completion, and start current computation cycle).

$$T_{SC} = \begin{cases} T_{PU}, & \text{if } T_{CPU} \leq T_{PU} \\ T_{CPU}, & \text{otherwise} \end{cases} \quad (11)$$

$$T_f = \max_{n \in L} (t_f(n)) \quad (12)$$

Using standard floating-point requires a high computational cost. As the largest layer, the computational workload of *H3\_CONV* is evenly partitioned among two PUs: *Conv2* and *Conv3*. However, in the cyclic schedule, *Conv2* causes the performance bottleneck as shown in **Fig. 15**. In this case, the CPU has to await for *Conv2* to finish the computation of the previous cycle in order to start the current computation cycle. In contrast, as the smallest layer, the computational workload of *HY\_OUT* is fully processed by the CPU. **Tab. 3** and **Fig. 14** show  $4\mu s$  as the processing latency of *HY\_OUT*. This latency is negligible compared to the overall performance assessment. Accelerating *HY\_OUT* would yield a negligible gain. Moreover, assigning a dedicated hardware PU to *HY\_OUT* would add data transfer and hardware interruption handling overheads, which makes this unprofitable.

Applying **Eq. (11)**, we obtain a latency of  $3.18ms$  per spike cycle. This deployment achieves an accuracy of 98.98% correct classification on the 10,000 image test set with 1000 spikes.

The post-implementation resource utilization and power dissipation are shown in **Tab. 4**. Each *Conv* PU instantiates an on-chip stationary weight matrix of 52,000 entries, which is sufficient to store  $W \in \mathbb{R}^{5 \times 5 \times 2 \times 32}$  and  $W \in \mathbb{R}^{5 \times 5 \times 32 \times 64}$  for *H1\_CONV* and *H3\_CONV*, respectively. In order to reduce BRAM utilization, we use a custom floating-point representation composed of 4-bit exponent and 4-bit mantissa. Each 8-bit entry is promoted to its standard floating-point representation for the dot-product computation. The methodology to find the appropriate bit-width parameters for custom floating-point representation is presented in Section V-B1.



**TABLE 4.** Resource utilization and power dissipation of processing units with standard floating-point (IEEE 754) computation.

PU	LUT	FF	DSP	BRAM 18K	Power (mW)
Spike	2,640	4,903	2	2	38
Conv	2,765	4,366	19	37	89
Pool	2,273	3,762	5	3	59
FC	2,649	4,189	8	9	66

The implementation of dot-product with standard floating-point arithmetic (IEEE 754) utilizes proprietary multiplier and adder floating-point operator cores. Vivado HLS accomplishes floating-point arithmetic operations by mapping them onto Xilinx LogiCORE IP cores, these floating-point operator cores are instantiated in the resultant RTL [59]. In this case, the implementation of the dot-product with the standard floating-point computation reuses the multiplier and adder cores already instantiated and used in other computation sections of *Conv* and *FC* processing units. The post-implementation resource utilization and power dissipation of the floating-point operator cores are shown in **Tab. 5**.

**TABLE 5.** Resource utilization and power dissipation of multiplier and adder floating-point (IEEE 754) operator cores.

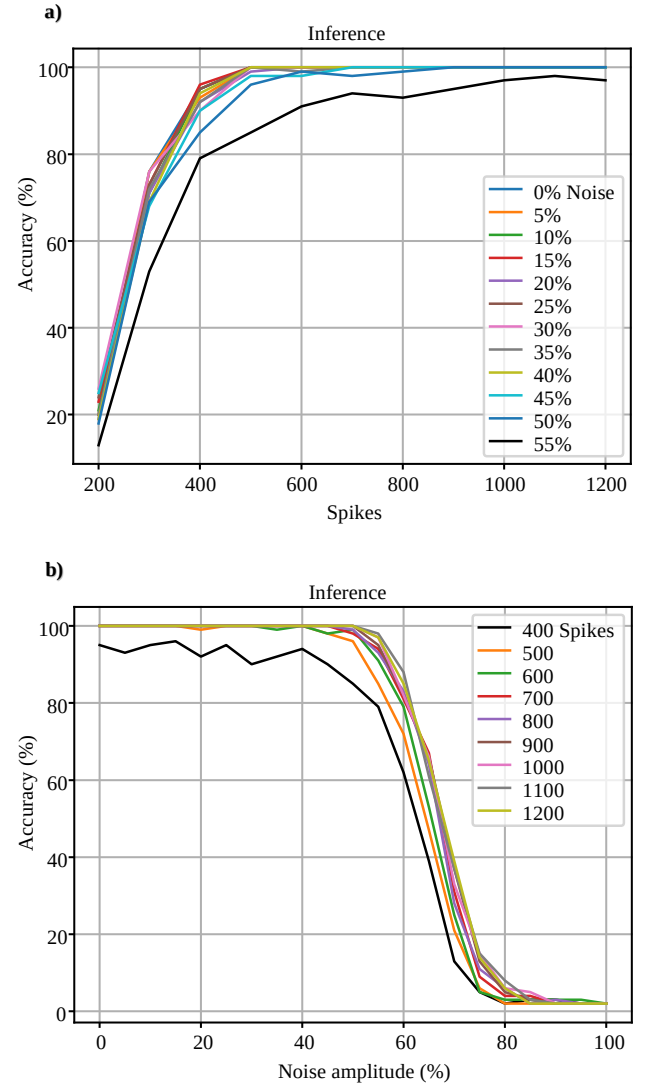
Core operation	DSP	FF	LUT	Latency (clk)	Power (mW)
Multiplier	3	151	325	4	7
Adder	2	324	424	8	6

### 3) Benchmark on noise tolerance plot

The noise tolerance plot serves as an intuitive visual model used to provide insights into accuracy degradation under approximate processing effects. This plot reveals inherent error resilience, and hence, approximation resilience. As an application-specific quality metric, this plot offers an effective method to estimate the overall quality degradation of the SbS network under different approximate processing effects, since both approximations and noise have qualitatively the same effect [30].

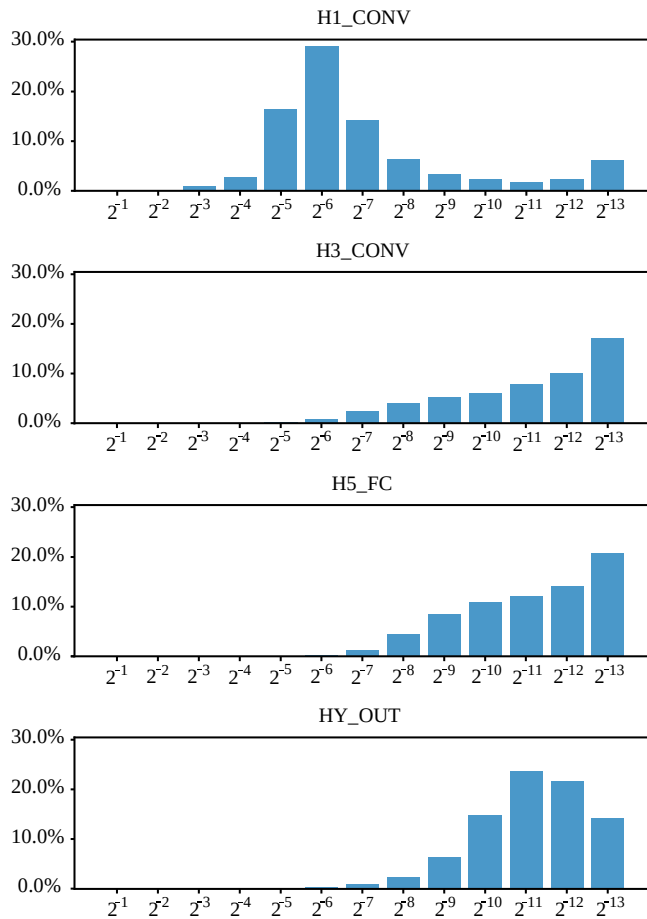
In order to experimentally obtain the noise tolerance plot, we measure the inference accuracy of the neural network with increasing number of spikes. Then we repeat the measurements with uniformly distributed noise applied on the input images. We gradually ascend the levels of the noise amplitude, until accuracy degradation is detected. **Fig. 16** demonstrates this method using 100 sample images.

As benchmark, the tolerance plot in **Fig. 16** reveals accuracy degradation having 50% noise and convergence with 400 spikes. In this case, the particular SbS network with precise processing demonstrates a remarkable inherent error resilience, hence, a great opportunity for approximate processing.

**FIGURE 16.** Noise tolerance on hardware PU with standard floating-point (IEEE 754) computation (benchmark/reference), (a) exhibits accuracy degradation applying 50% of noise amplitude, and (b) illustrates convergence of inference with 400 spikes.

## B. DESIGN EXPLORATION WITH HYBRID CUSTOM FLOATING-POINT AND LOGARITHMIC APPROXIMATION

In this section, we address a design exploration to evaluate our approach for SbS neural network simulation using hybrid custom floating-point and logarithmic approximation. First, we examine the synaptic weight matrix of each SbS network layer in order to determine the minimum requirements for numeric representation and memory storage. Second, we implement the proposed dot-product architecture using the minimal floating-point and logarithmic representation as design parameters. Finally, we evaluate the overall performance, the inference accuracy, the resource utilization, and the power dissipation.



**FIGURE 17.**  $\log_2$ -histogram of each synaptic weight matrix showing the percentage of matrix elements with given integer exponent.

### 1) Parameters for numeric representation of synaptic weight matrix

We obtain information for the numerical representation of the synaptic weight matrices from their  $\log_2$ -histograms presented in **Fig. 17**. These histograms show the distribution of synaptic weight values in each matrix. We observe that the minimum integer exponent value is  $-13$ . Hence, applying **Eq. (3)** and **Eq. (4)** to the given SbS network, we obtain  $E_{\min} = -13$  and  $N_E = 4$ , respectively. Therefore, 4-bits are required for the absolute binary representation of the exponents.

For quality configurability, the mantissa bit-width is a knob parameter that is tuned by the designer. This procedure leverages the builtin error-tolerance of neural networks and performs a trade-off between resource utilization and QoR. In the following subsection, we present a case study with 1-bit mantissa corresponding to the custom floating-point approximation.

### 2) Design exploration for dot-product with hybrid custom floating-point approximation

For this design exploration, we use a custom floating-point representation composed of 4-bit exponent and 1-bit man-

tissa. This format is used for the synaptic weight vector on the proposed dot-product architecture. Each *Conv* PU instantiates an on-chip stationary weight matrix for 52,000 entries of 5-bit. The available memory size is large enough to store  $W \in \mathbb{R}^{5 \times 5 \times 2 \times 32}$  and  $W \in \mathbb{R}^{5 \times 5 \times 32 \times 64}$  for *H1\_CONV* and *H3\_CONV*, respectively. The same dot-product architecture is implemented in the processing unit of the fully connected layer (*FC*). However, due to lack of BRAM resources, this PU can not instantiate on-chip stationary synaptic weight matrix. Instead, *FC* receives the  $\vec{W}(s_t)$  (weight vectors) during operation as well as  $\vec{h}_\mu$  and  $S_t$ . The hardware mapping and the computation schedule of this implementation are displayed in **Tab. 7** and **Fig. 18**.

As shown in the computation schedule in **Tab. 7** and **Fig. 18**, this implementation achieves a maximum hardware PU latency of  $1.30ms$  according to **Eq. (10)**, and a CPU latency of  $1.67ms$ . Therefore, applying **Eq. (11)**, we obtain a latency of  $1.67ms$  per spike cycle as shown in **Fig. 18**. In this case, the cyclic bottleneck is in the performance of the CPU.

This configuration achieves an accuracy of 98.97% correct classification on the 10,000 image test set with 1000 spikes. This indicates an accuracy degradation of 0.33%. For output quality monitoring, the noise tolerance plot in **Fig. 19** reveals accuracy degradation for noise higher than 50% on the input images, and convergence of inference with 400 spikes. Thus, the particular SbS network implementation under approximate processing effects demonstrates a minimal impact on the overall accuracy. This proves an inherent error resilience, and hence, remaining approximation budget.

The post-implementation resource utilization and power dissipation are shown in **Tab. 6**.

**TABLE 6.** Resource utilization and power dissipation of processing units with hybrid custom floating-point approximation.

PU	LUT	FF	DSP	BRAM 18K	Power (mW)
Conv	3,139	4,850	19	25	82
FC	3,265	5,188	8	9	66

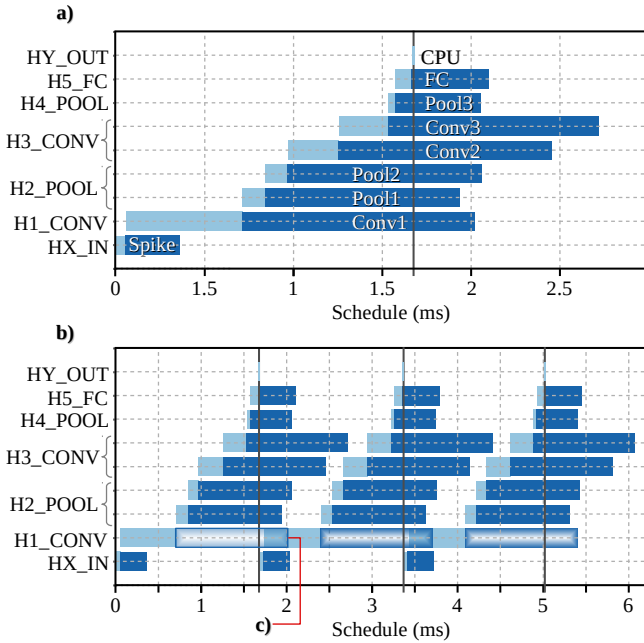
### 3) Design exploration for dot-product with hybrid logarithmic approximation

As the most efficient setup and yet the worst-case quality configuration, we use a 4-bit integer exponent for logarithmic representation of the synaptic weight matrix. Each *Conv* processing unit implements the proposed dot-product architecture including an on-chip stationary weight matrix for 52,000 entries of 4-bit integer each one to store  $W \in \mathbb{N}^{5 \times 5 \times 2 \times 32}$  and  $W \in \mathbb{N}^{5 \times 5 \times 32 \times 64}$  for *H1\_CONV* and *H3\_CONV*, respectively. The same dot-product architecture is implemented in the *FC* processing unit without stationary synaptic weight matrix. The hardware mapping and the computation schedule of this implementation are displayed in **Tab. 8** and **Fig. 20**.

As shown in the computation schedule in **Tab. 8** and **Fig. 20**, this implementation achieves a maximum hardware PU latency of  $1.27ms$  according to **Eq. (10)**, and a CPU

**TABLE 7.** Performance of hardware processing units with hybrid custom floating-point approximation.

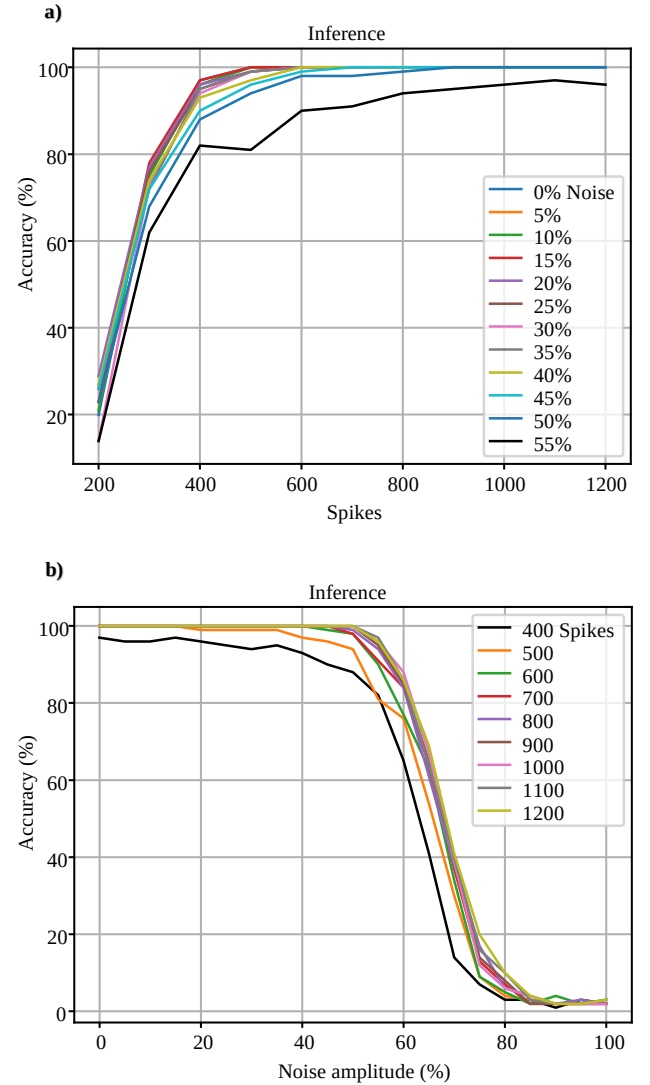
Hardware mapping		Computation schedule (ms)			
Layer	PU	$t_s$	$t_{CPU}$	$t_{PU}$	$t_f$
HX_IN	Spike	0	0.055	0.307	0.362
H1_CONV	Conv1	0.057	0.654	1.309	2.020
H2_POOL	Pool1	0.713	0.131	1.098	1.942
H3_CONV	Conv2	0.845	0.125	1.098	2.068
H4_POOL	Pool2	0.972	0.285	1.199	2.456
H5_FC	Conv3	1.258	0.279	1.184	2.721
H4_POOL	Pool3	1.538	0.037	0.484	2.059
H5_FC	FC	1.577	0.091	0.438	2.106
HY_OUT	CPU	1.669	0.004	0	1.673

**FIGURE 18.** Performance on processing units with hybrid custom floating-point approximation, (a) exhibits computation schedule, (b) presents cyclic computation schedule, and (c) shows the performance of *Conv2* from a previous computation cycle during the preprocessing of *H1\_CONV* on the current computation cycle without bottleneck.

latency of  $1.67ms$ . Therefore, applying Eq. (11), we obtain a latency of  $1.67ms$  per spike cycle as shown in Fig. 20. In this case, the cyclic bottleneck is in the CPU performance.

This quality configuration achieves an accuracy of 98.84% correct classification on the 10,000 image test set with 1000 spikes. This indicates an accuracy degradation of 0.46%. For output quality monitoring, the noise tolerance plot in Fig. 21 reveals accuracy degradation having 40% noise on the input images, and convergence of inference with 600 spikes. The particular SbS network implementation under approximate processing demonstrates a minor impact on the overall accuracy. This exhibits remaining budget for further approximate processing approaches.

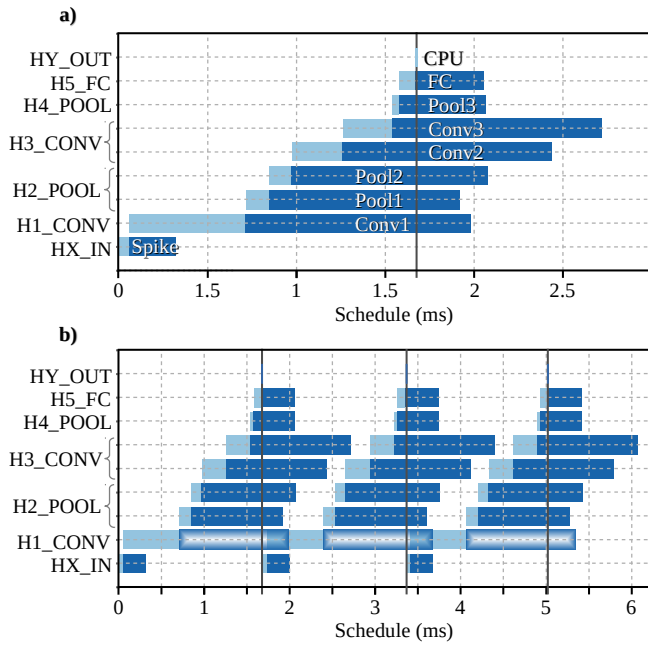
The post-implementation resource utilization and power dissipation are shown in Tab. 9.

**FIGURE 19.** Noise tolerance on hardware PU with custom floating-point approximation, (a) exhibits accuracy degradation applying 50% of noise amplitude, and (b) illustrates convergence of inference with 400 spikes.**TABLE 8.** Performance of hardware processing units with hybrid logarithmic approximation.

Hardware mapping		Computation schedule (ms)			
Layer	PU	$t_s$	$t_{CPU}$	$t_{PU}$	$t_f$
HX_IN	Spike	0	0.055	0.264	0.319
H1_CONV	Conv1	0.057	0.655	1.271	1.983
H2_POOL	Pool1	0.714	0.130	1.074	1.918
H3_CONV	Conv2	0.845	0.126	1.106	2.077
H4_POOL	Pool2	0.973	0.285	1.179	2.437
H5_FC	Conv3	1.258	0.278	1.176	2.712
H4_POOL	Pool3	1.538	0.037	0.488	2.063
H5_FC	FC	1.577	0.091	0.388	2.056
HY_OUT	CPU	1.669	0.004	0	1.673

### C. RESULTS AND DISCUSSION

As a reference, the SbS network simulation on embedded CPU using standard 32-bit floating-point achieves an accuracy of 99.3% with a latency of  $T_{SC} = 34.28ms$ . As a



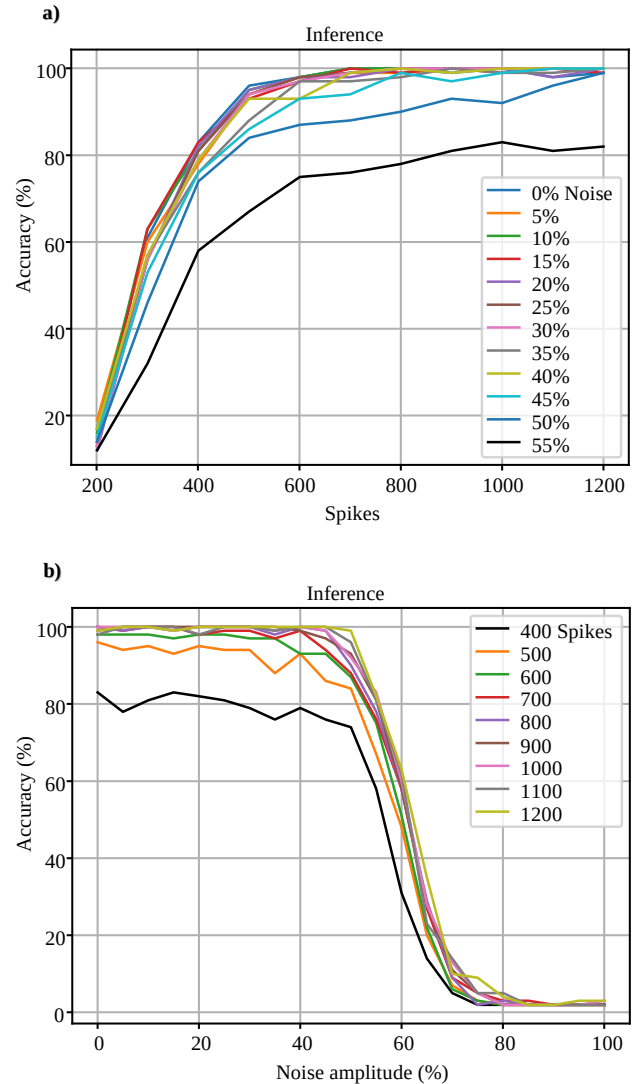
**FIGURE 20.** Performance of processing units with hybrid logarithmic approximation, (a) exhibits computation schedule, and (b) illustrates cyclic computation schedule.

**TABLE 9.** Resource utilization and power dissipation of processing units with hybrid logarithmic approximation.

PU	LUT	FF	DSP	BRAM 18K	Power (mW)
Conv	3,086	4,804	19	21	78
FC	3,046	4,873	8	8	66

second reference point, the network simulation on hardware processing units with standard floating-point achieves an accuracy of 98.98% with a latency  $T_{SC} = 3.18ms$ . As result we get a  $10.7\times$  latency enhancement and an accuracy degradation of 0.32%. The tolerance plot in Fig. 16 reveals accuracy degradation having 50% noise on the input images, and convergence of inference with 400 spikes. In this case, the SbS network deployment with precise computing proves extraordinary inherent error resilience, and hence, this represents a great potential for approximate processing.

As a demonstration of the proposed dot-product architecture, the SbS network simulation on hardware PUs with synaptic representation using 5-bit custom floating-point (4-bit exponent, 1-bit mantissa) and 4-bit logarithmic (4-bit exponent) achieve  $20.5\times$  latency enhancement and accuracy of 98.97% and 98.84%, respectively. This results in an accuracy degradation of 0.33% and 0.46%, respectively. For output quality monitoring, the noise tolerance plot in Fig. 19 and Fig. 21 reveal accuracy degradation when having 50% and 40% noise on the input images, and convergence of inference with 400 and 600 spikes, respectively. Therefore, the design exploration under the proposed approximate computing approach indicates sufficient inherent error resilience for further and more aggressive approximate processing approaches.



**FIGURE 21.** Noise tolerance on hardware PU with hybrid logarithmic approximation, (a) exhibits accuracy degradation applying 40% of noise amplitude, (b) illustrates convergence of inference with 600 spikes.

Regarding resource utilization and power dissipation with the proposed approach, the *Conv* processing units have a 43.24% reduction of BRAM, and a 12.35% of improvement in energy efficiency over the standard floating-point implementation. However, the proposed approach does not reuse the available floating-point operator cores instantiated from other computational sections (see **Tab. 5**). Therefore, the logic required for the dot-product must be implemented, which is reflected as additional utilization of LUT and FF resources. The experimental results of the design exploration are summarized in **Tab. 10**. The platform implementations are summarized in **Tab. 11**, and their power dissipation breakdowns are presented in **Fig. 22**.



TABLE 10. Experimental results.

Dot-product implementation	PU	Post-implementation resource utilization				Power (mW)	Latency		Accuracy (%) <sup>e</sup>	
		LUT	FF	DSP	BRAM 18K		$T_{SC}$ (ms)	Gain <sup>d</sup>	Noise 0%	50%
Standard floating-point computation <sup>a</sup>	Conv	2,765	4,366	19	37	89	3.18	10.7x	98.98	98.63
	FC	2,649	4,189	8	9	66				
Hybrid custom floating-point approx <sup>b</sup>	Conv	3,139	4,850	19	25	82	1.67	20.5x	98.97	98.47
	FC	3,265	5,188	8	9	66				
Hybrid logarithmic approximation <sup>c</sup>	Conv	3,086	4,804	19	21	78	1.67	20.5x	98.84	95.22
	FC	3,046	4,873	8	8	66				

<sup>a</sup> Reference with standard floating-point arithmetic (IEEE 754).<sup>b</sup> Synaptic weight with number representation composed of 4-bit exponent and 1-bit mantissa.<sup>c</sup> Synaptic weight with number representation composed of 4-bit exponent.<sup>d</sup> Acceleration with respect to the computation on embedded CPU (ARM Cortex-A9 at 666 MHz) with latency  $T_{SC} = 34.28ms$ .<sup>e</sup> Accuracy on 10,000 image test set with 1000 spikes.

TABLE 11. Platform implementations.

Platform implementation	Post-implementation resource utilization				Power (W)	Clock (MHz)	Latency		Accuracy (%) <sup>f</sup>
	LUT	FF	DSP	BRAM 18K			$T_{SC}$ (ms)	Gain <sup>e</sup>	
Ref. [14] <sup>a</sup>	42,740	57,118	49	92	2.519	250	4.65	7.4x	99.02
This work (standard floating-point computation) <sup>b</sup>	39,514	56,036	82	180	2.420	200	3.18	10.7x	98.98
This work (hybrid custom floating-point approx) <sup>c</sup>	42,021	58,759	82	156	2.369	200	1.67	20.5x	98.97
This work (hybrid logarithmic approximation) <sup>d</sup>	41,060	57,862	82	148	2.324	200	1.67	20.5x	98.84

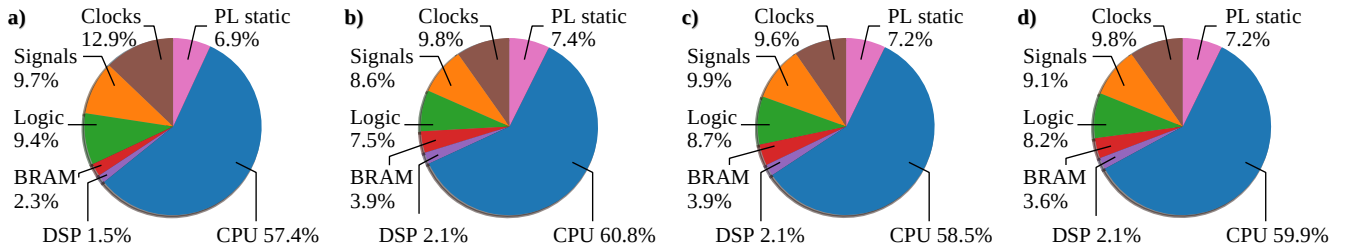
<sup>a</sup> Reference architecture with homogeneous AUs using standard floating-point arithmetic (IEEE 754).<sup>b</sup> Reference architecture with specialized heterogeneous PUs using standard floating-point arithmetic (IEEE 754).<sup>c</sup> Proposed architecture with specialized heterogeneous PUs using synaptic weight with number representation composed of 4-bit exponent and 1-bit mantissa.<sup>d</sup> Proposed architecture with specialized heterogeneous PUs using synaptic weight with number representation composed of 4-bit exponent.<sup>e</sup> Acceleration with respect to the computation on embedded CPU (ARM Cortex-A9 at 666 MHz) with latency  $T_{SC} = 34.28ms$ .<sup>f</sup> Accuracy on 10,000 image test set with 1000 spikes.

FIGURE 22. Power dissipation breakdown of platform implementations. (a) Ref. [14] architecture with homogeneous AUs using standard floating-point arithmetic (IEEE 754), (b) reference architecture with specialized heterogeneous PUs using standard floating-point arithmetic (IEEE 754), (c) proposed architecture with hybrid custom floating-point approximation, and (d) proposed architecture with hybrid logarithmic approximation.

## VI. CONCLUSIONS

In this work, we accelerate SbS neural networks with a dot-product functional unit based on approximate computing that combines the advantages of custom floating-point and logarithmic representations. This approach reduces computational latency, memory footprint, and power dissipation while preserving classification accuracy. For output quality monitoring, we applied noise tolerance plots as an intuitive visual measure to provide insights into the accuracy degradation of SbS networks under different approximate processing effects. This plot reveals inherent error resilience, hence, the possibilities for approximate processing.

We demonstrate our approach using a design exploration flow on a Xilinx Zynq-7020 with a deployment of SbS network for the MNIST classification task. This implementation achieves up to  $20.5\times$  latency enhancement,  $8\times$  weight memory footprint reduction, and 12.35% of energy efficiency

improvement over the standard floating-point hardware implementation, and incurs in less than 0.5% of accuracy degradation. Furthermore, with a noise amplitude of 50% added on top of the input images, the SbS network presents an accuracy degradation of less than 5%. As output quality monitor, the resulting noise tolerance plots demonstrate a sufficient QoR for minimal impact on the overall accuracy of the neural network under the effects of the proposed approximation technique. These results suggest available room for further and more aggressive approximate processing approaches.

In summary, based on the relaxed need for fully accurate or deterministic computation of SbS neural networks, approximate computing techniques allow substantial enhancement in processing efficiency with moderated accuracy degradation.

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## SUPPLEMENTARY MATERIAL

### A. SBS ALGORITHM

The SbS network inference is described in **Algorithm 2**, while spike production and layer update are described in **Algorithm 3** and **Algorithm 4**, respectively.

---

#### Algorithm 2: SbS network inference.

---

**input:** Layers of the network as  $H^l$ , where  $l$  is the layer index.  
**input:**  $N_L$  as the number of layers.  
**input:**  $N_X^l, N_Y^l$  as the size of layers.  
**input:**  $N_{Spk}$  as the number of spikes for inference (iterations).  
**output:**  $H^l$ .

```

1: for  $t = 0$  to  $N_{Spk} - 1$  do
2:   Initialization of  $H^l(i_X, i_Y, :)$  :
3:   if  $t == 0$  then
4:     for  $l = 0$  to  $N_L - 1$  do
5:       for  $i_X = 0, i_Y = 0$  to  $N_X^l - 1, N_Y^l - 1$  do
6:         for  $i_H = 0$  to  $N_H^l - 1$  do
7:            $H^l(i_X, i_Y, i_H) = 1/N_H^l$ 
8:         end for
9:       end for
10:    end for
11:   Production of spikes :
12:   for  $l = 0$  to  $N_L - 1$  do
13:     if  $l == 0$  then
14:       Draw spikes from input // (Algorithm 3)
15:     else
16:       Draw spikes from  $H^l$  // (Algorithm 3)
17:     end if
18:   end for
19:   Update layers :
20:   for  $l = 0$  to  $N_L - 1$  do
21:     Update  $H^l$  // (Algorithm 4)
22:   end for
23: end for

```

---

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#### Algorithm 3: Spike production.

---

**input:** Layer as  $H_t \in \mathbb{R}^{N_X \times N_Y \times N_H}$ , where  $N_X$  is the layer width,  $N_Y$  is the layer height,  $N_H$  is the length of  $\vec{h}$  (IP vector).  
**output:** Output spikes as  $S_t^{out} \in \mathbb{N}^{N_X \times N_Y}$

```

1: for  $i_X = 0, i_Y = 0$  to  $N_X - 1, N_Y - 1$  do
2:   Generate spike :
3:    $th = MT19937PseudoRandom() / (2^{32} - 1)$ 
4:    $acu = 0$ 
5:   for  $i_H = 0$  to  $N_H - 1$  do
6:      $acu = acu + H_t(i_X, i_Y, i_H)$ 
7:     if  $th \leq acu$  or  $i_H == N_H - 1$  then
8:        $S_t^{out}(i_X, i_Y) = i_H$ 
9:     end if
10:  end for
11: end for

```

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**Algorithm 4:** SbS layer update.

---

**input:** Layer as  $H \in \mathbb{R}^{N_X \times N_Y \times N_H}$ , where  
 $N_X$  is the layer width,  
 $N_Y$  is the layer height  
 $N_H$  is the length of  $\vec{h}$  (IP vector).  
**input:** Synaptic matrix as  $W \in \mathbb{R}^{K_X \times K_Y \times M_H \times N_H}$ , where  
 $K_X \times K_Y$  is the size of the convolution/pooling kernel,  
 $M_H$  is the length of  $\vec{h}$  from previous layer,  
 $N_H$  is the length of  $\vec{h}$  from this layer.  
**input:** Input spike matrix from previous layer as  
 $S_t^{in} \in \mathbb{N}^{N_{Xin} \times N_{Yin}}$ , where  
 $N_{Xin}$  is the width of the previous layer,  
 $N_{Yin}$  is the height of the previous layer.  
**input:** Strides of X and Y as  $stride_X$  and  $stride_Y$ ,  
respectively.  
**input:** Epsilon as  $\epsilon \in \mathbb{R}$ .  
**output:** Updated layer as  $H^{new} \in \mathbb{R}^{N_X \times N_Y \times N_H}$ .  
Update layer :  
1:  $z_X = 0$  // X and Y index for  $S_t^{in}$   
2:  $z_Y = 0$   
3: **for**  $i_Y = 0$  **to**  $N_Y - 1$  **do**  
4:   **for**  $i_X = 0$  **to**  $N_X - 1$  **do**  
5:      $\vec{h} = H(i_X, i_Y, :)$   
Update IP :  
6:   **for**  $j_X = 0, j_Y = 0$  **to**  $K_X - 1, K_Y - 1$  **do**  
7:      $s_t = S_t^{in}(z_X + j_X, z_Y + j_Y)$   
8:      $\vec{w} = W(j_X, j_Y, s_t, :)$   
9:      $\vec{p} = 0$   
Dot-product :  
10:      $r = 0$   
11:     **for**  $j_H = 0$  **to**  $N_H - 1$  **do**  
12:        $\vec{p}(j_H) = \vec{h}(j_H) \vec{w}(j_H)$   
13:        $r = r + \vec{p}(j_H)$   
14:     **end for**  
15:     **if**  $r \neq 0$  **then**  
Update IP vector :  
16:       **for**  $i_H = 0$  **to**  $N_H - 1$  **do**  
17:          $h^{new}(i_H) = \frac{1}{1+\epsilon} \left( h(i_H) + \epsilon \frac{\vec{p}(i_H)}{r} \right)$   
18:       **end for**  
Set the new H vector for the layer :  
19:        $H^{new}(i_X, i_Y, :) = \vec{h}^{new}$   
20:     **end if**  
21:   **end for**  
22:    $z_X = z_X + stride_X$   
23: **end for**  
24:    $z_Y = z_Y + stride_Y$   
25: **end for**

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# Accelerating Spike-by-Spike Neural Networks on FPGA with Hybrid Custom Floating-Point and Logarithmic Dot-Product Approximation

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**ABSTRACT** Spiking neural networks (SNNs) represent a promising alternative to conventional neural networks. In particular, the so called Spike-by-Spike (SbS) neural networks provide an exceptional noise robustness and a reduced complexity. However, deep SbS networks require a memory footprint and a computational cost unsuitable for embedded applications. To address this problem, this work exploits the intrinsic error resilience of neural networks to improve performance and to reduce the hardware complexity. More precisely, we design a dot-product hardware unit based on approximate computing with configurable quality using hybrid custom floating-point and logarithmic number representation. This approach reduces computational latency, memory footprint, and power dissipation while preserving inference accuracy. To demonstrate our approach, we address a design exploration flow using high-level synthesis and a Xilinx SoC-FPGA. The proposed design reduces  $20.5\times$  computational latency and  $8\times$  weight memory footprint, with less than 0.5% of accuracy degradation on a handwritten digit recognition task.

**INDEX TERMS** Artificial intelligence, spiking neural networks, approximate computing, logarithmic, parameterisable floating-point, optimization, hardware accelerator, embedded systems, FPGA

## I. INTRODUCTION

THE exponential improvement in computing performance and the availability of large amounts of data are boosting the use of artificial intelligence (AI) applications in our daily lives. Among the various algorithms developed over the years, neural networks (NNs) have demonstrated remarkable performance in a variety of image, video, audio, and text analytics tasks [1], [2]. Historically, artificial neural networks (ANNs) can be classified into three different generations [3]: the first one is represented by the classical McCulloch and Pitts neuron model using discrete binary values as outputs; the second one is represented by more complex architectures as multi-layer perceptrons (MLPs) and convolutional neural networks (CNNs) using continuous activation functions; while the third generation is represented by spiking neural

networks using spikes as means for information exchange between groups of neurons. Although the AI research is currently dominated by deep neural networks (DNNs) from the second generation, the SNNs belonging to the third generation are receiving considerable attention [3]–[6].

SNNs offer advantageous robustness and the potential to achieve a power efficiency closer to that of the human brain. SNNs operate reliably using stochastic elements that are inherently non-reliable mechanisms [7]. This provides superior resistance against adversary attacks [5], [8]. Beside robustness, SNNs have further advantages like the possibility of a more efficient asynchronous parallelization and higher energy efficiency than DNNs. For example, Loihi [9], a SNN developed by Intel, can solve LASSO optimization problems with an over three orders of magnitude better

energy-delay product than conventional approaches. These advantages are motivating large research programs by major companies (e.g., Intel [9] and IBM [10]) as well as pan-european projects in the domain of spiking networks [4].

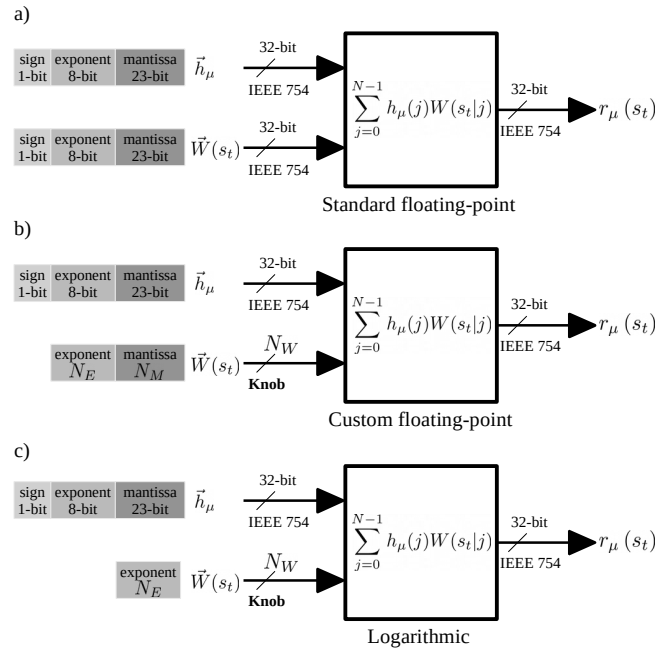
SNNs emulate the real behavior of neurons in different levels of detail. The more detailed the biological part is emulated, the greater the computational complexity [11], [12]. Most of today's SNNs use a very detailed model (e.g., Leaky Integrate-and-Fire (LIF)).

Alternatively, the Spike-by-Spike (SbS) neural network is a remarkable model for its reduced complexity, which is on the less realistic side of the SNN scale of biological realism [5], [13]. Consequently, the hardware complexity of SbS network implementations is greatly reduced [14], [15]. In spite of this, SbS still uses stochastic spikes as a means of transmitting information between populations of neurons and thus retains the advantageous robustness of SNNs.

The conceptual model in SbS (see Sec. III-A for a short review) differs fundamentally from conventional ANNs since (a) the building blocks of the network are inference populations (IP) which are an optimized generative representation with non-negative values, (b) time progresses from one spike to the next, preserving the property of stochastically firing neurons, and (c) a network has only a small number of parameters, which is an advantageous noise-robust stochastic version of Non-Negative Matrix Factorization (NNMF). The SbS network is placed between non-spiking NN and stochastically spiking NN, which offers advantages from both structures [13]. On one hand, the SbS model incorporates the inherent robustness of SNNs, which provide the possibility of more efficient asynchronous parallelization and superior resilience against disturbances based on the synaptic stochasticity; on the other hand, the SbS model incorporates the regular flow of information from CNNs, which are expressed on explicit vector operations.

As computational demanding algorithms, ANNs and SNNs in particular, must be addressed by specialized hardware architectures. A significant research effort has been performed in SNN accelerators, see e.g. Ref. [4], [9], [10], [16]–[18]. However, hardware accelerators that focus on SbS have only been partially investigated so far [14], [15]. Enhanced SbS accelerators will have a double impact. From an engineering point of view, they will contribute to the deployment of robust neural networks in small embedded systems [14]; from a scientific point of view, they will facilitate fundamental research for neuroscience [5], [19], [20].

A central point that can be optimized in current SbS accelerators is the use of approximation techniques. Most SbS models use floating-point numerical representation, which imposes high complexity of the required circuits for the floating-point operations. Model quantization has the potential to improve computational performance; however, this solution is often accompanied by quantization-aware training methods that, in some cases, are problematic or even inaccessible, particularly in deep SNN algorithms [21]. As



**FIGURE 1.** Dot-product hardware module with (a) standard floating-point (IEEE 754) arithmetic, (b) hybrid custom floating-point approximation, and (c) hybrid logarithmic approximation.

an alternative, based on the relaxed need for fully precise or deterministic computation of neural networks, approximate computing techniques allow substantial enhancement in processing efficiency with moderated accuracy degradation. Some research papers have shown the feasibility of applying approximate computing to the inference stage of neural networks [22]–[25]. Such techniques usually demonstrated small inference accuracy degradation, but significant enhancement in computational performance, resource utilization, and energy consumption. Hence, by taking advantage of the intrinsic error-tolerance of neural networks, approximate computing is positioned as a promising approach for inference on resource-limited devices.

In this paper, we accelerate SbS neural networks with a dot-product hardware design based on approximate computing with hybrid custom floating-point and logarithmic number representation. This hardware unit has a quality configurable scheme based on the bit truncation of the synaptic-weight vector. Fig. 1 illustrates the dot-product hardware module with standard floating-point (IEEE 754) arithmetic, and our approach with hybrid custom floating-point as well as logarithmic approximation. As a design parameter, the mantissa bit-width of the weight vector provides a tunable knob to trade-off between efficiency and quality of result (QoR) [26], [27]. Since the lower-order bits have smaller significance than the higher-order bits, truncating them may have only a minor impact on QoR [28], [29]. Further on, we can remove completely the mantissa bits in order to use only the exponent of a floating-point representation. Therefore, the most efficient setup and yet the worst-case quality configuration becomes a logarithmic representation,



which consequently leads to significant architectural-level optimizations using only adders and shifters for dot-product approximation in hardware. Moreover, since approximations and noise have qualitatively the same effect [30], we apply noise tolerance plots as an intuitive visual measure to provide insights into the quality degradation of SbS networks under approximate processing effects.

Our main contributions are as follows:

- We develop a hardware component for dot-product approximation. To perform the sum of pairwise products of two vectors, this hardware module has the following three design features: (1) the pairwise product is approximated by adding integer exponents and multiplying truncated mantissas, and the sum of products is done by accumulating denormalized integer products with barrel shifters, which increases computational throughput; (2) the synaptic weight vector uses either reduced custom floating-point or logarithmic representation, which reduces memory footprint; and (3) the neuron vector uses either standard or custom floating-point representation, which preserves QoR and overall inference accuracy.
- We address a design exploration with the proposed dot-product approximation using synaptic weight vectors with custom floating-point and logarithmic representation as shown in Fig. 1. We evaluate inference latency, accuracy degradation, resource utilization and power dissipation. Experimental results demonstrate  $20.5\times$  latency enhancement versus embedded CPU (ARM Cortex-A9 at 666MHz), and less than 0.5% of accuracy degradation on a handwritten digit recognition task (MNIST). This machine learning task simply provides a proof of concept to demonstrate the feasibility of our approximation technique for SbS neural network accelerators.
- We propose a noise tolerance plot as quality monitor, which serves as an intuitive visual model to provide insights into the accuracy degradation of SbS networks under approximate processing effects.
- Our proposed design for dot-product approximation is adaptable as a building block for other error resilient applications (e.g., image/video processing).

The rest of the paper is organized as follows. Section II covers the related work; Section III introduces the background to SbS networks; Section IV describes the system design and the approximate dot-product hardware module; Section V presents the experimental results thorough a design exploration flow; Section VI concludes the paper.

To promote the research on SbS networks, our design exploration framework is made available to the public as an open-source project at <http://www.ids.uni-bremen.de/sbs-framework.html>

## II. RELATED WORK

### A. APPROXIMATE COMPUTING IN NEURAL NETWORKS

Approximate computing has been used in a wide range of applications to increase the computational efficiency in

hardware [27]. For neural network applications, two main approximation strategies are used, namely network compression and classical approximate computing [17].

#### 1) Network compression

Researchers focusing on embedded applications started lowering the precision of weights and activation maps to shrink the memory footprint of the large number of parameters representing ANNs, a method known as network compression or quantization. This practice takes advantage of the intrinsic error-tolerance of neural networks, as well as their ability to compensate for approximation while training. In this way, reduced bit precision causes a small accuracy loss [31]–[34].

In hardware development, weight quantization (WQ) has shown up to  $2\times$  improvement in energy consumption with an accuracy degradation of less than 1% [35], [36]. Some advanced quantization methods yield to binary neural networks (BNNs) allowing the use of XNORs instead of the conventional costly multiply-accumulate circuits (MACs) [34]. In [37], Sun et al. report an accuracy of 98.43% on handwritten digit classification (MNIST) with a simple BNN. Hence, quantization is a powerful tool for improving the energy efficiency and memory requirements of ANN accelerators, with limited accuracy degradation.

In addition to quantization, network pruning reduces the model size by removing structural portions of the parameters and its associated computations [38], [39]. This method has been identified as an effective technique to improve the efficiency of DNN for applications with limited computational budget [40]–[42].

These methods can be used for SNNs as well. In [43], Rathi et al. report up to  $3.1\times$  improvement in energy consumption with an accuracy loss of around 3%. Weight quantization allows the designer to realize a trade-off between the accuracy of the SNN application and efficiency of resources. Approximate computing can also be applied at the neuron level, where irrelevant units are deactivated to reduce the computation cost of the SNNs [44]. This computation skipping can be applied randomly on synapses, training ANNs with stochastic synapses improves generalization, resulting in a better accuracy [45], [46]. Such methods are compatible with SNNs and have been tested both during training [47], [48] and operation [49], and even to define the connectivity between layers [50], [51]. Implementations of spiking neuromorphic systems in FPGA [52] and hardware [53] demonstrated that synaptic stochasticity allows to increase the final accuracy of the networks while reducing memory footprint.

Quantization is therefore a powerful technique to improve energy efficiency and memory requirements of ANN and SNN accelerators, with small accuracy degradation. However, this approach requires quantization-aware training methods that, in some cases, are problematic or even inaccessible, particularly in emerging deep SNN algorithms [21].

## 2) Classical approximate computing

This approach consists of designing processing elements that approximate their computation by employing modified algorithmic logic units [27]. In [54], Kim et al. have shown SNNs using carry skip adders achieving  $2.4\times$  latency enhancement and 43% more energy efficiency, with an accuracy degradation of 0.97% on a handwritten digit classification task (MNIST). Therefore, approximate computing provides important enhancement in energy efficiency and processing speed.

However, as the complexity of the dataset increases, as well as the depth of the network topology, such as ResNet [55] on ImageNet [56], the accuracy degradation becomes more important and may not be negligible anymore [34], especially for critical applications such as autonomous driving. Therefore, it is not certain that network compression techniques and approximate computing are suitable for all applications.

## B. SPIKE-BY-SPIKE NEURAL NETWORKS ACCELERATORS

Recently, Rotermund et al. demonstrated the feasibility of a neuromorphic SbS IP on a Xilinx Virtex 6 FPGA [15]. It provides a massively parallel architecture, optimized to reduce memory access and suitable for ASIC implementations. Nonetheless, this design is considerably resource-demanding if implemented as a full SbS network in today's embedded technology.

In Ref. [14], we presented a cross-platform accelerator framework for design exploration and testing of fully functional SbS network models in embedded systems. As a hardware/software (HW/SW) co-design solution, this framework offers a comprehensive high level embedded software API that allows the construction of scalable sequential SbS networks with configurable hardware acceleration. However, this design works entirely with standard floating-point arithmetic (IEEE 754). This represents a large memory footprint and inadequate computational cost for error resilient applications on resource-limited devices. In this article, we will use this design exploration framework to investigate approximate computing for efficient deployment of deep SbS networks on resource-limited devices.

## III. BACKGROUND

### A. SPIKE-BY-SPIKE NEURAL NETWORKS

Technically, SbS is a spiking neural network approach based on a generative probabilistic model. It iteratively finds an estimate of its input probability distribution  $p(s)$  (i.e. the probability of input node  $s$  to stochastically send a spike) by its latent variables via  $r(s) = \sum_i h(i)W(s|i)$ , where  $\bar{h}$  is an inference population composed of a group of neurons that compete with each other. An inference population sees only the spikes  $s_t$  (i.e. the index identifying the input neuron  $s$  which generated that spike at time  $t$ ) produced by its input neurons, not the underlying input probability distribution  $p(s)$  itself. By counting the spikes arriving at a group of SbS

neurons,  $p(s)$  is estimated by  $\hat{p}(s) = 1/T \sum_t \delta_{s,s_t}$  after  $T$  spikes have been observed in total. The goal is to generate an internal representation  $r(s)$  from the string of incoming spikes  $s_t$  such that the negative logarithm of the likelihood  $L = C - \sum_\mu \sum_s \hat{p}_\mu(s) \log(r_\mu(s))$  is minimized.  $C$  is a constant which is independent of the internal representation  $r_\mu(s)$  and  $\mu$  denotes one input pattern from an ensemble of input patterns. Applying a multiplicative gradient descent method on  $L$ , an algorithm for iteratively updating  $h_\mu(i)$  with every observed input spike  $s_t$  could be derived [5]

$$h_\mu^{new}(i) = \frac{1}{1+\epsilon} \left( h_\mu(i) + \epsilon \frac{h_\mu(i)W(s_t|i)}{\sum_j h_\mu(j)W(s_t|j)} \right) \quad (1)$$

where  $\epsilon$  is a parameter that also controls the strength of sparseness of the distribution of latent variables  $h_\mu(i)$ . Furthermore,  $L$  can also be used to derive online and batch learning rules for optimizing the weights  $W(s|i)$ . The interested reader is referred to [5] for a more detailed exposition.

From a practical point of view, SbS provides a mechanism to obtain a sparse representation of input patterns. Given a set of training samples  $\{x_\eta\}$ , it learns weights ( $W$ ), that allow to express the input patterns as a linear sparse non-negative combination of features. During inference, it provides a mechanism for expressing each test input  $x_\mu$  as  $x_\mu \approx W h_\mu$  where all entries are non-negative.

The inference procedure consists in generating indices  $s_t$  distributed according to a categorical distribution of the input pattern  $s_t \sim \text{Categorical}(x_\mu(0), x_\mu(1), \dots, x_\mu(N-1))$ . Starting with a random  $h$  and executing iteratively Eq. (1) the SbS algorithm finds  $h_\mu$ . The fundamental concept of SbS can be extended from vector to matrix inputs. In this case, the linear operation  $W h_\mu$  can be replaced by a convolution to obtain a convolutional SbS layer. A detailed description of the SbS algorithm is presented in the supplementary material of this paper.

### B. BASIC NETWORK OVERVIEW

SbS network models can be constructed in sequential layered structures [13]. Each layer consists of many inference populations or IPs (represented by  $\bar{h}$ ), while the communication between them is organized by a low bandwidth signal – the spikes.

The SbS layer update is summarized in Algorithm 1. This is an iterative algorithm, where we denote the number of spikes ( $N_{Spk}$ ) as the number of iterations. As a generative model, each iteration updates the internal representation ( $H$ ) based on the input spikes ( $S_t^{in}$ ). A basic SbS network architecture for handwritten digit classification (MNIST) is shown in Fig. 2 and Tab. 1. Each IP is an independent computational entity, this allows to design specialized hardware architectures that can be massively parallelized (see Fig. 3).

### C. COMPUTATIONAL COST

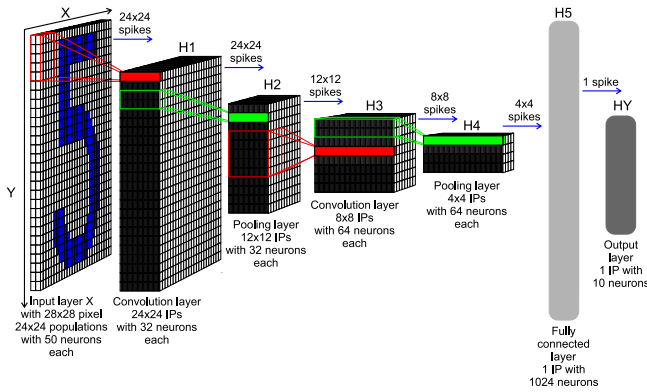
The number of multiply-accumulate (MAC) operations required for inference of an SbS layer is defined

**Algorithm 1: SbS layer update.**

```

1: for  $t \leftarrow 0$  to  $N_{Spk} - 1$  do
2:   for  $x \leftarrow 0, y \leftarrow 0$  to  $N_X - 1, N_Y - 1$  do
3:      $S_t^{out}(x, y) \sim \text{Categorical}(H(x, y, :))$ 
4:     for  $\Delta_X \leftarrow 0, \Delta_Y \leftarrow 0$  to  $K_X - 1, K_Y - 1$  do
5:        $spk \leftarrow S_t^{in}(x + \Delta_X, y + \Delta_Y)$ 
6:       for  $i \leftarrow 0$  to  $N_H - 1$  do
7:          $\Delta h(i) \leftarrow H(x, y, i) \cdot W(\Delta_X, \Delta_Y, spk, i)$ 
8:          $r \leftarrow r + \Delta h(i)$ 
9:       end for
10:      for  $i \leftarrow 0$  to  $N_H - 1$  do
11:         $H^{new}(x, y, i) \leftarrow \frac{1}{1+\epsilon} (H(x, y, i) + \frac{\epsilon}{n} \Delta h(i))$ 
12:      end for
13:    end for
14:  end for
15: end for

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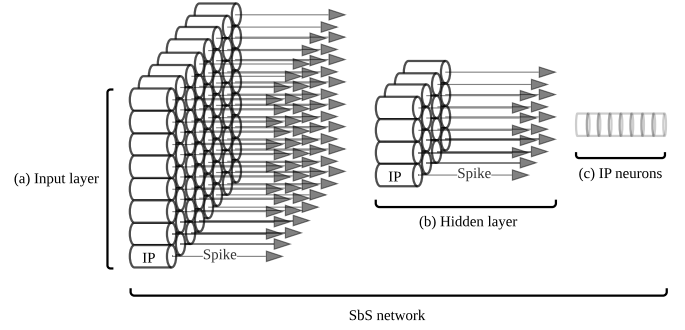
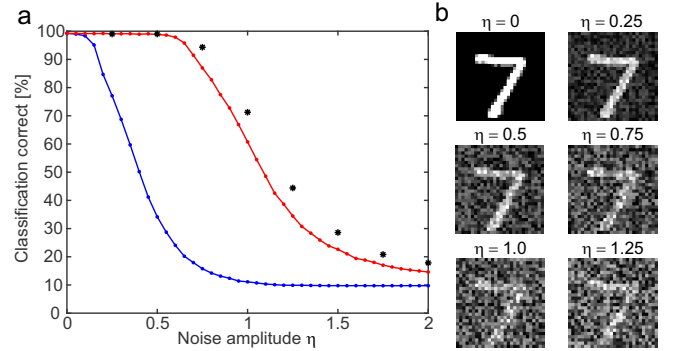
**FIGURE 2.** SbS network architecture for handwritten digit classification task.**TABLE 1.** SbS network architecture for handwritten digit classification task.

Layer ( $H^l$ )	Layer size			Kernel size	
	$N_X$	$N_Y$	$N_H$	$K_X$	$K_Y$
Input ( $H_X$ )	28	28	2	-	-
Convolution ( $H_1$ )	24	24	32	5	5
Pooling ( $H_2$ )	12	12	32	2	2
Convolution ( $H_3$ )	8	8	64	5	5
Pooling ( $H_4$ )	4	4	64	2	2
Fully connected ( $H_5$ )	1	1	1024	4	4
Output ( $H_Y$ )	1	1	10	1	1

by  $NOPS_{MAC} = N_{Spk} N_X N_Y K_X K_Y (3N_H + 2)$ , where  $N_{Spk}$  is the number of spikes (iterations),  $N_X N_Y$  is the size of the layer,  $K_X K_Y$  is the size of the kernel for convolution/pooling, and  $N_H$  is the length of  $\vec{h}$ . The computational cost of SbS network models is higher compared to equivalent CNN models and lower compared to regular SNN models (e.g., LIF) [11].

**D. ERROR RESILIENCE**

To illustrate the error resilience of SbS networks, we present a classification performance under positive additive uniformly distributed noise as external disturbance. Fig. 4

**FIGURE 3.** SbS IPs as independent computational entities, (a) illustrates an input layer with a massive amount of IPs operating as independent computational entities, (b) shows a hidden layer with an arbitrary amount of IPs as independent computational entities, (c) exhibits a set of neurons grouped in an IP.**FIGURE 4.** (a) Performance classification of SbS NN versus equivalent CNN, and (b) example of the first pattern in the MNIST test data set with different amounts of positive additive uniformly distributed noise.

presents a comparison of the classification performance of an SbS network and a standard CNN, with the same amount of neurons per layer as well as the same layer structure. We trained both neural networks for handwritten digit classification on MNIST dataset [57] (see [13] for details). The figure shows the correctness for the MNIST test set with its 10000 patterns in dependency of the noise level for positive additive uniformly distributed noise. The blue curve shows the performance for the CNN, while the red curve shows the performance for the SbS network with 1200 spikes (iterations). Beginning with a noise level of 0.1, the respective performances are different with a p - level of at least  $10^{-6}$  (tested with the Fisher exact test). Increasing the number of spikes per SbS population to 6000 (performance values shown as black stars), shows that more spikes can improve the performance under noise even more.

**IV. SYSTEM DESIGN**

In this section, we revise the system design of Ref. [14] where we presented a scalable hardware architecture composed of generic homogeneous accelerator units (AUs). This design works entirely with standard floating-point arithmetic (IEEE 754), which represents an unnecessary overhead for error resilient applications. Furthermore, this architecture

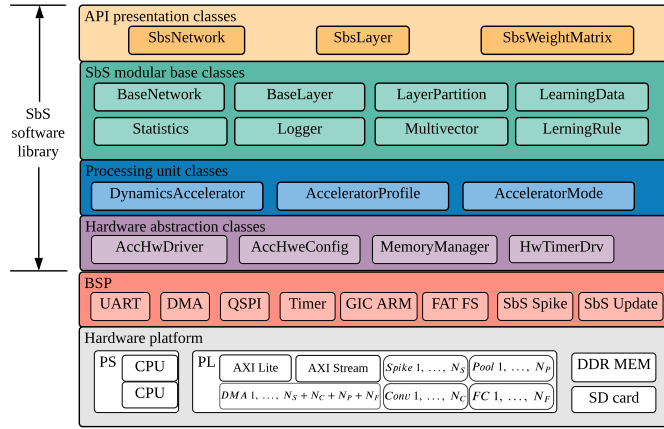


FIGURE 5. System-level overview of the embedded software architecture.

does not implement stationary synaptic weight matrices in the hardware AUs, resulting in heavy data movement, longer computational latency, and higher power consumption.

In this publication, we present an enhanced hardware architecture composed of specialized heterogeneous processing units (PUs) with hybrid custom floating-point and logarithmic dot-product approximation. This approach represents an advantageous design for error resilient applications in resource-constrained devices due to the reduced computational costs and memory footprint. Furthermore, the proposed approach allows the implementation of stationary synaptic weight matrices. These novelties result in an improved overall system design.

Regarding the software architecture, this is structured as a layered object-oriented application framework written in the C programming language. This offers a comprehensive high level embedded software application programming interface (API) that allows the construction of scalable sequential SbS networks with configurable hardware acceleration. Conceptually this design is modular, reusable, and extensible. The overall structure is depicted in Fig. 5.

#### A. HARDWARE ARCHITECTURE

As a hardware/software co-design, the system architecture is an embedded CPU+FPGA-based platform, where the acceleration of SbS network computation is based on asynchronous<sup>1</sup> execution in parallel heterogeneous processing units: *Spike* (input layer), *Conv* (convolution), *Pool* (pooling), and *FC* (fully connected). Fig. 6 illustrates the system hardware architecture as a scalable structure. For hyperparameter configuration, each PU uses AXI-Lite interface. For data transfer, each PU uses AXI-Stream interfaces via Direct Memory Access (DMA) allowing data movement with high transfer rate. Each PU asserts an interrupt flag once the job or transaction is complete. This interrupt event is handled by the embedded CPU to collect results and start a new transaction.

<sup>1</sup>The system is synchronous at the circuit level, but the execution is asynchronous in terms of jobs.

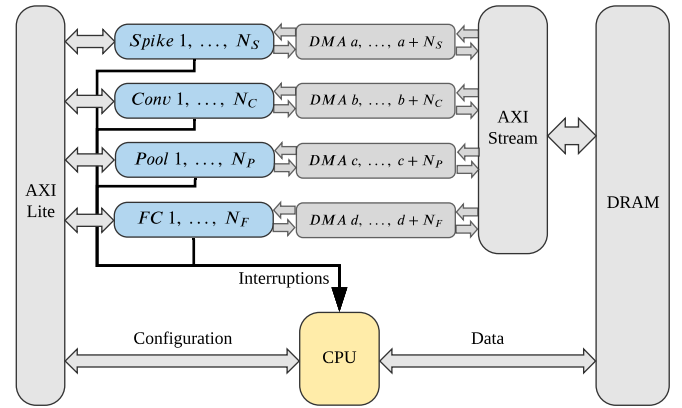


FIGURE 6. System-level hardware architecture with scalable number of heterogeneous PUs: *Spike*, *Conv*, *Pool*, and *FC*

The hardware architecture can resize its resource utilization by changing the number of PUs instances prior to the hardware synthesis, this provides scalability with a good trade-off between area and throughput. The dedicated PUs for *Conv* and *FC* implement the proposed dot-product approximation as a system component. The PUs are written in C using Vivado HLS (High-Level Synthesis) tool. In this publication, we illustrate the integration of the approximate dot-product component on the *Conv* processing unit.

#### B. CONV PROCESSING UNIT

This hardware module computes the IP dynamics defined by Eq. (1) and offers two modes of operation: *configuration* and *computation*.

##### 1) Configuration mode

In this mode of operation, the PU receives and stores in on-chip memory (BRAM) the hyperparameters to compute the IP dynamics:  $\epsilon$  as the epsilon,  $N$  as the length of  $\vec{h}_\mu \in \mathbb{R}^N$ ,  $K \in \mathbb{N}$  as the size of the convolution kernel, and  $H \in \mathbb{N}$  as the number of IPs to process per transaction.  $H$  is the number of IPs forming a layer or a partition.

Additionally, the processing unit also stores in on-chip memory (BRAM) the synaptic weight matrix using a number representation with a reduced memory footprint. Fundamentally, the synaptic weight matrix is defined by  $W \in \mathbb{R}^{K \times K \times M \times N}$  with  $0 \leq W(s_t|j) \leq 1$  and  $\sum_{s_t=0}^{M-1} W(s_t|j) = 1$  [13]. Hence,  $W$  employs only positive normalized real numbers. Therefore,  $W$  is deployed using a reduced floating-point or logarithmic representation as follows:

- Custom floating-point representation. In this case,  $W$  is deployed with a reduced floating-point representation using the user defined bit-width for the exponent and for the mantissa. For example, 4-bit exponent, 1-bit mantissa; as a result: 5-bit custom floating-point. The methodology to determine the required bit-width is described in Section IV-C.



- Logarithmic representation. In this case, the synaptic weight matrix is  $W \in \mathbb{N}^{K \times K \times M \times N}$  with positive natural numbers. Since  $0 \leq W(s_t|j) \leq 1$  and  $\sum_{s_t=0}^{M-1} W(s_t|j) = 1$ ,  $W$  has only negative values in the logarithmic domain. Hence, the sign bit is omitted, and the values are represented in its positive form. Therefore,  $W$  is deployed with a representation using the necessary bit-width for the exponent according to the given application. For example, 4-bit exponent. The methodology to determine the required bit-width is described in Section IV-C.

In order to deploy different SbS network models, the *Conv* processing units can be configured with different synaptic weight matrices and hyperparameters as required through the embedded software.

## 2) Computation mode

In this mode of operation, the PU executes a transaction to process a group of IPs using the previously given hyperparameters and synaptic weight matrix. This process operates in six stages as shown in Fig. 7. In the first two stages, the PU receives  $h_\mu \in \mathbb{R}^N$ , then the PU calculates the emitted spike, and stores it in  $S^{new} \in \mathbb{N}^H$  (output spike vector). From the third to the fifth stage, the PU receives  $S_t \in \mathbb{N}^{K \times K}$  (input spike matrix), then it computes the update dynamics, and then it dispatches  $\vec{h}_\mu^{new} \in \mathbb{R}^N$  (updated IP). This process repeats for  $H$  number of loops (for each IP of the layer or partition). Finally, the  $S^{new}$  is dispatched.

The computation of the update dynamics (see Fig. 7(d)) operates in two modular stages: *dot-product* and *neuron update*. First, the *dot-product* module calculates the sum of pairwise products of  $\vec{h}_\mu$  and  $\vec{W}(s_t)$ , each pairwise product is stored as intermediate results. Subsequently, the *neuron update* module calculates Eq. (1) reusing previous results and parameters.

The calculation of the dot-product of Eq. (1) represents a considerable computational cost using standard floating-point in non-quantized network models. Fortunately, the pair product of  $h_\mu(j)$  and  $W(s_t|j)$  was defined by us as an approximable factor in the dot-product of Eq. (1). In the following section, we focus on an optimized dot-product hardware design based on approximate computing.

## C. DOT-PRODUCT HARDWARE MODULE

This dot-product hardware module is part of an application-specific architecture optimized to approximate the dot-product of arbitrary length, see Eq. (2). For quality configurability, we parameterized the mantissa bit-width of  $\vec{W}(s_t)$ , which provides a tunable trade-off between resource utilization and QoR. Since the lower-order bits have smaller significance than the higher-order bits, removing them may have only a minor impact on QoR. We designate this as hybrid custom floating-point approximation (see Fig. 8(a)).

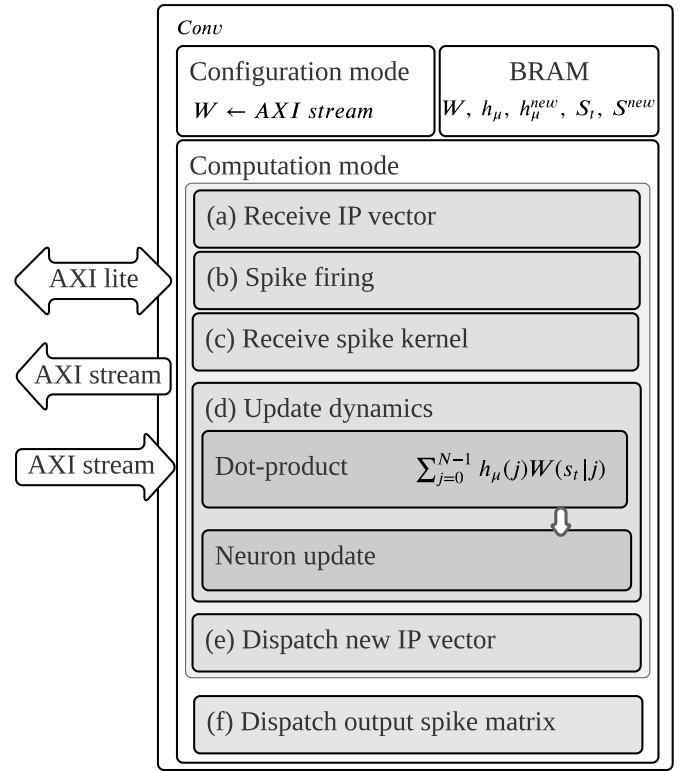


FIGURE 7. The *Conv* processing unit and its six stages: (a) receive IP vector, (b) spike firing, (c) receive spike kernel, (d) update dynamics, (e) dispatch new IP vector, (f) dispatch output spike matrix.

$$r_\mu(s_t) = \sum_{j=0}^{N-1} h_\mu(j)W(s_t|j) \quad (2)$$

Further on, we remove the mantissa bits completely in order to use only the exponent of a floating-point representation. Hence, the worst-case quality and yet the most efficient configuration becomes a logarithmic representation. Consequently, this structure leads to advantageous architectural optimizations using only adders and barrel shifters for dot-product approximation in hardware. We designate this as hybrid logarithmic approximation (see Fig. 8(b)).

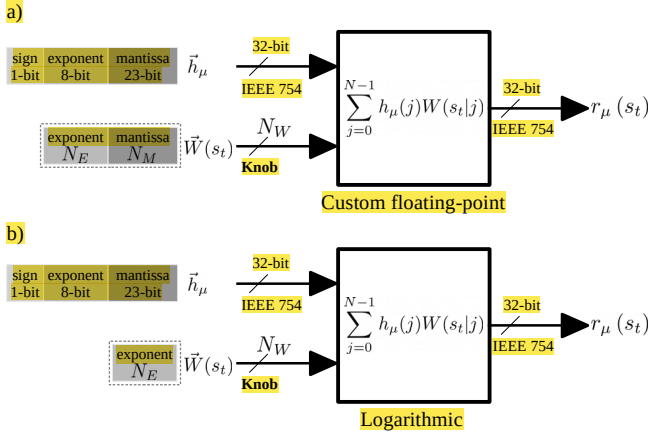
In order to determine the required bit-width for the number representation, we use Eq. (3), Eq. (4), and Eq. (5).

$$E_{\min} = \log_2(\min_{\forall i}(W(i))) \quad (3)$$

$$N_E = \lceil \log_2(|E_{\min}|) \rceil \quad (4)$$

$$N_W = N_E + N_M \quad (5)$$

The Eq. (3) obtains the exponent of the minimum entry value in the synaptic weight matrix. Since  $0 \leq W(s_t|j) \leq 1$  and  $\sum_{s_t=0}^{M-1} W(s_t|j) = 1$ ,  $W$  has only negative values in the



**FIGURE 8.** Dot-product hardware module with (a) hybrid custom floating-point approximation, and (b) hybrid logarithmic approximation.

logarithmic domain; hence, by searching for the smallest value, we obtain the biggest negative exponent ( $E_{\min}$ ). Then, the Eq. (4) obtains the necessary bit-width to represent the exponent ( $N_E$ ). Finally, we obtain the total bit-width by incorporating both exponent and mantissa bit-widths in Eq. (5).  $N_M$  denotes the mantissa bit-width, this is a knob parameter that is tuned by the designer to trade-off between resource utilization and QoR. The bit-width concept is illustrated in Fig. 8.

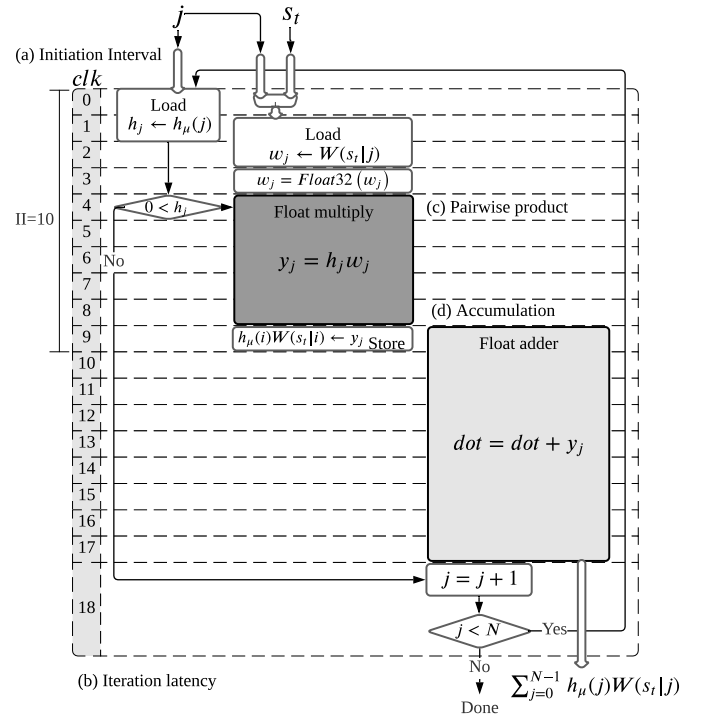
In this section, we will present three pipelined hardware modules with standard floating-point (IEEE 754) computation, hybrid custom floating-point approximation, and hybrid logarithmic approximation.

#### 1) Dot-product with standard floating-point computation

The hardware module to calculate the dot-product with standard floating-point computation is shown in Fig. 9. This diagram presents the hardware blocks and their clock cycle schedule. This module loads both  $h_\mu(j)$  and  $W(s|j)$  from BRAM, then the PU executes the pairwise product (Fig. 9(c)) and accumulation (Fig. 9(d)). The intermediate results of  $h_\mu(j)W(s_t|j)$  are stored in BRAM for reuse in the neuron update. The latency in clock cycles of this hardware module is defined by Eq. (6), where  $N$  is the dot-product length. This latency equation is obtained from the general pipelined hardware latency formula:  $L = (N - 1)II + IL$ , where  $II$  is the initiation interval (Fig. 9(a)), and  $IL$  is the iteration latency (Fig. 9(b)). Both  $II$  and  $IL$  are obtained from the high-level synthesis analysis. The equation for the latency with standard 32-bit floating-point is:

$$L_{f32} = 10N + 9 \quad (6)$$

In this design, the high-level synthesis tool infers computational blocks with considerable latency cost for standard floating-point. In the case of floating-point multiplication (Fig. 9(c)), the synthesis infers a hardware block with a latency cost of 5 clock cycles. Theoretically, this block would handle exponents addition, mantissas multiplication,



**FIGURE 9.** Dot-product hardware module with standard floating-point (IEEE 754) computation, (a) exhibits the initiation interval of 10 clock cycles, (b) presents the iteration latency of 9 clock cycles, (c) shows the pairwise product block in dark-gray, and (d) illustrates the accumulation block in light-gray.

and mantissa correction if needed. Moreover, in the case of floating-point addition (Fig. 9(d)), the synthesis infers a hardware block with a latency cost of 9 clock cycles. Seemingly, this block would handle mantissas alignment, addition, and correction if needed. Therefore, the use of standard floating-point in high-level synthesis results in high computational cost, which represents unnecessary overhead in error tolerant applications.

#### 2) Dot-product with hybrid custom floating-point and logarithmic approximation

The hardware module to calculate dot-product with hybrid custom floating-point approximation is shown in Fig. 10. In this design,  $h_\mu(j)$  uses standard 32-bit floating-point number representation, and  $W(s|j)$  uses a positive reduced custom floating-point number representation, where the mantissa bit width is the quality configurability knob. This parameter is tuned by the designer to trade-off between QoR and resource utilization, thus, energy consumption.

As the most efficient setup and yet the worst-case quality configuration, by completely truncating the mantissa of  $W(s|j)$  leads to a slightly different hardware architecture using only adders and shifters, which computes the dot-product with hybrid logarithmic approximation. This is shown in Fig. 11.

Additionally, the exponent bit-width of  $W(s|j)$  is a design parameter for efficient resource utilization and it is defined based on the application or deployment needs.

The hybrid custom floating-point and logarithmic approximation designs work in three phases: *Computation*, *Threshold-test*, and *Result normalization*.

- Phase I, *Computation*:

This phase approximates the magnitude of the dot-product in a denormalized representation. This is calculated in two iterative steps over each vector element: *pairwise product* and *accumulation*, where *pairwise product* is executed either in hybrid custom floating-point or hybrid logarithmic approximation described below.

- Pairwise product.

- Hybrid custom floating-point approximation. As shown in Fig. 10(c) in dark-gray, the pairwise product is approximated by adding exponents and multiplying mantissas of both  $W(s|i)$  and  $h_\mu(i)$ . If the mantissa multiplication results in an overflow, then it is corrected by increasing the exponent and shifting the resulting mantissa by one position to the right. Then we get  $h_\mu(j)W(s_t|j)$  as an intermediate result which is stored for future reuse in the neuron update calculation. In this design the pairwise product has a latency of 5 clock cycles.

- Hybrid logarithmic approximation. As shown in Fig. 11(c) in dark-gray, the pairwise product is approximated by adding  $W(s|i)$  to the exponent of  $h_\mu(i)$ , since  $W(s|j)$  values are represented in the logarithmic domain and  $h_\mu(j)$  in standard floating-point. In this design the pairwise product has a latency of one clock cycle.

- Accumulation. As shown in both Fig. 10(d) and Fig. 11(d) in light-gray, first, it is obtained the denormalized representation of  $h_\mu(j)W(s_t|j)$  by shifting its mantissa using its exponent as shifting parameter (barrel shifter). Then, this denormalized representation is accumulated to obtain the approximated magnitude of the dot-product.

The process of pairwise product and accumulation iterates over each element of the vectors. The computation latency is given by Eq. (7) for hybrid custom floating-point, and Eq. (8) for hybrid logarithmic, where  $N$  is the length of the vectors. Both pipelined hardware modules have the same throughput, since both have two clock cycles as initiation interval.

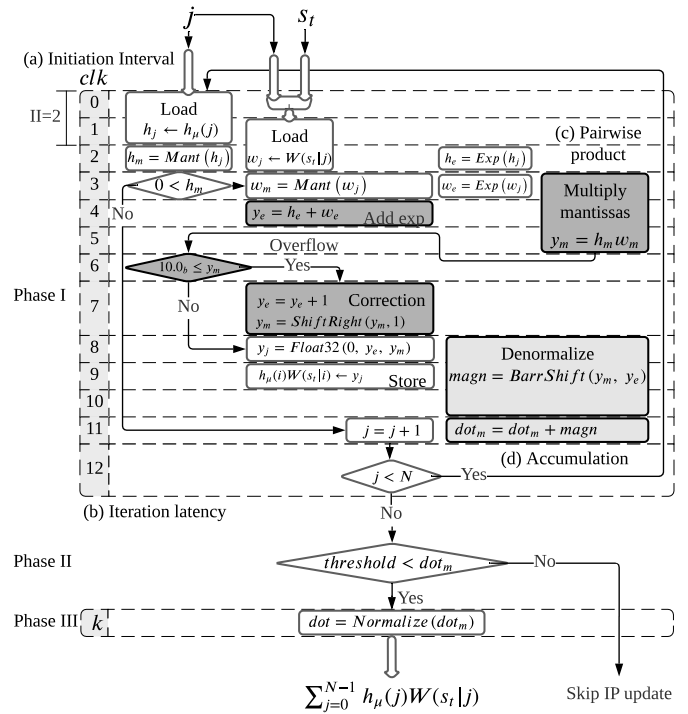
$$L_{custom} = 2N + 11 \quad (7)$$

$$L_{log} = 2N + 7 \quad (8)$$

- Phase II, *Threshold-test*:

The accumulated denormalized magnitude is tested to be above of a predefined threshold, it must be above zero, since the dot-product is the denominator in Eq. (1).

If passing the threshold, then the next phase is executed.



**FIGURE 10.** Dot-product hardware module with hybrid custom floating-point approximation, (a) exhibits the initiation interval of 2 clock cycles, (b) presents the iteration latency of 13 clock cycles, (c) shows the pairwise product blocks in dark-gray, and (d) illustrates the accumulation blocks in light-gray.

Otherwise the rest of update dynamics is skipped. The threshold-test takes one clock cycle.

- Phase III, *Result-normalization*:

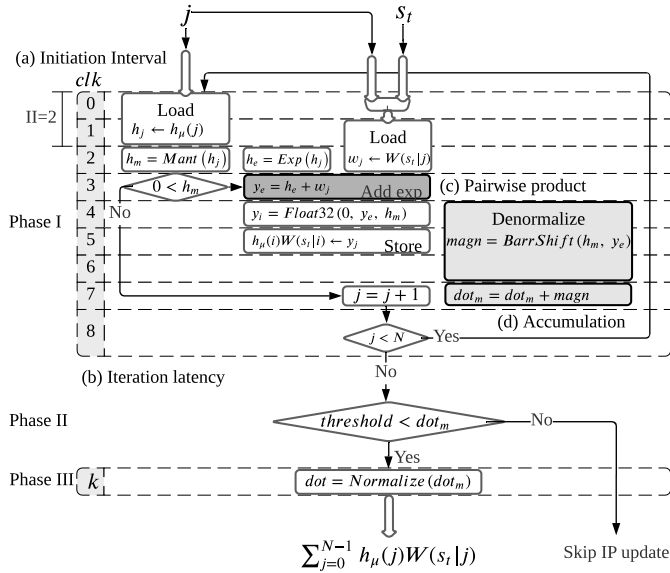
In this phase, the dot-product is normalized to obtain the exponent and mantissa in order to convert it to standard floating-point for later use in the neuron update. The normalization is obtained by shifting the approximated dot-product magnitude in a loop until it is in the form of a normalized mantissa where the iteration count represents the exponent of the dot-product. Each iteration takes one clock cycle.

The total latency of the hardware module with hybrid custom floating-point and hybrid logarithmic approximation is the accumulated latency of the three phases.

The proposed architectures with approximation approach exceeds the performance of the design with standard floating-point. This performance enhancement is achieved by decomposing the floating-point computation into an advantageous handling of exponent and mantissa using intermediate accumulation in a denormalized representation and only one final normalization.

## V. EXPERIMENTAL RESULTS

The proposed architecture is demonstrated on a Xilinx Zynq-7020. This device integrates a dual ARM Cortex-A9 based processing system (PS) and programmable logic (PL) equivalent to Xilinx Artix-7 (FPGA) in a single chip [58]. The Zynq-7020 architecture conveniently maps the custom logic



**FIGURE 11.** Dot-product hardware module with hybrid logarithmic approximation, (a) exhibits the initiation interval of 2 clock cycles, (b) presents the iteration latency of 9 clock cycles, (c) shows the pairwise product block in dark-gray, and (d) illustrates the accumulation blocks in light-gray.

and software in the PL and PS respectively as an embedded system.

In this platform, we implement the proposed hardware architecture to deploy the SbS network structure shown in Fig. 2 for handwritten digit classification task using MNIST data set. The SbS model is trained in Matlab without any quantization method, using standard floating-point. The resulting synaptic weight matrices are deployed on the embedded system. There, the SbS network is built as a sequential model using the API from the SbS embedded software framework [14]. This API allows to configure the computational workload of the neural network, which can be distributed among the hardware processing units and the embedded CPU.

For the evaluation of our approach, we address a design exploration by reviewing the computational latency, inference accuracy, resource utilization, and power dissipation. First, we benchmark the performance of SbS network simulation on the embedded CPU, and then repeat the measurements on hardware processing units with standard floating-point computation. Afterwards, we evaluate our dot-product architecture, addressing a design exploration with hybrid custom floating-point approximation, as well as the hybrid logarithmic approximation. Finally, we present a discussion of the presented results.

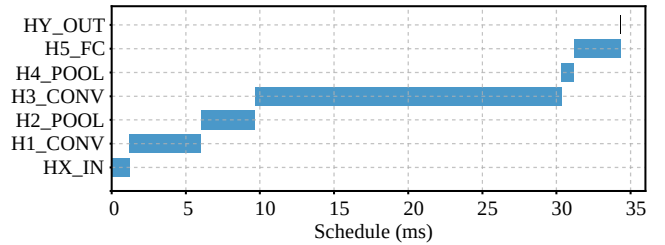
## A. PERFORMANCE BENCHMARK

### 1) Benchmark on embedded CPU

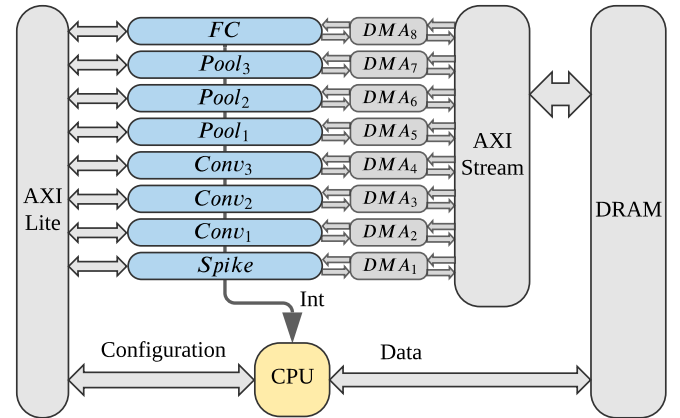
We examine the performance of the CPU for SbS network simulation with no hardware coprocessing. In this case, the embedded software builds the SbS network as a sequential model mapping the entire computation to the CPU (ARM

**TABLE 2.** Computation on embedded CPU.

Layer	Latency (ms)
HX_IN	1.184
H1_CONV	4.865
H2_POOL	3.656
H3_CONV	20.643
H4_POOL	0.828
H5_FC	3.099
HY_OUT	0.004
TOTAL	34.279



**FIGURE 12.** Computation on embedded CPU.



**FIGURE 13.** System overview of the top-level architecture with 8 processing units.

Cortex-A9) at 666 MHz and a power dissipation of 1.658W.

The SbS network computation on the CPU achieves a latency of 34.28ms per spike with an accuracy of 99.3% correct classification on the 10,000 image test set with 1000 spikes. The latency and schedule of the SbS network computation are displayed in Tab. 2 and Fig. 12 respectively.

### 2) Benchmark on processing units with standard floating-point computation

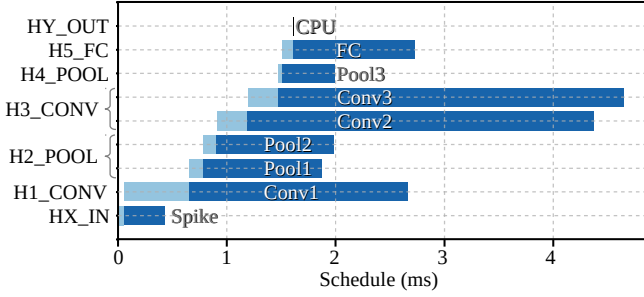
To benchmark the computation on hardware PUs with standard floating-point, we implement the system architecture shown in Fig. 13. In this case, the embedded software builds the SbS network as a sequential model mapping the network computation to the hardware processing units at 200 MHz as clock frequency.

The layers of the neural network with the most neurons are partitioned for asynchronous parallel processing. Since H2\_POOL and H3\_CONV are the layers with the most neu-



**TABLE 3.** Performance of processing units with standard floating-point (IEEE 754) computation.

Hardware mapping		Computation schedule (ms)			
Layer	PU	$t_s$	$t_{CPU}$	$t_{PU}$	$t_f$
HX_IN	Spike	0	0.056	0.370	0.426
H1_CONV	Conv1	0.058	0.598	2.002	2.658
H2_POOL	Pool1	0.658	0.126	1.091	1.875
H2_POOL	Pool2	0.785	0.125	1.075	1.985
H3_CONV	Conv2	0.911	0.280	3.183	4.374
H3_CONV	Conv3	1.193	0.279	3.176	4.648
H4_POOL	Pool3	1.473	0.037	0.481	1.991
H5_FC	FC	1.512	0.101	1.118	2.731
HY_OUT	CPU	1.615	0.004	0	1.619

**FIGURE 14.** Performance of processing units with standard floating-point (IEEE 754) computation.

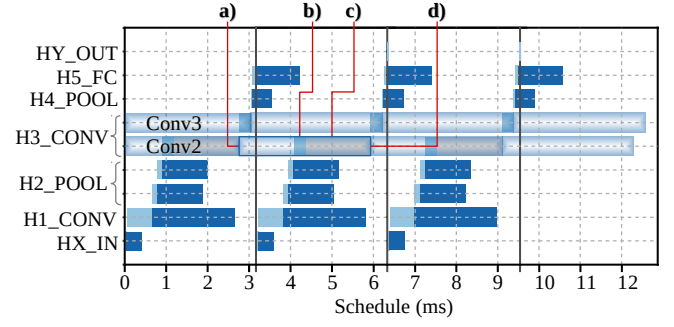
rons, the computational workload is distributed between two PUs for each one of these layers. The output layer *HY\_OUT* is fully processed by the CPU, since it is the layer with fewest neurons. The hardware mapping and the computation schedule of this deployment are displayed in **Tab. 3** and **Fig. 14**.

In the computation schedule, the following terms are defined as follows:  $t_s(n)$  as the start time for the processing of the neural network layer (as a compute node)  $n \in L$  where  $L$  represents the set of layers;  $t_{CPU}(n)$  as the CPU preprocessing time;  $t_{PU}(n)$  as the PU latency; and  $t_f(n)$  as the finish time. For data preparation, the  $t_{CPU}(n)$  is the duration in which the CPU writes a DRAM buffer with  $\vec{h}_\mu$  (vector of neuron latent variables) of the current processing layer and  $S_t$  (input spike matrix) from its preceding layer. This buffer is streamed to the PU via DMA.

The total execution time of the CPU is defined by **Eq. (9)**. In a cyclic spiking inference, the execution time of the network computation is the longest path among the processing units including the CPU. This is denoted as the latency of an spike cycle and it is defined by **Eq. (11)**. The total execution time of the network computation is the last finish time ( $t_f$ ) in the schedule defined by **Eq. (12)**.

$$T_{CPU} = \sum_{n \in L} t_{CPU}(n) \quad (9)$$

$$T_{PU} = \max_{n \in L} (t_{PU}(n)) \quad (10)$$

**FIGURE 15.** Performance bottleneck of cyclic computation on processing units with standard floating-point (IEEE 754) arithmetic, (a) exhibits the starting of  $t_{PU}$  of *Conv2* on a previous computation cycle, (b) presents  $t_{CPU}$  of *Conv2* on the current computation cycle, (c) shows the CPU waiting time (in gray color) for *Conv2* as a busy resource (awaiting for *Conv2* interruption), and (d) illustrates the  $t_f$  from the previous computation cycle, the starting of  $t_{PU}$  on the current computation cycle (*Conv2* interruption on completion, and start current computation cycle).

$$T_{SC} = \begin{cases} T_{PU}, & \text{if } T_{CPU} \leq T_{PU} \\ T_{CPU}, & \text{otherwise} \end{cases} \quad (11)$$

$$T_f = \max_{n \in L} (t_f(n)) \quad (12)$$

Using standard floating-point requires a high computational cost. As the largest layer, the computational workload of *H3\_CONV* is evenly partitioned among two PUs: *Conv2* and *Conv3*. However, in the cyclic schedule, *Conv2* causes the performance bottleneck as shown in **Fig. 15**. In this case, the CPU has to await for *Conv2* to finish the computation of the previous cycle in order to start the current computation cycle. **In contrast, as the smallest layer, the computational workload of *HY\_OUT* is fully processed by the CPU. **Tab. 3** and **Fig. 14** show  $4\mu s$  as the processing latency of *HY\_OUT*. This latency is negligible compared to the overall performance assessment. Accelerating *HY\_OUT* would yield a negligible gain. Moreover, assigning a dedicated hardware PU to *HY\_OUT* would add data transfer and hardware interruption handling overheads, which makes this unprofitable.**

Applying **Eq. (11)**, we obtain a latency of  $3.18ms$  per spike cycle. This deployment achieves an accuracy of 98.98% correct classification on the 10,000 image test set with 1000 spikes.

The post-implementation resource utilization and power dissipation are shown in **Tab. 4**. Each *Conv* PU instantiates an on-chip stationary weight matrix of 52,000 entries, which is sufficient to store  $W \in \mathbb{R}^{5 \times 5 \times 2 \times 32}$  and  $W \in \mathbb{R}^{5 \times 5 \times 32 \times 64}$  for *H1\_CONV* and *H3\_CONV*, respectively. In order to reduce BRAM utilization, we use a custom floating-point representation composed of 4-bit exponent and 4-bit mantissa. Each 8-bit entry is promoted to its standard floating-point representation for the dot-product computation. The methodology to find the appropriate bit-width parameters for custom floating-point representation is presented in Section V-B1.

**TABLE 4.** Resource utilization and power dissipation of processing units with standard floating-point (IEEE 754) computation.

PU	LUT	FF	DSP	BRAM 18K	Power (mW)
Spike	2,640	4,903	2	2	38
Conv	2,765	4,366	19	37	89
Pool	2,273	3,762	5	3	59
FC	2,649	4,189	8	9	66

The implementation of dot-product with standard floating-point arithmetic (IEEE 754) utilizes proprietary multiplier and adder floating-point operator cores. Vivado HLS accomplishes floating-point arithmetic operations by mapping them onto Xilinx LogiCORE IP cores, these floating-point operator cores are instantiated in the resultant RTL [59]. In this case, the implementation of the dot-product with the standard floating-point computation reuses the multiplier and adder cores already instantiated and used in other computation sections of *Conv* and *FC* processing units. The post-implementation resource utilization and power dissipation of the floating-point operator cores are shown in **Tab. 5**.

**TABLE 5.** Resource utilization and power dissipation of multiplier and adder floating-point (IEEE 754) operator cores.

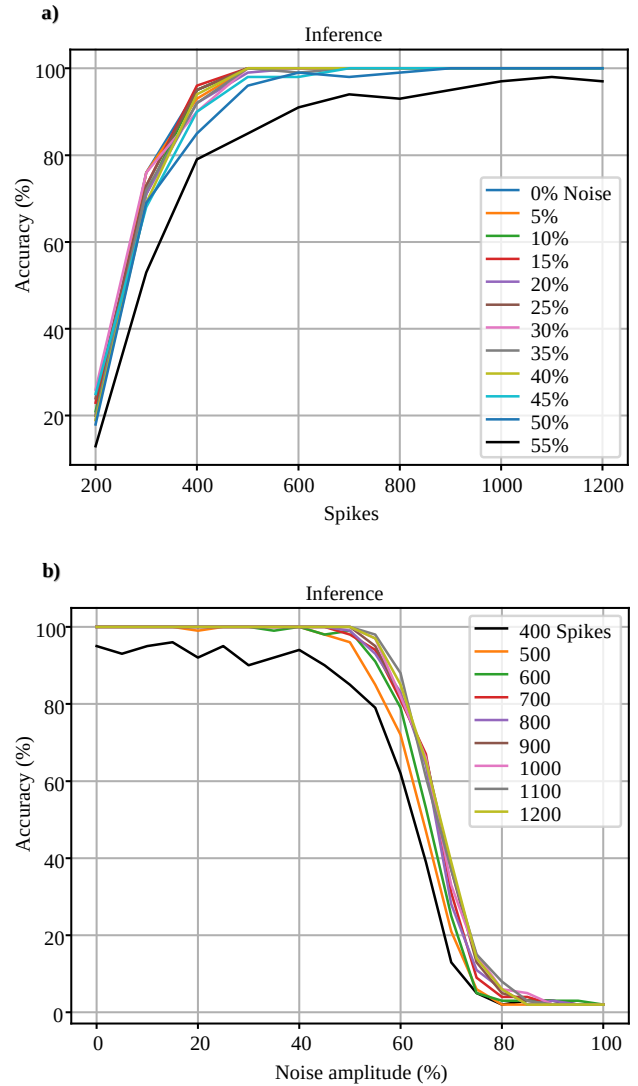
Core operation	DSP	FF	LUT	Latency (clk)	Power (mW)
Multiplier	3	151	325	4	7
Adder	2	324	424	8	6

### 3) Benchmark on noise tolerance plot

The noise tolerance plot serves as an intuitive visual model used to provide insights into accuracy degradation under approximate processing effects. This plot reveals inherent error resilience, and hence, approximation resilience. As an application-specific quality metric, this plot offers an effective method to estimate the overall quality degradation of the SbS network under different approximate processing effects, since both approximations and noise have qualitatively the same effect [30].

In order to experimentally obtain the noise tolerance plot, we measure the inference accuracy of the neural network with increasing number of spikes. Then we repeat the measurements with uniformly distributed noise applied on the input images. We gradually ascend the levels of the noise amplitude, until accuracy degradation is detected. **Fig. 16** demonstrates this method using 100 sample images.

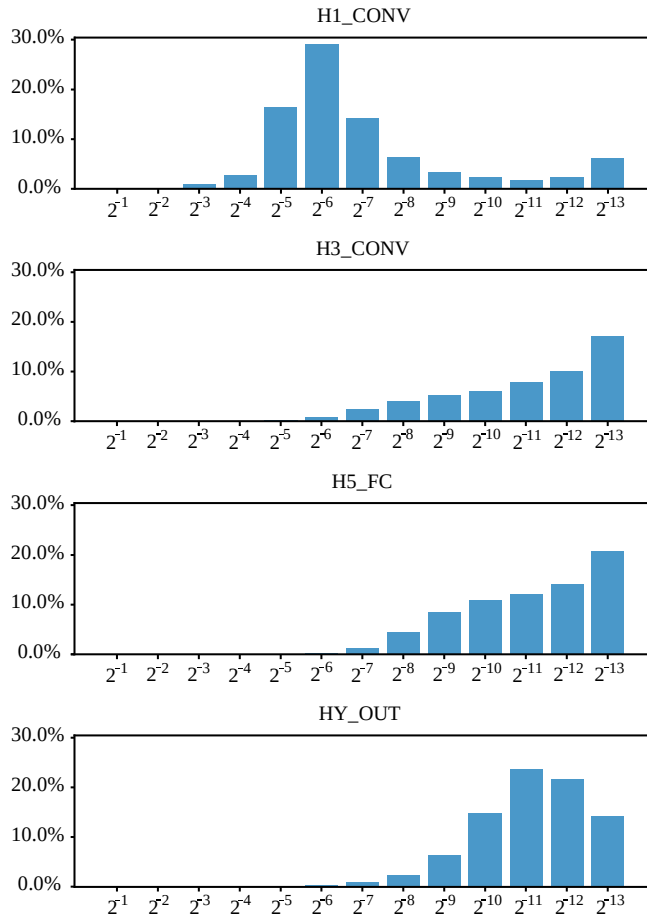
As benchmark, the tolerance plot in **Fig. 16** reveals accuracy degradation having 50% noise and convergence with 400 spikes. In this case, the particular SbS network with precise processing demonstrates a remarkable inherent error resilience, hence, a great opportunity for approximate processing.



**FIGURE 16.** Noise tolerance on hardware PU with standard floating-point (IEEE 754) computation (benchmark/reference), (a) exhibits accuracy degradation applying 50% of noise amplitude, and (b) illustrates convergence of inference with 400 spikes.

## B. DESIGN EXPLORATION WITH HYBRID CUSTOM FLOATING-POINT AND LOGARITHMIC APPROXIMATION

In this section, we address a design exploration to evaluate our approach for SbS neural network simulation using hybrid custom floating-point and logarithmic approximation. First, we examine the synaptic weight matrix of each SbS network layer in order to determine the minimum requirements for numeric representation and memory storage. Second, we implement the proposed dot-product architecture using the minimal floating-point and logarithmic representation as design parameters. Finally, we evaluate the overall performance, the inference accuracy, the resource utilization, and the power dissipation.



**FIGURE 17.**  $\log_2$ -histogram of each synaptic weight matrix showing the percentage of matrix elements with given integer exponent.

### 1) Parameters for numeric representation of synaptic weight matrix

We obtain information for the numerical representation of the synaptic weight matrices from their  $\log_2$ -histograms presented in Fig. 17. These histograms show the distribution of synaptic weight values in each matrix. We observe that the minimum integer exponent value is  $-13$ . Hence, applying Eq. (3) and Eq. (4) to the given SbS network, we obtain  $E_{\min} = -13$  and  $N_E = 4$ , respectively. Therefore, 4-bits are required for the absolute binary representation of the exponents.

For quality configurability, the mantissa bit-width is a knob parameter that is tuned by the designer. This procedure leverages the builtin error-tolerance of neural networks and performs a trade-off between resource utilization and QoR. In the following subsection, we present a case study with 1-bit mantissa corresponding to the custom floating-point approximation.

### 2) Design exploration for dot-product with hybrid custom floating-point approximation

For this design exploration, we use a custom floating-point representation composed of 4-bit exponent and 1-bit man-

tissa. This format is used for the synaptic weight vector on the proposed dot-product architecture. Each *Conv* PU instantiates an on-chip stationary weight matrix for 52,000 entries of 5-bit. The available memory size is large enough to store  $W \in \mathbb{R}^{5 \times 5 \times 2 \times 32}$  and  $W \in \mathbb{R}^{5 \times 5 \times 32 \times 64}$  for *H1\_CONV* and *H3\_CONV*, respectively. The same dot-product architecture is implemented in the processing unit of the fully connected layer (*FC*). However, due to lack of BRAM resources, this PU can not instantiate on-chip stationary synaptic weight matrix. Instead, *FC* receives the  $\vec{W}(s_t)$  (weight vectors) during operation as well as  $\vec{h}_\mu$  and  $S_t$ . The hardware mapping and the computation schedule of this implementation are displayed in Tab. 7 and Fig. 18.

As shown in the computation schedule in Tab. 7 and Fig. 18, this implementation achieves a maximum hardware PU latency of 1.30ms according to Eq. (10), and a CPU latency of 1.67ms. Therefore, applying Eq. (11), we obtain a latency of 1.67ms per spike cycle as shown in Fig. 18. In this case, the cyclic bottleneck is in the performance of the CPU.

This configuration achieves an accuracy of 98.97% correct classification on the 10,000 image test set with 1000 spikes. This indicates an accuracy degradation of 0.33%. For output quality monitoring, the noise tolerance plot in Fig. 19 reveals accuracy degradation for noise higher than 50% on the input images, and convergence of inference with 400 spikes. Thus, the particular SbS network implementation under approximate processing effects demonstrates a minimal impact on the overall accuracy. This proves an inherent error resilience, and hence, remaining approximation budget.

The post-implementation resource utilization and power dissipation are shown in Tab. 6.

**TABLE 6.** Resource utilization and power dissipation of processing units with hybrid custom floating-point approximation.

PU	LUT	FF	DSP	BRAM 18K	Power (mW)
Conv	3,139	4,850	19	25	82
FC	3,265	5,188	8	9	66

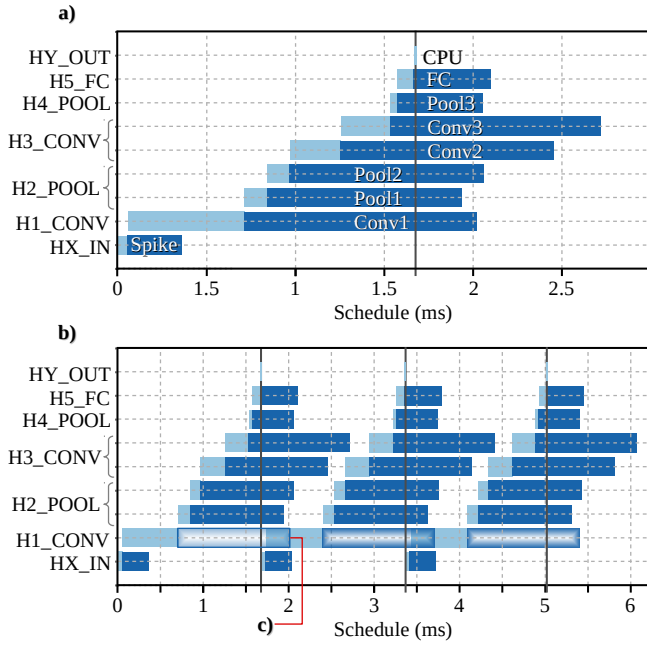
### 3) Design exploration for dot-product with hybrid logarithmic approximation

As the most efficient setup and yet the worst-case quality configuration, we use a 4-bit integer exponent for logarithmic representation of the synaptic weight matrix. Each *Conv* processing unit implements the proposed dot-product architecture including an on-chip stationary weight matrix for 52,000 entries of 4-bit integer each one to store  $W \in \mathbb{N}^{5 \times 5 \times 2 \times 32}$  and  $W \in \mathbb{N}^{5 \times 5 \times 32 \times 64}$  for *H1\_CONV* and *H3\_CONV*, respectively. The same dot-product architecture is implemented in the *FC* processing unit without stationary synaptic weight matrix. The hardware mapping and the computation schedule of this implementation are displayed in Tab. 8 and Fig. 20.

As shown in the computation schedule in Tab. 8 and Fig. 20, this implementation achieves a maximum hardware PU latency of 1.27ms according to Eq. (10), and a CPU

**TABLE 7.** Performance of hardware processing units with hybrid custom floating-point approximation.

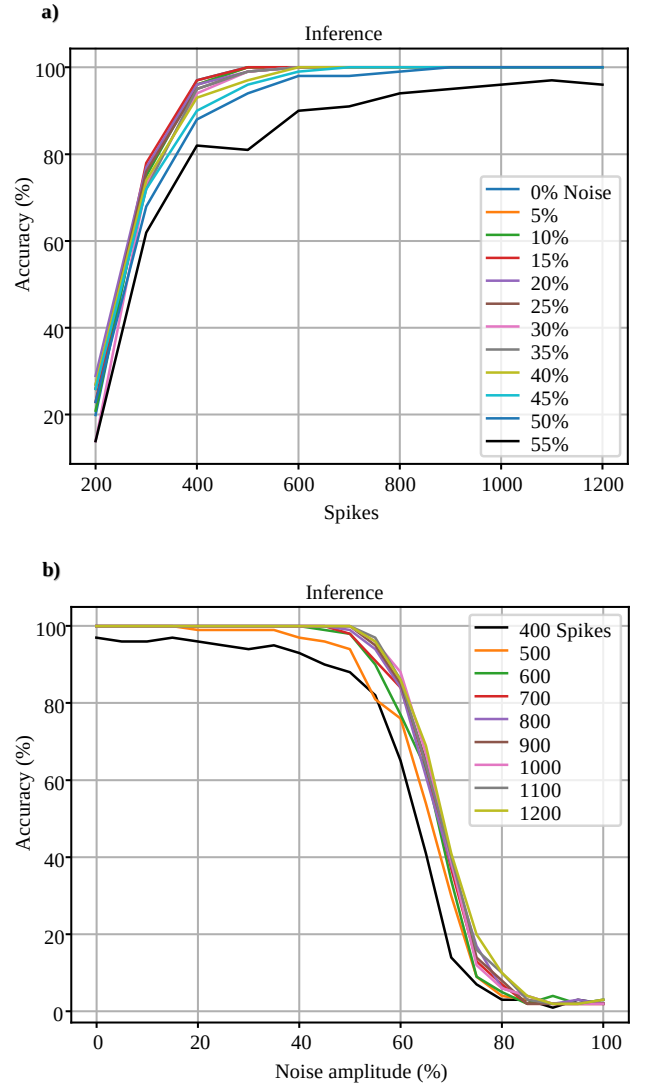
Hardware mapping		Computation schedule (ms)			
Layer	PU	$t_s$	$t_{CPU}$	$t_{PU}$	$t_f$
HX_IN	Spike	0	0.055	0.307	0.362
H1_CONV	Conv1	0.057	0.654	1.309	2.020
H2_POOL	Pool1	0.713	0.131	1.098	1.942
H3_CONV	Conv2	0.845	0.125	1.098	2.068
H4_POOL	Pool2	0.972	0.285	1.199	2.456
H5_FC	Conv3	1.258	0.279	1.184	2.721
H4_POOL	Pool3	1.538	0.037	0.484	2.059
H5_FC	FC	1.577	0.091	0.438	2.106
HY_OUT	CPU	1.669	0.004	0	1.673

**FIGURE 18.** Performance on processing units with hybrid custom floating-point approximation, (a) exhibits computation schedule, (b) presents cyclic computation schedule, and (c) shows the performance of *Conv2* from a previous computation cycle during the preprocessing of *H1\_CONV* on the current computation cycle without bottleneck.

latency of  $1.67ms$ . Therefore, applying Eq. (11), we obtain a latency of  $1.67ms$  per spike cycle as shown in Fig. 20. In this case, the cyclic bottleneck is in the CPU performance.

This quality configuration achieves an accuracy of 98.84% correct classification on the 10,000 image test set with 1000 spikes. This indicates an accuracy degradation of 0.46%. For output quality monitoring, the noise tolerance plot in Fig. 21 reveals accuracy degradation having 40% noise on the input images, and convergence of inference with 600 spikes. The particular SbS network implementation under approximate processing demonstrates a minor impact on the overall accuracy. This exhibits remaining budget for further approximate processing approaches.

The post-implementation resource utilization and power dissipation are shown in Tab. 9.

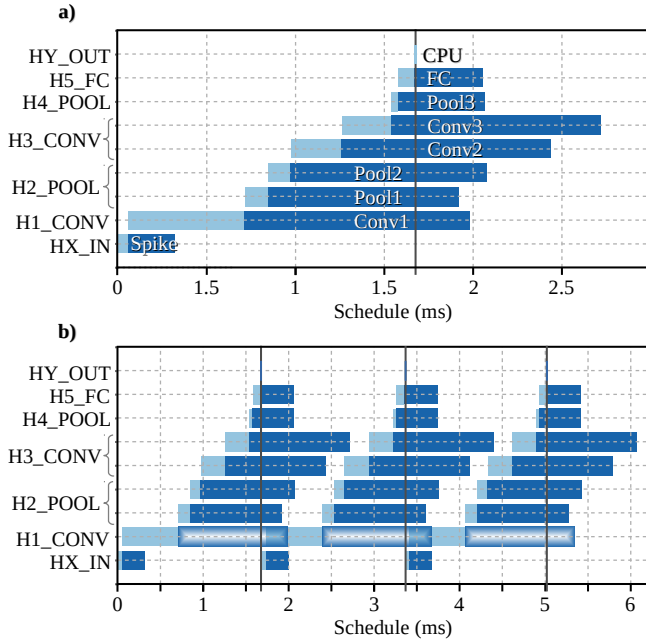
**FIGURE 19.** Noise tolerance on hardware PU with custom floating-point approximation, (a) exhibits accuracy degradation applying 50% of noise amplitude, and (b) illustrates convergence of inference with 400 spikes.**TABLE 8.** Performance of hardware processing units with hybrid logarithmic approximation.

Hardware mapping		Computation schedule (ms)			
Layer	PU	$t_s$	$t_{CPU}$	$t_{PU}$	$t_f$
HX_IN	Spike	0	0.055	0.264	0.319
H1_CONV	Conv1	0.057	0.655	1.271	1.983
H2_POOL	Pool1	0.714	0.130	1.074	1.918
H3_CONV	Conv2	0.845	0.126	1.106	2.077
H4_POOL	Pool2	0.973	0.285	1.179	2.437
H5_FC	Conv3	1.258	0.278	1.176	2.712
H4_POOL	Pool3	1.538	0.037	0.488	2.063
H5_FC	FC	1.577	0.091	0.388	2.056
HY_OUT	CPU	1.669	0.004	0	1.673

### C. RESULTS AND DISCUSSION

As a reference, the SbS network simulation on embedded CPU using standard 32-bit floating-point achieves an accuracy of 99.3% with a latency of  $T_{SC} = 34.28ms$ . As a





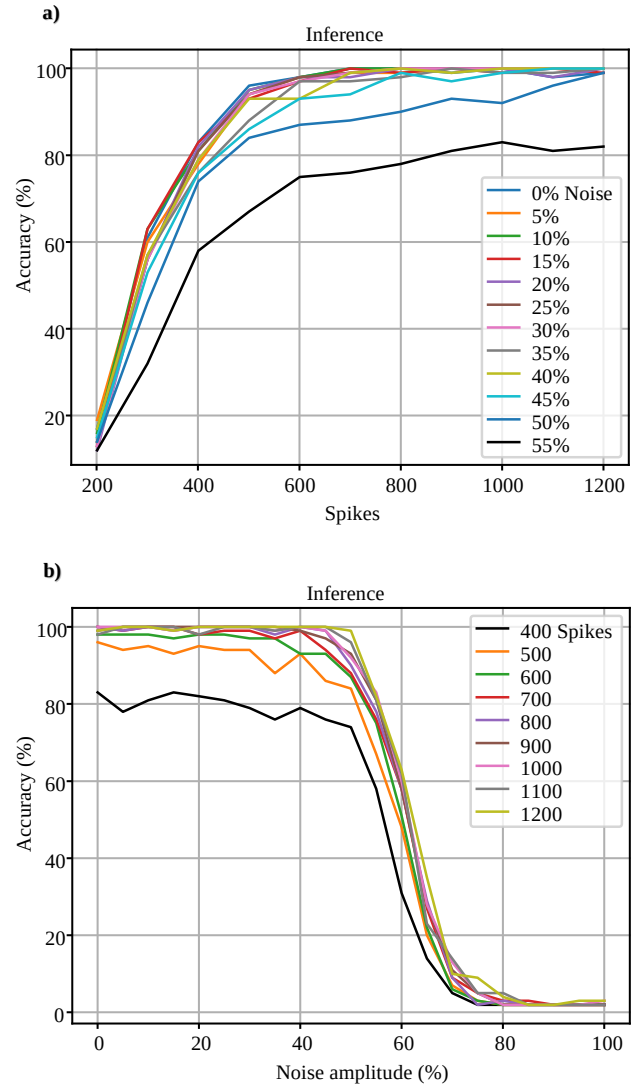
**FIGURE 20.** Performance of processing units with hybrid logarithmic approximation, (a) exhibits computation schedule, and (b) illustrates cyclic computation schedule.

**TABLE 9.** Resource utilization and power dissipation of processing units with hybrid logarithmic approximation.

PU	LUT	FF	DSP	BRAM 18K	Power (mW)
Conv	3,086	4,804	19	21	78
FC	3,046	4,873	8	8	66

second reference point, the network simulation on hardware processing units with standard floating-point achieves an accuracy of 98.98% with a latency  $T_{SC} = 3.18ms$ . As result we get a  $10.7\times$  latency enhancement and an accuracy degradation of 0.32%. The tolerance plot in Fig. 16 reveals accuracy degradation having 50% noise on the input images, and convergence of inference with 400 spikes. In this case, the SbS network deployment with precise computing proves extraordinary inherent error resilience, and hence, this represents a great potential for approximate processing.

As a demonstration of the proposed dot-product architecture, the SbS network simulation on hardware PUs with synaptic representation using 5-bit custom floating-point (4-bit exponent, 1-bit mantissa) and 4-bit logarithmic (4-bit exponent) achieve  $20.5\times$  latency enhancement and accuracy of 98.97% and 98.84%, respectively. This results in an accuracy degradation of 0.33% and 0.46%, respectively. For output quality monitoring, the noise tolerance plot in Fig. 19 and Fig. 21 reveal accuracy degradation when having 50% and 40% noise on the input images, and convergence of inference with 400 and 600 spikes, respectively. Therefore, the design exploration under the proposed approximate computing approach indicates sufficient inherent error resilience for further and more aggressive approximate processing approaches.



**FIGURE 21.** Noise tolerance on hardware PU with hybrid logarithmic approximation, (a) exhibits accuracy degradation applying 40% of noise amplitude, (b) illustrates convergence of inference with 600 spikes.

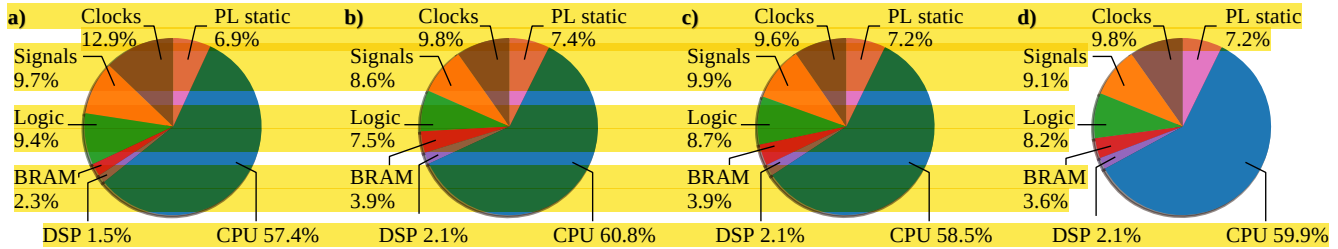
Regarding resource utilization and power dissipation with the proposed approach, the *Conv* processing units have a 43.24% reduction of BRAM, and a 12.35% of improvement in energy efficiency over the standard floating-point implementation. However, the proposed approach does not reuse the available floating-point operator cores instantiated from other computational sections (see Tab. 5). Therefore, the logic required for the dot-product must be implemented, which is reflected as additional utilization of LUT and FF resources. The experimental results of the design exploration are summarized in Tab. 10. The platform implementations are summarized in Tab. 11, and their power dissipation breakdowns are presented in Fig. 22.

**TABLE 10.** Experimental results.

Dot-product implementation	PU	Post-implementation resource utilization				Power (mW)	Latency		Accuracy (%) <sup>e</sup>	
		LUT	FF	DSP	BRAM 18K		$T_{SC}$ (ms)	Gain <sup>d</sup>	Noise 0%	50%
Standard floating-point computation <sup>a</sup>	Conv	2,765	4,366	19	37	89	3.18	10.7x	98.98	98.63
	FC	2,649	4,189	8	9	66				
Hybrid custom floating-point approx <sup>b</sup>	Conv	3,139	4,850	19	25	82	1.67	20.5x	98.97	98.47
	FC	3,265	5,188	8	9	66				
Hybrid logarithmic approximation <sup>c</sup>	Conv	3,086	4,804	19	21	78	1.67	20.5x	98.84	95.22
	FC	3,046	4,873	8	8	66				

<sup>a</sup> Reference with standard floating-point arithmetic (IEEE 754).<sup>b</sup> Synaptic weight with number representation composed of 4-bit exponent and 1-bit mantissa.<sup>c</sup> Synaptic weight with number representation composed of 4-bit exponent.<sup>d</sup> Acceleration with respect to the computation on embedded CPU (ARM Cortex-A9 at 666 MHz) with latency  $T_{SC} = 34.28ms$ .<sup>e</sup> Accuracy on 10,000 image test set with 1000 spikes.**TABLE 11.** Platform implementations.

Platform implementation	Post-implementation resource utilization				Power (W)	Clock (MHz)	Latency		Accuracy (%) <sup>f</sup>
	LUT	FF	DSP	BRAM 18K			$T_{SC}$ (ms)	Gain <sup>e</sup>	
Ref. [14] <sup>a</sup>	42,740	57,118	49	92	2.519	250	4.65	7.4x	99.02
This work (standard floating-point computation) <sup>b</sup>	39,514	56,036	82	180	2.420	200	3.18	10.7x	98.98
This work (hybrid custom floating-point approx) <sup>c</sup>	42,021	58,759	82	156	2.369	200	1.67	20.5x	98.97
This work (hybrid logarithmic approximation) <sup>d</sup>	41,060	57,862	82	148	2.324	200	1.67	20.5x	98.84

<sup>a</sup> Reference architecture with homogeneous AUs using standard floating-point arithmetic (IEEE 754).<sup>b</sup> Reference architecture with specialized heterogeneous PUs using standard floating-point arithmetic (IEEE 754).<sup>c</sup> Proposed architecture with specialized heterogeneous PUs using synaptic weight with number representation composed of 4-bit exponent and 1-bit mantissa.<sup>d</sup> Proposed architecture with specialized heterogeneous PUs using synaptic weight with number representation composed of 4-bit exponent.<sup>e</sup> Acceleration with respect to the computation on embedded CPU (ARM Cortex-A9 at 666 MHz) with latency  $T_{SC} = 34.28ms$ .<sup>f</sup> Accuracy on 10,000 image test set with 1000 spikes.**FIGURE 22.** Power dissipation breakdown of platform implementations. (a) Ref. [14] architecture with homogeneous AUs using standard floating-point arithmetic (IEEE 754), (b) reference architecture with specialized heterogeneous PUs using standard floating-point arithmetic (IEEE 754), (c) proposed architecture with hybrid custom floating-point approximation, and (d) proposed architecture with hybrid logarithmic approximation.

## VI. CONCLUSIONS

In this work, we accelerate SbS neural networks with a dot-product functional unit based on approximate computing that combines the advantages of custom floating-point and logarithmic representations. This approach reduces computational latency, memory footprint, and power dissipation while preserving classification accuracy. For output quality monitoring, we applied noise tolerance plots as an intuitive visual measure to provide insights into the accuracy degradation of SbS networks under different approximate processing effects. This plot reveals inherent error resilience, hence, the possibilities for approximate processing.

We demonstrate our approach using a design exploration flow on a Xilinx Zynq-7020 with a deployment of SbS network for the MNIST classification task. This implementation achieves up to  $20.5\times$  latency enhancement,  $8\times$  weight memory footprint reduction, and 12.35% of energy efficiency

improvement over the standard floating-point hardware implementation, and incurs in less than 0.5% of accuracy degradation. Furthermore, with a noise amplitude of 50% added on top of the input images, the SbS network presents an accuracy degradation of less than 5%. As output quality monitor, the resulting noise tolerance plots demonstrate a sufficient QoR for minimal impact on the overall accuracy of the neural network under the effects of the proposed approximation technique. These results suggest available room for further and more aggressive approximate processing approaches.

In summary, based on the relaxed need for fully accurate or deterministic computation of SbS neural networks, approximate computing techniques allow substantial enhancement in processing efficiency with moderated accuracy degradation.

## ACKNOWLEDGMENTS

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## SUPPLEMENTARY MATERIAL

### A. SBS ALGORITHM

The SbS network inference is described in Algorithm 2, while spike production and layer update are described in Algorithm 3 and Algorithm 4, respectively.

#### Algorithm 2: SbS network inference.

**input:** Layers of the network as  $H^l$ , where  $l$  is the layer index.  
**input:**  $N_L$  as the number of layers.  
**input:**  $N_X^l, N_Y^l$  as the size of layers.  
**input:**  $N_{Spk}$  as the number of spikes for inference (iterations).  
**output:**  $H^l$ .

```

1: for  $t = 0$  to  $N_{Spk} - 1$  do
    Initialization of  $H^l(i_X, i_Y, :)$  :
2:   if  $t == 0$  then
3:     for  $l = 0$  to  $N_L - 1$  do
4:       for  $i_X = 0, i_Y = 0$  to  $N_X^l - 1, N_Y^l - 1$  do
5:         for  $i_H = 0$  to  $N_H^l - 1$  do
6:            $H^l(i_X, i_Y, i_H) = 1/N_H^l$ 
7:         end for
8:       end for
9:     end for
10:   end if
    Production of spikes :
11:   for  $l = 0$  to  $N_L - 1$  do
12:     if  $l == 0$  then
13:       Draw spikes from input // (Algorithm 3)
14:     else
15:       Draw spikes from  $H^l$  // (Algorithm 3)
16:     end if
17:   end for
    Update layers :
18:   for  $l = 0$  to  $N_L - 1$  do
19:     Update  $H^l$  // (Algorithm 4)
20:   end for
21: end for

```

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#### Algorithm 3: Spike production.

**input:** Layer as  $H_t \in \mathbb{R}^{N_X \times N_Y \times N_H}$ , where  $N_X$  is the layer width,  $N_Y$  is the layer height,  $N_H$  is the length of  $\vec{h}$  (IP vector).  
**output:** Output spikes as  $S_t^{out} \in \mathbb{N}^{N_X \times N_Y}$

```

1: for  $i_X = 0, i_Y = 0$  to  $N_X - 1, N_Y - 1$  do
    Generate spike :
2:    $th = MT19937PseudoRandom() / (2^{32} - 1)$ 
3:    $acu = 0$ 
4:   for  $i_H = 0$  to  $N_H - 1$  do
5:      $acu = acu + H_t(i_X, i_Y, i_H)$ 
6:     if  $th \leq acu$  or  $i_H == N_H - 1$  then
7:        $S_t^{out}(i_X, i_Y) = i_H$ 
8:     end if
9:   end for
10: end for

```

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**Algorithm 4:** SbS layer update.

---

**input:** Layer as  $H \in \mathbb{R}^{N_X \times N_Y \times N_H}$ , where  
 $N_X$  is the layer width,  
 $N_Y$  is the layer height  
 $N_H$  is the length of  $\vec{h}$  (IP vector).  
**input:** Synaptic matrix as  $W \in \mathbb{R}^{K_X \times K_Y \times M_H \times N_H}$ , where  
 $K_X \times K_Y$  is the size of the convolution/pooling kernel,  
 $M_H$  is the length of  $\vec{h}$  from previous layer,  
 $N_H$  is the length of  $\vec{h}$  from this layer.  
**input:** Input spike matrix from previous layer as  
 $S_t^{in} \in \mathbb{N}^{N_{Xin} \times N_{Yin}}$ , where  
 $N_{Xin}$  is the width of the previous layer,  
 $N_{Yin}$  is the height of the previous layer.  
**input:** Strides of X and Y as  $stride_X$  and  $stride_Y$ ,  
respectively.  
**input:** Epsilon as  $\epsilon \in \mathbb{R}$ .  
**output:** Updated layer as  $H^{new} \in \mathbb{R}^{N_X \times N_Y \times N_H}$ .  
**Update layer :**  
1:  $z_X = 0$  // X and Y index for  $S_t^{in}$   
2:  $z_Y = 0$   
3: **for**  $i_Y = 0$  **to**  $N_Y - 1$  **do**  
4:   **for**  $i_X = 0$  **to**  $N_X - 1$  **do**  
5:      $\vec{h} = H(i_X, i_Y, :)$   
   **Update IP :**  
6:     **for**  $j_X = 0$ ,  $j_Y = 0$  **to**  $K_X - 1$ ,  $K_Y - 1$  **do**  
7:        $s_t = S_t^{in}(z_X + j_X, z_Y + j_Y)$   
8:        $\vec{w} = W(j_X, j_Y, s_t, :)$   
9:        $\vec{p} = 0$   
   **Dot-product :**  
10:        $r = 0$   
11:       **for**  $j_H = 0$  **to**  $N_H - 1$  **do**  
12:          $\vec{p}(j_H) = \vec{h}(j_H) \vec{w}(j_H)$   
13:          $r = r + \vec{p}(j_H)$   
14:       **end for**  
15:       **if**  $r \neq 0$  **then**  
   **Update IP vector :**  
16:       **for**  $i_H = 0$  **to**  $N_H - 1$  **do**  
17:          $h^{new}(i_H) = \frac{1}{1+\epsilon} \left( h(i_H) + \epsilon \frac{\vec{p}(i_H)}{r} \right)$   
18:       **end for**  
   **Set the new H vector for the layer :**  
19:        $H^{new}(i_X, i_Y, :) = \vec{h}^{new}$   
20:       **end if**  
21:     **end for**  
22:      $z_X = z_X + stride_X$   
23:   **end for**  
24:    $z_Y = z_Y + stride_Y$   
25: **end for**

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DAVID ROTERMUND started his scientific career as a chemical technical assistant in 1992 and received a pre-diploma in electrical engineering at the Hochschule Bremen (City University for Applied Science) in 1996. In 2002, he finished his studies of physics at the University of Bremen with a diploma (specialization in neuroscience and solid state physics). In 2007 he received his PhD "Extraction of information from the dynamical activities of neural networks". Among other neuroscience projects, he participated in several project in the field of neuroprosthetics like the German-Israeli joint project "Models and Experiments towards Adaptive Control of Motor Prostheses" (METACOMP), the research focus Neurotechnology at the University of Bremen, and the Creative Unit "I-See: The artificial eye – chronic wireless interface to the visual cortex". In the BMBF project KALOMED, where the goal was to design a fully wireless recording system that can be implanted under the skull of an user, he worked as project organizer and hardware/ software/ firmware designer as well as data miner. He will be the co-organizer of the upcoming Era-Net Neuron (a joint Canadian / EU project) for the development of advanced techniques in the field of visual cortex prosthesis. Beside his research in the field of neuroprosthetics, he is keenly interested in information processing using spiking neuronal networks.



KLAUS R. PAWELZIK received his PhD in the field of Nonlinear Dynamics in 1990. From 1991 till March 1998 he was research assistant at several well-known institutes in Germany and the US. Since April 1998 he is a tenured professor for Theoretical Physics and Theoretical Biology at the University of Bremen. He works mainly on topics in Theoretical Neuroscience, but also on problems in Neuro-technology and studies models of other complex adaptive systems. His many publications underline his expertise in these fields. Currently he is the director of the Center of Cognitive Sciences at the University of Bremen and has raised a number of third-party funds, among them several in the field of Neuro-technology. There he recently filed a patent with the title "Artificial neural network data processing apparatus and data processing method".



ALBERTO GARCIA-ORTIZ obtained the diploma degree in Telecommunication Systems from the Polytechnic University of Valencia (Spain) in 1998. After working for two years at Newlogic in Austria, he started the Ph.D. at the Institute of Microelectronic Systems, Darmstadt University of Technology, Germany. In 2003, he received from the Department of Electrical Engineering and Information Technology of the university the Ph.D. degree with "summa cum laude."

From 2003 to 2005, he worked as a Senior Hardware Design Engineer at IBM Deutschland Development and Research in Böblingen. After that he joined the start-up AnaFocus (Spain), where he was responsible for the design and integration of AnaFocus' next generation Vision Systems-on-Chip. He is currently full professor for the chair of integrated digital systems at the university of Bremen. Dr. Garcia-Ortiz received the "Outstanding dissertation award" in 2004 from the European Design and Automation Association. In 2005, he received from IBM an innovation award for contributions to leakage estimation. Two patents are issued with that work. He serves as editor of JOLPE and is reviewer of several conferences, journals, and European projects.

His interests include low-power design and estimation, communication-centric design, SoC integration, and variations-aware design.

...

**Original Manuscript ID:** Access-2021-01435

**Original Article Title:** “Accelerating Spike-by-Spike Neural Networks on FPGA with Hybrid Custom Floating-Point and Logarithmic Dot-Product Approximation”

**To:** IEEE Access Editor

**Re:** Response to reviewers

Dear Editor,

Thank you for allowing a resubmission of our manuscript, with an opportunity to address the reviewers' comments.

We are uploading (a) our point-by-point response to the comments (below) (response to reviewers), (b) an updated manuscript with yellow highlighting indicating changes, and (c) a clean updated manuscript without highlights (PDF main document).

Best regards,

Yarib Nevarez et al.

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**Reviewer#1, Concern # 1:**

Section I / Paragraph 2: It mentions that “Among the family of SNNs, the SbS neural network is remarkable.” Here, several things are not clear.

- Why is the SbS network remarkable?
- What does the family of SNNs refer to and how does one family differ from each other?
- The motivation why studying and accelerating the SbS network are not clear.

**Concern:** Why is the SbS network remarkable?

**Author response:** The Spike-by-Spike (SbS) neural network is a remarkable model for its reduced complexity, which is on the less realistic side of the SNN scale of biological realism. Consequently, the hardware complexity of SbS network implementations is greatly reduced. In spite of this, SbS still uses stochastic spikes as a means of transmitting information between populations of neurons and thus retains the advantageous robustness of SNNs. These advantages range from offering the potential to achieve energy efficiency closer to that of the human brain, superior resistance against adversary attacks, and the possibility of more efficient asynchronous parallelization.

**Author action:** We updated the manuscript by clarifying this point in Section I (page 2).

**Concern:** What does the family of SNNs refer to and how does one family differ from each other?

**Author response:** SNNs emulate the real behavior of neurons in different levels of detail. The more detailed the biological part is emulated, the greater the computational complexity. Most of today’s SNNs use a very detailed model (e.g., Leaky Integrate-and-Fire (LIF)). In contrast, the SbS neural network is a model on the less realistic side of the SNN scale of biological realism.

**Author action:** We updated the manuscript by clarifying this point in Section I (page 2).

**Concern:** The motivation why studying and accelerating the SbS network are not clear.

**Author response:** Hardware accelerators that focus on SbS have only been partially investigated so far. Enhanced SbS accelerators will have a double impact. From an engineering point of view, they will contribute to the deployment of robust neural networks in small embedded systems; from a scientific point of view, they will facilitate fundamental research for neuroscience.

**Author action:** We updated the manuscript by clarifying this point in Section I (page 2).

**Reviewer#1, Concern # 2:**

Section I / Paragraph 2: It mentions that “These properties place the SbS network in between non-spiking NN and stochastically spiking NN, offering advantages from both structures.” It is not clear how the SbS network can offer advantages from both structures.



**Author response:** On one hand, the SbS model incorporates the inherent robustness of SNNs, which provide the possibility of more efficient asynchronous parallelization and superior resilience against disturbances based on the synaptic stochasticity; on the other hand, the SbS model incorporates the regular flow of information from CNNs, which are expressed on explicit vector operations.

**Author action:** We updated the manuscript by clarifying this point in Section I (page 2).

### Reviewer#1, Concern # 3:

Section I / Paragraph 3: It mentions that “deep SbS networks are high compute and data intensive, ...” It is suggested to provide the supporting data.

**Author response:** The computational cost of SbS network models is higher compared to equivalent CNN models and lower compared to regular SNN models (e.g., Leaky Integrate-and-Fire). We have added the SbS algorithm and the computational cost in the paper.

**Author action:** We updated the manuscript by providing a simplified SbS algorithm and the computational cost in multiply-accumulate (MAC) operations in Section III- C (page 4 and 5).

### Reviewer#1, Concern # 4:

Section III-A: The explanation of SbS fundamental directly focuses on its computational aspects, without discussing the basic network overview, such as the network architecture/topology, synaptic connections, spike/information coding, etc. Therefore, this makes the following discussion difficult to follow.

**Author response / action:** We updated the manuscript by adding further explanations of SbS model in Section III – A (page 4), the basic network overview in Section III – B (page 4), a simplified algorithm in Section III – C (page 5), and detailed algorithm in supplementary materials (page 17 and 18).

### Reviewer#1, Concern # 5:

Section III-A / Paragraph 4:

- What does the “tensor flow network” mean?
- What is the type of noise used for the observation in Fig. 2?
- It is not clear the context of the number of spikes that is discussed in this paragraph.

**Concern:** What does the “tensor flow network” mean?

**Author response:** This was refereeing to the CNN implemented in tensor flow.

**Author action:** We have corrected this in the paper, Section III – D (page 5).

**Concern:** What is the type of noise used for the observation in Fig. 2?

**Author response:** We used positive additive uniformly distributed noise.

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**Author action:** We have added this information in Fig. 2 (page 5).

**Concern:** It is not clear the context of the number of spikes that is discussed in this paragraph.

**Author response:** The number of spikes is denoted as the number of iterations the SbS algorithm updates its internal representation (as a generative model).

**Author action:** We updated the manuscript by clarifying that the number of spikes represents the number of iterations for the SbS algorithm in Section III – B, C and D (page 4 and 5).

**Reviewer#1, Concern # 6:**

Section IV-A:

- It mentions that the system design from reference [46] is revisited. What are the differences between the proposed architecture in manuscript with the design from [46]? It is suggested to clarify the novelty.
- It mentions that “The hardware architecture can resize its resource utilization by changing the number of PUs instances, ...” Does it mean the proposed system supports the reconfiguration at run-time? If so, it is suggested to explain how the reconfiguration is performed.

**Concern:** It mentions that the system design from reference [46] is revisited. What are the differences between the proposed architecture in manuscript with the design from [46]? It is suggested to clarify the novelty.

**Author response:** As architectural novelty, our proposed approach in this publication is based on specialized heterogeneous processing units with approximate computing. In contrast, our previous work [46] is based on generic homogeneous accelerator units with standard floating-point, which represents elevated memory and computational costs.

**Author action:** We updated the manuscript by clarifying this point in the first two paragraphs in Section IV (page 5 and 6). In addition, we added a platform comparison table. This table compares our previous publication and the resulting platforms from the design exploration on this publication. This table contains resource utilization, power dissipation, latency, and accuracy. This table is included at the end of Section V-C (page 16).

**Concern:** It mentions that “The hardware architecture can resize its resource utilization by changing the number of PUs instances, ...” Does it mean the proposed system supports the reconfiguration at run-time? If so, it is suggested to explain how the reconfiguration is performed.

**Author response:** The proposed system does not support the reconfiguration at run-time. The hardware architecture resizes its resource utilization by changing the number of PUs instances prior to the hardware synthesis.

**Author action:** We updated the manuscript by clarifying this point in section IV-A, second paragraph (page 6).

**Reviewer#1, Concern # 7:**

Section IV-B: It is still not clear how the bitwidth is decided for each parameter that is considered for the computation. It should be explained when discussing the custom floating-point and logarithmic representation. Otherwise, it seems like a pre-selected bitwidth without justification. For example, the partial discussion in the Section V-B.1 and Section V-B.2 can be used here, but should be supported with justification.

**Author response:**

We use either hybrid custom floating-point or logarithmic number representation on the synaptic weight matrix. We keep everything else with standard floating-point number representation.

Both the custom floating-point and logarithmic number representation have the same exponent bit width extracted from its floating-point representation. The mantissa bit width is a knob parameter to trade off resource utilization and quality-of-result. Removing mantissa results in the logarithmic number representation.

Since the synaptic weight matrix is composed of entries with normalized values, we have exponents ranging from negative values to zero.

Therefore, for each synaptic weight matrix, we look for the smallest value, which corresponds to the largest negative exponent in the values of the matrix. Hence, the bit width of the exponent is determined according to this value. Also, to further reduce the bit width, since all exponents are negative numbers, the sign bit is removed (to reduce bit width), then the exponent is handled as negative on the hardware.

**Author action:** We updated the manuscript by describing the method to determine the required bit width in Section IV-C (page 7 and 8), where we placed the formulas with their discussion and an illustrative figure.

**Reviewer#1, Concern # 8:**

Section V-A.2: What are the reasons of computing CONV layers (H2\_POOL and H3\_CONV) on processing units (PUs), and computing HY\_OUT on CPU. Isn't it faster computing them all on the PUs?

**Author response:** Yes. Computing on hardware PUs is faster than on CPU. However, HY\_OUT is made up of a small vector of 10 neurons, which we decided to process on the CPU based on its processing latency of 4 microseconds. This latency is negligible compared to the overall performance assessment, accelerating HY\_OUT would yield a negligible gain. Furthermore, assigning a dedicated hardware PU to HY\_OUT would add data transfer and hardware interruption handling overheads, which makes this unprofitable.

**Author action:** We updated the manuscript by stating this point in Section V-A.2 (page 11).

**Reviewer#1, Concern # 9:**

Section V-B.1: It says that the detailed discussion on the number format is provided in Section IV-A, but the discussion is not there. It seems to be a wrong referencing and should be corrected.

**Author response:** Yes. Thanks for the observation.

**Author action:** We updated the manuscript by removing the content referring to Section IV-A. The paragraph containing this reference is removed as this content is now placed in Section IV-C. This content discussed the convenient properties of the synaptic weight matrix to ignore the sign bit, as well as the method for determining the bit width (page 7 and 8).

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2 In short, we simplified the rest of the content in this section (Section V-B.1, page 13) simply by discussing the  
3 log-2 histograms of the synaptic weight matrices and using the formulas (from Section IV-C, page 7 and 8) to  
4 obtain the bit width.  
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8 **Reviewer#1, Concern # 10:**  
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10 Section V-C: Table 8 shows that the proposed architectures (hybrid custom floating-point and hybrid  
11 logarithmic) consume larger LUT and FF resources. What are the reasons? It is also suggested to provide a  
12 breakdown of the power consumption for compute and memory units.  
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14 **Author response:**  
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16 The dot-product with standard floating-point arithmetic (IEEE 754) utilizes floating-point operator cores  
17 (LogiCORE IPs) that are already implemented in other computational sections of the hardware kernel, this is  
18 reuse. However, the proposed architecture does not reuse the already instantiated LogiCORE IPs. Instead,  
19 the logic required for the hybrid custom floating-point and logarithmic approximation must be implemented.  
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21 In other words, when using standard floating-point (IEEE 754), the HLS tool implements floating-point  
22 operator cores (LogiCORE IPs) to perform floating-point arithmetic operations. These operator cores are  
23 implemented trading logic (LUT) resources for DSP usage according to the given implementation directives.  
24 These core instances can be reused over the entire hardware kernel. Our dot-product with standard floating-  
25 point computation utilizes one multiplier and one adder arithmetic core. These cores are reused from other  
26 computational blocks.  
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29 **Author action:**  
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31 We updated the manuscript by adding the discussion regarding the floating-point operator cores used in the  
32 PUs in Section V-A.2 (page 12). We added a table showing the resource utilization and power dissipation of  
33 the multiplier and adder floating-point cores (provided by the analysis resource viewer of Vivado HLS). We  
34 complement our discussion section with this topic (page 15). We support our statements with a Xilinx  
35 application note reference (Hrica, J., 2012. Floating-point design with vivado HLS. *Xilinx Application Note*.)  
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37 Regarding the breakdown of the power consumption, we added this information at the end of the discussion  
38 section (page 16). We added the breakdown of the power consumption for each platform architecture  
39 implemented: (1) our previous publication, (2) standard floating-point computation, (3) hybrid custom  
40 floating-point approximation, and (4) hybrid logarithmic approximation. This information is provided by the  
41 project summary overview, power on-chip section from Vivado.  
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45 **Reviewer#1, Concern # 11:**  
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47 Section V-A.3 / Paragraph 1: It mentions “This plot reveals inherent ...” Shouldn’t it be “This plot reveals  
48 inherent ...”?  
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50 **Author response:** Thank you for this remark.  
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52 **Author action:** We updated the manuscript by correcting the mistake in Section V-A.3 (page 12).  
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**Reviewer#2, Concern # 1:**

This paper only uses MNIST as the data set for evaluation. SNN training algorithm is still in its infancy, but even so, it is not very suitable to take such a toy test as the evaluation benchmark for a hardware design. Existing SNN training studies have supported CIFAR-level test set and spiking-CNN. It is suggested that the authors improve the work in this regard.

**Author response:** We agree that MNIST is a basic data set unsuitable for evaluation of state-of-the-art machine learning algorithms. However, we use this basic machine learning task simply to provide a proof of concept to demonstrate the feasibility of our approximation technique for neural network accelerators.

**Author action:** We updated the manuscript by stating this point in Section I (page 3).

**Reviewer#2, Concern # 2:**

This paper stated that "... SbS networks provide numerous advantages over traditional ANNs and CNNs". I don't think it is right: SNN may have the potential to surpass ANN, but it has a long way to go to prove itself in typical applications.

**Author response:** We agree that SNN have the potential to surpass ANN in typical applications; however, SNNs are still in their infancy. One of our motivations is to facilitate/support fundamental research for computational neuroscience.

**Author actions:** We updated the manuscript by stating the potential advantages of SNNs over traditional ANNs and CNNs (page 1 and 2). Moreover, we declare that one of our motivations is to facilitate fundamental research for neuroscience in Section I (page 2).

**Note:** *References suggested by reviewers should only be added if it is relevant to the article and makes it more complete. Excessive cases of recommending non-relevant articles should be reported to [ieeeaccess@ieee.org](mailto:ieeeaccess@ieee.org)*