Accelerating Conv2D and DepthwiseConv2D Tensor Operations for TensorFlow Lite on Embedded FPGA with Hybrid Custom Floating-Point Approximation

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***Abstract*—Convolutional neural networks (CNNs) have become ubiquitous in the field of image processing, computer vision, and artificial intelligence (AI). Given the high computational demands of CNNs, dedicated hardware accelerators have been implemented to improve compute performance in FPGAs and ASICs. However, most commercial general-purpose deep learning processing units (DPUs) struggle with support for low-power, resource-limited embedded devices. In this paper, we present a tensor processor (TP) as a dedicated hardware accelerator for TensorFlow (TF) Lite on embedded FPGA. We accelerate Conv2D and DepthwiseConv2D tensor operations with fixed-point and floating-point. The proposed compute optimization performs vector dot-product with hybrid custom floating-point and logarithmic approximation. This approach accelerates computation, reduces energy consumption and resource utilization. To demonstrate the potential of the proposed architecture, we address a design exploration with four compute engines: (1) fixed-point, (2) Xilinx floating-point LogiCORE IP, (3) hybrid custom floating-point approximation, and (4) hybrid logarithmic approximation. The hardware design is implemented with high-level synthesis (HLS). A single TP running at 150 MHz on a Xilinx Zynq-7020 achieves 45X runtime acceleration and 951X power reduction on Conv2D tensor operation compared with ARM Cortex-A9 at 666MHz, and 4.5X compared with the equivalent implementation with floating-point LogiCORE IP. The entire hardware design and the implemented TF Lite software extensions are available as an open-source project.**

***Index Terms*—Artificial intelligence, convolutional neural networks, depthwise separable convolution, hardware accelerator, TensorFlow Lite, embedded systems, FPGA, custom floating-point, logarithmic computation, approximate computing**

I. Introduction

THE constant research and the rapid evolution of artificial neural networks (ANNs) are driving the transition to smarter and more powerful AI applications, where CNN-based models represent the essential building blocks of deep learning algorithms in computer vision tasks [1]. Applications such as smart surveillance, medical imaging, natural language processing, robotics, and autonomous navigation have been powered by CNN-based models in industry and academia [2]. Nonetheless, dedicated hardware is often a required to accelerate execution due to the high computational demands of CNNs. In terms of pure computational throughput, graphics processing units (GPUs) offer the best performance. In terms of power consumption, FPGA solutions are well known to be more energy efficient (than GPUs) [3]. As a result, numerous FPGA accelerators have been proposed, targeting both high performance computing (HPC) for data-centers and embedded systems applications [4]–[6]. However, most commercial deep learning processing units (DPUs) are not designed for low-power, resource-limited embedded FPGAs.

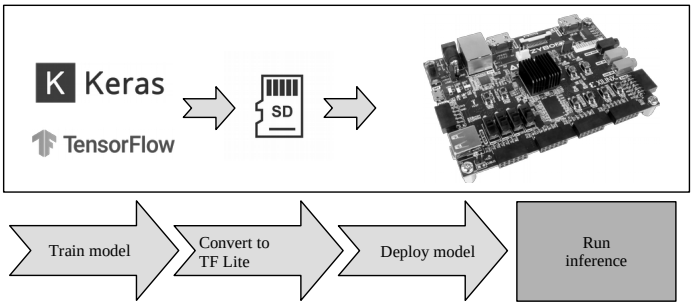

Fig. 1. Deployment workflow.

In this paper, we present a tensor processor compatible with TensorFlow Lite to accelerate Conv2D and DepthwiseConv2D operations on embedded FPGA. This implementation is integrated in a hardware/software co-design framework to accelerate tensor operations on FPGAs. This framework employs TensorFlow Lite delegates [7] as a bridge between the TFLite runtime and the proposed architecture. To control resource utilization and energy consumption, we implement the tensor operations as hardware engines, where they are optionally instantiated in the FPGA fabric as needed. Further on, to accelerate floating-point computation, we apply the hybrid custom floating-point and logarithmic dot-product approximation technique presented in [8].

To operate the proposed solution, the user would train a custom CNN-based model on TensorFlow or Keras, then this is converted into a TensorFlow Lite model (standard floating-point and 8-bit fixed-point quantization are supported), then the model is stored in a micro SD card along with the embedded

software and FPGA configuration bitstream. See **Fig.** 1.

Our main contributions are as follows:

1) We present a tensor processor as a dedicated hardware accelerator for TensorFlow Lite on embedded FPGA. We accelerate Conv2D and DepthwiseConv2D tensor operations with fixed-point and floating-point.
2) We develop a hardware/software co-design framework targeting low-power and resource-constrained AI applications. The parameterized and modular architecture enables design exploration with different compute hardware approaches.
3) We demonstrate the potential of the proposed architecture by address a design exploration with four compute engines: (1) fixed-point, (2) Xilinx floating-point LogiCORE IP, (3) hybrid custom floating-point approximation, and (4) hybrid logarithmic approximation. We explore half-precision, brain floating-point, TensorFloat, and custom reduced formats for approximate processing, including logarithmic computation. Detailed compute and accuracy performance reports are presented.

To promote the research in this field, our entire work is made available to the public as an open-source project at .

II. Related work

A. TensorFlow models on the Google's Edge TPU

The Edge Tensor Processing Unit (TPU) is an ASIC designed by Google that provides high performance machine learning (ML) inference for TensorFlow Lite models [9]. This implementation uses PCIe and I2C/GPIO to interface with an iMX 8M SoC. The reported throughput and power efficiency are 4 trillion operations per second (TOPS) and 2 TOPS per watt, respectively [10]. The Edge TPU supports 40 tensor operators including Conv2d and DepthwiseConv2d [11].

However, the Edge TPU has disadvantages.

- Power dissipation: The Edge TPU System-on-Module (SoM) requires up to 3A at 5V DC power supply [10], which can be unsuitable for very low-power applications.
- **Model compatibility**: The Edge TPU supports only TensorFlow Lite models that are fully 8-bit quantized and then compiled specifically for the Edge TPU [12]. As a limitation, the 8-bit quantization method requires a representative dataset that can be inaccessible.

III. Background

A. Conv2D tensor operation

The Conv2D tensor operation is described in **Eq.** (1). Where X represents the input feature maps, W represents the convolution kernel (known as filter) and b represents the bias for the output feature maps [13].

$$Conv2D\left(W,x\right)_{i,j,o} = \sum_{k,l,m}^{K,L,M} W_{(o,k,l,m)} \cdot X_{(i+k,j+l,m)+b_o} \quad (1)$$

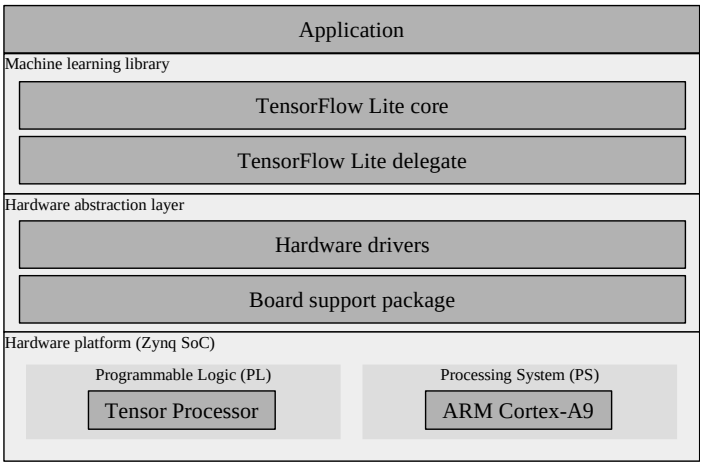

Fig. 2. System-level overview of the proposed embedded software stack.

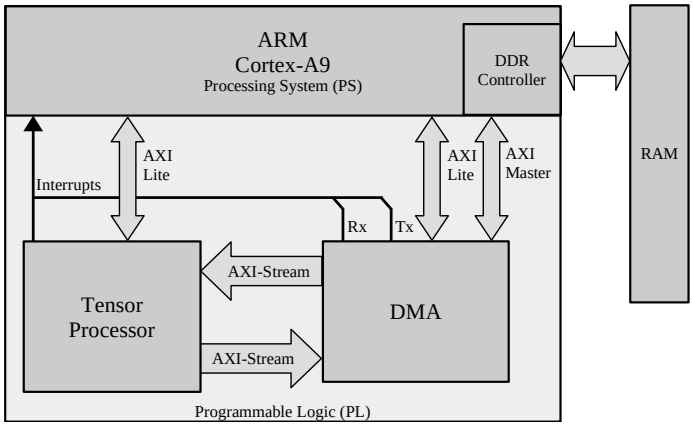

Fig. 3. System-level architecture of the proposed embedded platform.

B. DepthwiseConv2D tensor operation

The DepthwiseConv2D tensor operation is described in **Eq.** (2). Where X represents the input feature maps, W represents the convolution kernel (known as filter), and b represents the bias for the output feature maps.

$$DConv2D\left(W,y\right)_{i,j,n} = \sum_{k,l}^{K,L} W_{(k,l,n)} \cdot X_{(i+k,j+l,n)} + b_o \quad (2)$$

IV. System Design

The proposed system architecture is a hardware/software framework to investigate tensor acceleration with target on Zynq devices. The system-on-chip (SoC) architecture is illustrated in **Fig.** 3. The software stack is shown in **Fig.** 2.

A. Tensor processor

The TP is a dedicated hardware module to compute tensor operations. The hardware architecture is described in **Fig.** 4. This architecture implements on-chip storage, high performance off-chip communication with AXI-Stream, and communication with CPU via AXI-Lite and interrupt. This hardware architecture is implemented with HLS. The tensor operators are implemented based on the C++ TF Lite micro kernels [14].

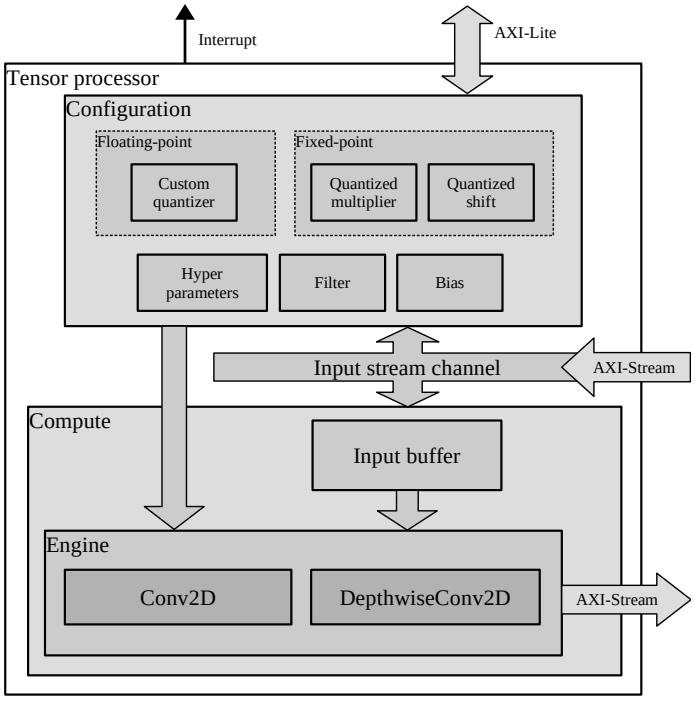

Fig. 4. Hardware architecture of the proposed tensor processor.

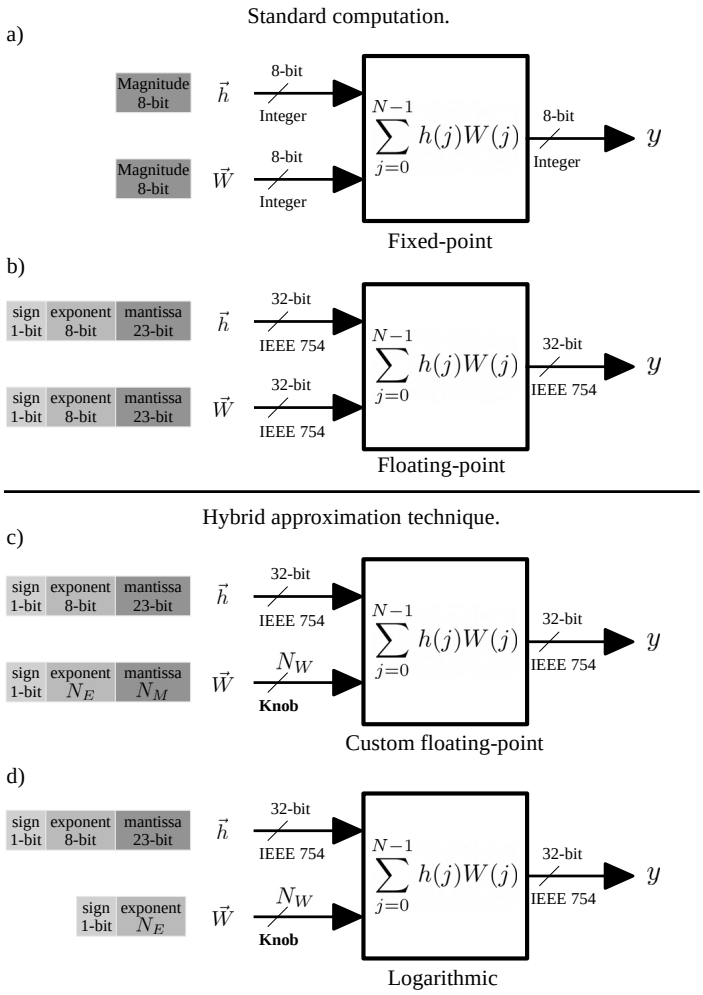

Fig. 5. Hardware alternatives for vector dot-product.

This accelerator offers two modes of operation: *configuration* and *execution*.

1) Configuration mode: In this mode, the TP receives operator ID and the hyperparameters for execution: stride, dilation, padding, offset, activation, quantized activation, depth-multiplier, input shape, filter shape, bias shape, and output shape. Afterwards the accelerator receives: filter tensor, bias tensor, and quantization vectors.

2) Execution mode: In this mode, the TP performs the tensor operator according to the hyperparameters received during configuration. With the delegate infrastructure, the input and output tensors are moved though the DMA from the memory regions allocated by TF Lite.

B. Compatibility

This hardware accelerator is compatible with TF Lite 8-bit quantized models and standard floating-point formats. For this purpose, we implement the compute engines with regular integers and floating-point LogiCORE IPs.

C. Floating-point optimization

We optimize the floating-point computation adopting the dot-product with hybrid custom floating-point and logarithmic approximation presented in [8]. This approach: (1) denormalize input numbers, (2) performs computation in integer format for exponent and mantissa, (3) normalize the result into IEEE 754. This design implements a pipelined vector dot-product with a latency of $2N + II$, where N and II are the vector length and initiation interval, respectively. A pipelined vector dot-product implemented with Xilinx floating-point LogiCORE IP presents a latency of $10N + II$ [8]. **Fig.** 5 illustrates the vector dot-product implemented in this work.

V. Experimental results

The proposed hardware/software framework is demonstrated on a Xilinx Zynq-7020 SoC (Zybo-Z7 development board). We implement the proposed hardware architecture on the programmable logic (PL) at 150 MHz. The TFLite micro library is cross-compiled for the processing system (PS), composed of ARM Cortex-A9 CPU at 666MHz with NEON floating-point unit (FPU) [15].

To evaluate the performance, we build model A and B in TensorFlow, see **Fig.** 6. Model B incorporates separable convolutions to evaluate DConv operations. These models are evaluated with the following hardware implementations:

1) Fixed-point.
2) Floating-point LogiCORE.
3) **Hybrid custom floating-point approximation.**
4) **Hybrid logarithmic approximation.**

A. Fixed-point models

To evaluate the compute performance on fixed-point, we deploy model A and B with 8-bit fixed-point quantization. The compute performance on model A and B is presented in **Tab.** I. A runtime execution of model A is illustrated in **Fig.** 7.

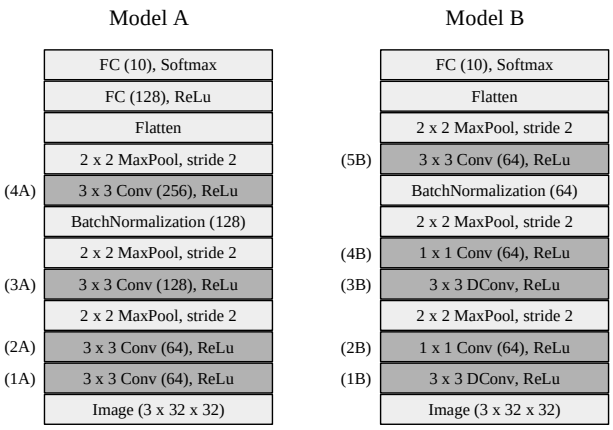

Fig. 6. CNN-based models for case study.

TABLE I
COMPUTE PERFORMANCE WITH FIXED-POINT ON MODEL A AND B.

Tensor operation		CPU	TP (fixed-point)			Accel.
Operation	**MOP**	**t (ms)**	**t (ms)**	**MOP/s**	**GOP/W**	
Model A						
(1A) Conv	1.769	700.22	55.19	32.06	0.23	**12.69**
(2A) Conv	37.748	12,666.91	297.08	127.06	0.93	**42.64**
(3A) Conv	18.874	6,081.01	142.99	131.99	0.97	**42.53**
(4A) Conv	18.874	5,543.77	122.58	153.97	1.13	**45.23**
Model B						
(1B) DConv	0.027	13.43	0.63	43.74	0.25	**21.25**
(2B) Conv	0.196	129.95	11.57	16.98	0.12	**11.23**
(3B) DConv	0.147	69.18	3.33	44.26	0.25	**20.77**
(4B) Conv	1.048	378.78	9.96	105.25	0.77	**38.02**
(5B) Conv	2.359	694.60	16.46	143.22	1.05	**42.20**

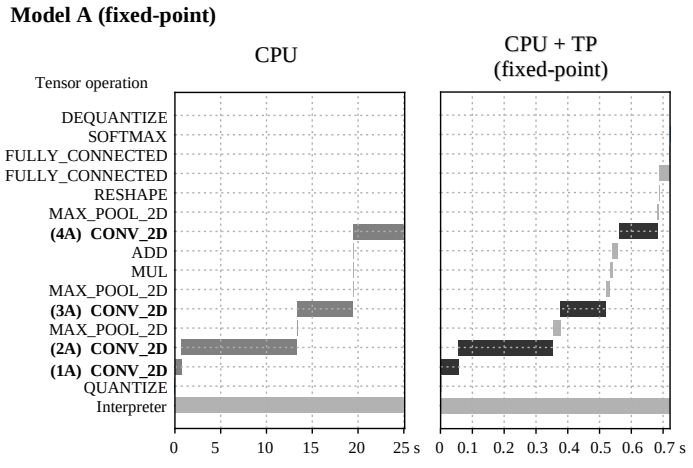

Fig. 7. Compute performance with fixed-point on model A.

B. Floating-point models

The compute performance with floating-point LogiCORE IP is presented in **Tab.** II. The compute performance with hybrid custom floating-point approximation is presented in **Tab.** III. In these tables, we find the peak acceleration on the forth convolution operator of model A. The LogiCORE implementation accelerates 9.77X, and the proposed technique accelerates 44.87X, which is 4.59X faster.

TABLE II
COMPUTE PERFORMANCE WITH FLOATING-POINT LOGICORE ON MODEL A AND B.

Tensor operation		CPU	TP (floating-point LogiCORE)			Accel.
Operation	**MOP**	**t (ms)**	**t (ms)**	**MOP/s**	**GOP/W**	
Model A						
(1A) Conv	1.769	670.95	120.07	14.73	0.21	**5.59**
(2A) Conv	37.748	12,722.13	1,328.08	28.42	0.40	**9.58**
(3A) Conv	18.874	6,094.85	636.53	29.65	0.42	**9.58**
(4A) Conv	18.874	5,564.79	569.30	33.15	0.47	**9.77**
Model B						
(1B) DConv	0.027	11.51	1.557	17.75	0.23	**7.39**
(2B) Conv	0.196	94.82	20.487	9.59	0.13	**4.62**
(3B) DConv	0.147	58.84	8.355	17.64	0.23	**7.04**
(4B) Conv	1.048	368.66	40.271	26.03	0.37	**9.15**
(5B) Conv	2.359	697.08	72.981	32.32	0.46	**9.55**

TABLE III
COMPUTE PERFORMANCE WITH HYBRID CUSTOM FLOATING-POINT APPROXIMATION ON MODEL A AND B.

Tensor operation		CPU	TP (hybrid custom floating-point)			Accel.
Operation	**MOP**	**t (ms)**	**t (ms)**	**MOP/s**	**GOP/W**	
Model A						
(1A) Conv	1.769	670.95	68.50	25.83	0.39	**9.8**
(2A) Conv	37.748	12,722.13	307.83	122.63	1.85	**41.33**
(3A) Conv	18.874	6,094.85	147.97	127.55	1.93	**41.19**
(4A) Conv	18.874	5,564.79	124.03	152.17	2.30	**44.87**
Model B						
(1B) DConv	0.027	11.51	1.41	19.63	0.27	**8.17**
(2B) Conv	0.196	94.82	20.34	9.43	0.14	**4.66**
(3B) DConv	0.147	58.84	6.58	22.41	0.31	**8.94**
(4B) Conv	1.048	368.66	12.75	82.23	1.24	**28.91**
(5B) Conv	2.359	697.08	17.14	137.68	2.08	**40.68**

For comparison, **Fig.** 8 shows the runtime executions of model A with the proposed floating-point solutions. **Fig.** 9 presents execution of model B, which incorporates separable convolutions with both Conv and DConv operations.

C. Accuracy performance

To evaluate the accuracy performance, we train A an B models for image classification with CIFAR-10 dataset. We deploy the models with a baseline accuracy of 76.6% for model A, and 68.8% for model B.

For accuracy evaluation, we implement the floating-point formats listed in **Tab.** IV. The base floating-point representation is quantized with bit-truncation and -rounding. The accuracy performance is presented in **Fig.** 10.

D. Resource utilization and power dissipation

The resource utilization and power dissipation of the TP is listed in **Tab.** V. The implementations with hybrid custom floating-point and logarithmic approximation are the most power efficient.

The estimated power dissipation of the CPU is $1.4W$. The estimated power dissipation of the TP implementing Conv operator with hybrid custom floating-point is $66mW$. This implementation achieves a peak acceleration of $44.87\times$. This results in a peak power efficiency improvement of $951\times$.

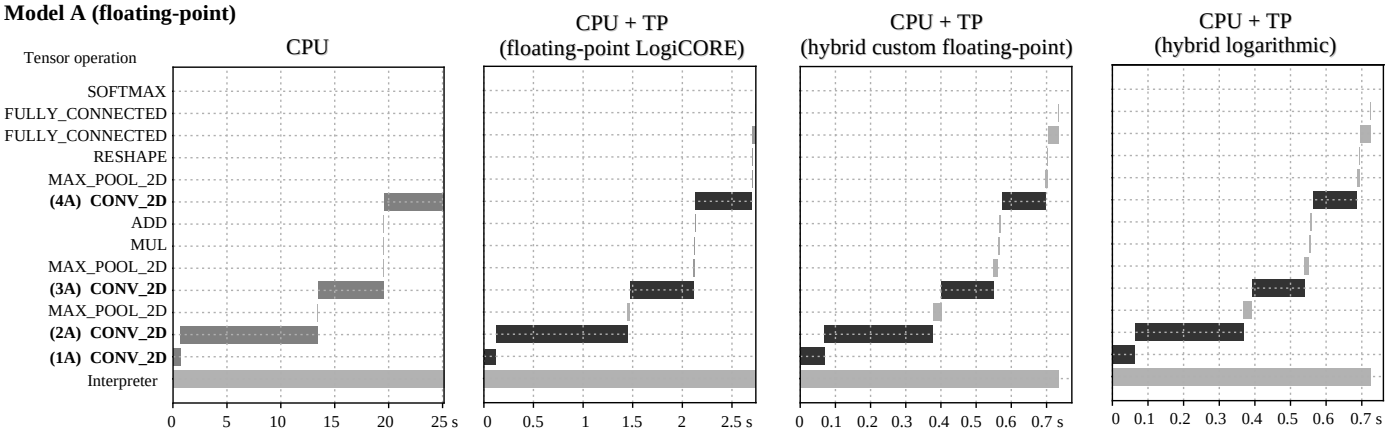

Fig. 8. Compute performance with the proposed floating-point solutions on model A.

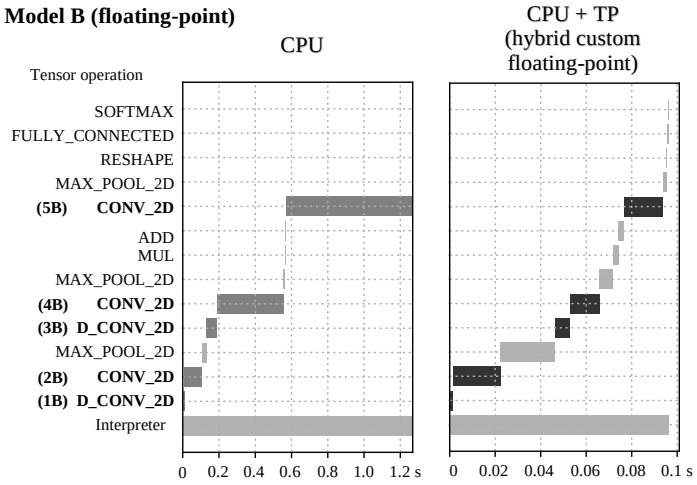

Fig. 9. Compute performance on model B (floating-point).

TABLE IV
IMPLEMENTED FLOATING-POINT FORMATS FOR ACCURACY EVALUATION.

Floating-point formats				
Name	**Size (bits)**	**Sign**	**Exponent**	**Mantissa**
Logarithmic	6	1	5	0
S1-E5-M1	7	1	5	1
S1-E5-M2	8	1	5	2
S1-E5-M3	9	1	5	3
S1-E5-M4	10	1	5	4
Float16	16	1	5	10
BFloat16	16	1	8	7
Tensor Float	19	1	8	10
Float32	32	1	8	23

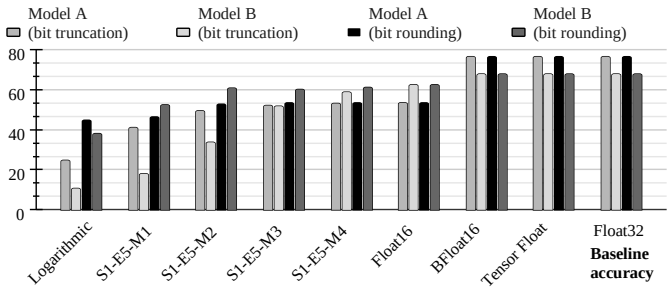

Fig. 10. Accuracy performance using hybrid custom floating-point approximation with various formats.

TABLE V
RESOURCE UTILIZATION AND POWER DISSIPATION OF THE PROPOSED TP ENGINES.

TP engine	Post-implementation resource utilization LUT	FF	DSP	BRAM 18K	Power (W)
Fixed-point					
Conv	5,677	4,238	78	70	0.136
DConv	7,232	5,565	106	70	0.171
Conv + DConv	12,684	8,015	160	70	0.248
Floating-point LogiCore					
Conv	4,670	3,909	59	266	0.070
DConv	6,263	5,264	82	266	0.075
Conv + DConv	10,871	7,726	123	266	0.119
Hybrid custom floating-point					
Conv	6,787	4,349	56	74	0.066
DConv	8,209	5,592	79	74	0.072
Conv + DConv	14,590	8,494	117	74	0.108
Hybrid logarithmic					
Conv	6,662	4,242	54	58	0.060
DConv	8,110	5,380	77	58	0.066
Conv + DConv	14,370	8,175	113	58	0.105

The power dissipation of the Zynq device is presented in **Fig.** 11.

VI. CONCLUSIONS

In this paper, we present a tensor processor as a dedicated hardware accelerator for TensorFlow Lite on embedded FPGA. We accelerate Conv2D and DepthwiseConv2D tensor operations with fixed-point and floating-point. The proposed compute optimization performs vector dot-product with hybrid custom floating-point and logarithmic approximation. This approach accelerates computation, reduces energy consumption and resource utilization. To demonstrate the potential of the proposed architecture, we presented a design exploration with four compute engines: (1) fixed-point, (2) Xilinx floating-point LogiCORE IP, (3) hybrid custom floating-point approximation,

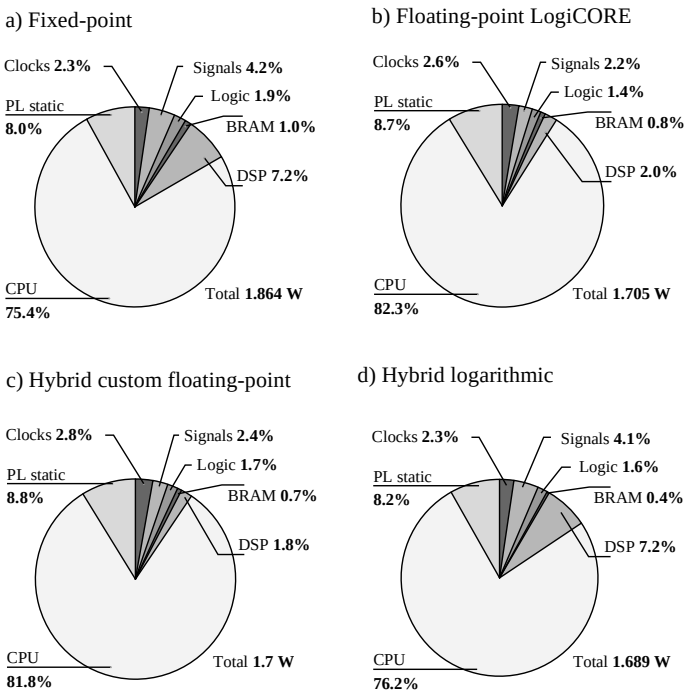

Fig. 11. Estimated power dissipation of the Zynq-7020 SoC with different TP engines.

and (4) hybrid logarithmic approximation.

A single tensor processor running at 150 MHz on a Xilinx Zynq-7020 achieves 45X runtime acceleration and 951X power reduction on Conv2D tensor operation compared with ARM Cortex-A9 at 666MHz, and 4.5X compared with the equivalent implementation with floating-point LogiCORE IP.

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