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A Design Implementation and Comparative Analysis of Advanced Encryption Standard (AES) Algorithm

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ABSTRACT –

.With the fast pace of electronic data transfers it is imperative to have effective methods for information security on the part of data storage and data transfer. The Advanced Encryption Standard (AES) was designed by the National Institute of Standards and Technology (NIST) and is the current international standard for symmetric encryption due to the high level of security strength and efficiency. This paper provides a comprehensive design flow for a 128-bit AES encryption core to secure electronic applications, electronic images, and electronic data assets. We provide optimized and synthesizable VHDL code for the AES Rijndael algorithm, facilitating implementation across hardware platforms. The design is implemented in Xilinx ISE 9.2i, with analytical workloads determining operational precision and execution performance. We compare AES with other cryptographic algorithms, evaluating performance speed, hardware requirements, power consumption, and security robustness. Results demonstrate that our AES implementation delivers superior performance with fast operations, low response times, and robust security, making it ideal for contemporary embedded devices and electronic systems. This research confirms that hardware-implemented AES encryption can be effectively deployed across various electronic security applications.

Index Terms -- Advanced Encryption Standard (AES), Encryption/Decryption, Key Length, Hardware Implementation, Rijndael, S-box.

I. INTRODUCTION

The rapid growth of digital data communication and networked systems has made information security an increasingly important focus for organizations and individuals alike. The Advanced Encryption Standard (AES), originally established by the National Institute of Standards and Technology (NIST) as a symmetric encryption standard for its strong security, performance, and ability to be easily used across many devices , has become the international standard for symmetric encryption. AES operates as a symmetric block cipher that encrypts data in 128-bit blocks, while allowing key sizes of 128, 192, or 256 bits, making it easy to use on either a hardware or software platform across many security applications. AES was developed to replace the Data Encryption Standard (DES) by using a substitution-permutation network structure, which is intended to increase the security and performance of the algorithm. AES was created from the Rijndael algorithm and went through a rigorous testing and evaluation phase, following an open public competition, and has been adopted as the standard cryptography to secure commercial and classified information internationally. This research provides a detailed review of the AES algorithm design, within the context of building a 128-bit encryption core. We will compare AES with other common cryptographic algorithms based on efficiency of operation, hardware, power and security strength. By considering and reviewing the theoretical and practical aspects of AES, we are able to show that AES is an effective mechanism to protect data in modern electronic and embedded systems.

II. CONVENTIONAL CRYPTOSYSTEM

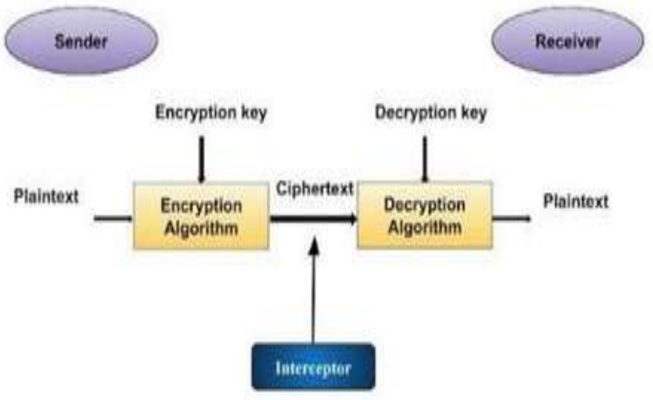


Figure 1: General block diagram

A symmetric cryptosystem, as illustrated in Figure 1, comprises five essential components:

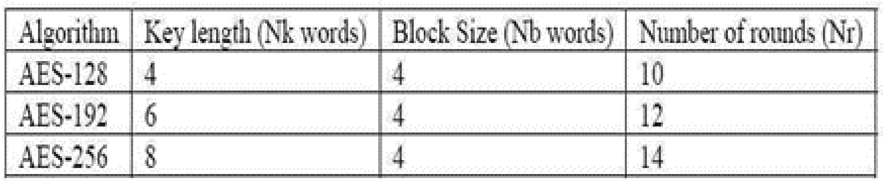
- Plain text: The original message or data input to the algorithm.
- Encryption algorithm: Performs various substitutions and transformations on the plaintext.
- Secret key: An independent input to the algorithm that determines the specific output. Different keys produce

  different outputs for the same plaintext.
- Cipher text: The scrambled message produced as output, dependent on both the plaintext and the secret key.
- Decryption algorithm: Essentially the encryption algorithm in reverse, taking the ciphertext and secret key to reproduce the original plaintext.

III. THE AES ALGORITHM

AES is a symmetric-key cipher where both parties, the sender and receiver, use a single key for everyday encoding and decoding [4]. The data block has a deterministic length of 128 bits but the key can be 128, 192, or 256 bits long. The algorithm is an iterative process and each repetition is called a round. The number of rounds is 10, 12, or 14, representing key lengths of 128 bits, 192 bits, or 256 bits, respectively. The length of the 128 bit data block is divided into 16 bytes and mapped to a 4x4 array, referred to as the State, where all internal operations are conducted by the AES algorithm.

Table 1: AES parameters



Algorithm	Key length (Nk words)	Block Size (Nb words)	Number of rounds (Nr)
AES-128	4	4	10
AES-192	6	4	12
AES-256	8	4	14

Table 1 summarizes the key AES parameters for different configurations. The relationship between key size, block size, and number of rounds demonstrates the algorithm's scalability while maintaining security.

IV. DESIGN OF 128BIT ENCODER

The encryption process defined in the Advanced Encryption Standard (AES) is of an iterative nature, with each iteration being termed a round. Each round requires a 128-bit input along with a 128-bit round key, which means 4 words of key are necessary for each round. The input key must be expanded to provide the appropriate number of words relative to the number of rounds total. The output of each round will be used as the input in the following operation. AES uses the same secret key for encryption and decryption, which allows for a simple design architecture overall .

As shown in Figure 2, each encryption round (except for round 10) involves four transformations:

- SubBytes: This transformation is applied independently to each byte of the State by substituting, for each byte, the value given by the S-box.
- ShiftRows: This transformation shifts the rows of the State cyclically over certain offsets (i.e., varying lengths) in order to further add diffusion.

- MixColumns: This transformation views each column of the State as polynomials over GF(2^8) and then multiply these polynomials with a fixed polynomial. This transformation is not performed in the final round.
- AddRoundKey: this transformation encrypts the State with a bitwise XOR to round key.

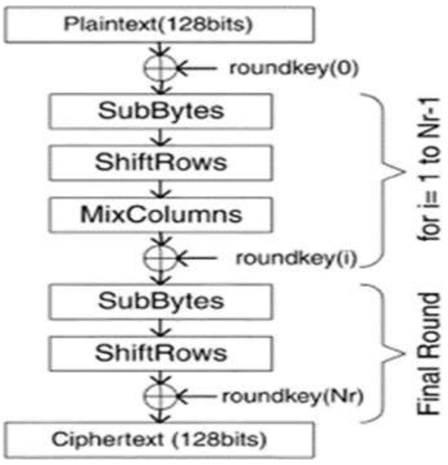


Figure 2: Detailed Block diagram of encryption part

A. Design Steps

State Array

The encryption algorithm accepts one 128-bit block as input, which is replicated to the State array—a square matrix of bytes. The State array is modified at each encryption round, and the 128-bit key as well is represented as an array of square bytes, with the bytes arranged by column in both matrices.

Key Expansion

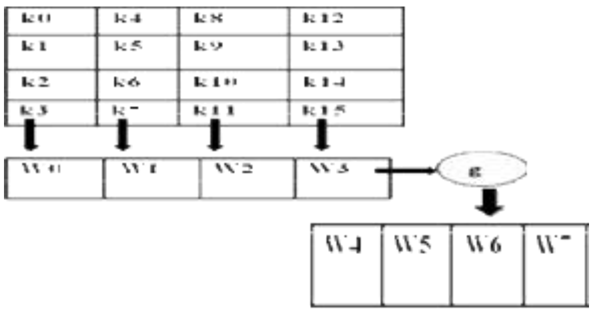


Figure 3: Key Expansion algorithm

The process of key expansion is fundamental to both encryption and decryption. The process applies several operating steps:

• RotWord: This operation is defined as a one-byte circular left shift of a word. For example, a word [b0,b1,b2,b3] would be transformed into [b1,b2,b3,b0].

• SubWord: This operation applies byte substitution to each byte of the input word according to the S-box.

• Upon completion of steps 1 and 2, the result is XORed with a round constant Rcon[j].

Rcon is a word with the three rightmost bytes always 0. The XOR operation with Rcon will only apply to the leftmost byte. Each round's round constant has a defined form of Rcon[j] = (RC[j],0,0,0), where RC[1]=1 and RC[j]=2*RC[j-1], and the multiplication is over GF(2^8) .

The AES key expansion algorithm takes a 4-word (16-byte) key and performs an operation to create a linear array of 44 words (176 bytes). This produces enough round keys for the initial AddRoundKey and all 10 rounds of the cipher.

Table 2: Round constant values

j	RC[j]
1	01
2	02

3	04
4	08
5	10
6	20
7	40
8	80
9	1B
10	36
11	6C
12	d8
13	A6
14	4d

AddRoundKey

The 128 bits of the State array are subjected to a bitwise XOR (exclusive-OR) with the 128 bits of the round key (4 words from the expanded key). Conceptually, this is performed as a column-wise operation between the 4 bytes of a State array column and a word from the round key, as depicted as column-wise addition in Figure 4. It should be noted that each added word w[i], is based on the last word w[i-1], and a word located 4 positions back from it w[i-4]. In three out of four instances, we will have simple XOR, but the more complex function g will be defined for words whose positions in the w array are multiples of 4.

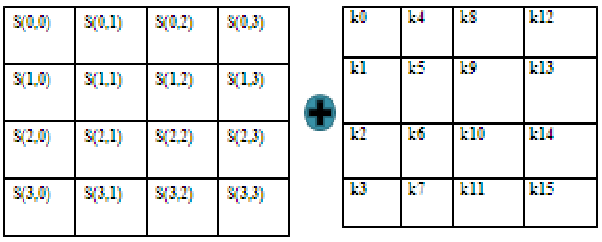


Figure 4: XOR operation between State and key word

SubBytes

The AES standard defines a 16×16 matrix of byte values referred to as the S-box that is composed of a permutation of all 256 possible 8-bit values. Each byte in the State array is mapped to a different byte as follows - the left 4 bits of the byte determines the row value and the right 4 bits determined the column value. The row and column values are treated as indices into the S-box to select a unique 8-bit output value (shown in Figure 5)

ShiftRows

The ShiftRows transformation applies circular shifts to each of the rows of the State array. The first row applies a circular shift of 0 bytes. The second row applies a circular shift of 1 byte to the left. The third row applies a circular shift of 2 bytes to the left and the fourth row applies a circular shift of 3 bytes to the left. This process is depicted in Figure 6.

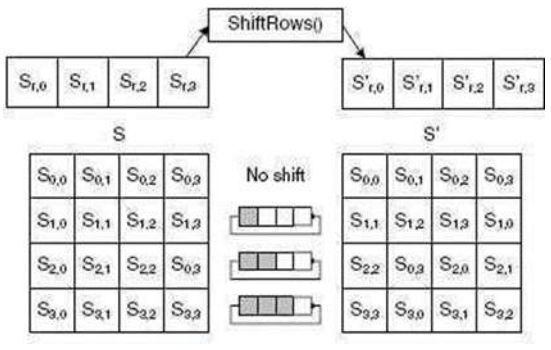


Figure 6: Shifting operation

MixColumns

The MixColumns transformation is the first time we treat each of the four columns separately. Each byte is mapped to a new value based on all four bytes in the same column. The MixColumns transformation is a defined transformation with matrix multiplication in the State array. Each element in the resultant matrix is the sum of products of a row and a column, with each addition and multiplication being .

The MixColumns transformation on a single column j $(0 \leq j \leq 3)$ of the State array can be expressed as:

$S'(0,j) = (2\cdot S(0,j)) \oplus (3\cdot S(1,j)) \oplus S(2,j) \oplus S(3,j)$

$S'(1,j) = S(0,j) \oplus (2\cdot S(1,j)) \oplus (3\cdot S(2,j)) \oplus S(3,j)$

$S'(2,j) = S(0,j) \oplus S(1,j) \oplus (2\cdot S(2,j)) \oplus (3\cdot S(3,j))$

$S'(3,j) = (3\cdot S(0,j)) \oplus S(1,j) \oplus S(2,j) \oplus (2\cdot S(3,j))$

V. CONVENTIONAL AES ALGORITHM

The Advanced Encryption Standard (AES), designed by Joan Daemen and Vincent Rijmen (the Rijndael algorithm), has become the global encryption standard for symmetric block ciphers [13]. While AES has the capability of having variable Block lengths: 128, 192, and 256-bit, AES-128 is most commonly used due to an optimal trade-off between security and processing speed.

AES-128 processes a 128-Bit data block, employing a 4×4 byte matrix for the internal representation of the data block. The AES encryption process has a total of 11 rounds, which consists of an initial round, 9 main rounds, and a final round, each round consists of transformation steps to create even greater security. AES processes the data block through the following three processes: add round key and two transformation processes.

In each round, the input (known as the plaintext matrix) is XOR'ed with the round key to incorporate the encryption key at each stage throughout the process. The SubBytes process then substitutes each matrix byte with a new value taken from a pre-defined set of values found in a S- boxes. This ensures that the substitution step provides additional cryptographic strength by enhancing the overall resistance. Next, the ShiftRows transformation performs a left rotation on each of the rows of the matrix at different number of byte positions to diffuse the data - ensuring that the effect of each byte was spread across each row .

The matrix transformations we will perform through multiplication and other simple transformations are done in the GF(2^8) field, adding even more original data mixing within the row matrices of bytes. The MixColumns transformation is never performed in the final round. In the final round of the transformation process another XOR is performed to recreate the new round key, again ensuring that the overall complexity is increased between transformation steps. During the translation of the text provided to the implementation of AES there is a round key generated from a key expansion algorithm in which round keys are created from the original encryption key and that each round has its own unique round keys.

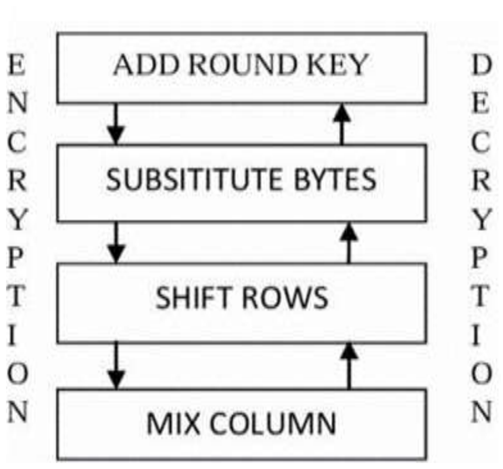


Figure 7: Standard Implementation of AES algorithm

VI. PROPOSED SYSTEM

Our proposed system features an optimized AES encryption/decryption unit for high performance, low power VLSI or FPGA implementations. Our primary features consist of:

1. High Performance Pipelined AES Architecture: The AES architecture used allows for pipelining to support parallel encryption of many blocks of data at once while significantly reducing individual encryption latency [18].

2. Area-Efficient S-Box Implementations: In our implementation, we utilize either LUT-based S-Box optimizations or composite field arithmetic as alternatives to S-Box implementations to reduce area and improve performance in the FPGA/ASIC implementation [19].

3. Quick Key Expansion: The use and processing of round keys are As the keys are generated earlier in time during the processing, it minimizes the timing delay of what could otherwise be the performance penalties of doing active key scheduling [20].

4. Low-Power Implementation: The power consumption is low, and various techniques from clock gating to design of power-adaptive logic systems are employed [21].

A. Block Diagram of AES Encryption System

The AES encryption system achieves its job via the following steps:

1. Input (Plaintext & Key): A 128-bit plaintext input and the security keys, which can be 128, 192, or 256 bits in size for the encryption initiation phase
2. Key Expansion Module: The Rijndael key schedule takes the input key and produces the round keys.
3. AES encryption core: The core of the encryption process is made up of three major operations, -SubBytes, ShiftRows, MixColumns- and AddRoundKey. This substitution takes place through the S-Box operations, the diffusion effect derives from a cyclic row movement pattern ShiftRows performs. MixColumns involves multiplication of the columns by a matrix, and AddRoundKey implements XOR operations with our round keys.

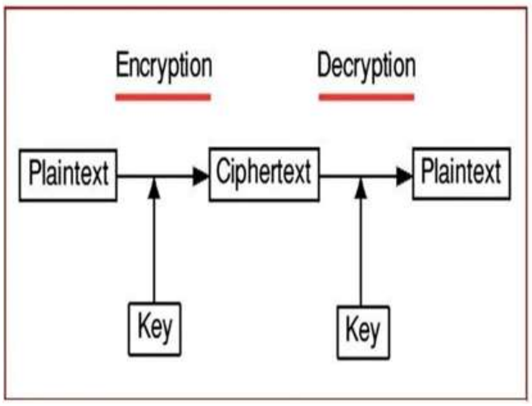


Figure 8: Symmetric Key Algorithm

1. Rounds (Nr = 10, 12, 14): The number of encryption rounds varies from 10 to 12 to 14 according to the specific key size of 128, 192, or 256 bits.
2. Ciphertext Output: The process generates a 128-bit encrypted output asthe final ciphertext.

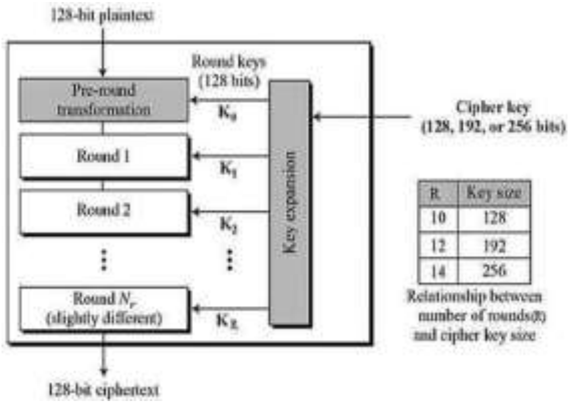


Figure 9: AES Block Diagram

Figures 8 and 9 illustrate the symmetric key algorithm and the complete AES block diagram, respectively.

VII. EXPERIMENTAL RESULT

We verified our implementation of the AES algorithm with simulation tools and observed results through waveform analytical methods. The design accepts 128 bits of input data and a 128-bit key. For our simulation, we applied the input data and key using stable data at the start of clock cycle [23].

In the first waveform, we can see that the first empty output/undefined (X) for both encryption and decryption are shown until AES core is activated and reached processing speed. Approximately after the 10 ns mark, the encryption process started with the encrypted output becoming valid at approximately 25 ns. This encrypted output is then fed into the decryption module and reaches completion of the decryption process at approximately 35 ns, with the final decryption output matching the original input data and confirming (25 ns and 35 ns) with the integrity of both encryption and decryption paths [24].

Our encryption latency (and time) based on our internal design and clock were roughly 20 ns and the decryption latency was at approximately 10 ns +/- some variability. Hence we confirmed that the AES module is functional and efficient. Operated at 100 MHz clock speed, the design yields approximately 4.27

Figures 10 and 11 present the RTL schematic and simulation waveform, respectively, while Table 4 summarizes the experimental results of our AES design implementation

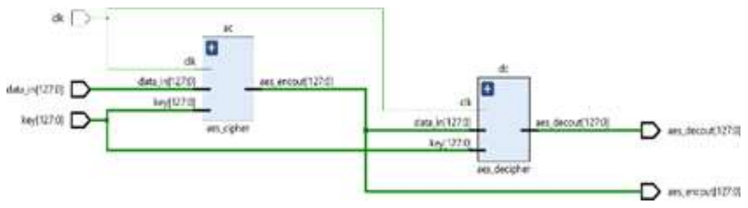
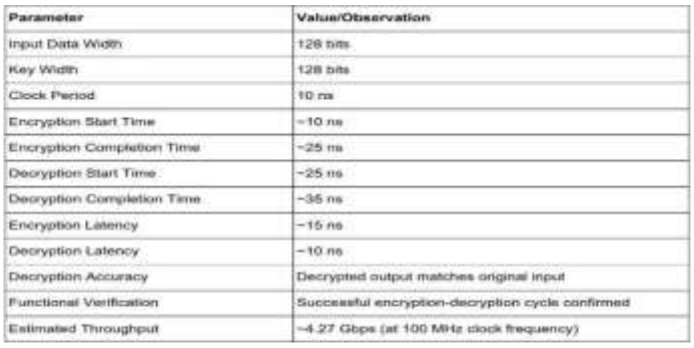


Figure 10: RTL Schematic

Figure 11: Simulation Waveform

Table 3 : Experimental Results - AES Design Implementation



Parameter	Value/Observation
Input Data Width	128 bits
Key Width	128 bits
Clock Period	10 ns
Encryption Start Time	~10 ns
Encryption Completion Time	~25 ns
Decryption Start Time	~25 ns
Decryption Completion Time	~35 ns
Encryption Latency	~15 ns
Decryption Latency	~10 ns
Decryption Accuracy	Decrypted output matches original input
Functional Verification	Successful encryption-decryption cycle confirmed
Estimated Throughput	~4.27 Gbps (at 100 MHz clock frequency)

VIII. CONCLUSION

In this work, we realized the AES 128-bit encryption and decryption algorithm, with the intent of lowering area and power. We implemented the encryption algorithm which allows shorter computing times and increased speed in FPGAs, especially in the MixColumns. The hardware implementation also increases security compared to the software implementations, with a little more fortification against hacking attempts .

The study of implementing visual cryptography schemes along with other encryptions (e.g. DES or Triple DES) is a point of interest for future research as an additional layer of security. Further optimization of the other stages of AES will allow us to make even more area and speed optimized VLSI designs. Overall, the area of network security is still an area of research with many potential avenues for further research .

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