Additional UVM components

how an complete UVM with all features, coverage, contraist, randomiztion, sva looks like?

Ah! You’re asking about a **complete, feature-rich UVM environment**—the kind that is used in real SoC/GPU verification projects. Let’s break this down carefully and then I’ll give you a structured example of how it all ties together. I’ll also include **constraints, randomization, SVA, coverage, sequences, and agents** in a single illustrative setup.

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1. UVM Testbench Architecture

A full UVM testbench has multiple layers:

1. **Interface (DPI or SystemVerilog)** – connects DUT to TB
2. **Driver** – drives signals to DUT
3. **Monitor** – observes DUT outputs
4. **Sequencer** – provides sequences to the driver
5. **Sequences** – randomized or constrained transactions
6. **Agent** – encapsulates driver, sequencer, monitor
7. **Environment (env)** – contains multiple agents, scoreboards, coverage collectors
8. **Scoreboard** – compares expected vs actual outputs
9. **Coverage** – functional coverage for transactions and interface
10. **Test** – configures environment, sets sequences
11. **SVA Assertions** – for protocol correctness

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2. Example: UVM Environment for a simple AXI4-lite Slave

Interface:

```systemverilog
interface axi_if(input logic clk, resetn);
   logic [31:0] awaddr, wdata, rdata;
   logic awvalid, wvalid, wready, rvalid;
endinterface
```

Transaction Class with Randomization & Constraints:

systemverilog

```systemverilog
class axi_transaction extends uvm_sequence_item;
  rand bit [31:0] addr;
  rand bit [31:0] data;
  rand bit [1:0] size;

  constraint addr_c { addr inside {[0:1023]}; }
  constraint data_c { data < 32'hFFFF_FFFF; }

  `uvm_object_utils(axi_transaction)

  function new(string name="axi_transaction");
    super.new(name);
  endfunction
endclass
```

Driver:

systemverilog

```systemverilog
class axi_driver extends uvm_driver #(axi_transaction);
  virtual axi_if vif;

  `uvm_component_utils(axi_driver)

  function new(string name, uvm_component parent);
    super.new(name,parent);
  endfunction

  task run_phase(uvm_phase phase);
    axi_transaction tr;
    forever begin
      seq_item_port.get_next_item(tr);
      @(posedge vif.clk);
      vif.awaddr <= tr.addr;
      vif.wdata  <= tr.data;
      vif.awvalid <= 1;
```

```
            vif.wvalid  <= 1;
            @(posedge vif.clk);
            vif.awvalid <= 0;
            vif.wvalid <= 0;
            seq_item_port.item_done();
        end
    endtask
endclass
```

Monitor:

systemverilog

```
class axi_monitor extends uvm_monitor;
    virtual axi_if vif;
    uvm_analysis_port #(axi_transaction) ap;

    `uvm_component_utils(axi_monitor)

    function new(string name, uvm_component parent);
        super.new(name,parent);
    endfunction

    task run_phase(uvm_phase phase);
        axi_transaction tr;
        forever begin
            @(posedge vif.clk);
            if(vif.rvalid) begin
                tr = axi_transaction::type_id::create("tr");
                tr.data = vif.rdata;
                ap.write(tr);
            end
        end
    endtask
endclass
```

Environment with Agent & Scoreboard:

systemverilog

```
class axi_env extends uvm_env;
   axi_agent agent;
   axi_scoreboard scoreboard;

   `uvm_component_utils(axi_env)

   function new(string name, uvm_component parent);
      super.new(name,parent);
   endfunction

   function void build_phase(uvm_phase phase);
      agent = axi_agent::type_id::create("agent", this);
      scoreboard = axi_scoreboard::type_id::create("scoreboard", this);
   endfunction
endclass
```

Sequence Example:

```systemverilog
class axi_sequence extends uvm_sequence #(axi_transaction);
   `uvm_object_utils(axi_sequence)

   task body();
      axi_transaction tr;
      repeat (10) begin
         tr = axi_transaction::type_id::create("tr");
         assert(tr.randomize());
         start_item(tr);
         finish_item(tr);
      end
   endtask
endclass
```

Functional Coverage:

systemverilog

```
covergroup axi_cg @(posedge vif.clk);
    coverpoint addr {
        bins low = {0:255};
        bins mid = {256:767};
        bins high = {768:1023};
    }
    coverpoint data;
endgroup
```

SVA Assertions:

```systemverilog
// Simple write handshake assertion
property write_valid;
    @(posedge clk) disable iff(!resetn)
    awvalid |-> wvalid;
endproperty
assert property(write_valid);
```

Test Class:

```systemverilog
class axi_test extends uvm_test;
    axi_env env;

    `uvm_component_utils(axi_test)

    function new(string name, uvm_component parent);
        super.new(name,parent);
    endfunction

    task run_phase(uvm_phase phase);
        axi_sequence seq = axi_sequence::type_id::create("seq");
        seq.start(env.agent.sequencer);
    endtask
endclass
```

✅ What this includes

- Randomized and constrained transactions
- UVM sequences and driver/monitor/agent
- Environment with scoreboard
- Functional coverage bins
- SVA assertions
- Test that instantiates and runs sequences

If you want, I can **draw a complete diagram showing the full UVM stack** and then provide a **fully integrated RTL+UVM example with multiple agents, AXI channels, coverage, SVA, and scoreboard checks**, just like a real SoC verification environment.

Do you want me to do that?

any other remaining things to add

Yes — what I shared is a **good base**, but a **full, industrial-strength UVM environment** usually has **a few more critical pieces** to be complete. Let's list them carefully:

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1. Configuration & Factory Overrides

- Use `uvm_config_db` to pass parameters (like transaction width, address range) from test to agents or drivers.
- Use `type_id::set_type_override` or factory patterns to swap components easily for different DUT variants.

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2. Multiple Agents / Multi-Channel Support

- In a complex SoC, you may have multiple AXI/APB channels.
- Each agent should handle its own interface but coordinate through environment.
- **Cross-agent synchronization** is sometimes needed (e.g., bus arbitration).

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3. Scoreboards & Reference Models

- A **functional model** of DUT (reference model) that predicts expected outputs.
- Scoreboard compares DUT outputs vs model.
- Can include **error logging and coverage** for mismatches.

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4. Transaction-Level Coverage

- Not just interface coverage, but also **cross-coverage**, e.g., combinations of address + data patterns, corner cases.
- **Covergroups** can be hierarchical (per agent or global).

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5. Advanced Randomization

- Conditional constraints, weighted randomization.
- **Sequence items can be randomized with dependencies**.
- Use `randc` for cyclic random variables if needed.

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6. Sequences & Sequence Libraries

- **Parallel sequences** for bus contention testing.
- **Virtual sequences** to coordinate multiple agents in one high-level scenario.

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7. Callbacks / Phase Hooks

- Allow **extension points** for coverage or monitoring without modifying the agent.
- Use `uvm_callbacks` for injecting behaviors.

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8. Error Injection / Fault Modeling

- Create **error sequences** to test DUT robustness (invalid transactions, timing violations, protocol errors).

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9. Assertions (SVA)

- Add **more protocol checks**, e.g.,
  - Address alignment
  - Read/write ordering
  - Timeout or deadlock detection
- Can be **inline** or in separate SVA modules.

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10. Reporting & Logging

- `uvm_report_*` macros for debug messages.
- Categorize messages (`UVM_INFO`, `UVM_WARNING`, `UVM_ERROR`, `UVM_FATAL`).
- Add **transaction logging** for replay.

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11. Regression & Test Management

- **Multiple testcases** for corner cases.
- Regression scripts to run all tests with different seeds.
- Use `uvm_test_top` to control large test suites.

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12. Coverage Closure

- Functional coverage **collected across sequences**.
- Coverage can drive **test generation**, i.e., fill holes in testing.

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13. Optional

- **Parameterized sequences** for DUT variants.
- **Scoreboard queues** for multiple outstanding transactions.
- **Memory models** for caches or FIFOs.

So in short, what I gave you is a **working example**, but a *complete* environment in industry would also include:

- Config/factory usage
- Multi-agent & virtual sequences
- Reference models & scoreboards

- Advanced coverage (transaction-level, cross-coverage)
- Callbacks & error injection
- Regression/test management + logs
- SVA for all protocol rules

If you want, I can **draw a full UVM block diagram** showing **all these components integrated**, so you can see exactly what a professional verification environment looks like — agents, sequences, scoreboard, coverage, SVA, test control, factory, etc.

Do you want me to do that next?

ok now list List them

Here's a **comprehensive list of all features/components in a complete UVM environment**:

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1. Core Components

1. **Interface** – connects DUT signals to UVM TB
2. **Transaction (Sequence Item)** – randomized, constrained data structures
3. **Driver** – converts sequence items to pin-level DUT signals
4. **Monitor** – observes DUT signals and converts to transaction-level items
5. **Sequencer** – controls which sequences the driver executes
6. **Sequence** – randomized or constrained test scenarios
7. **Agent** – encapsulates driver, sequencer, monitor; can be active or passive
8. **Environment (Env)** – top-level container for agents, scoreboards, coverage, etc.
9. **Scoreboard** – compares DUT outputs to reference model
10. **Test** – instantiates environment, sequences, and sets test-specific config

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2. Randomization & Constraints

11. **Random variables in transactions**
12. **Constraints** – conditional, weighted, or cross-field constraints
13. **Cyclic randomization (`randc`)** – for exhaustive patterns

14. **Dependent randomization** – transaction fields dependent on each other

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3. Functional Coverage

15. **Covergroups** – per transaction, per interface
16. **Cross-coverage** – combinations of multiple fields or agents
17. **Coverage bins** – low, mid, high, corner cases
18. **Coverage collection & closure analysis** – identify untested scenarios

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4. SVA Assertions

19. **Protocol assertions** – e.g., handshake rules, timing, ordering
20. **Inline assertions** – in RTL or monitor
21. **Separate assertion modules** – reusable, for multiple DUTs

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5. Advanced Features

22. **Factory & Type Overrides** – swap components at runtime
23. **uvm_config_db** – configure components dynamically
24. **Callbacks & Phase Hooks** – extend functionality without modifying agents
25. **Virtual Sequences** – coordinate multiple agents in complex scenarios
26. **Error Injection / Fault Modeling** – invalid transactions, delays, etc.
27. **Parallel sequences / contention scenarios**

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6. Reporting & Logging

28. *uvm_report_ macros** – info, warning, error, fatal
29. **Transaction logging / debug messages**
30. **Scoreboard reporting** – mismatches, pass/fail

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7. Regression & Test Management

31. **Multiple testcases** – corner cases, random tests
32. **Regression scripts** – automated runs with different seeds
33. **Seed control** – reproducibility of random tests

34. **Test control via uvm_test_top** – run all tests systematically

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8. Optional / Advanced

35. **Memory / Cache Models** – for complex DUTs
36. **Multi-agent support** – multiple interfaces/channels
37. **Cross-agent synchronization** – arbitration, shared resources
38. **Parameterized sequences / transactions** – support multiple DUT variants
39. **Queueing & transaction tracking** – multiple outstanding requests
40. **Coverage-driven verification (CDV)** – generate tests to fill coverage holes

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This list covers **everything a professional SoC/GPU UVM environment includes** — randomization, constraints, sequences, monitors, agents, coverage, assertions, scoreboards, test control, reporting, and advanced features like virtual sequences and error injection.

If you want, I can **draw a single, labeled UVM block diagram showing all 40 items integrated**, so you can visualize the full environment like in real industry projects. Do you want me to do that?

anything extra?

Yes — beyond the 40 items already listed, a **truly industrial-strength UVM environment** often includes a few **extra/advanced features** that make it more robust, scalable, and maintainable. Here's what's typically added:

Extra / Advanced Features in Full UVM Environments

1. Advanced Functional Verification

1. **Constrained-random stress testing** – push DUT to corner cases under heavy load.
2. **Coverage-driven test generation (CDV)** – automatically generate new sequences to fill coverage holes.

3. **Formal Verification Integration** – combine UVM simulation with SVA/formal checks.
4. **Temporal Assertions / Sequence-based Assertions** – assert behavior across multiple cycles.
5. **Protocol-aware coverage** – e.g., burst types, transaction sequences, error conditions.

2. Multi-DUT / System-level Verification

6. **Multiple DUT instances** – verifying multi-core or multi-channel SoCs.
7. **Top-level system environment** – multiple agents across multiple buses, interacting together.
8. **Virtual interfaces for modularity** – swap different DUTs/interfaces without changing testbench.

3. Debug, Logging & Analysis

9. **Transaction recording & replay** – save and replay transactions for debugging.
10. **Waveform-driven coverage correlation** – cross-check signals with transaction coverage.
11. **Hierarchical coverage reports** – per agent, per environment, per interface.
12. **Advanced logging infrastructure** – including severity, timestamps, hierarchical components.

4. Testbench Architecture & Reuse

13. **Parameterized testbenches** – reuse same TB for different DUT configurations.
14. **Library of reusable sequences / drivers / monitors** – makes scaling easier.
15. **UVM Callbacks for plug-ins** – allows injecting behavior or monitoring externally.
16. **Test plan automation** – linking coverage goals to automated test generation.

5. Advanced Randomization & Constraints

17. **Dynamic constraint modification at runtime** – adjust constraints during simulation.
18. **Weighted random variables** – test common and rare scenarios.
19. **Random delays / interleaving** – introduce random latency or contention.
20. **Cross-field, cross-agent, cross-sequence constraints** – for complex multi-agent interactions.

6. Integration with Other Verification Tools

21. **Integration with formal, emulation, or FPGA prototyping flows**.
22. **Remote or cloud-based simulation** – for very large SoC verification.

23. **Coverage merging & database support** – merge coverage from multiple runs or machines.
24. **Automated test result dashboards** – for regression management.

✅ So, if you include these extras along with the 40 items I listed before, you end up with a **full-featured, professional-grade UVM verification environment** like those used at **Intel, Qualcomm, AMD, or NVIDIA** for complex SoC/GPU designs.

If you want, I can now **draw a single diagram that shows all 60+ items integrated into a real-world UVM environment**, showing how drivers, monitors, agents, sequences, coverage, SVA, scoreboards, and advanced features interact.

Do you want me to do that?

how communication between components of UVM established?

Ah! Communication in UVM is **central to how the testbench works**, so let's go **step by step**. In UVM, components don't directly access each other's internals. Instead, communication happens **through standardized ports, exports, and analysis mechanisms**.

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1. Primary Communication Mechanisms in UVM

Mechanism	Purpose	Example
TLM Ports/Exports	Transaction-level communication (send/receive transactions)	`uvm_analysis_port`, `uvm_blocking_put_port`, `uvm_sequence_item_port`
uvm_config_db	Passing configuration parameters or handles down the hierarchy	Driver gets interface handle from test via `uvm_config_db#(virtual interface)`

Mechanism	Purpose	Example
Callbacks / Hooks	Allow monitoring or extending behavior without changing component code	`uvm_callback` in driver or monitor
Events / Semaphores	Synchronization between components	`uvm_event` for custom synchronization
SVA / Assertions	Implicitly observe DUT signals (communication through interface)	Assertions alert testbench of protocol violations

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2. Transaction-Level Modeling (TLM) Communication

UVM uses **TLM ports** for sending transactions between components. The main ones:

a. Sequencer → Driver

- **Purpose:** Sequencer sends sequence items (transactions) to driver.
- **Mechanism:** `uvm_sequence_item_port` / `uvm_sequence_item_export`

```systemverilog
// In Driver
uvm_driver #(axi_transaction) extends uvm_driver;
    seq_item_port.get_next_item(tr);  // Receives transaction from sequencer
    seq_item_port.item_done();        // Notifies sequencer that it's done
endclass
```

- **Flow:** `Sequence -> Sequencer -> Driver -> DUT`

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b. Monitor → Scoreboard / Coverage

- **Purpose:** Monitor observes DUT signals and sends transactions to scoreboard or coverage collector.
- **Mechanism:** `uvm_analysis_port`

```systemverilog
```

```
class axi_monitor extends uvm_monitor;
  uvm_analysis_port #(axi_transaction) ap;
  // When transaction captured:
  ap.write(tr);  // Send transaction to connected subscriber (scoreboard)
endclass
```

- Scoreboard subscribes to the analysis port:

systemverilog

```
monitor.ap.connect(scoreboard.analysis_export);
```

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c. Agent Communication

- **Driver, Sequencer, Monitor** communicate **internally through ports/exports**.
- Environment can connect multiple agents via **analysis ports** to a scoreboard or functional coverage collector.

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3. Configuration Communication

- Test passes parameters or handles to components:

systemverilog

```
uvm_config_db#(virtual axi_if)::set(this, "env.agent.driver", "vif", vif_handle);
```

- Driver retrieves it:

systemverilog

```
uvm_config_db#(virtual axi_if)::get(this, "", "vif", vif);
```

---

4. Virtual Sequences / Multi-Agent Coordination

- **Virtual sequences** coordinate multiple agents:

systemverilog

```
vseq.start(agent1.sequencer);
vseq.start(agent2.sequencer);
```

- This ensures complex scenarios where agents act together.

---

5. Summary of Component Communication

From	To	Mechanism
Sequence	Sequencer	`start_item()`, `finish_item()`
Sequencer	Driver	`uvm_sequence_item_port`
Driver	DUT	Direct signal drive through virtual interface
DUT	Monitor	Observe via virtual interface
Monitor	Scoreboard / Coverage	`uvm_analysis_port.write()`
Test / Environment	Components	`uvm_config_db.set/get()`
Any Component	Extensible Hooks	`uvm_callbacks`

✅ Key Points

1. Components communicate **indirectly** via TLM ports/exports, analysis ports, or config_db.
2. Direct access to another component is **discouraged**; modularity is maintained.
3. Virtual sequences allow **multi-agent coordination** without breaking encapsulation.
4. SVA communicates **implicitly** via signal observation.

If you want, I can **draw a diagram showing all the communication paths in a UVM testbench** — from sequence to DUT to monitor, scoreboard, coverage, and back — which makes this much clearer visually.

Do you want me to do that?