- **Directly Compatible for Use With:**
  SN54LS181/SN74LS181,
  SN54S281/SN74S281, SN54S381,
  SN74S381, SN54S481/SN74S481

PIN DESIGNATIONS

ALTERNATIVE	DESIGNATIONS[†]	PIN NOS.	FUNCTION
$\overline{G0}, \overline{G1}, \overline{G2}, \overline{G3}$	G0, G1, G2, G3	3, 1, 14, 5	CARRY GENERATE INPUTS
$\overline{P0}, \overline{P1}, \overline{P2}, \overline{P3}$	P0, P1, P2, P3	4, 2, 15, 6	CARRY PROPAGATE INPUTS
C_n	$\overline{C}_n$	13	CARRY INPUT
$C_{n+x}, C_{n+y}, C_{n+z}$	$\overline{C}_{n+x}, \overline{C}_{n+y}, \overline{C}_{n+z}$	12, 11, 9	CARRY OUTPUTS
$\overline{G}$	Y	10	CARRY GENERATE OUTPUT
$\overline{P}$	X	7	CARRY PROPAGATE OUTPUT
V_{CC}		16	SUPPLY VOLTAGE
GND		8	GROUND

[†]Interpretations are illustrated in the 'LS181, 'S181 data sheet.

logic symbol[‡]
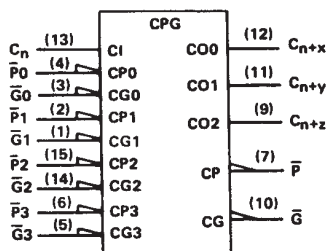
[‡]This symbol is in accordance with ANSI/IEEE Std. 91-1984 and
IEC Publication 617-12.
Pin numbers shown are for D, J, N, and W packages.

SN54S182 . . . J OR W PACKAGE
SN74S182 . . . D OR N PACKAGE
(TOP VIEW)

SN54S182 . . . FK PACKAGE
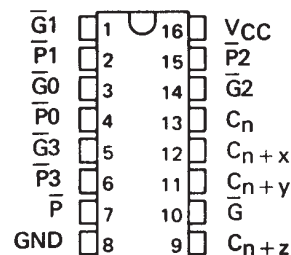(TOP VIEW)

NC - No internal connection

description

The SN54S182 and SN74S182 are high-speed, look-ahead carry generators capable of anticipating a carry across four binary adders or group of adders. They are cascadable to perform full look-ahead across n-bit adders. Carry, generate-carry, and propagate-carry functions are provided as enumerated in the pin designation table above.

When used in conjunction with the 'LS181 or 'S181 arithmetic logic unit (ALU), these generators provide high-speed carry look-ahead capability for any word length. Each 'S182 generates the look-ahead (anticipated carry) across a group of four ALUs and, in addition, other carry look-ahead circuits may be employed to anticipate carry across sections of four look-ahead packages up to n-bits. The method of cascading 'S182 circuits to perform multilevel look-ahead is illustrated under typical application data.
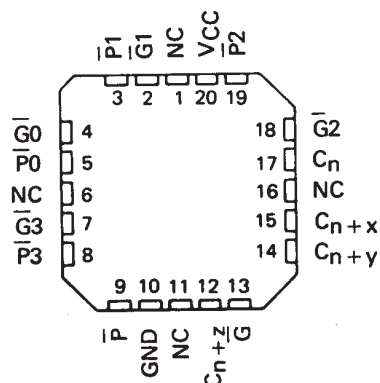
The carry functions (inputs, outputs, generate, and propagate) of the look-ahead generators are implemented in the compatible forms for direct connection to the ALU. Reinterpretations of carry functions as explained on the 'LS181 and 'S181 data sheet are also applicable to and compatible with the look-ahead generator. Logic equations for the 'S182 are:

$C_{n+x} = G0 + P0\, C_n$

$C_{n+y} = G1 + P1\, G0 + P1\, P0\, C_n$

$C_{n+z} = G2 + P2\, G1 + P2\, P1\, G0 + P2\, P1\, P0\, C_n$ or

$\overline{G} = \overline{G3 + P3\, G2 + P3\, P2\, G1 + P3\, P2\, P1\, G0}$

$\overline{P} = \overline{P3\, P2\, P1\, P0}$

$\overline{C}_{n+x} = \overline{Y0\,(X0 + C_n)}$

$\overline{C}_{n+y} = \overline{Y1\,[X1 + Y0\,(X0 + C_n)]}$

$\overline{C}_{n+z} = \overline{Y2\,\{X2 + Y1\,[X1 + Y0\,(X0 + C_n)]\}}$

$Y = Y3\,(X3 + Y2)\,(X3 + X2 + Y1)\,(X3 + X2 + X1 + Y0)$

$X = X3 + X2 + X1 + X0$

TEXAS INSTRUMENTS

FUNCTION TABLE FOR $\overline{G}$ OUTPUT

INPUTS							OUTPUT
$\overline{G3}$	$\overline{G2}$	$\overline{G1}$	$\overline{G0}$	$\overline{P3}$	$\overline{P2}$	$\overline{P1}$	$\overline{G}$
L	X	X	X	X	X	X	L
X	L	X	X	L	X	X	L
X	X	L	X	L	L	X	L
X	X	X	L	L	L	L	L
All other combinations							H

FUNCTION TABLE FOR $\overline{P}$ OUTPUT

INPUTS				OUTPUT
$\overline{P3}$	$\overline{P2}$	$\overline{P1}$	$\overline{P0}$	$\overline{P}$
L	L	L	L	L
All other combinations				H

FUNCTION TABLE FOR C_{n+x} OUTPUT

INPUTS			OUTPUT
$\overline{G0}$	$\overline{P0}$	C_n	C_{n+x}
L	X	X	H
X	L	H	H
All other combinations			L

FUNCTION TABLE FOR C_{n+y} OUTPUT

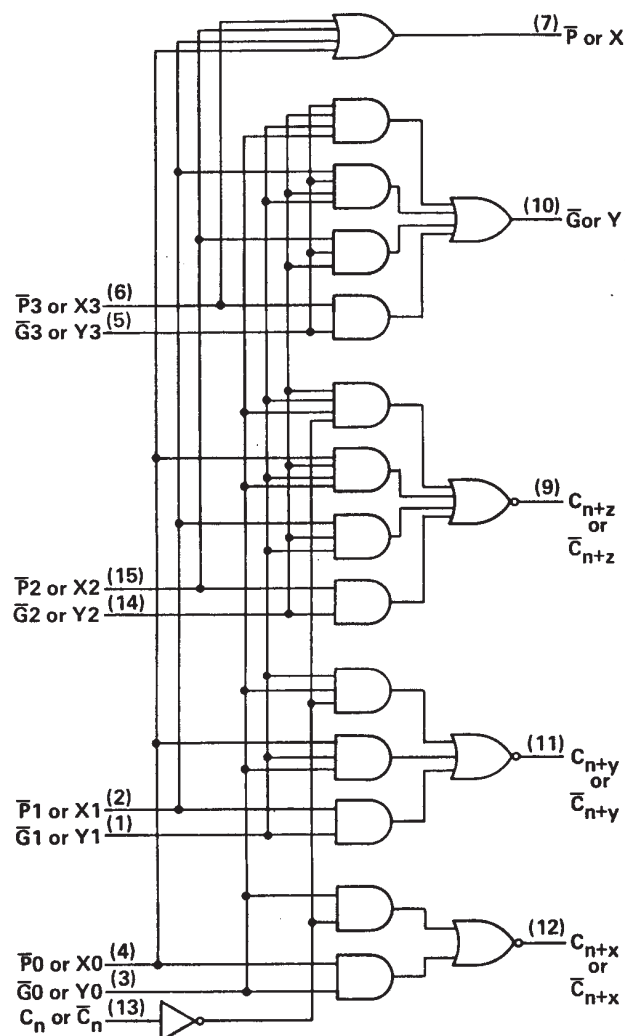| INPUTS					OUTPUT
$\overline{G1}$	$\overline{G0}$	$\overline{P1}$	$\overline{P0}$	C_n	C_{n+y}
L	X	X	X	X	H
X	L	L	X	X	H
X	X	L	L	H	H
All other combinations					L

FUNCTION TABLE FOR C_{n+z} OUTPUT

INPUTS							OUTPUT
$\overline{G2}$	$\overline{G1}$	$\overline{G0}$	$\overline{P2}$	$\overline{P1}$	$\overline{P0}$	C_n	C_{n+z}
L	X	X	X	X	X	X	H
X	L	X	L	X	X	X	H
X	X	L	L	L	X	X	H
X	X	X	L	L	L	H	H
All other combinations							L

H = high level, L = low level, X = irrelevant
Any inputs not shown in a given table are irrelevant with respect to that output.
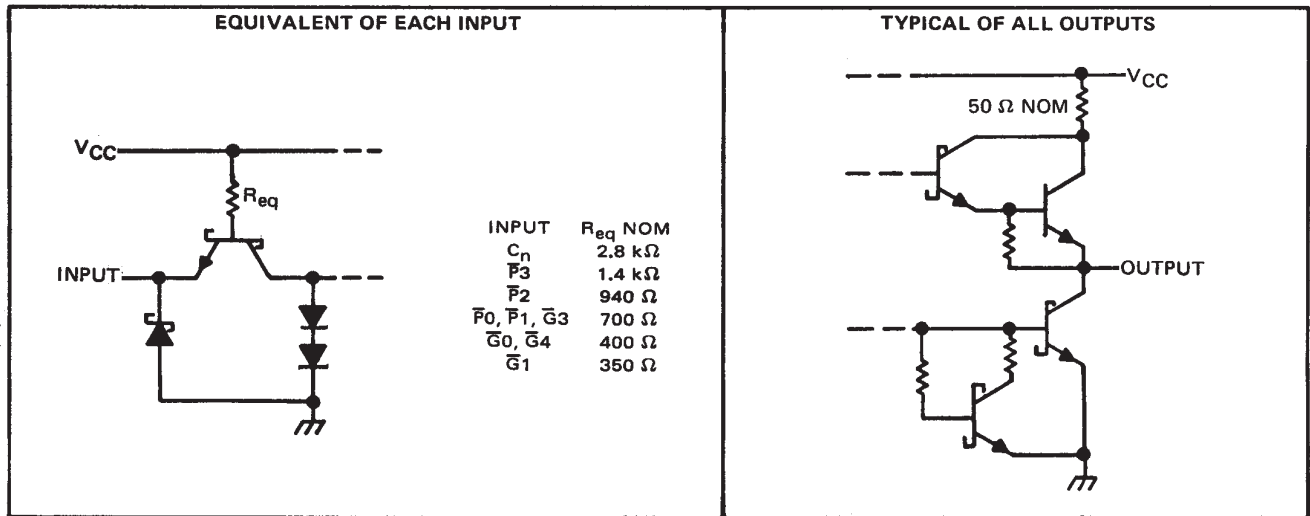
logic diagram (positive logic)

Pin numbers shown are for D, J, N, and W packages.

schematics of inputs and outputs

EQUIVALENT OF EACH INPUT	TYPICAL OF ALL OUTPUTS

INPUT	R_{eq} NOM
C_n	2.8 kΩ
$\overline{P}3$	1.4 kΩ
$\overline{P}2$	940 Ω
$\overline{P}0$, $\overline{P}1$, $\overline{G}3$	700 Ω
$\overline{G}0$, $\overline{G}4$	400 Ω
$\overline{G}1$	350 Ω

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Interemitter voltage (see Note 2)	5.5 V
Operating free-air temperature range: SN54S182	−55°C to 125°C
SN74S182	0°C to 70°C
Storage temperature range	−65°C to 150°C

NOTES: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter input transistor. For these circuits, this rating applies to each $\overline{G}$ input in conjunction with any other $\overline{G}$ input or in conjunction with any $\overline{P}$ input.

recommended operating conditions

	SN54S182			SN74S182			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−1			−1	mA
Low-level output current, I_{OL}			20			20	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS[†]	SN54S182			SN74S182			UNIT
			MIN	TYP[‡]	MAX	MIN	TYP[‡]	MAX	
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −18 mA			−1.2			−1.2	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −1 mA	2.5	3.4		2.7	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 20 mA			0.5			0.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V			1			1	mA
I_{IH} High-level input current	C_n input	V_{CC} = MAX, V_I = 2.7 V			50			50	μA
	$\overline{P3}$ input				100			100	
	$\overline{P2}$ input				150			150	
	$\overline{P0}$, $\overline{P1}$, or $\overline{G3}$ input				200			200	
	$\overline{G0}$ or $\overline{G2}$ input				350			350	
	$\overline{G1}$ input				400			400	
I_{IL} Low-level input current	C_n input	V_{CC} = MAX, V_I = 0.5 V			−2			−2	mA
	$\overline{P3}$ input				−4			−4	
	$\overline{P2}$ input				−6			−6	
	$\overline{P0}$, $\overline{P1}$, or $\overline{G3}$ input				−8			−8	
	$\overline{G0}$ or $\overline{G2}$ input				−14			−14	
	$\overline{G1}$ input				−16			−16	
I_{OS}	Short-circuit output current§	V_{CC} = MAX	−40		−100	−40		−100	mA
I_{CCH}	Supply current, all outputs high	V_{CC} = 5 V, See Note 3		35	65		35	70	mA
I_{CCL}	Supply current, all outputs low	V_{CC} = MAX, See Note 4		69	99		69	109	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time and duration of the short-circuit test should not exceed one second.
NOTES: 3. I_{CCH} is measured with all outputs open, inputs $\overline{P3}$ and $\overline{G3}$ at 4.5 V, and all other inputs grounded. MAX is determined at 5.5 V.
   4. I_{CCL} is measured with all outputs open; inputs $\overline{G0}$, $\overline{G1}$, and $\overline{G2}$ at 4.5 V; and all other inputs grounded.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	$\overline{G0}$, $\overline{G1}$, $\overline{G2}$, $\overline{G3}$, P0, P1, P2, or P3	C_{n+x}, C_{n+y}, or C_{n+z}			4.5	7	ns
t_{PHL}					4.5	7	
t_{PLH}	$\overline{G0}$, $\overline{G1}$, $\overline{G2}$, $\overline{G3}$, P1, P2, or P3	$\overline{G}$	R_L = 280 Ω, C_L = 15 pF, See Note 5		5	7.5	ns
t_{PHL}					7	10.5	
t_{PLH}	$\overline{P0}$, $\overline{P1}$, $\overline{P2}$, or $\overline{P3}$	$\overline{P}$			4.5	6.5	ns
t_{PHL}					6.5	10	
t_{PLH}	C_n	C_{n+x}, C_{n+y}, or C_{n+z}			6.5	10	ns
t_{PHL}					7	10.5	

NOTE 5: Load circuits and voltage waveforms are shown in Section 1.

TYPICAL APPLICATION DATA
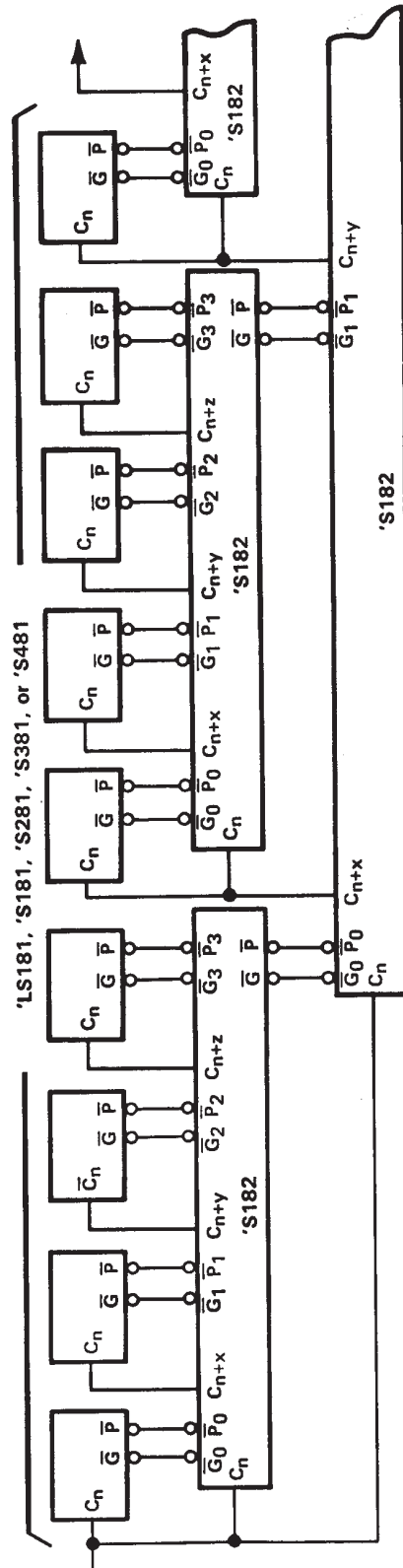
64-BIT ALU, FULL-CARRY LOOK-AHEAD IN THREE LEVELS

Remaining inputs and outputs of 'LS181, 'S181, 'S281, 'S381, and 'S481 are not shown.

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
JM38510/07802BEA	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 07802BEA
JM38510/07802BEA.A	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 07802BEA
M38510/07802BEA	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 07802BEA
SN54S182J	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54S182J
SN54S182J.A	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54S182J
SNJ54S182FK	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SNJ54S 182FK
SNJ54S182FK.A	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SNJ54S 182FK
SNJ54S182J	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SNJ54S182J
SNJ54S182J.A	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SNJ54S182J

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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PACKAGE MATERIALS INFORMATION

TUBE

T - Tube height

L - Tube length

W - Tube width

B - Alignment groove width

*All dimensions are nominal

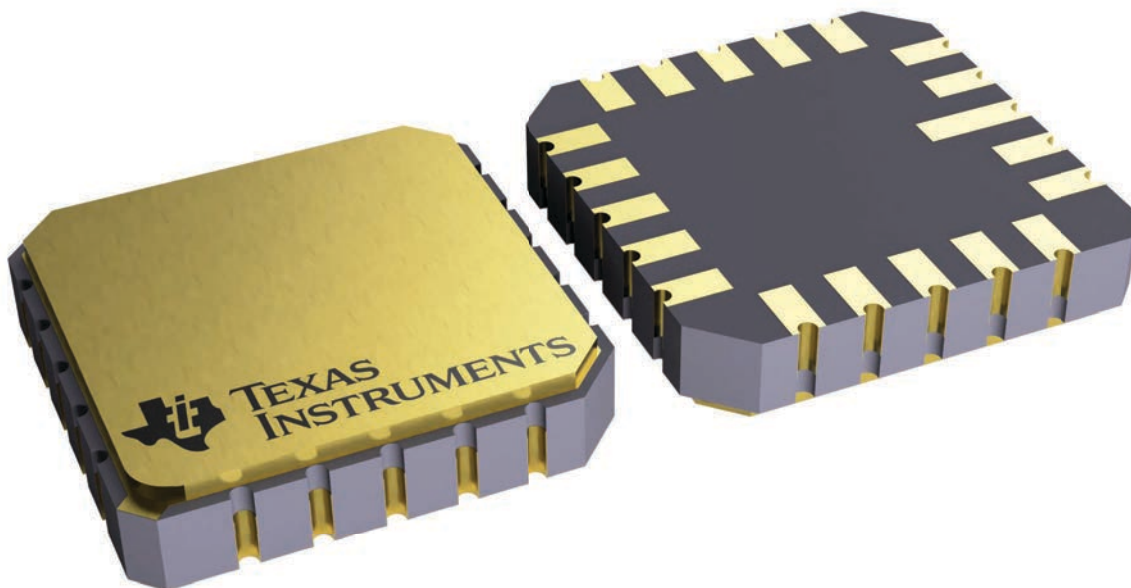| Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SNJ54S182FK	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54S182FK.A	FK	LCCC	20	55	506.98	12.06	2030	NA

FK 20

8.89 x 8.89, 1.27 mm pitch

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4229370VA\

J (R-GDIP-T**)   CERAMIC DUAL IN-LINE PACKAGE
14 LEADS SHOWN

DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

B

14   8

1   7

0.065 (1,65)
0.045 (1,14)

C

0.005 (0,13) MIN

0.060 (1,52)
0.015 (0,38)

0.200 (5,08) MAX

A

Seating Plane

0.130 (3,30) MIN

0.026 (0,66)
0.014 (0,36)

0.100 (2,54)

0°-15°

0.014 (0,36)
0.008 (0,20)

4040083/F 03/03

NOTES: A. All linear dimensions are in inches (millimeters).
         B. This drawing is subject to change without notice.
         C. This package is hermetically sealed with a ceramic lid using glass frit.
         D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
         E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

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