Design of a 10-bit 1.2 GS/s Digital-to-Analog Converter in 90 nm CMOS

A thesis submitted in partial fulfillment
of the requirements for the degree of
Master of Science in Engineering

by

Tyler J. Moody
B.S.E.E., Wright State University, 2013

2015
Wright State University

Wright State University
SCHOOL OF GRADUATE STUDIES

August 18, 2015

I HEREBY RECOMMEND THAT THE THESIS PREPARED UNDER MY SUPERVISION BY Tyler J. Moody ENTITLED Design of a 10-bit 1.2 GS/s Digital-to-Analog Converter in 90 nm CMOS BE ACCEPTED IN PARTIAL FULFILLMENT OF THE REQUIREMENTS FOR THE DEGREE OF Master of Science in Engineering.

Saiyu Ren, Ph.D
Thesis Director

Brian D. Rigling, Ph.D.
Chair, Department of Electrical Engineering

Committee on
Final Examination

Saiyu Ren, Ph.D

Raymond E. Siferd, Ph.D

John M. Emmert, Ph.D

Robert E. W. Fyffe, Ph.D.
Vice President for Research and
Dean of the Graduate School

ABSTRACT

Moody, Tyler. M.S.Egr., Department of Electrical Engineering, Wright State University, 2015. *Design of a 10-bit 1.2 GS/s Digital-to-Analog Converter in 90 nm CMOS.*

Digital analog converters bridge the gap between digital signal processing chips, and power amplifiers that transmit analog signals. Communications systems require ever increasing bandwidth, however data converters are typically the bottleneck in these systems. This thesis presents the design of a high speed current steering DAC using CMOS 90 nm technology. The resolution of the converter is 10 bits, segmented into 6 thermometer encoded MSB current cells, and 4 binary weighted LSB current cells. Each of the sub-components, such as the binary-thermometer encoder, digital latch, current cell, reconstruction filter, are discussed in detail. The current cells were designed with transistor matching, and output impedance effects in mind to achieve high performance. The DNL of the converter was measured to be 0.02 LSB, while the INL is 0.29 LSB. With a clock frequency of 1.2 GHz, the SFDR was measured to be 72.07 dB with an input of 596.48 MHz.

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Acknowledgment

I would like to take this opportunity to extend my thanks to my family and friends for constantly giving me words of encouragement. Secondly, I would like to thank my advisor, Dr. Saiyu Ren, for her support and enthusiasm towards my work. Finally, I would like to thank Dr. Raymond Siferd, and Dr. Marty Emmert for being on my committee, and for mentoring me throughout my graduate studies.

Dedicated to

My family and friends.

Introduction

1.1 DAC Overview

Data converters are one of the most important circuits in electronic systems. The purpose of data converters is to bridge the gap between the analog and digital world. An example of a radio frequency transceiver can be seen in Fig. 1.1. The antenna receives a radio signal which is amplified using a low noise amplifier. An analog to digital converter (ADC) takes the analog signal from the low noise amplifier and converts it to a digital signal. This digital signal, made up of N binary bits, is sent to a digital signal processor where the signal can be manipulated as needed. The converse of this is the digital to analog converter (DAC). The digital output from the signal processor is sent to the DAC in order to be converted back to an analog signal. Finally, the analog output is amplified using a power amplifier and transmitted through an antenna.

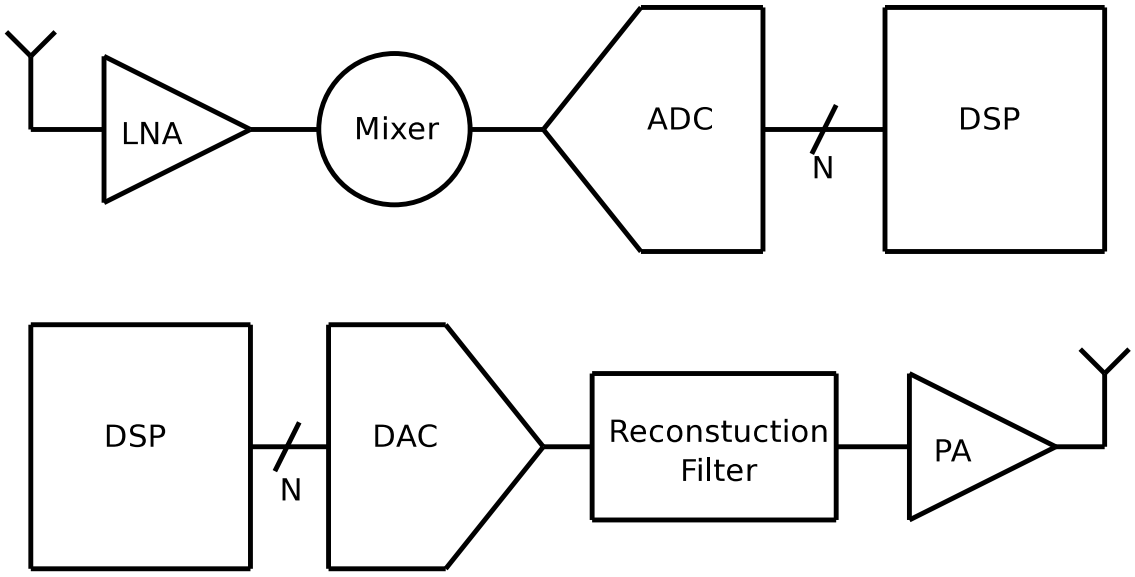

Figure 1.1: Block diagram of the RF transceiver.

The performance of these data converters often prove to be the bottleneck in electronic systems. With the growing demand for high bandwidth communications, it is important to develop high speed converters. Great care is needed to design a data converter that is fast, accurate, consumes little power, and takes up minimum area. Historically high speed data converters were implemented using technologies such as SiGe or GaAs [1][2]. The downside to these technologies is that they are expensive to manufacture, consume large amounts of power, and can not be integrated on the same chip as traditional CMOS DSP. To counter these trade offs, research has been done to implement high bandwidth converters using standard CMOS technologies.

Digital to analog converters work by taking the binary word, and outputting a reference voltage. For each binary code, a corresponding reference voltage exists. These reference voltages create a pulse amplitude modulated signal that has a staircase-like pattern. The number of binary inputs the DAC receives is known as the resolution. A DAC with a resolution of N will need to produce 2^N reference voltages. The binary word input

D of the DAC can be characterized as

$$D = \sum_{m=0}^{N-1} 2^m (b_m) \tag{1.1}$$

where m is the index of the binary word, and b is the '1' or '0' value of the bit at that index. Many DAC architectures work by having a reference voltage that is divided into smaller references that correspond to the digital input. With this reference voltage V_{ref}, the analog output at any given digital input can be determined by

$$v_{out} = V_{ref} \left(\frac{D}{2^N} \right) \tag{1.2}$$

The least significant bit (LSB) is the bit b_0 in the digital word. In converters, the term one LSB is often associated with the minimum step size in the analog output. The LSB can be defined as

$$LSB = \frac{V_{ref}}{2^N} \tag{1.3}$$

Since the minimum analog output voltage corresponds with the digital word consisting of all '0', the maximum analog output voltage will be one LSB less than V_{ref}. The range from the minimum output voltage to the maximum is known as the full scale range. The full scale voltage V_{FS} can be written as

$$V_{FS} = \frac{2^N - 1}{2^N} \cdot V_{ref} \tag{1.4}$$

The output of the DAC can be described as a series of rectangular functions. This is caused by the DAC acting as a sample hold, holding the output level for $\frac{1}{f_s}$, where f_s is the sampling frequency [3]. The rectangular pulse in time domain will form the function $\frac{\sin x}{x}$, known as the sinc function, in the frequency domain. The frequency response characteristic

of the DAC output can be written as

$$|H(2\pi f_{in})| = \frac{1}{f_s} \frac{\sin \frac{\pi f_{in}}{f_s}}{\pi \frac{f_{in}}{f_s}} \tag{1.5}$$

This output characteristic is known as sinc weighting [4], which can be problematic for the converter. The roll-off caused by the sinc weighting causes the amplitude of the output to be attenuated as the signal frequency increases. By inserting values for the sampling frequency and input frequency into equation 1.5, the reduction of signal power from the sinc weighting can be found. At the Nyquist frequency the output is attenuated by 3.92 dB, the output decreases to zero at the sampling frequency. Oversampling the converter, or using special filters can compensate for the sinc roll-off.

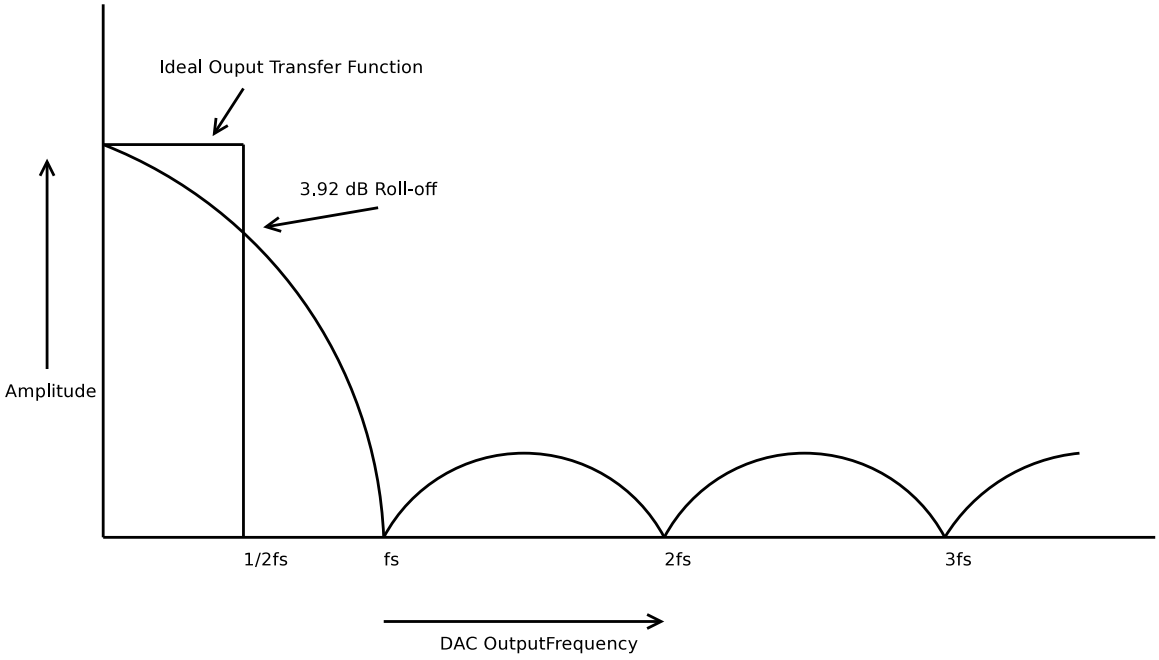

Figure 1.2: Sinc weighted output transfer function.

Another issue associated with the rectangular pulse output is the creation of signal aliases [4]. Ideally, the DAC bandwidth would be limited to less than the Nyquist frequency. However, high frequency distortion components caused by the output pulses will surpass

the Nyquist frequency and produce images. If the input signal is much less than the Nyquist frequency, the sinc function will attenuate the images. This technique is impractical since much of the bandwidth of the converter can not be utilized.

To suppress the images, a low pass anti-aliasing filter is used on the DAC output. This filter is also known as a reconstruction filter because it smooths the rectangular output into a smooth sine-like output. In order to maximize the converter bandwidth, the reconstruction filter needs a very sharp response. An ideal reconstruction filter would have a brick wall response [4], attenuating everything passed the Nyquist frequency. In practice, a brick wall filter cannot be designed. Designing a filter with a large amount of attenuation in a short transition band requires an analog filter consisting of many orders. High order filters add complexity and increase the area of the design. Increasing the transition band of the filter reduces the filter complexity, but the bandwidth of the DAC will be sacrificed.

1.2 DAC Architectures

There are many different architectures to convert digital signals to an analog output. Choosing the appropriate architecture depends on the application of the converter. Requirements such as area, power, bandwidth, accuracy must be considered. Generally DACs are subset into high bandwidth or high resolution. As the operating speeds increase, it becomes harder to design a high resolution DAC.

Some DAC architectures are simple, consisting of only a few switches and resistors. However, these DACs are limited in speed, resolution, and suffer from device mismatch error. These architectures were improved and techniques were devised to mitigate poor performance. Examples of these techniques include dynamic element matching (DEM) that improves accuracy, and the use of different coding schemes such as thermometer encoding.

Digital to analog converters can be categorized based on two bandwidth and sampling criteria [5]. The first category is the Nyquist rate converter, where the DAC operates be-

tween DC and the Nyquist frequency. In practice it is very difficult for the converter to operate at the Nyquist frequency because the design of the necessary anti-aliasing filter would require infinite filter orders. Most converters operate at a bandwidth that is less than the Nyquist frequency. This is the second category, known as an oversampling DAC. With the bandwidth set to a fraction of the sampling rate, the reconstruction filter can more easily be implemented. The oversampling converter concept can be extended by adding noise shaping circuits to increase the output resolution.

The main building block in every DAC is a component that creates an appropriate analog output level by dividing a reference voltage. Elements such as resistors split the reference voltage into smaller voltage or current levels. Transistor current sources can also create output currents that are converted to the analog output voltage by the load resistors. Capacitors are also used in some architectures to store charge from the reference voltage and discharge it to the output.

1.2.1 Resistor String DAC

The simplest DAC architecture is the resistor string [5] as seen in Fig. 1.3. It is made up of 2^N resistors in series, each resistor corresponding to one LSB. A reference voltage is connected at one end of the resistor string, and ground at the other. Switches are connected after each resistor, the output of each switch is tied together to form the DAC output. The digital input must go through a $N : 2^N$ encoder, which then enables or disables the switches. When the switch is enabled, a voltage division of the reference occurs which becomes the analog output.

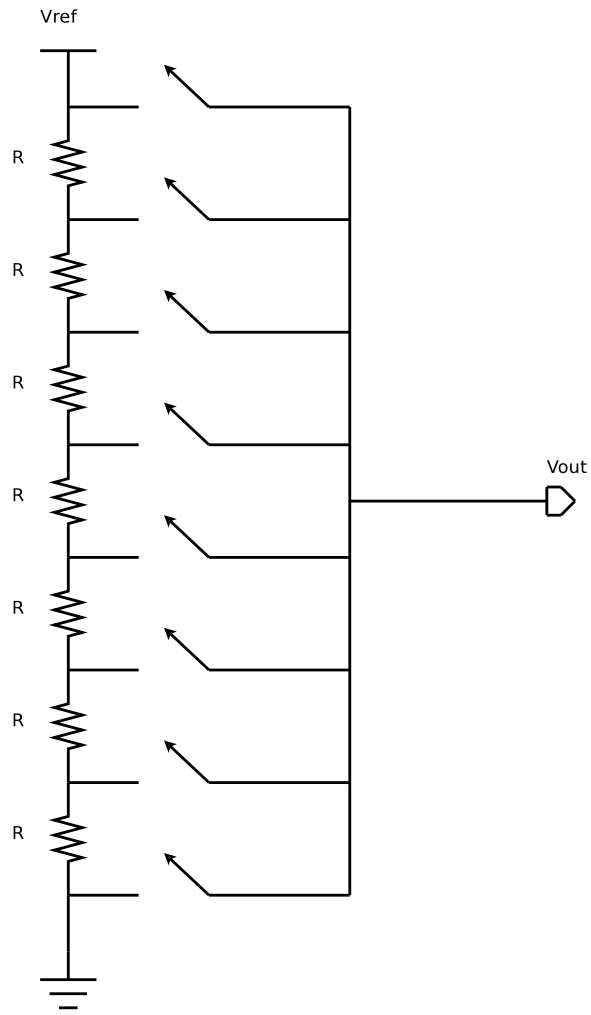

Figure 1.3: Resistor string architecture.

The advantage of the resistor string DAC is that it is simple, and is guaranteed to be monotonic. The disadvantage of the resistor string DAC is the large number of resistors needed for higher resolution converters. These resistors take up a large amount of area, and can be difficult to match properly leading to linearity errors. Since there are many switches connected to the output in parallel, parasitic capacitance can limit the speed of the converter.

1.2.2 Binary Weighted Resistor Ladder DAC

The binary weighted resistor DAC shown in Fig. 1.4 is built using a resistor ladder network consisting of N resistors. The MSB resistor has a resistance of R, the resistor value will increase by two for each descending bit. Each resistor is connected to a switch that is controlled by the digital input. The output of the switches are all connected to an op amp. A reference voltage connected to the resistor ladder allows current to flow through the resistors to ground, or the virtual ground in the op amp to form the output.

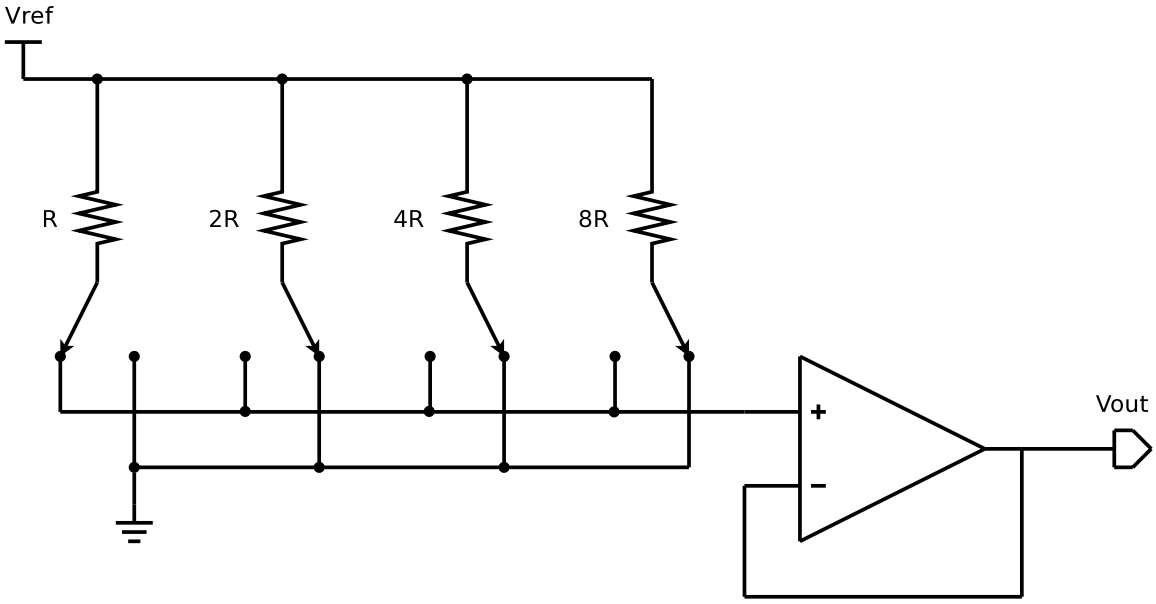

Figure 1.4: Binary weighted resistor architecture.

The problem with this architecture is that in higher resolution designs, the difference in resistor values becomes large. Process variation in fabrication makes matching of resistors difficult. If the MSB resistance is off by 1% in an 8 bit DAC of this design, an error of more than one LSB will occur.

1.2.3 R-2R DAC

The R-2R is an improvement on the binary weighted resistor architecture in that it only uses resistors of two different resistances. A resistor ladder is formed by having a series of resistors of value R, then rungs of resistors of value 2R. Depending on how the reference voltage is arranged, the R-2R can be described as being in voltage mode or current mode. In voltage mode, the the switches switch between V_{ref} and ground. The output is taken at the end of the resistor network. Current mode is shown in Fig. 1.5. It works by having the switches switch between the output and ground, while the reference voltage is connected to the resistor ladder.

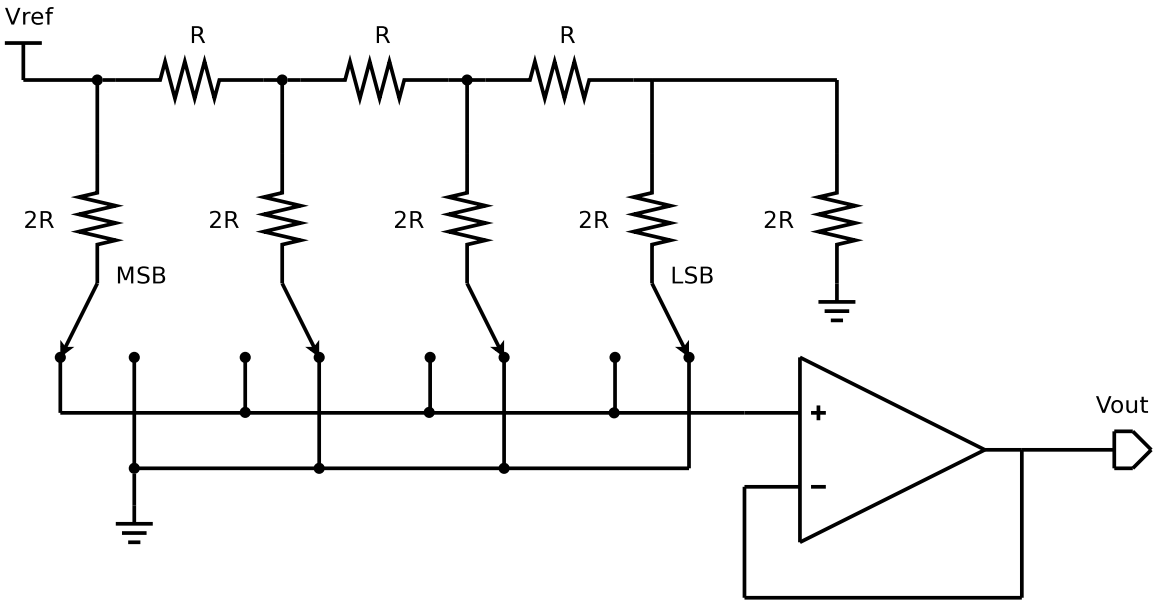

Figure 1.5: R-2R architecture.

The advantage of the R-2R DAC is that it only requires $2N$ resistors, and only two resistor values. The output impedance for this design is always constant. This is because the equivalent resistance on each side of the ladder rung is 2R. Resistor mismatch is still an issue when designing a high resolution converter. Often times current source transistors are used in conjunction with the resistor ladder network to further increase linearity. The current mode R-2R DAC must use an operational amplifier to switch the reference voltage

between ground and virtual ground. The op amp output buffer can affect the performance of the DAC by limiting the bandwidth, and causing linearity errors. When implementing the voltage mode R-2R, the switches must operate from ground to V_{ref}, which can be difficult to design. For current mode, glitches can appear at the output since the switches are directly attached to the output node.

1.2.4 Charge Scaling DAC

The charge scaling DAC is similar to the resistor based architectures, except capacitors are used instead. The converter can be implemented in a binary weighted fashion, or using a C-2C network as seen in Fig. 1.6. One difference with the charge scaling architecture is the need for a reset switch that discharges all the capacitors between each conversion.

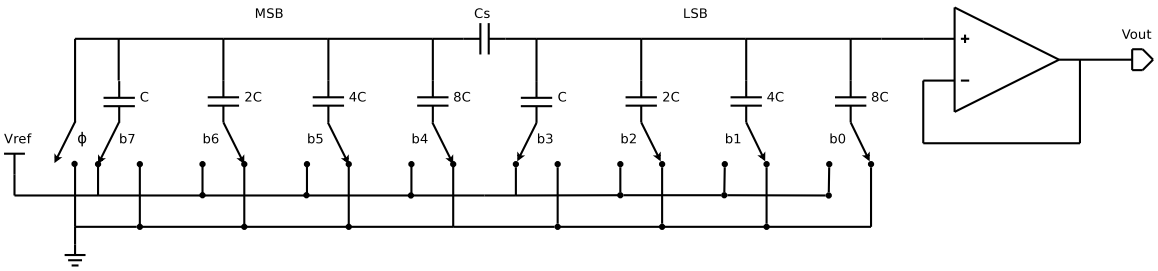

Figure 1.6: Charge scaling architecture.

With the emergence of sub-micron CMOS technologies, capacitors can be fabricated that take up less area than resistors [5]. In high resolution binary weighted designs, the capacitor sizes for the MSBs can be prohibitively large. A technique known as a split array can be used to keep the area down [6]. This works by adding an attenuation capacitor in the capacitor ladder to separate the MSBs and LSBs. The attenuation capacitor in parallel with the LSB array must equal the first capacitor in the MSB array in order to properly terminate the capacitor array. The series capacitance of the LSB capacitors from 0 to k, plus the terminating capacitor, is denoted as C_{array}. The first capacitor in the MSB array can be written as C_{k+1}. Now the attenuation capacitor C_s can be solved for by using

equation 1.6.

$$\frac{1}{C_{k+1}} = \frac{1}{\frac{1}{(C_s)} + \frac{1}{(C_{array})}} \tag{1.6}$$

The charge scaling converter is popular because it is fast, accurate, and easily implemented in CMOS. The disadvantage of the architecture is that it requires an op amp which can limit performance. Parasitic loading of the capacitors from the op amp can limit the resolution of the converter [3], this can be solved by using a switched capacitor integrator. This design also suffers from charge feedthrough errors in the output.

1.2.5 Current Steering

The current steering DAC is the preferred architecture for high bandwidth converters [7]. This architecture is shown in Fig. 1.7. It works by summing the current produced by an array of current sources. A load resistor is connected to the output of the current sources on one end, and the supply voltage at the other. When the current source is enabled, current flows through the load resistor. This current is sinked by the current source, thereby converting the current into a voltage. The output voltage is formed from the voltage division between the power supply connected to the resistor, and the voltage drop produced by the current draw from the current sources. Since an op amp is not required to form the output voltage, higher performance can be achieved.

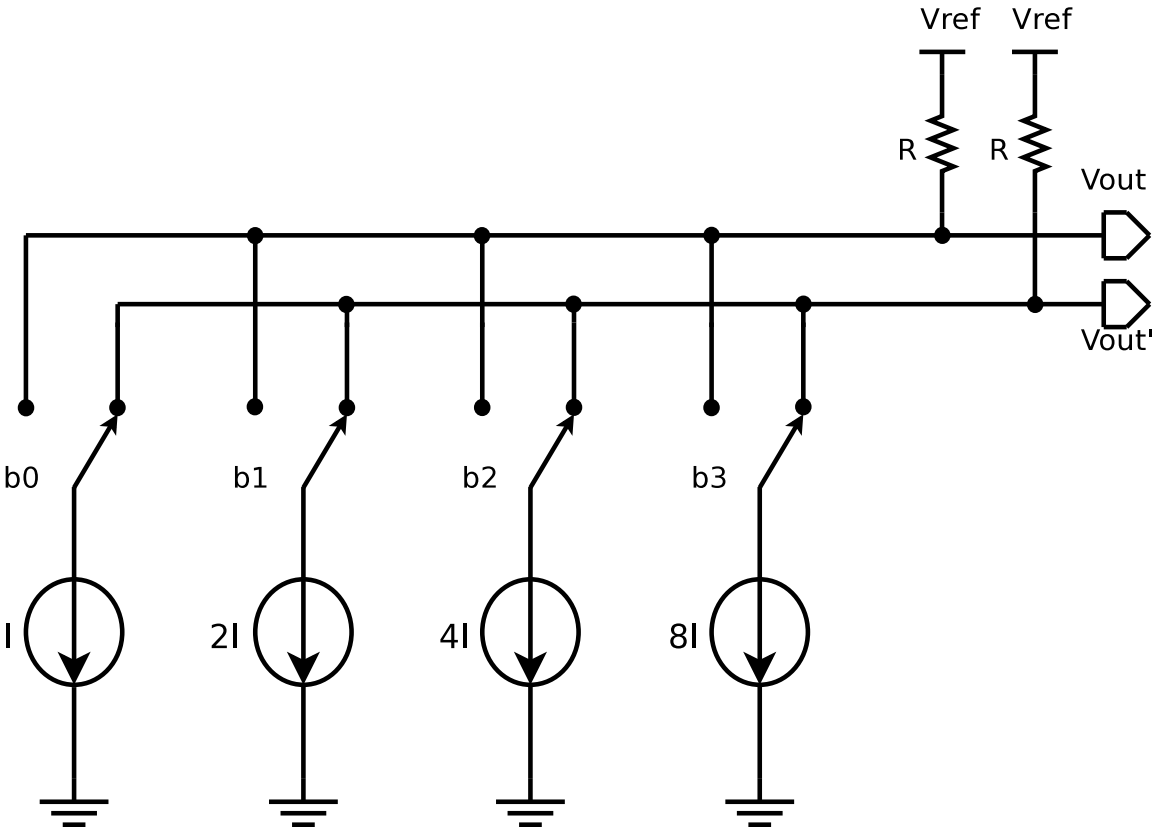

Figure 1.7: Current steering architecture.

A binary weighted current steering DAC can easily be implemented, only N number of current sources and switches are needed. The problem with the binary weighted design is that a large glitch can occur at the output when several current sources are being switched at once [8]. For example, when the MSB current source switches on, all the other current sources will be turning off. If the MSB current source does not reach its final value before the other sources switch off, then a glitch will occur.

A method to reduce glitches is to use unary weighted current sources, every current cell produces a unit current of I. In this design, the LSB will consist of a single unary current cell, the MSB will be comprised of 2^{N-1} current sources. In order to send the correct control signals to the unary current cells, a binary to thermometer encoder is used. Thermometer coding is preferred over binary because only one bit switches at a time, eliminating the MSB current source glitch. The difference between binary and thermometer

Table 1.1: Binary vs. Thermometer Code

Decimal	Binary	Thermometer
0	000	0000000
1	001	0000001
2	010	0000011
3	011	0000111
4	100	0001111
5	101	0011111
6	110	0111111
7	111	1111111

code can be seen in Table 1.1.

In theory, a thermometer encoded current steering DAC should provide higher speed than the binary weighted design. As resolutions surpass 10 bits, the amount of current sources required becomes very large. This is an issue since all of these cells will consume a large amount of area. The routing required to control thousands of current cells introduces a large amount of parasitic capacitance that will limit the speed of the converter. The thermometer coded design also requires the thermometer encoder which adds complexity, and increases power consumption from the logic gates.

A trade off between high speed, and reduced area and complexity is the segmented design. In a segmented design, the most significant bits of the converter are implemented using thermometer coding, while the least significant bits are binary weighted. The optimal ratio between binary weighted bits and thermometer coded bits must be determined before designing the converter. From the work in [9], the amount of segmentation for a 10 bit DAC should be approximately 30-70%, where 0% is fully binary and 100% is unary. To optimize area and obtain the best INL, the segmentation should be close to 70%.

1.2.6 Sigma-Delta

Sigma-Delta (also referred to as delta-sigma) use oversampling and noise shaping to obtain a high resolution converter. The required components are a Nyquist rate DAC, an interpolator, a Σ-Δ modulator, and an analog filter. Oversampling is when the bandwidth is limited to a fraction of of the sampling frequency; the ratio of the sampling frequency over the bandwidth is the oversampling ratio. An increase of half a bit of the output resolution can be obtained by doubling the oversampling ratio [7]. There is a practical limit on oversampling, attempting to increase the resolution by several bits becomes impractical. To increase the resolution without using a high oversampling ratio, the quantization noise of the DAC is shaped into higher frequencies.

The interpolator basically increases the frequency of the digital input to the oversampling frequency by placing zeros in the signal. The interpolation function adds images to the signal, so a digital filter is used to remove these images. The Σ-Δ modulator truncates the N bit input to create quantization noise. This noise is then shaped out of the signal bandwidth using high pass filters. The M bits output from the Σ-Δ modulator then go to a M bit Nyquist rate DAC. This DAC must have a linearity requirement than can handle the final output resolution of the oversampled DAC [5]. Since the range between the DAC bandwidth and sampling frequency is increased through the oversampling, the number of orders required on the output filter is reduced.

The Σ-Δ DAC offers high resolution, however the bandwidth is usually less than 100 MHz. With the low bandwidth, this converter is not suitable for RF bandwidth conversion. This architecture is often used for audio conversion, medium bandwidth applications, or applications requiring high resolution. An advantage with this architecture is that much of the modulation and filtering is done in the digital domain. This is preferred to doing complicated signal processing in the analog domain. It is difficult to design the M bit DAC because it must have the linearity of the final N bit output.

1.3 Non-Ideal DAC

In a non-ideal DAC, many errors will degrade the performance of the the converter. One of the errors found in digital to analog converters is component mismatch. When the circuit is fabricated, the components will not be the exact size, or have the same oxide thickness as designed. These process variations will cause mismatch in the resistors or transistors that create the analog output voltages, reducing accuracy. Special techniques have been developed for sizing components, arranging components in a layout, or adding special sub-circuits that mitigate the mismatch errors.

The second cause of degraded DAC performance comes from glitches in the output. Glitches can occur from charge feedthrough errors, or from timing skew from components within the DAC. Charge feedthrough happens when charge builds up between the drain and gate of a CMOS switch. When the switch changes state, the charge of this coupling capacitance is discharged to the output of the switch. Switches in converters have to be carefully designed to ensure charge feedthrough does not reduce the quality of the output. Timing skew causes switching components to change out of unison. In a DAC, the elements that produce the analog output need to switch at the same time, or else there will be a spike in the output.

When designing a current steering DAC, the finite output impedance of the current cells must be taken into consideration to maintain accuracy. The current cells are typically made up of transistors acting as current mirrors, with the drain of the current mirror connected to the DAC output. As the output voltage changes, the drain voltage on the current mirror will also change. Since the current mirror does not have infinite output impedance, the changing drain voltage will cause the reference current to vary. Adding an output buffer, or designing the current cells with increased output impedance in mind will ensure the cells produce an accurate reference.

1.4 Performance Metrics

The performance of a DAC can be expressed in terms of its static performance and dynamic performance. Static performance metrics analyze the accuracy of the converters output versus the expected output at a given code. Typically the input is swept to produce the full range of binary codes so the DAC output appears as the characteristic staircase plot. The voltage level at each code is measured to determine the accuracy. Measuring the performance this way provides good insight on how accurate the DAC is once the output settles, however the dynamic performance is more important. The dynamic accuracy of the DAC is measured by applying a sinusoidal input to an analog digital converter, which then supplies the DAC with the digital inputs. The DAC then reconstructs the sinusoid, then FFT analysis can be done to see how the DAC performs.

1.4.1 Static Linearity

The two main static performance metrics are the differential nonlinearity (DNL), and the integral nonlinearity (INL). Differential nonlinearity is the difference of the output level between two adjacent codes. Often times DNL is measured in terms of LSB, in an ideal case the difference between two codes will be 1 LSB. If the step between two adjacent codes are 1.25 LSB instead of 1 LSB, then the DNL is said to be $\frac{1}{4}$ LSB. In order to maintain sufficient accuracy, the DNL must be between $\pm\frac{1}{2}$. In order to guarantee the output is monotonically increasing, the DNL should never be greater than 1 LSB [10]. Non-monotonic behavior can produce large errors in the output. Some DAC architectures are designed in a way to guarantee monotonicity.

Integral nonlinearity is the measure of the the actual output voltage level minus the ideal level. One way to measure INL is to sweep the digital input and plot the analog output. A line is then drawn from zero and full scale, the the output deviation from this line is the INL. The INL per code can also be defined as the summation of the DNL from

each previous codes. As with DNL, the acceptable range of values for the INL is $\pm\frac{1}{2}$ LSB. In order to maintain monotonicity in the output, the INL must be be less than $\frac{1}{2}$ LSB for every code. An example of a DNL and INL error can be visualized in Fig. 1.8. In Fig. 1.9 the output transfer function of a DAC is shown with DNL and INL errors. The the error at code 010 shows a DNL of 1.5 LSB, which causes an INL of 1.5 LSB. At code 101 the DNL is -0.5 LSB and INL is -0.5 LSB.

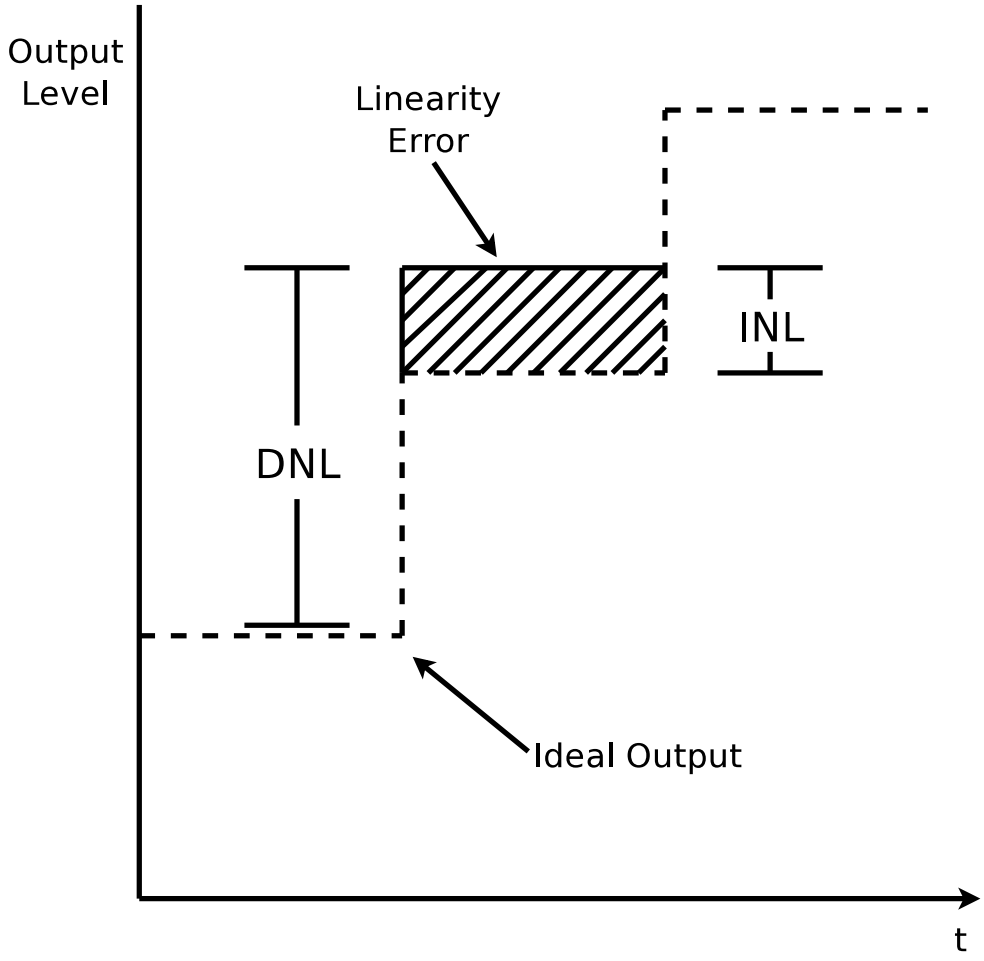

Figure 1.8: DAC output code with static linearity error.

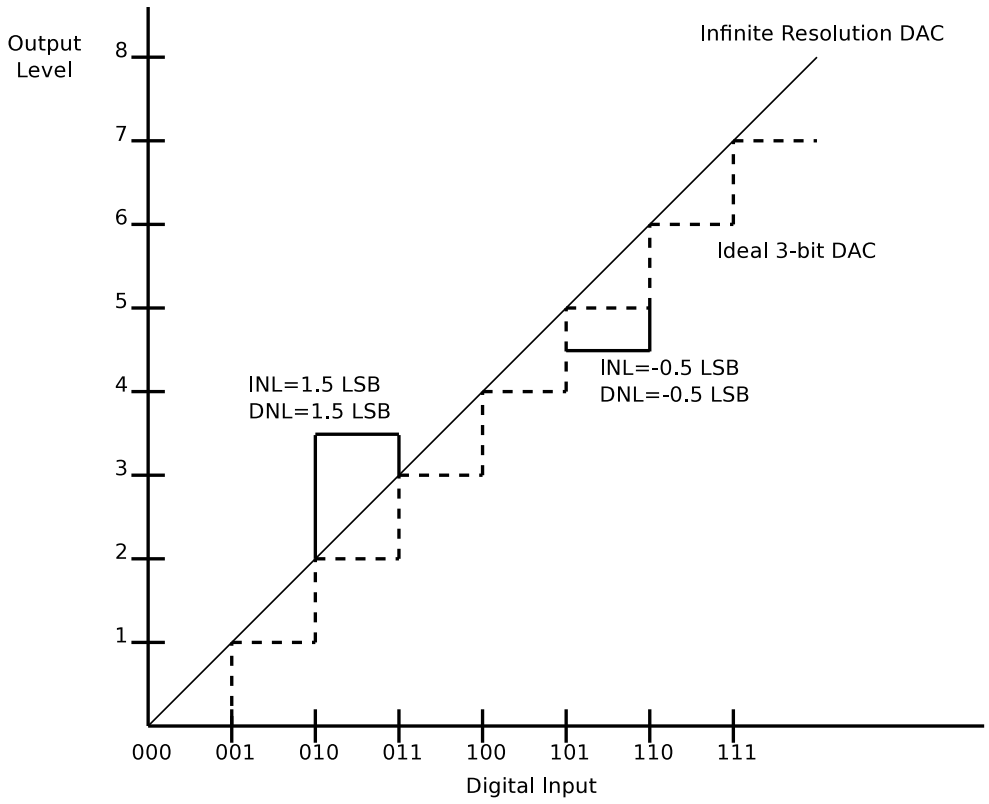

Figure 1.9: 3-bit DAC output with DNL and INL errors.

Other linearity issues associated with digital to analog converters are offset and gain errors. Offset error is when all output codes are uniformly increased by a DC voltage. This error usually does not impact the performance of the converter, but must be compensated when measuring the DNL and INL. Gain error is when the output varies from the ideal best fit line in a linear or non-linear fashion. A linear gain error will not affect the performance of the converter, however a non-linear gain will cause distortion.

1.4.2 Rise Time

The rise time of the converter is how long it takes the output to settle to certain percentage of the LSB [8]. The output can either move from zero to full scale, or in a binary weighted architecture it may be important to know the mid-scale settling time. When the input changes ,there is a delay before the output begins to rise. Once the output begins to

rise, the speed it rises depends on the slew rate of the converter. As the output reaches the final value there may be overshoot and ripple that will increase the settling time.

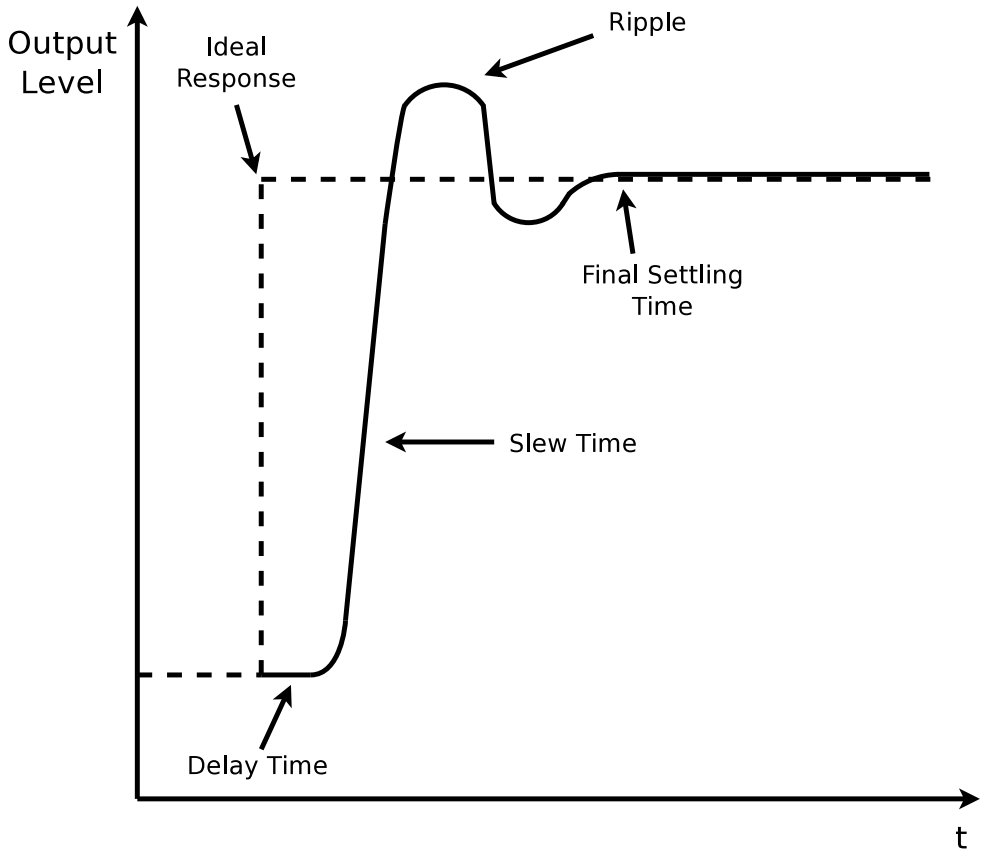

Figure 1.10: Rise time of a real DAC.

The overshoot, or undershoot in the rising output causes glitches. These glitches can occur from clock feedthrough, capacitance loading, or timing mismatch in the switching components [7]. The glitch energy can be estimated by approximating the glitch as a triangle, then taking the area. Special design techniques can be used to reduce the glitches in the DAC.

1.4.3 Signal to Noise Ratio

In real world applications, the dynamic measurements provide a better idea of how the converter performs. This is done by applying a full scale sinusoid with a set frequency to

the converter. For some communications applications, the converter may have to handle multiple-tone input. Special metrics such as intermodulation distortion can be used for these applications.

The first dynamic specification is the signal to noise ratio (SNR) of the DAC. The SNR is defined as the spectral power of the input compared to the noise floor. The input signal must be at full scale in order to measure the SNR. Smaller amplitude will reduce the SNR, which is intuitive since the signal to noise ratio is directly proportional to the input signal power. In the ideal case, the noise floor would only consist of the quantization noise produced by the converter. In practical converters, errors from linearity, glitches, clock skew, and output settling time will increase the noise floor. The RMS quantization error can be expressed as

$$Q_{RMS} = \frac{V_{LSB}}{\sqrt{12}} \tag{1.7}$$

which can be divided by the RMS value of the input signal to obtain the equation for SNR.

$$SNR_{dB} = \frac{\frac{2^N(V_{LSB})}{2\sqrt{2}}}{\frac{V_{LSB}}{\sqrt{12}}} \tag{1.8}$$

By simplifying equation 1.8, the ideal SNR for a N bit converter can be written as

$$SNR_{dB} = 6.02N + 1.76(dB) \tag{1.9}$$

It can be seen from this equation that for each bit of resolution, the DAC must provide an increase of about 6 dB signal to noise ratio.

1.4.4 Spurious Free Dynamic Range

One of the most important specifications for digital to analog converters is the spurious free dynamic range (SFDR). This is the measure of the fundamental signal versus the second

highest distortion component (spur). Typically in a DAC, the largest spur will either be the second or third order harmonics, or their aliases. The plot in Fig. 1.11 shows the fundamental signal and spurs consisting of harmonic distortion.

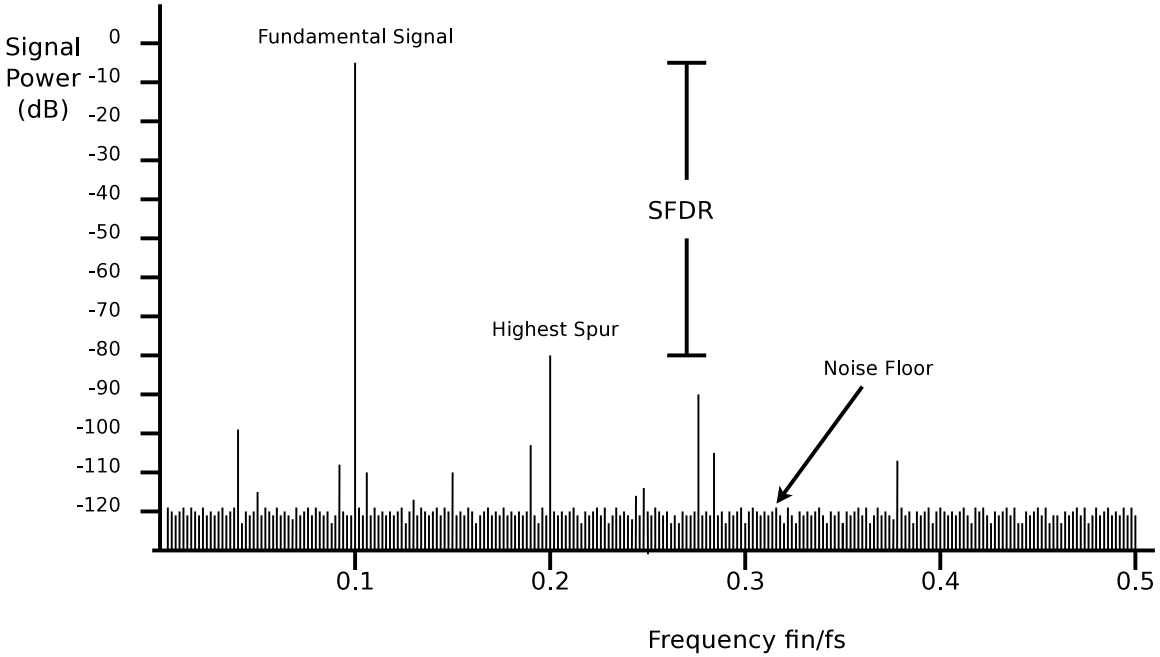

Figure 1.11: Example FFT plot with spurs.

As mentioned previously, the linearity can will impact the dynamic performance. The influence of INL error can be calculated to determine its effect on the SFDR [11]. This is only applicable to low frequencies, but helps estimate the SFDR before glitches and other errors factor in. An approximation of SFDR based on the the max INL can be written as

$$SFDR \approx 20Log\left(\frac{2^N}{INL_{max}}\right) \tag{1.10}$$

From the work in [5], it can be seen that the shape of the INL curve will determine which harmonic distortion order will dominate the SFDR. An arch shaped INL curve will cause the second order harmonic to be the dominant spur, while an 'S' shaped INL curve will cause the third order harmonic to be the highest spur.

1.4.5 Effective Number of Bits

The practical resolution of the converter will degrade at high frequencies. Since the DAC is not ideal, harmonics and distortion will be present, causing the reduced resolution. The effective number of bits (ENOB) is the measure of this reduced resolution. From the SNR equation, the ideal signal to noise ratio is determined from a given resolution. Working in reverse, the resolution is calculated by factoring in the distortion; replacing the SNR variable with the SFDR. By measuring the SFDR of the converter, the real resolution of the output can be determined using equation 1.11.

$$ENOB = \frac{SFDR - 1.76}{6.02} \tag{1.11}$$

1.5 Objective of This Thesis

The objective of this thesis is to design and implement a high speed digital to analog converter in CMOS 90 nm technology. To facilitate this, a current steering architecture is used to obtain a bandwidth in the several hundred megahertz. The design of the current cells in order to reach the required accuracy and speed is discussed. Finally, interleaving techniques are investigated to achieve even higher conversion speeds.

Current Steering DAC

2.1 Design Overview

To achieve high bandwidth, the current steering architecture was chosen. High resolution converters of greater than 12 bits have been implemented. However, increased resolution makes it more difficult to obtain high speeds. A 10 bit design was chosen to balance resolution and ease of achieving high bandwidth.

A block diagram of the current steering DAC is shown in Fig. 2.1. Two sub-DACs are used to segment the bits. The first four LSBs (B0, B1, B2, B3) are sent to a binary weighted sub-DAC. MSBs (B4-B9) are converted using a thermometer encoded sub-DAC. The MSB current cells are arranged in a matrix pattern. Since there are 6 MSB bits, there will be 63 current cells. These current cells are arranged in an 8x8 pattern. One binary to thermometer encoder is used to address the current cell matrix columns, while another encoder addresses the rows. The column encoder takes the binary bits B4, B5, and B6 and outputs the 8 bit thermometer control signals. The row decoder does the same, taking bits B7, B8, and B9. The Cadence schematic of the DAC is shown in Fig. 2.2.

Located in each current cell is a local decoder that receives the outputs of the thermometer encoders. The outputs of the local decoder is then sent to a latch, which drives the current switches. The differential current switches steer the current produced by the current sink between two differential outputs, I_{out} and $\overline{I_{out}}$. The current output of both sub-DACs are tied to each other. The output currents are converted to voltage through the

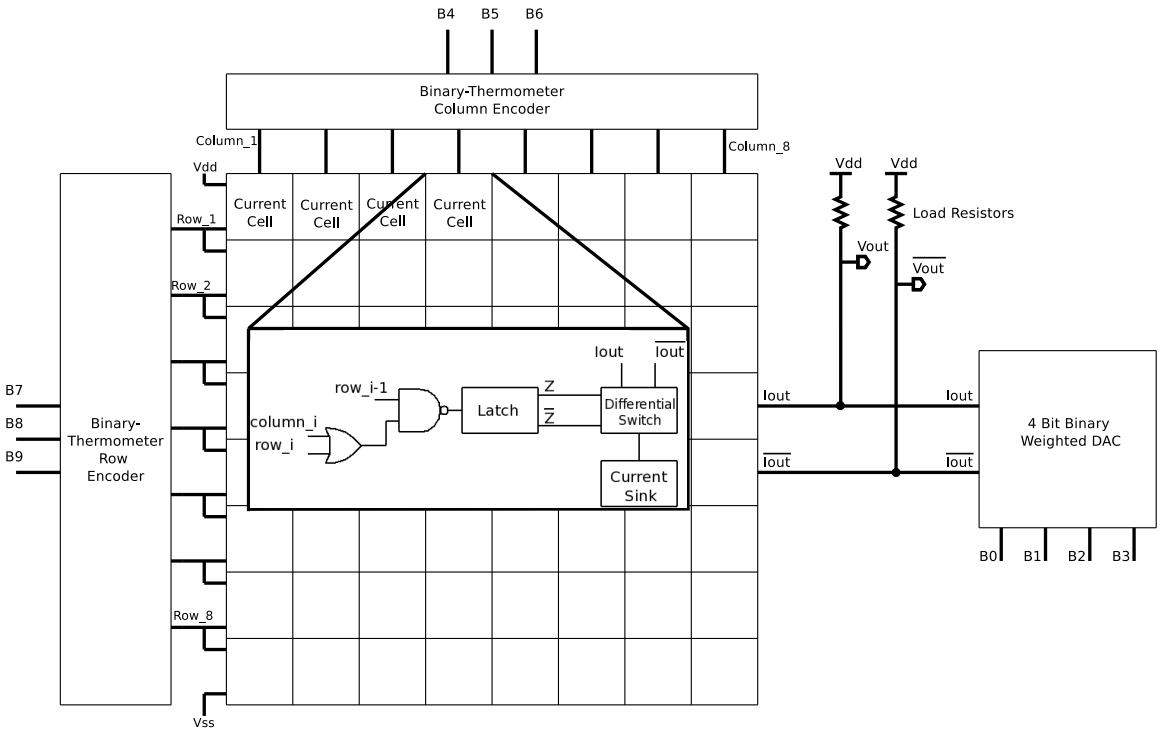

Figure 2.1: Block Diagram of current steering DAC.

load resistors. Each load resistor is connected to V_{dd} at one end, and all of the current cells at the other end. The final output voltage can be found by subtracting V_{dd} by the current sinked by the current cells over the load resistance, as seen in equation 1.2.

$$V_{out} = V_{dd} - \frac{I_{out}}{R_L} \tag{2.1}$$

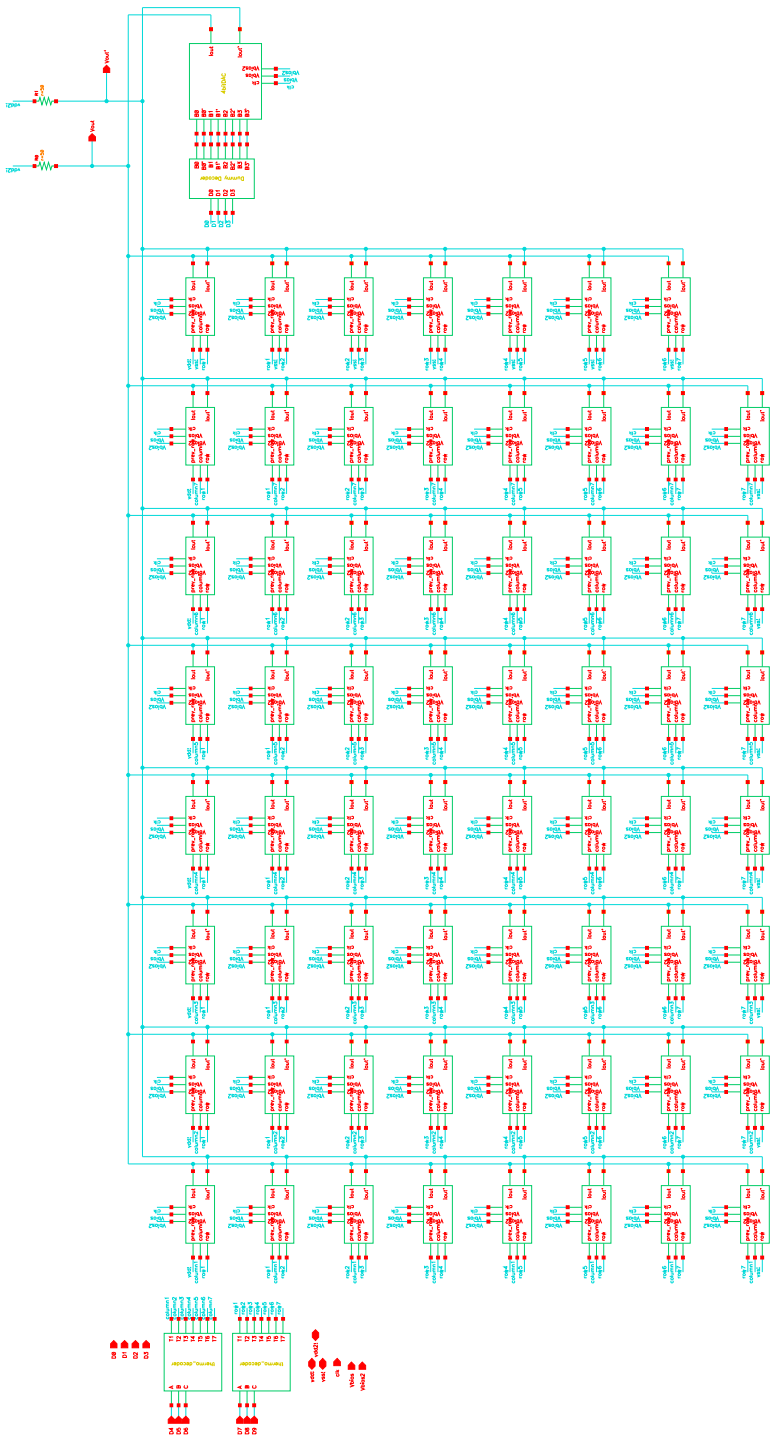

Figure 2.2: Cadence schematic implementation of the current steering DAC.

Usually a dummy decoder is placed between the LSB inputs and the binary weighted current cells. This is done to ensure the delays are the same between the LSB cells and the thermometer encoded cells. In this design, flip flops are used instead of latches in order to eliminate the need for the dummy decoder. This is because the digital input signals can arrive to the flip flops with clock skew, as long as they get there before the falling edge of the clock. At the falling edge of the clock, the digital values are held in the flip flop and output to the current cells.

The LSB sub-DAC is made up of four binary weighted current cells. The Cadence schematic of the LSB sub-DAC can be seen in Fig. 2.3. The binary weighted current cells produce a unit current of I for the least significant bit, followed by $2I$, $4I$, and $8I$. The MSB array is made up of current cells that produce current of $16I$. The full scale output voltage was set to be 500 mV. With the 50 Ω load resistors, the full scale current is 10 mA. By dividing the full scale current by 2^{1024} the LSB current is 9.76 μA. The rest of the current cells produce currents of 19.53 μA, 39.06 μA, 78.12 μA, 156.25 μA.

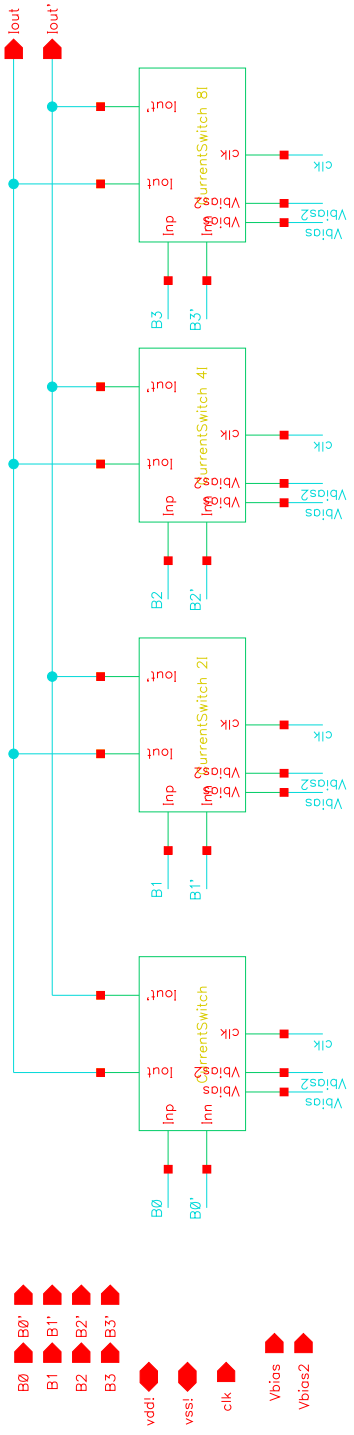

Figure 2.3: Cadence schematic implementation of the four bit sub-DAC.

2.2 Digital Sub-circuits

2.2.1 Thermometer Encoder

The thermometer encoder can be implemented in a 1-D, or 2-D way [12]. The one dimensional design uses a single encoder to convert the binary bits and address each current cell. The two dimensional encoder allows the current cells to be arranged in a matrix. Two encoders are required to address the rows and columns in the current cell matrix. The advantage of using the 2-D design is that the complexity of the thermometer encoder can be reduced, which is why this method was chosen.

The encoders must be carefully designed to achieve high speed and low power. The logic for the encoders are easily obtained by doing a Karnaugh map for each thermometer output, a list of the Boolean equations can be seen in table 2.1. In the equations, A is the MSB bit, so it would map to the binary input $B6$ for the column encoder. The variable B would map to $B5$, and so on. By rearranging the equations using inverted inputs, it can be seen that a NAND and NOR function occurs on the first two bits. The outputs from this first level of logic then gets input to either a NAND or NOR, along with the third binary input to form the output. The design in [12] presents an iterative approach for creating the thermometer encoder. For each additional binary input, another row of NAND and NOR

Table 2.1: Thermometer Encoder Output Equations

Encoder Output	Equation
T1	$A + B + C$
T2	$A + B$
T3	$A + (B \cdot C)$
T4	A
T5	$A \cdot (B + C)$
T6	$A \cdot B$
T7	$A \cdot B \cdot C$

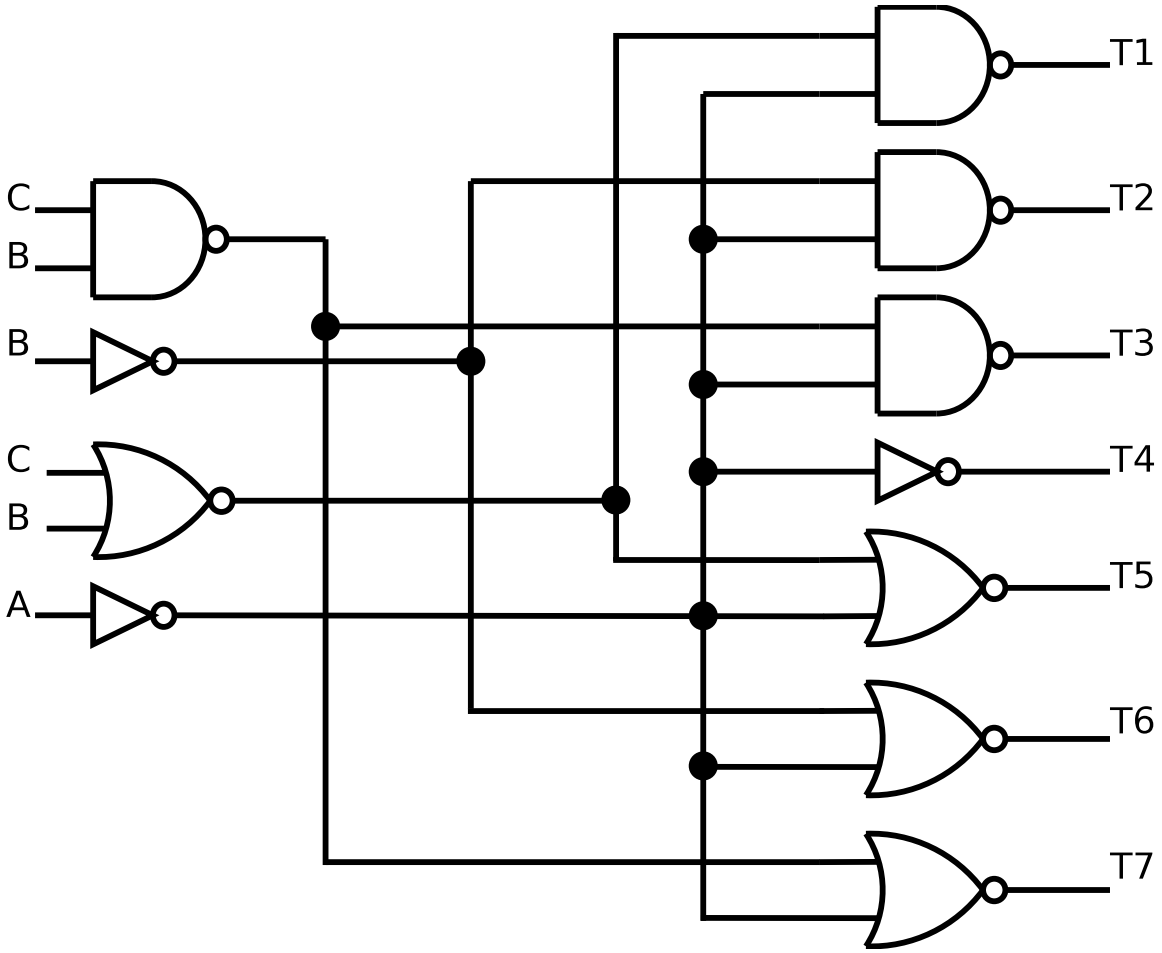

Figure 2.4: Gate level schematic of 3 bit binary-thermometer encoder.

gates are used. This approach reduces the area by eliminating redundant logic.

The full thermometer encoder design, with corresponding inputs for the column encoder, can be seen in Fig. 2.4. The logic gates were sized large enough to ensure high speed and drive strength. NAND and NOR logic is used for optimal delay and area. If the encoder was implemented using the equations from table 2.1, 56 transistors would be required. By removing the redundant logic, the transistor count is reduced to 38. The output waveform of the encoder is shown in Fig. 2.9.

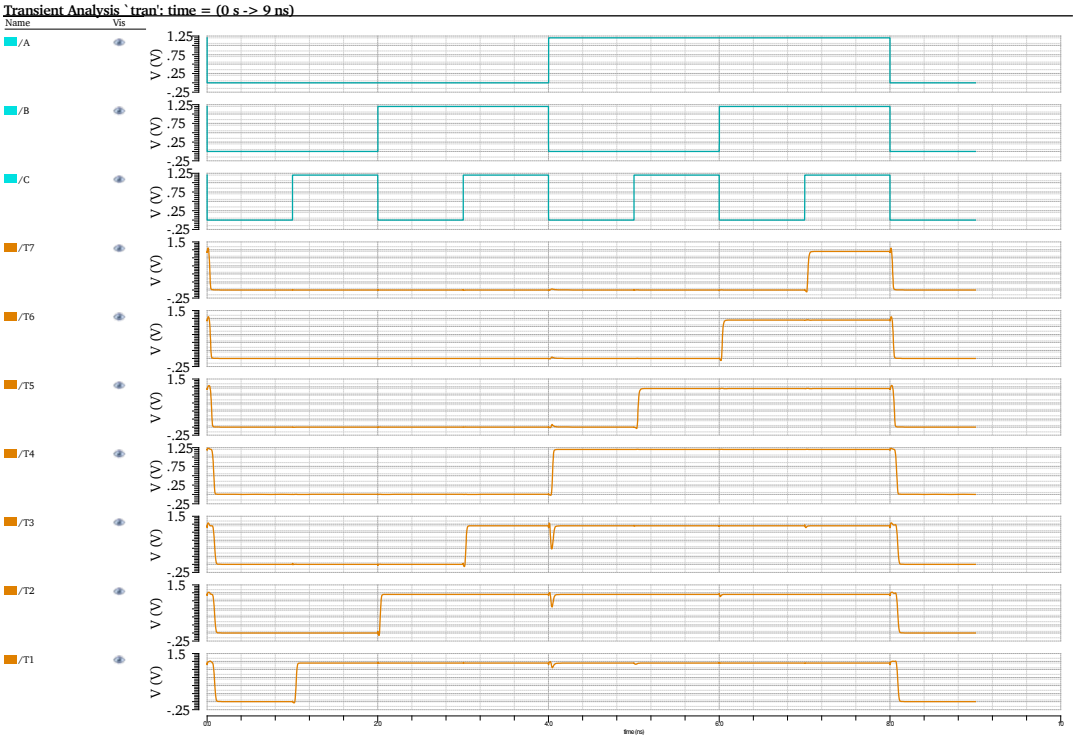

Figure 2.5: Thermometer encoder output waveform.

2.2.2 Local Decoder

The local decoder receives outputs from the thermometer encoders. Each current cell is indexed by row i and column j. The local decoder consists of an OR and NAND gate with inputs row_i, row_{i-1}, and $column_j$. These are used to determine if the current cell should be turned on. An inverter is used to create differential outputs that will control the differential current switches. The outputs from the local decoder are then sent to a master-slave latch to re-time all of the input signals.

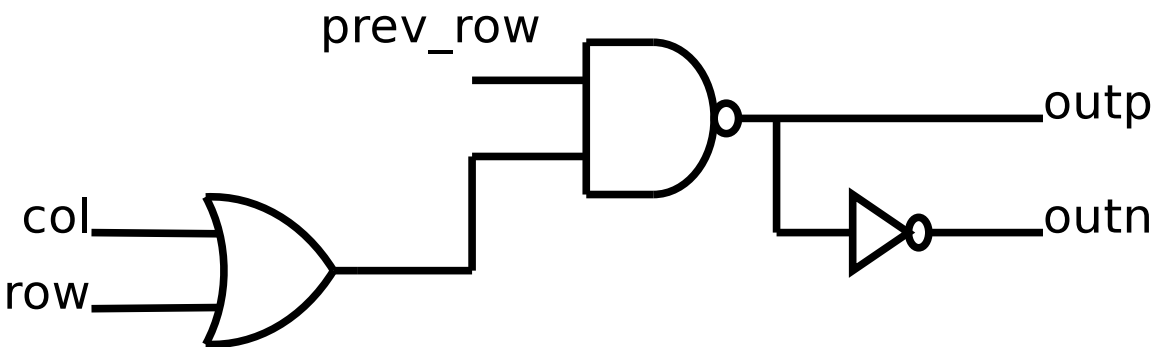

Figure 2.6: Gate diagram of local decoder.

2.2.3 Latch

A master-slave latch is placed between the local decoder and the current cell switch transistors. This type of latch, shown in Fig. 2.7, consists of two cascaded D latches and an inverter placed in the clock path. The purpose of the latch is to synchronize all the input signals so the current cell switches switch in unison. A standard latch can be used, however this requires high timing accuracy from the thermometer encoder. Timing skew from the thermometer encoder outputs will cause distortion to occur [13]. To relax the timing demands, a master-slave latch is used in this design. By using this method, the inputs to the latch just have to arrive before the changing clock edge.

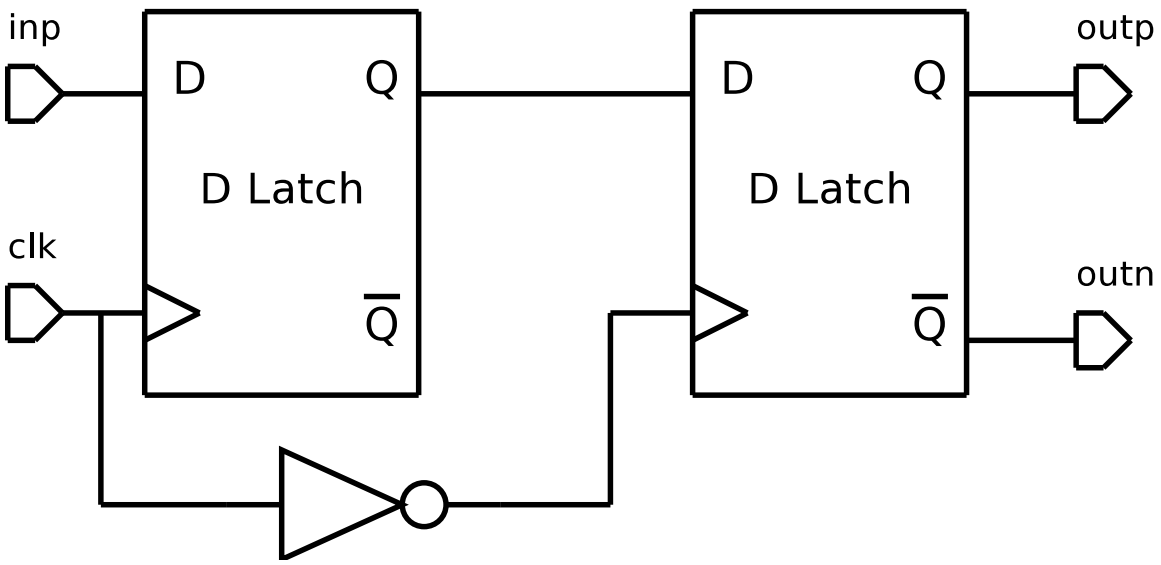

Figure 2.7: Block diagram of master-slave latch.

Since the current cell has differential outputs, the latch includes differential input and output. A simple latch can be created using cross coupled inverters. The latch used in this thesis can be seen in Fig. 2.8. The digital inputs are connected to a pair of pass gate transistors. These transistors are controlled by the clock. When the clock signal is high, the digital signals enter the latch. The cross coupled inverters form a feedback loop that holds the digital value. A set of inverters are placed at the end of each latch stage to boost the signal strength between the stages. The two latches are cascaded to create the master-slave flip flop. A falling edge flip flop design is used, which means the first stage is controlled when clock is zero and the second stage is controlled when the clock is positive. The functionality of the master-slave latch has been tested with a clock speed over 2 GHz. The waveform in Fig. 2.9 shows a 2 GHz clock signal, input, and differential outputs.

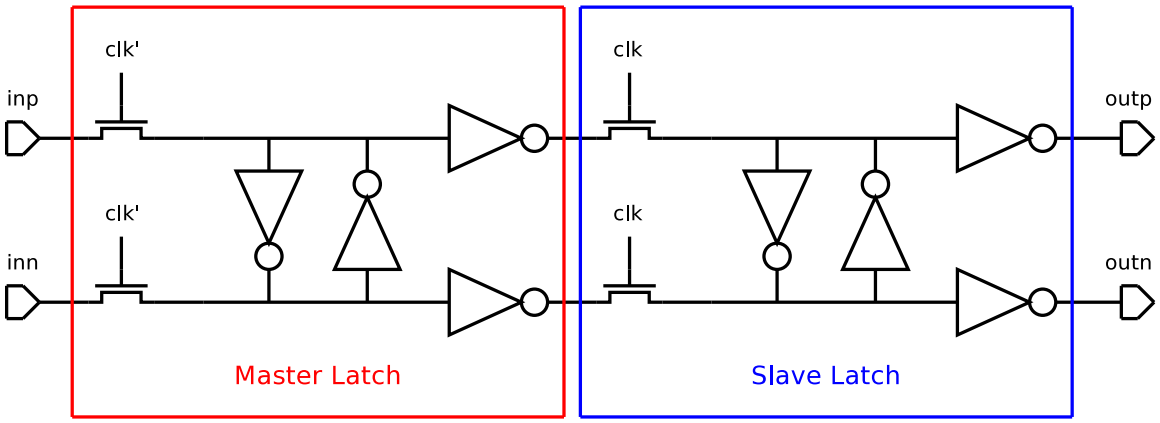

Figure 2.8: Schematic of implemented latches used for the flip flop.

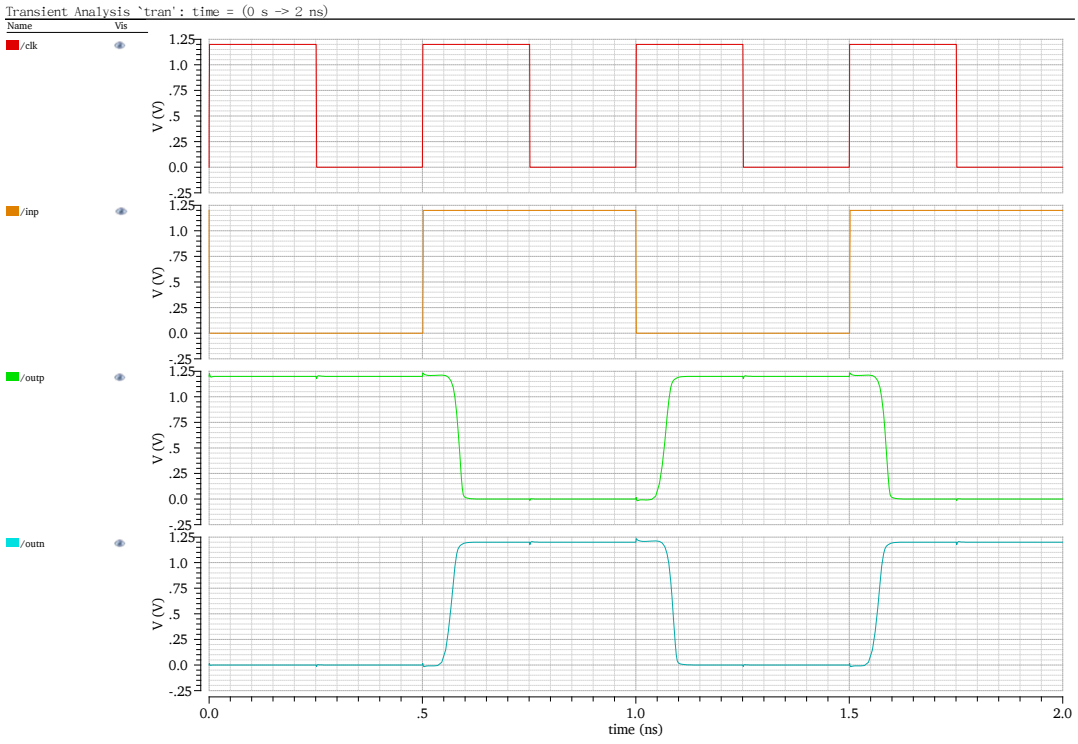

Figure 2.9: Latch waveform with 2 GHz clock, input, and differential output.

2.2.4 Switch Driver

To reduce the impact of glitches in the current cells, the crossing points of the differential current switch control signals can be modified. The two ways to do this is to either change the rising time of the signals, or reduce the voltage swing of the signals [13]. The change in rise time can be done by delaying, or slowing the rise time of one of the differential signals. Modified latches such as [9] incorporate this technique. The other technique reduces the swing of the control signals by raising the logic low voltage of the control signal. This method is used in [13] and [14], and is preferred since the rise times of the control signals are symmetrical.

This thesis uses a switch driver that reduces the voltage swing of the current cell control signals, which can be seen in Fig. 2.10. The driver works by having two NMOS transistors that are controlled by the digital output from the master-slave latch. When the digital input is zero, the driver output will be V_{dd} since the transistor will be turned off. When the digital input is high, the transistor will turn on. This causes some of the current from the the resistor to be sinked to the current source, causing the output voltage level to decrease. The resistor and current source are set up so that the driver will output 1.2 V for a logic one, and 800 mV for a logic zero. The reduced swing output from the switch driver can be seen in Fig. 2.11.

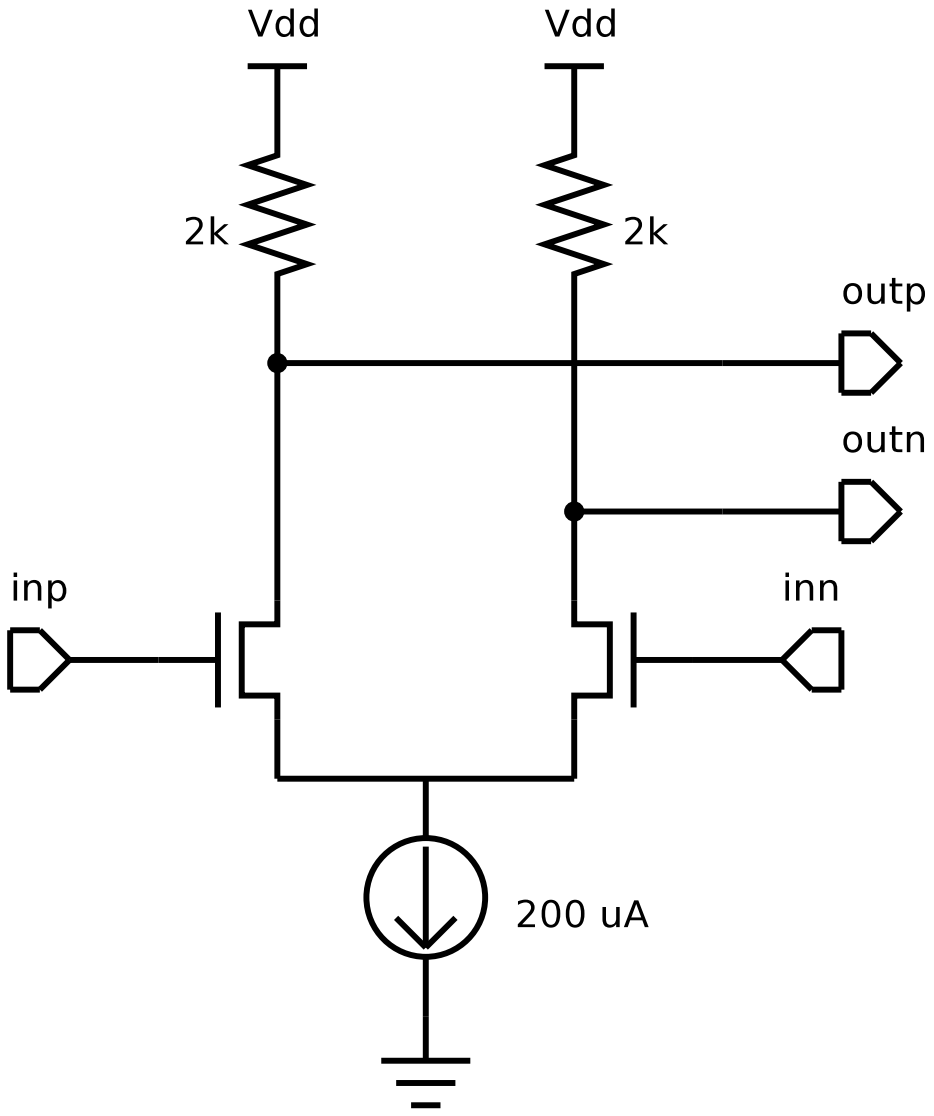

Figure 2.10: Schematic of reduced swing switch driver circuit.

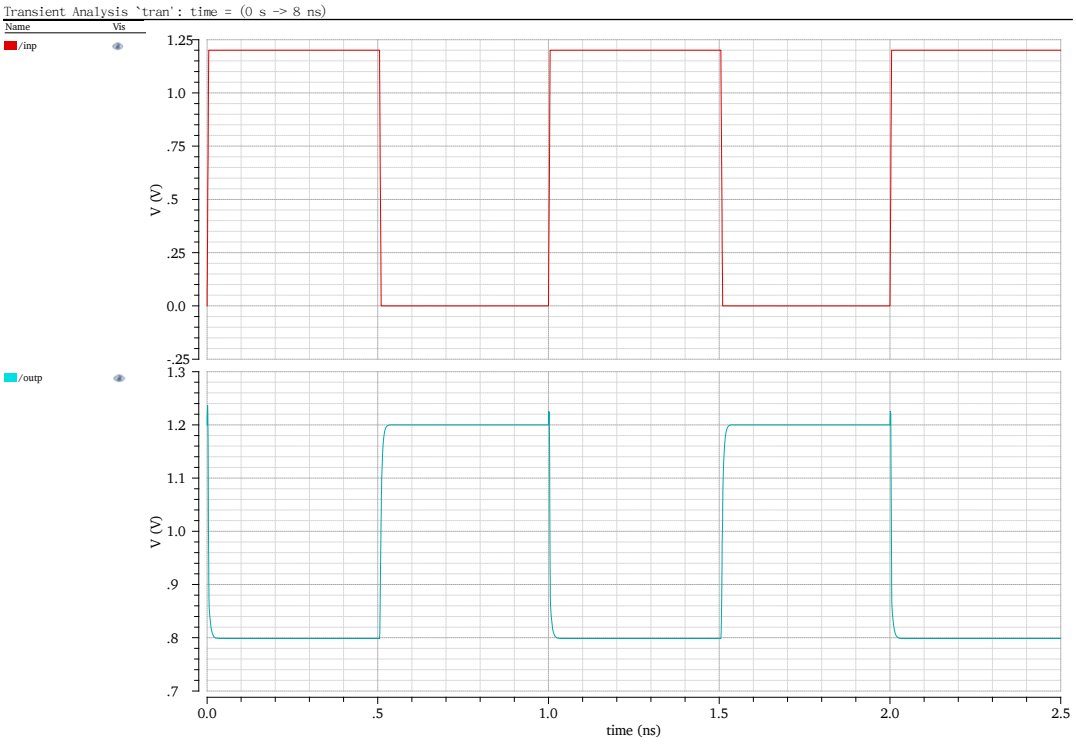

Figure 2.11: Switch driver waveform with output that swings from 800 mV to 1.2 V.

2.3 Current Cell Design

The current cell is the main sub-circuit to the current steering DAC. Design of the current cell must take into account transistor mismatch, output impedance, area, and power consumption. Inaccuracies in the current cell will greatly reduce the static and dynamic performance of the converter. A basic current cell consists of differential switches and a current sink. The differential switches receive control signals from the local decoder and latch sub-circuits. The switches determine which output the current will be sinked from. The basic current cell suffers from several issues that limits the DAC performance. More complicated current cell designs will be discussed.

2.3.1 Pelgrom Model

Through process variation the size of the current sink transistors can vary. The variance in transistor size impacts the accuracy of the reference current being produced. In order to improve transistor matching, the transistors can be sized larger, however this increases area. The Pelgrom model was developed to characterize the relationship for device matching between two transistors based on their area and distance from each other [15]. This can be adapted to determine the size of the current sink transistor based on matching constraints. The minimum transistor area can be calculated from equation 2.2

$$(WL)_{min} = \frac{A_\beta^2 + (\frac{4A_{vt}^2}{(V_{gs}-V_t)^2})}{2(\frac{\sigma I}{I})^2} \tag{2.2}$$

where A_{vt} is the threshold voltage mismatch parameter, A_β is the current factor mismatch parameter; both of these being process dependent variables. The relative standard deviation of the current source is denoted as $\frac{\sigma I}{I}$ [16]. In order to maintain an $INL \leq 0.5$ LSB, $\frac{\sigma I}{I}$ is defined as

$$\frac{\sigma I}{I} \leq \frac{1}{2C\sqrt{2^n}} \tag{2.3}$$

where n is the resolution of the converter, $C = inv\_norm(0.5 \pm \frac{yield}{2})$ with $yield$ being the number of DACs produced with an $INL \leq 0.5$ LSB. To maintain a high yield, the value of C was chosen to equal 3σ [17]. This results in

$$\frac{\sigma I}{I} \leq \frac{1}{2(3)\sqrt{2^{10}}} = 0.52\% \tag{2.4}$$

The values for A_{vt} and A_β are estimated to be 3 mVμm and 1 $\%\mu$m, respectively. By applying these values to equation 2.2, the transistor area can be determined. In Fig. 2.12, the transistor area is plotted versus the overdrive voltage. It can be observed that by increasing the overdrive voltage, the minimum area required for matching decreases. A

minimum area is advantageous, however a large overdrive voltage reduces the headroom for the current cells. With the modified current cell that will be discussed later, a higher overdrive voltage can be used. For this converter, an overdrive voltage of 750 mV was chosen to produce a current source area of 3 μm^2.

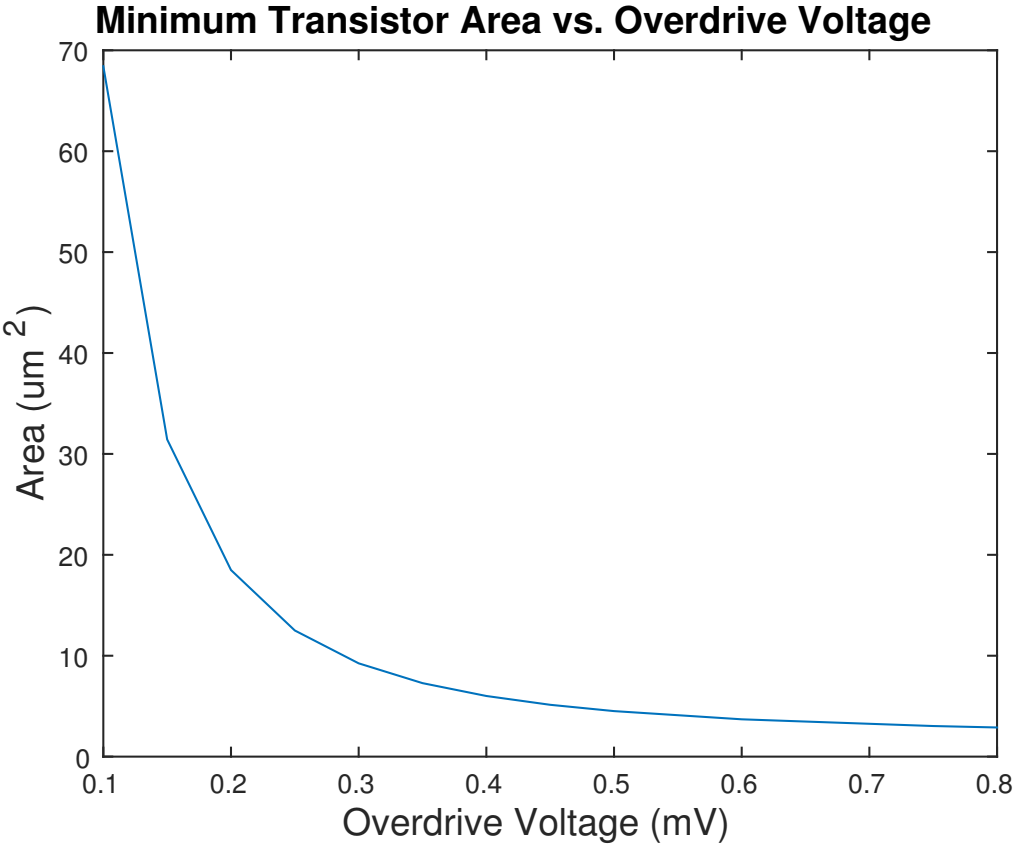

Figure 2.12: The minimum transistor area based on matching considerations.

With the minimum current source area determined, the length and width of the transistor can now be solved. The reference current for the LSB current cell was calculated to be 9.76 μA, which is then inserted to the I_{ds} equation. The process gain factor, K_n, was set to 300 $\frac{\mu A}{V^2}$ and the overdrive voltage of 750 mV as used. Solving the I_{ds} equation, $(\frac{W}{L}) = 0.12$. To meet the minimum area requirements, the length of the transistor could be chosen to equal 5 μm, making the width approximately 600 nm. To increase the output impedance of the current cells, the length of all the current cells are set to 6 μm. The gate

widths were scaled appropriately for the weighted current cells. The next section further explains the importance of current cell output impedance.

2.3.2 Output Impedance

The output impedance of the DAC is based on the load resistance and the unit resistance of each current cell. In the current steering architecture, the amount of current cells turned on depends on the input code. The code dependent nature of the output impedance causes the the DNL and INL to vary. The current cell output resistance influences the INL by approximately

$$INL = \frac{NR_L}{4r_o} \tag{2.5}$$

where R_L is the load resistance, and r_o is the output resistance of the current cell [18]. The INL of the converter will impact the dynamic performance of the converter. Distortion caused by the the non-ideal output impedance will degrade the SNDR and SFDR of the converter. Since the output impedance of the converter greatly influences both the static and dynamic performance of the converter, the current cells must be carefully designed to obtain the best performance.

In an ideal case, the current cell would have infinite output impedance. The cell can be designed to have a very large impedance, which should provide an acceptable level of performance. One of the main dynamic performance metrics for the DAC is the SFDR. The required current cell output impedance for a given SFDR is [7],

$$R_{unit} \geq R_L \cdot 10^{\frac{6(N-2)+SFDR}{20}} \tag{2.6}$$

where R_L the load resistance and N is the resolution of the converter. It can be seen in Fig. 2.13 the required output impedance to obtain various SFDR measurements. Based on the calculations, the necessary output resistance needed for an 65 dB SFDR, with a 50 Ω load

resistance, is 25 MΩ.

When designing the current cells to achieve a high output impedance, it should be noted that the LSB current cell has the most stringent impedance requirements. The output impedance of the overall converter can be represented as

$$Z_{out} = \frac{R_{unit}}{n} \tag{2.7}$$

where R_{unit} is the LSB current cell impedance, and n is the decimal code that the DAC is converting [19]. If the LSB impedance is set to 25 MΩ, then the cell with a current weight of $2I$ requires an output impedance of 12.5 MΩ, $16I$ requires 1.56 MΩ, and so on. Based on the output impedance of a MOSFET, the impedance is inversely proportional to the drain current. This is convenient since the small current produced by the LSB cell can easily have a large output resistance. It will be more difficult for the larger current cells to maintain a large output resistance, but based off of equation 2.7 their resistance requirement is relaxed.

There are two solutions to improve the output impedance, the first is to use an output buffer op-amp, and the second is to use a cascode current source architecture [13]. The output buffer solution creates a near infinite output impedance since the inputs to the op-amp form a virtual ground. The downside of using the output buffer is that it adds more complexity to the circuit, and the performance of the buffer could negatively impact the performance of the converter. Another solution is to add cascode transistors to the current source. Not only is the impedance of the current cell increased, but the cascode transistor reduces the output capacitance associated with the current source. The cascode transistor isolates the large current source transistor capacitance from the output, which improves current cell performance.

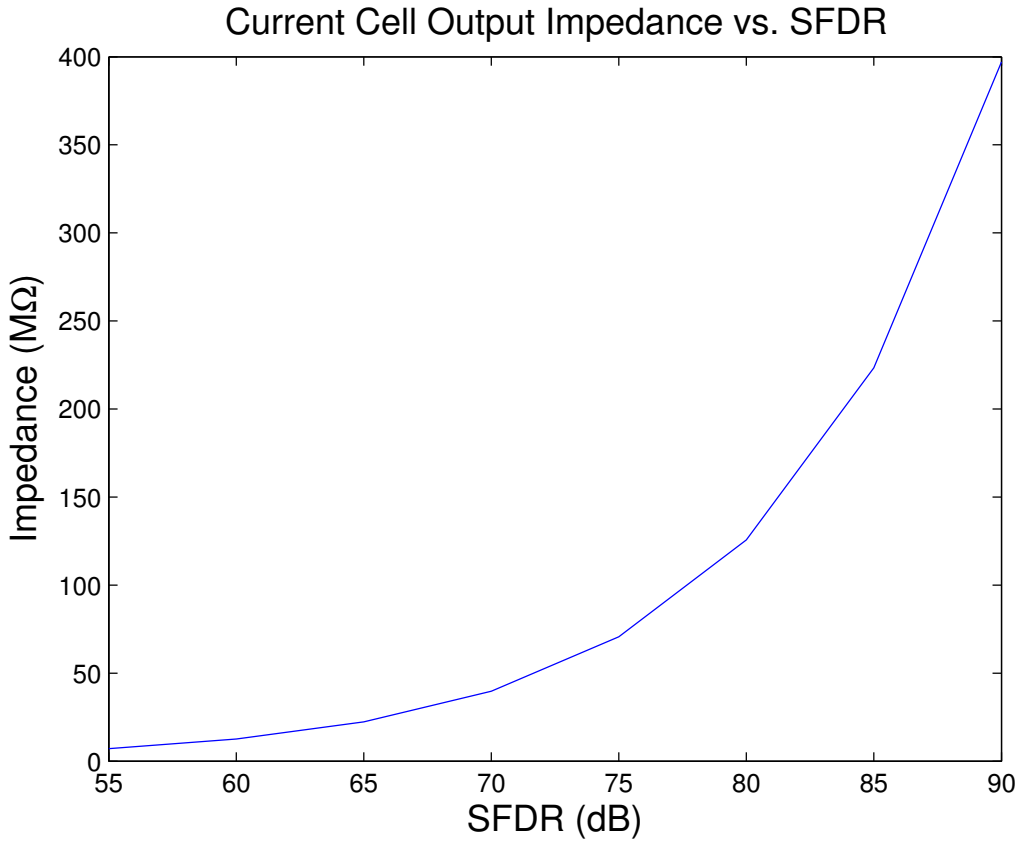

Figure 2.13: Minimum current cell output impedance vs. converter SFDR.

2.3.3 Current Source Architecture

Three different current cell architectures were studied to obtain the best performance for the DAC. The first architecture is the basic current cell. This architecture consists of a single current source to produce the reference current, and a pair of differential switches. The second architecture, seen in Fig. 2.14, improves the performance by cascoding the current source transistor. This will greatly increase the output impedance and reduce the output capacitance of the current cell. The main disadvantage with the cascode current cell is that the area is increased, and the need for an additional bias voltage. The final architecture consists of the cascoded current source, but also adds cascode transistors between the differential switches and the output. The advantage of this design is that it further increases output impedance, and reduces the effects of clock feedthrough to the output.

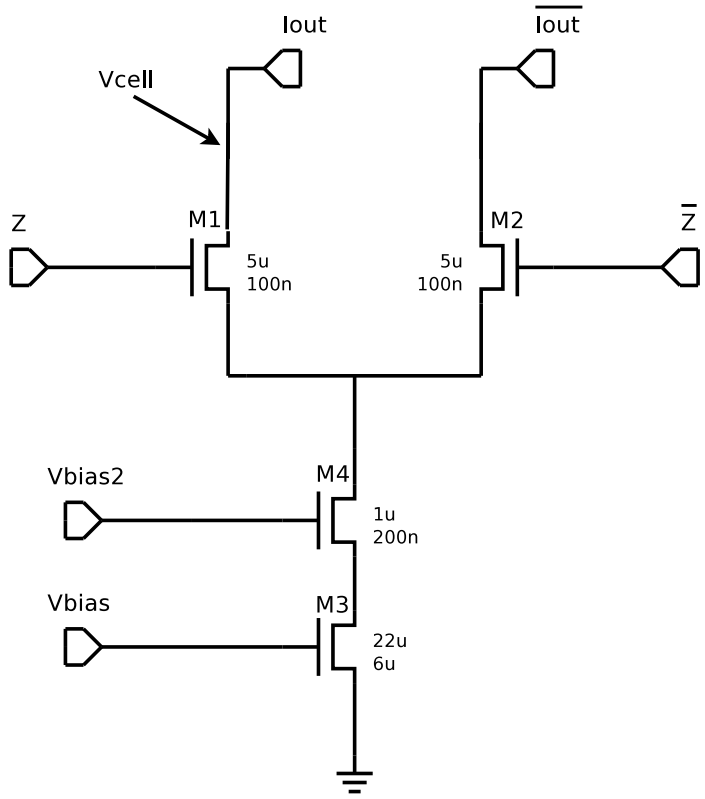

Figure 2.14: Cascode current sink architecture.

Each current cell design was analyzed to see which provided the most accurate reference current. This was done by sweeping the the output voltage (V_{cell}) and measuring the corresponding current produced by the current cell. The current source transistors were sized with a length of 6 nm. In order to have a similar reference current between the three designs, the width of the current source transistor was adjusted. The transistors were sized to produce an output current of one LSB.

The basic single transistor current sink and the cascode current sink were simulated to find the output current deviation across the operation range. The current cells output voltage operates between 1.2 V to 700 mV to obtain the 500 mV full scale range. It was observed that the output of the basic current cell varied by 130 nA. The output impedance can be solved by dividing the change in V_{cell} by the change in current. This means the output resistance of the basic current cell is about 3.85 MΩ.

The cascode current source design has a change in current of 80 nA across the full

scale range. This leads to an output resistance of 6.25 MΩ. The increased output impedance from adding the cascode transistor has almost doubled the linearity of the current cell compared to the single transistor current sink. The accuracy and output impedance can be further improved by adding cascode transistors to the differential switches.

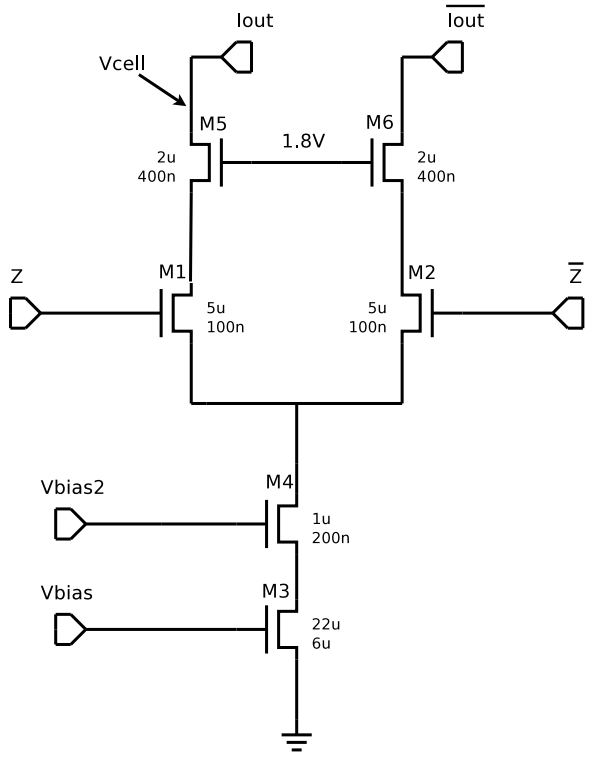

Figure 2.15: Cascode switch current cell architecture.

The current cell in this converter uses the cascode switch architecture, which can be seen in Fig. 2.15. The added transistors between the switches and the outputs increase the current cell impedance, and also reduce the output capacitance. The output capacitance is based on the number of current cells that are active at any given time. The cascode transistor buffers the switches from the changing output capacitance. Charge is stored at the node between the current sink and the differential switches. As the switch turns on, this capacitance is discharged to the output [13]. The capacitance within the current cell reduces the switching time, slowing down the speed of the converter. The discharging of this capacitance also produces glitches in the output, which will affect linearity and

dynamic performance.

One of the issues of using a process with a low V_{dd} is that the headroom of the current cells are limited. This problem is solved by replacing the cascode switch transistor with a thick gate oxide transistor [14]. This allows the cascode to be biased to a voltage higher than the 1.2 V V_{dd}. The improved cascoded switch transistor can be biased to 1.8 V, providing enough headroom for a 500 mV full scale range. With the increased voltage headroom, the current cells operation range has shifted up to be between 1.8 V and 1.3 V. The waveform of the improved current cell is shown in Fig. 2.16. It shows that the reference current varies by 7 nA, giving an output resistance of 71 MΩ. This is a massive improvement over the previous current cell designs, which will allow high linearity with inputs frequencies in the several hundred megahertz range.

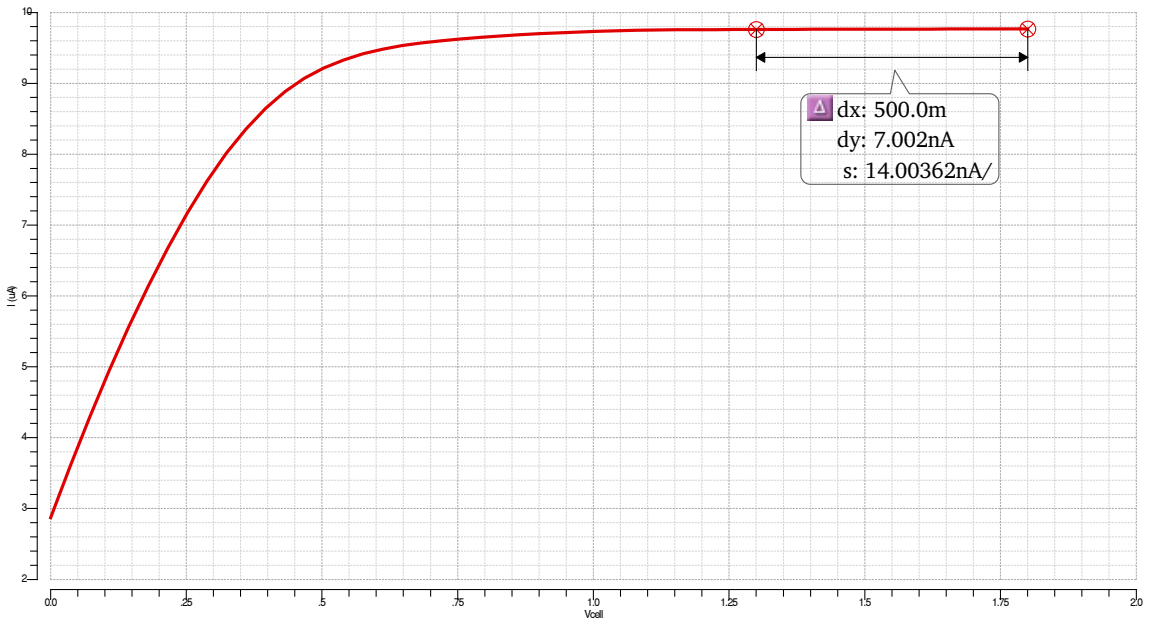

Figure 2.16: LSB output current through the full scale operating range.

2.4 Filter Design

In an ideal DAC, the output signal spectrum would look like a brickwall filter after the Nyquist frequency. In practice, the converter produces many undesirable spectral images past the Nyquist frequency. These images cause distortion in the baseband. The output of the DAC consists of rectangular pulses summed together. In the frequency domain this become a weighted sinc function. This sinc function in the output is what causes the spectral images. To reduce the impact of the spectral images, a reconstruction filter is applied to the output of the converter. This filter consists of a multi-order low pass filter. By filtering the output, the pulse-like output is smoothed to appear sinusoidal.

For this design, a Butterworth low pass filter was chosen. This is because the Butterworth filter has a maximally flat response opposed to other common filter types. In order to design the filter, the quality factor, Q must be determined. When designing multi-order filters, the appropriate Butterworth normalized polynomial coefficients are chosen. The equation 2.8 shows the general low pass filter transfer function [20].

$$A(s) = \frac{A_0}{\prod_i (1 + a_i s + b_i s^2)} \tag{2.8}$$

It can be seen that for multi-order filters, the denominator is the product of polynomials that take the same basic form. This means that cascading multiple first and second order filters will create the final n order filter. The quality factor Q can be related to the polynomial coefficients a_i and b_i by the relation

$$Q = \frac{\sqrt{b_i}}{a_i} \tag{2.9}$$

In order to correctly design the filter, a polynomial coefficient table is used. A list of the coefficients required for a Butterworth filter can be seen in table 2.2. Each stage of the filter

Table 2.2: Normalized Butterworth Coefficients

n	i	a_i	b_i
1	1	1.0	0.0
2	1	1.4142	1.0
3	1	1.0	0.0
	2	1.0	1.0
4	1	1.8478	1.0
	2	0.7654	1.0
5	1	1.0	1.0
	2	1.6180	1.0
	3	0.6180	1.0
6	1	1.9319	0.0
	2	1.4142	1.0
	3	0.5176	1.0
7	1	1.0	0.0
	2	1.8019	1.0
	3	1.2470	1.0
	4	0.4450	1.0
8	1	1.9616	1.0
	2	1.6629	1.0
	3	1.1111	1.0
	4	0.3902	1.0
9	1	1.0	0.0
	2	1.8794	1.0
	3	1.5321	1.0
	4	1.0	1.0
	5	0.3473	1.0
10	1	1.9754	1.0
	2	1.7820	1.0
	3	1.4142	1.0
	4	0.9080	1.0
	5	0.3129	1.0

will be designed using the appropriate values of a_i and b_i.

The first step in designing the reconstruction filter is to determine the number of orders needed. In order to have a perfect low pass brick wall filter that attenuates everything after the Nyquist frequency, an infinite order filter would be required. The requirement for the number of orders required can be relaxed by increasing the bandwidth between the cutoff frequency and the stop band frequency. A trade off occurs by using a larger order of filter. The bandwidth of the converter will be increased but the area and complexity of the circuit will also increase. By using the transfer function for the Butterworth filter, the number of filter orders n required can be determined. The Butterworth transfer function can be

defined as

$$\frac{1}{A_{min}} = \frac{1}{\sqrt{1+\epsilon^2(\frac{\omega_s}{\omega_p})^{2n}}} \tag{2.10}$$

Where A_{min} is the magnitude of the gain at the stop band frequency. The pass band frequency in radian is denoted as ω_p, where the stop band frequency is ω_s [21]. Finally, ϵ is set to one in order to have the gain of the filter through the pass band equal to 0 dB. However, if it is desired to change the pass band gain, equation 2.11 can be used. The magnitude of the pass band A_{max} is specified, and the new ϵ can be calculated.

$$A_{max} = \sqrt{1+\epsilon^2} \tag{2.11}$$

To determine the number of orders needed with a stop band frequency of 600 MHz and a pass band frequency of 590 MHz, equation 2.11 is used. The value for the stop band magnitude was chosen to be 40 dB, ϵ was set to 1. Solving for n, the number of orders required is 274, which is an unrealistic size. The calculations were repeated keeping the same parameters, but reducing the pass band frequency to 400 MHz. This produces a filter that only needs 12 orders.

A basic first order low pass filter is constructed using a single resistor and capacitor. The second order filter consists of an operational amplifier, along with resistors and capacitors. The n-order filter is simply constructed by cascading several first or second order filters to get the desired number of orders. A common second order filter architecture is the Sallen-Key topology. The low pass Sallen-Key filter design can be seen in Fig. 2.17. It is observed that the filter uses an operational amplifier with two resistors and two capacitors. When designing the Sallen-Key low pass filter, the value of Q and cutoff frequency ω_0 are required. Each second order stage in the filter must be designed using a different Q value, but the cutoff maintains constant. The Q value for each stage are derived from the normalized Butterworth polynomial coefficient table. There are two capacitors (C_1 and C_2), and

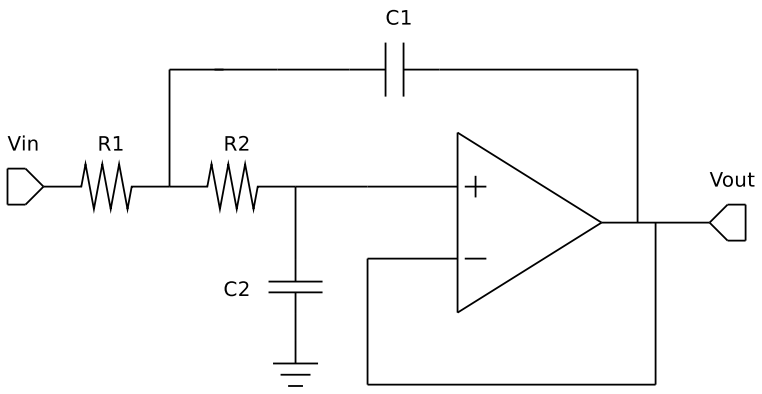

Figure 2.17: Second order Sallen-Key low pass filter.

two resistors (R_1 and R_2) in each stage. The value for C_1 is fixed, the other components are solved by using the following equations [20].

$$C_2 = \frac{4C_1 b}{a^2} \tag{2.12}$$

$$R_1 = \frac{aC_2 - \sqrt{a^2C_2^2 - 4bC_1C_2}}{2\omega_0 C_1 C_2} \tag{2.13}$$

$$R_2 = \frac{aC_2 + \sqrt{a^2C_2^2 - 4bC_1C_2}}{2\omega_0 C_1 C_2} \tag{2.14}$$

The values of a and b are from the Butterworth coefficient table. A 10 order Butterworth filter is used in this thesis. The values of a will be 1.9754, 1.782, 1.4142, 0.908, and 0.3129. The value of b will be one for each stage.

The Sallen-Key topology can add resistors to the negative feedback path to provide gain to the filter, however in this design a unity gain buffer configuration was used. Frequency analysis was used to verify the the cutoff frequency of the filter. From the frequency response plot in Fig. 2.18, the output magnitude is approximately 0 dB through the pass band. The cutoff frequency was measured to be 431 MHz. At the stop band frequency 600 MHz, the output is attenuated to -24.7 dB. With the pass band set to 400 MHz, the first Nyquist image will be located at 800 MHz. From the simulation, it was found that the

Figure 2.18: Frequency response of 10 order low pass filter.

output is reduced to -50 dB at 800 MHz.

2.5 Results

2.5.1 DAC Test Bench

Once the DAC was completed, a test bench was created which can be seen in Fig. 2.19. To test the dynamic performance of the DAC, an ADC was required. Instead of constructing a 10 bit ADC, an ideal circuit was used from the Cadence ahdlLib. This library contains ideal circuits built using Verilog-A. The output from the ADC was fed into the digital inputs of the current steering DAC. To compare the outputs from the current steering DAC to the ideal output, a DAC from the ahdlLib was added to the test bench. Next, the filters were placed on the outputs of the current steering DAC. Since the converter has differential outputs, a filter was placed on each output. Finally, an ideal differential amplifier was used to combine the two differential outputs into the final single ended output.

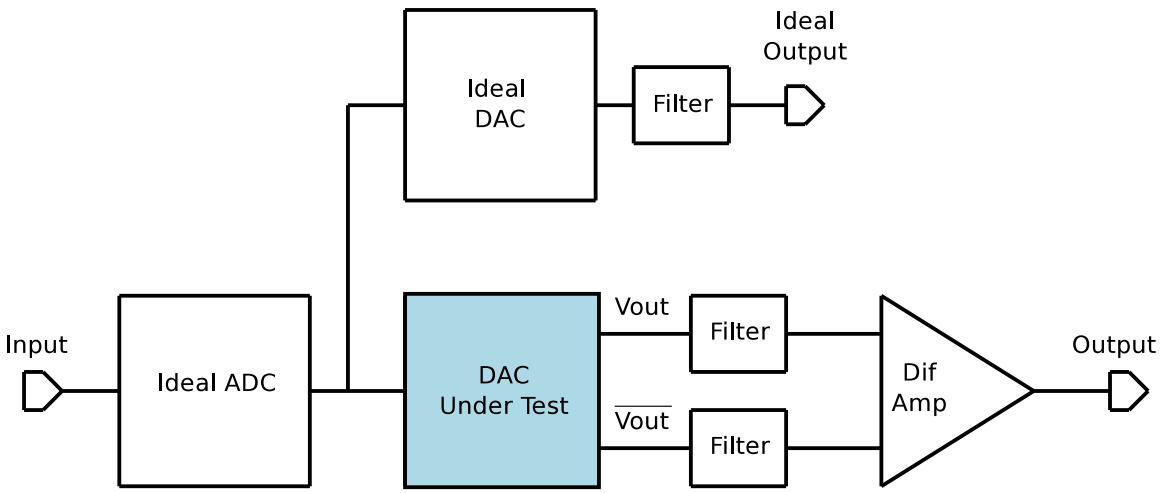

Figure 2.19: Converter test bench.

2.5.2 Static Performance

The ahdlLib was again utilized to measure the INL and DNL of the converter. The library contains a module that will calculate INL, and another for DNL. Each module increments through all possible digital codes, which will be connected to the input of the DAC. The analog output from the converter will the be fed back to the module so that it can compare the DACs output to the ideal value. While simulating, the module will generate a text file containing every code, and the INL or DNL at that code. At the end of the simulation, the module will display the worst non-linearity. The ramp output from zero to full scale can be seen in Fig. 2.20. The DNL for the converter can be seen in Fig 2.21. The worst DNL was measured to be 0.022 LSB. The INL for every code can be seen in Fig. 2.22. From the plot, the worst case INL was found to be 0.29 LSB.

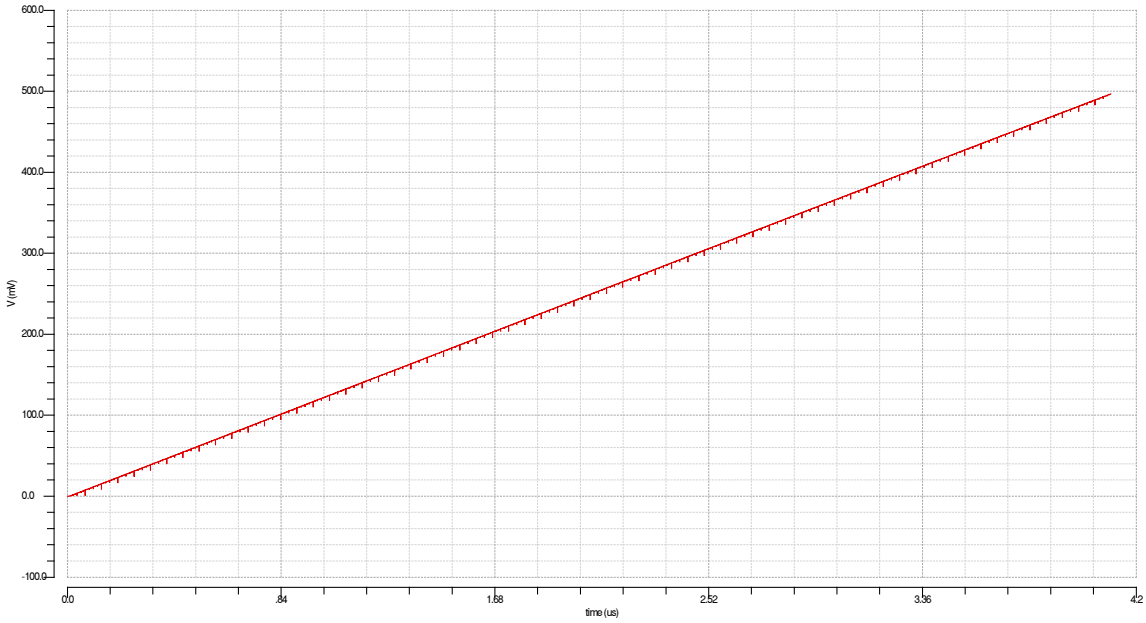

Figure 2.20: Ramp output from zero to full scale.

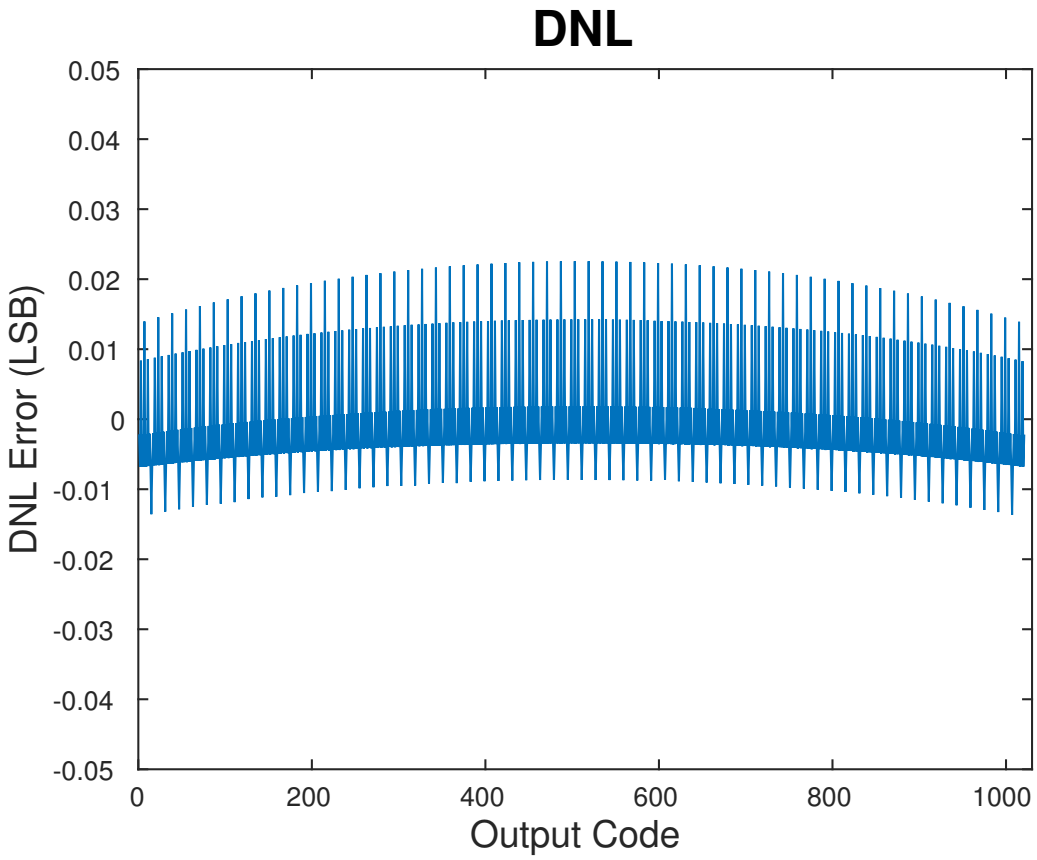

Figure 2.21: Differential non-linearity plot.

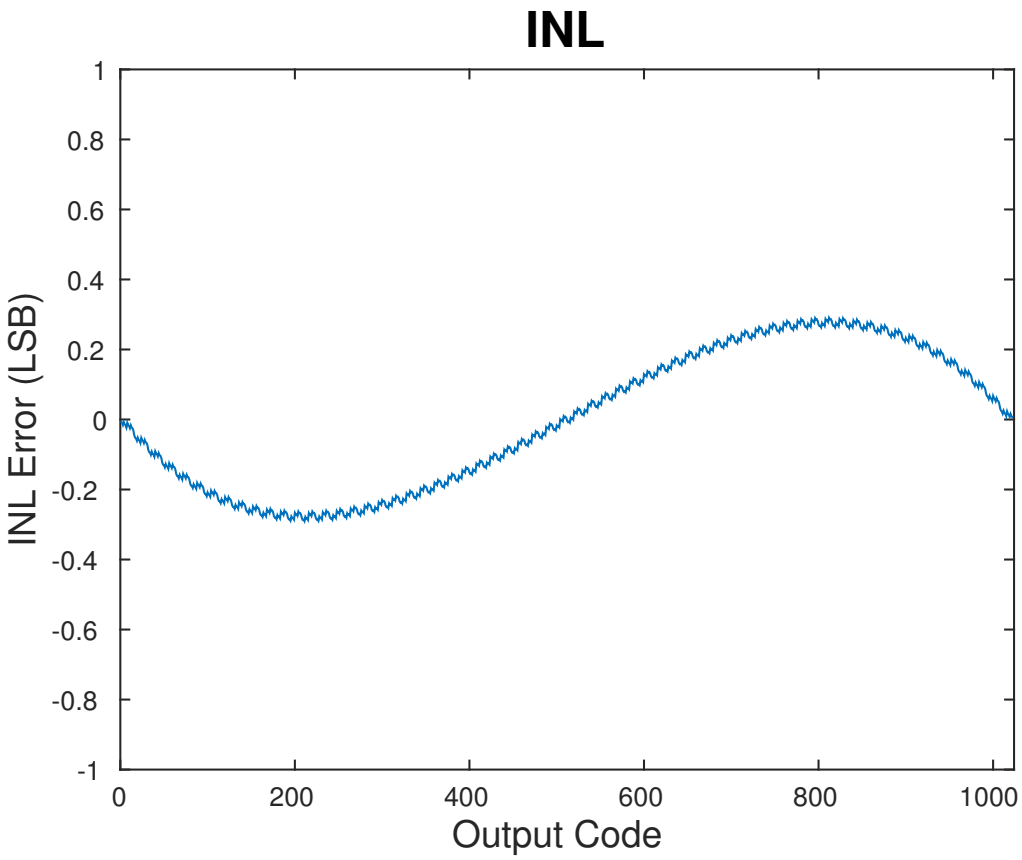

Figure 2.22: Integral non-linearity plot.

2.5.3 Propagation Delay and Rise Time

The propagation delay through the digital sub-circuits, and the rise time of the DAC current cells determine the maximum clocking speed of the converter. While there are many difficulties in designing the analog sub-circuits, the performance of the digital front end is important. The propagation delay between the input reaching the converter, and the time it reaches the latches, partially determines the clock frequency of the circuit. The propagation delay for the thermometer encoder, local decoder, latch, and switch driver were measured to be 70 ps, 12 ps, and 76.6 ps, 4.6 ps respectively.

The rise time of the converter was measured to see how fast the output transitions. A

step input was given to the DAC so that the output would changed from zero to half the full scale range. The mid scale range was used instead of the full scale range since the DAC rarely transitions from zero all the way to the full scale during normal operation. The measurement was taken when the output settled within 1 LSB of the final step response. The rise time of the converter was measured to be 400 ps.

2.5.4 Dynamic Performance

The dynamic performance and power consumption are two of the biggest factors in the figure of merit that will be used to compare this converter with other designs. The compared works from literature report the DAC performance without the use of the reconstruction filter. In order to have a similar comparison, the DAC presented in this thesis was tested with and without the filter. The lack of filter allows the DAC to operate near the Nyquist frequency of 600 MHz. The resulting SFDR and ENOB from a 600 MHz input will be used in the performance comparison section.

The converters dynamic performance was measured by applying a single tone sinusoidal input to the ideal ADC, then analyzing the output from the DAC. Fourier analysis was done to visualize the noise levels harmonics. To reduce distortion in the FFT plot, the sampling frequency and the input frequency should be set to a particular relationship. This relationship is known as coherent sampling. Coherent sampling is used so that M number of cycles of the input signal fit into N FFT bins. The ratio of input frequency, and sampling frequency, in order to satisfy coherent sampling is defined as

$$\frac{f_{in}}{f_{sample}} = \frac{M}{N} \tag{2.15}$$

The value of N is set to a power of two, for most of the simulations it is equal to 1024. It is ideal to have M equal a prime number. The process of finding the appropriate values of f_{in} and M is to set the input frequency to the desired value. The value of M is then

calculated and the closest prime number is chosen to be the new M. Finally, the coherent ratio is solved again for f_{in} which will be slightly off from the initial value.

Spurious free dynamic range is one of the most important performance metrics for high speed digital to analog converters. The following plots show FFT of the converter output with the reconstruction filter. The FFT plot in figure 2.23 shows the SFDR with a low frequency input. The measured SFDR with a 55.07 MHz input was found to be 75.1 dB. In fig. 2.24, an input of 394.92 MHz is applied to the DAC. This input frequency is near the cutoff frequency of the reconstruction filter, and produces a SFDR of 68.6 dB.

The SFDR versus input frequency for the converter with, and without, the filter can be seen in Fig 2.25. It can be seen that the SFDR of the filtered converter reaches a maximum of 78 dB, then begins to drop after 225 MHz. As the input approaches 400 MHz, the SFDR starts to increase again. The low frequency SFDR of the unfiltered converter is 69.33 dB. Finally, the SFDR for the unfiltered DAC is 72.07 dB near the Nyquist frequency.

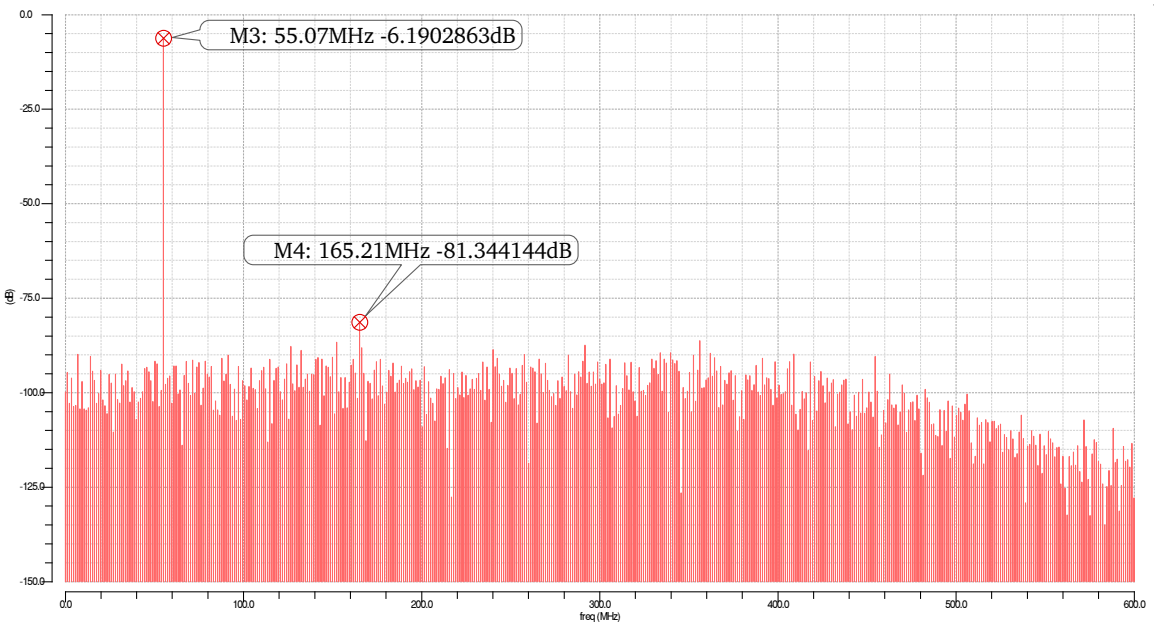

Figure 2.23: SFDR of filtered converter with 55.07 MHz input signal and 1.2 GHz clock.

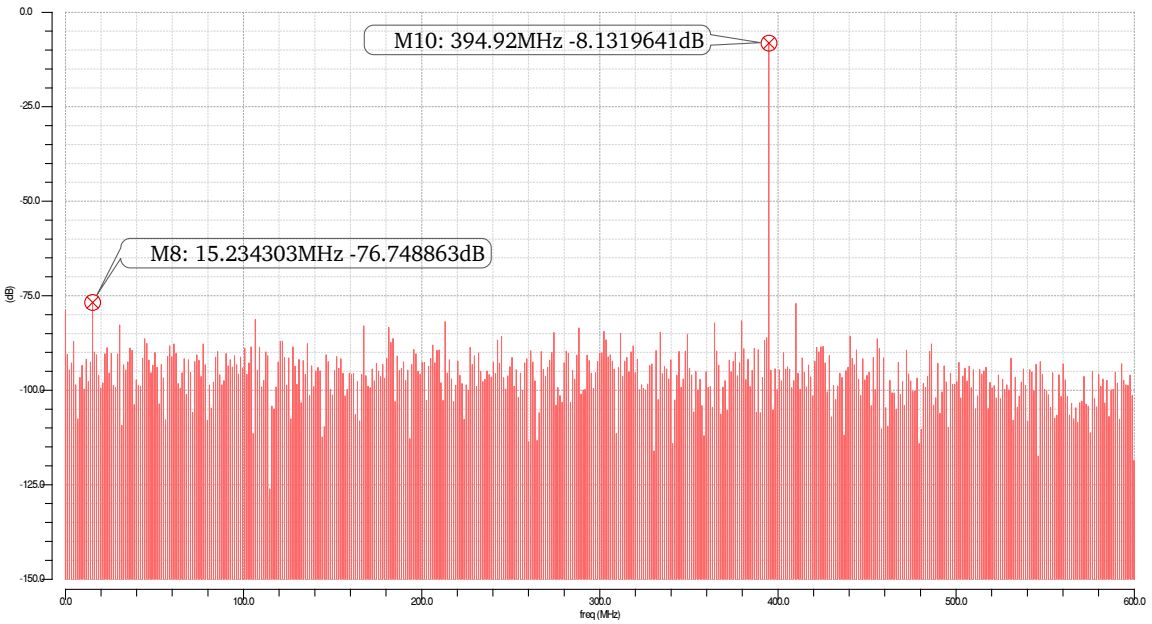

Figure 2.24: SFDR of filtered converter with 394.92 MHz input signal and 1.2 GHz clock.

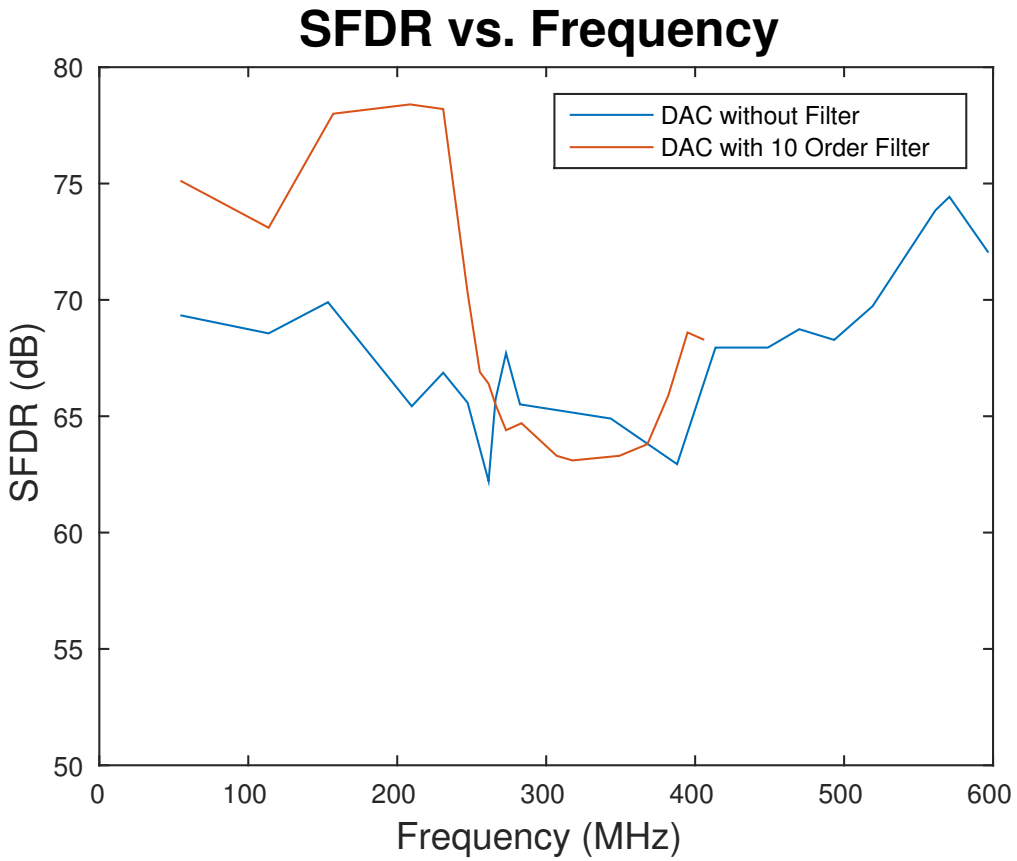

Figure 2.25: SFDR of converter with and without filter for a range of frequencies.

2.5.5 Power Dissipation

The power dissipation of the DAC can be categorized into the digital sub-circuits, and the analog circuits. The analog power dissipation is based on the current drawn through the load resistor by the converter. Since the load resistor is 50 Ω, and the full scale voltage is 0.5 V, the max current draw will be 10 mA. In addition to this, the digital circuits will consume power. The average power dissipation for the thermometer encoder is 83.5 μW, the buffer array is 638 μW, the local decoder is 34 μW, the latch is 83.9 μW, and the switch driver is 223 μ. Since these digital sub-circuits are used more than once in the converter, Table 2.3 shows the overall power contribution of the digital circuits. From the table, it can be seen that the switch driver consumes the most power out of the digital circuits. This is because there is a driver in each of the 67 current cells. The total power consumption of the DAC is measured to be 43 mW with an input frequency of 596 MHz.

Table 2.3: DAC Average Power

Sub-Circuit	Quantity	Average Power (mW)
Thermometer Encoder	2	0.167
Buffer Array	2	1.277
Local Decoder	63	2.278
Latch	67	5.628
Switch Driver	67	14.941
Current Cells	-	18

2.5.6 Performance Comparison

Several converters of similar resolution, speed, and technology exist in literature. A few of these converters are compared with the one presented in this thesis. A summary of key performance measures can be seen in table 2.4. From the table it can be seen that the converter presented in this thesis has the second lowest power consumption, consuming 43

mW. The DNL measurement of this converter is the best of the compared works at 0.02 LSB, while the converter in [22] had the worst DNL at 0.5. The best INL measurements came from [9] and [16], both having 0.2 LSB. The highest INL came from [22] at 1.2 LSB, while the converter presented has an INL of 0.52 LSB. This work shows the highest SFDR, and is 50 MS/s off from the highest sampling rate. The converter in [23] has a SFDR of 61 dB, while this work has a SFDR that is 11 DB higher with a sampling rate that is 20% faster. The 12 bit converter in [22] has the highest sampling rate, and the second highest SFDR of the compared converters.

A figure of merit from [22] was also used to compare all of the designs. The equation for the FOM takes into account the low frequency ENOB, high frequency ENOB, sampling frequency, total power. The equation for the FOM can be seen in equation 2.16.

$$FOM = \frac{f_s(2^{ENOB_{LF}})(2^{ENOB_{HF}})}{P_{Total}} \tag{2.16}$$

The units for the FOM are $10^4 \frac{GHz}{mW}$. The works in [23] and [22] have the highest FOM of the compared works. However this thesis has a FOM that is almost three times that of the best compared design. It can be seen, the converter in this thesis performs comparably, or outperforms, several converters from literature.

Table 2.4: Performance Comparison

	[9]	[17]	[23]	[16]	[22]	This Work
Technology	0.35 μm	90 nm	90 nm	0.35 μm	90 nm	90 nm
Resolution	10	10	10	10	12	10
Power Dissipation (mW)	125	23	49	110	128	43
DNL (LSB)	0.1	-	-	0.14	0.5	0.02
INL (LSB)	0.2	-	-	0.2	1.2	0.29
Update Rate (MS/s)	500	1000	800	1000	1250	1200
SFDR (dB)	51	50.64	61	61.2	66	72
Bandwidth (MHz)	240	308.59	193.2	490	625	600
ENOB	8.18	8.12	9.84	9.87	10.67	11.66
FOM ($10^4 \frac{GHz}{mW}$)	0.09	0.86	4.84	2.46	7.36	21.71

Parallel Path DAC

One method to increase the performance of a digital to analog converter is to use an even amount of parallel DACs, and combining their outputs. The final output is formed by either multiplexing between the outputs of each sub-DAC, or summing the outputs together. Using multiple DACs in parallel creates challenges for the designer by increasing area, and circuit complexity. The benefits of the parallel architecture is the sampling rate can be greatly increased. Another advantage is that Nyquist images can potentially be canceled out, reducing the demands of the reconstruction filter.

There are two methods of using parallel DACs: data interleaving, and time interleaving. The difference between these two methods are the manner in which the digital inputs are supplied to the parallel DACs, and how the outputs are combined.

3.1 Data Interleaving

Data interleaving involves parallel DACs that receive alternating (interleaved) digital input samples. The outputs of each sub-DAC are combined to form a composite output. The data interleaving technique is illustrated in 3.1. It can be seen that four parallel DACs alternate receiving samples from the input signal.

The alternating input architecture requires additional hardware to handle the input. The digital input stream must be N faster for N number of parallel converters. In order for the interleaved DACs to operate in a staggered fashion, the clock signal controlling each

sub-DAC must be phase shifted. With two parallel DACs, the clock on each DAC is 180 degrees out of phase. For more than two sub-DACs, a demultiplexer must be used to direct the digital inputs to each sub-DAC.

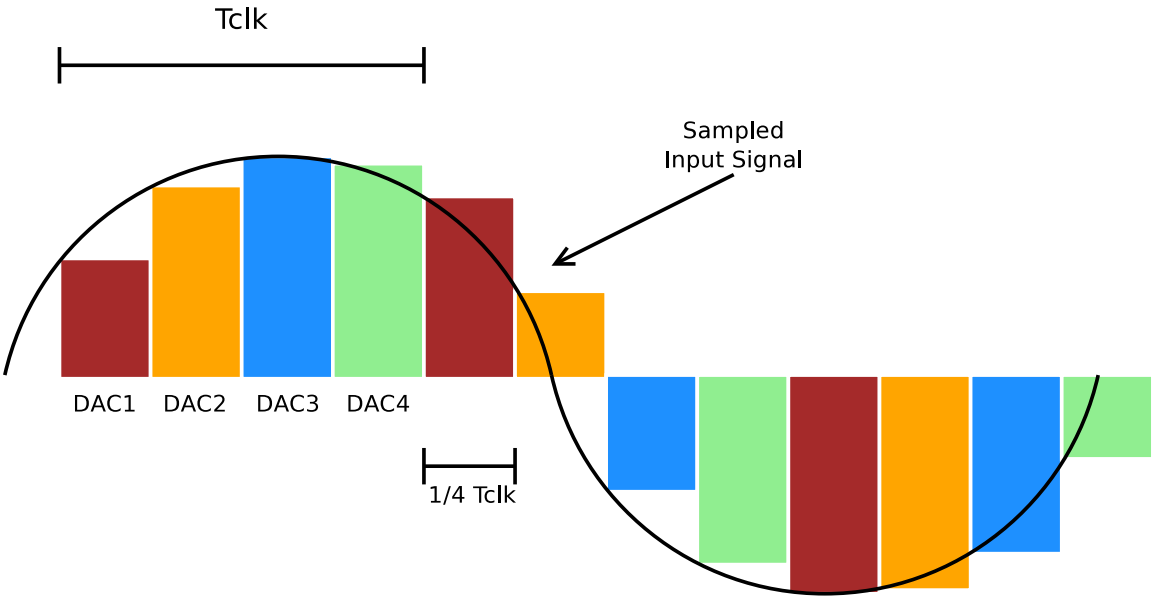

Figure 3.1: Data interleaving with four parallel DACs receiving alternate data samples.

From the work in [24], the effect of summing the outputs of the parallel DACs is the reduction of Nyquist aliases. Two DACs alternate input samples, and the outputs are summed together. The two DACs are reproducing the same signal, but at different time samples. This causes both converters to output the fundamental signal, and Nyquist images that are opposite phase. When the two outputs are summed, the out of phase images cancel and the fundamental remains.

A high bandwidth converter using the above technique was proposed in [25]. Here four DACs clocked at 10 GHz were able to output a signal of 3.513 GHz. The parallel path architecture was able to cancel out the first three Nyquist images and reduce spurs.

A similar architecture found in [26] uses a technique known as L-fold interpolation. In this interpolation technique, each sub-DAC is clocked out of phase from each other. Instead of the sub-DAC receiving its own input sample when its clock is high, all sub-DACs

receive the same digital sample. The benefits of using L-fold interpolation is the reduction of aliases. This occurs because the DAC frequency response forms a sinc^2 function instead of the normal sinc function [27]. Further analysis in [26] showed that by purposefully adding a particular amount delay offset to the sub-DAC clocks, attenuation of images can occur. The optimum amount of delay t_0 required to reduce aliases of frequency f_z can be calculated by

$$t_0 = \frac{m}{2f_z} - \frac{1}{2f_s} \tag{3.1}$$

where m is an odd number the and f_s is the sampling frequency. The clock delay can easily be obtained by adding digital logic in the clock path.

Another method of using parallel DACs is to switch between the outputs of the sub-DACs instead of adding them. An analog multiplexer is added to the output of both sub-DACs. The multiplexer directs the appropriate DAC to the output, while the inactive DAC is connected to a dummy output. The use of a dummy output is known as a return to zero (RZ) hold operation. When the DAC output is changing, glitches can appear. During the output transition, the DAC output will be connected to the dummy output. Once the output is settled, it will be switched to the real output. The advantage to an RZ DAC is the reduction in switching errors and improved linearity. Since the output is only active for half the time, the signal power will be heavily attenuated [28]. Stand alone DACs using RZ have been implemented before, but using RZ in conjunction with interleaving solves the issue of the reduced output power [29].

Several high speed converters have been implemented using interleaved methods. A 12 bit, 1.7 GS/s interleaved design with a multiplexed output is presented in [28]. Here, two RZ DACs are interleaved with an analog multiplexer on the output. A similar architecture was used in [30] to achieve 11 GS/s with 9 bits of resolution. The design in [31] uses switch transistors in each current cell to direct the output to the dummy output. This is done instead of having multiplexers on the outputs of the whole sub-DACs. This converter uses four, 3 GS/s input streams that are multiplexed together to make a 12 GS/s input. This

high speed input is then converted with two interleaved DACs. A 6 bit, 28 GS/s converter is presented in [32]. This design places the multiplexing switch transistors in the current cell. Another 6 bit DAC seen in [33], reached a sampling speed 56 GS/s. Finally, the design in [34] summed the outputs of two sub-DACs to cancel Nyquist images. Each sub-DAC was then made up of two RZ interleaved DACs to obtain a total conversion rate of 100 GS/s.

3.2 Implementation

The interleaved current steering DAC was implemented in the output summing configuration. Using this interleaved method, it was verified that the Nyquist images were reduced as expected. The block diagram of the interleaved DACs can be seen in Fig 3.2. The input comes from an ideal ADC that creates digital samples at 2.4 GHz. The clock speed on each sub-DAC is 1.2 GHz, and the clock phases are opposite phase of each other. The two positive outputs are shorted together, as well as the negative outputs. The differential outputs are converted to a single ended output via the differential amplifier. Finally, a low order filter is used to smooth the rectangular-like output into a sinusoid.

The transient output of the two times interleaved DAC is shown in 3.3. The top waveform is the clock that controls the ideal ADC. It can be seen the period of this clock is half of the sub-DAC clocks. The next two plots are the sub-DAC clocks, which can be seen to be 180 degrees out of phase. Finally, the summed output of the two sub-DACs is shown. The output clearly updates at a rate corresponding to the ADC clock.

The spectral performance of the parallel converters were tested by giving an input frequency of 325.78 MHz. The FFT plot of the output can be seen in Fig. 3.4. It is observed that the spurs and harmonics are greatly reduced, the measured SFDR is 75 dB. Next, the Nyquist image reduction property was tested. The plot in Fig. 3.5 shows the spectrum of a single DAC with a 596.48 MHz input. This input is near the Nyquist frequency, which is 600 MHz. The first Nyquist image is very prominent, having a signal power equal to the

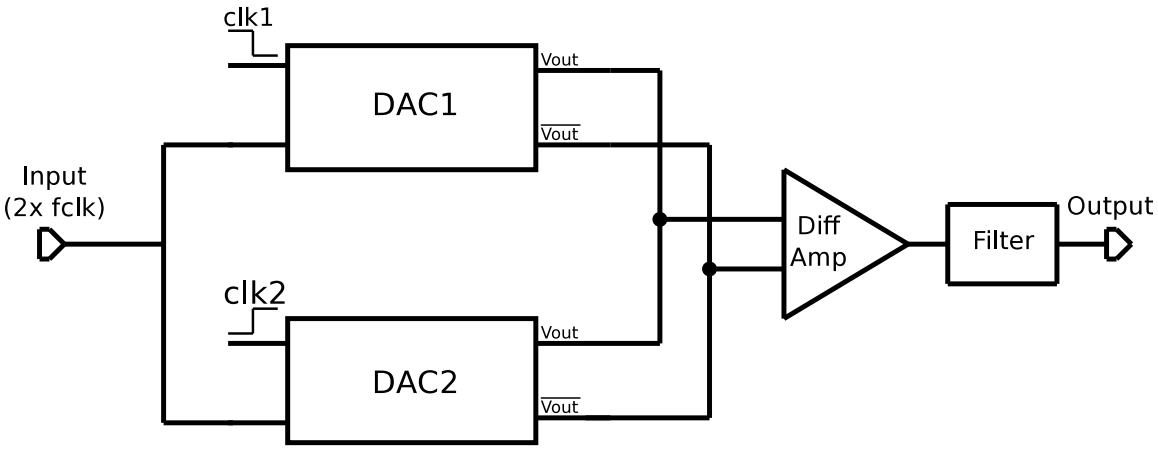

Figure 3.2: Block diagram of parallel DAC architecture.

fundamental signal. In Fig. 3.6, the spectrum of the interleaved DAC is shown. It can be seen that the image signal power is attenuated nearly 50 dB.

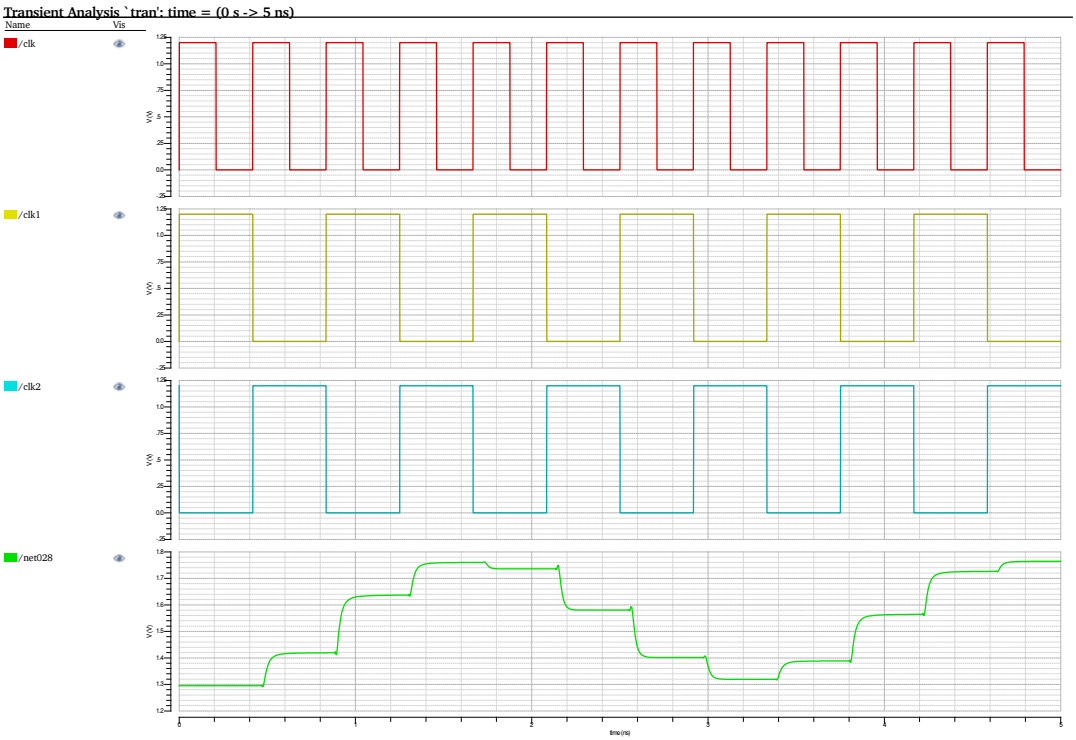

Figure 3.3: Parallel DAC with ADC clock, sub-DAC clocks, and summed DAC output.

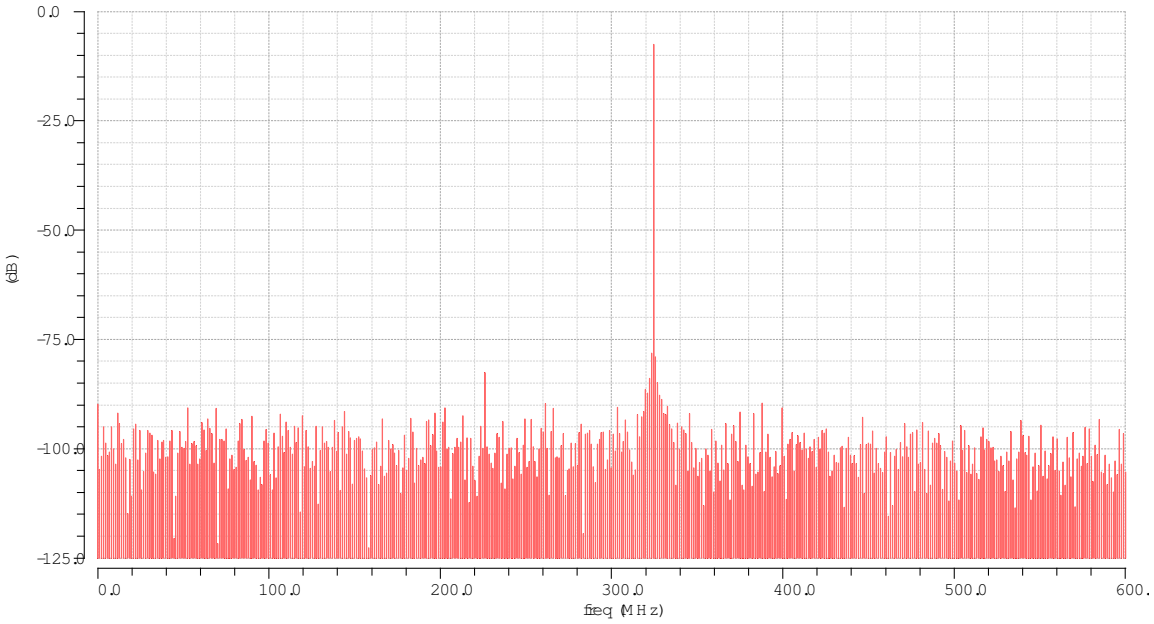

Figure 3.4: Interleaved DAC output FFT with 325.78 MHz input.

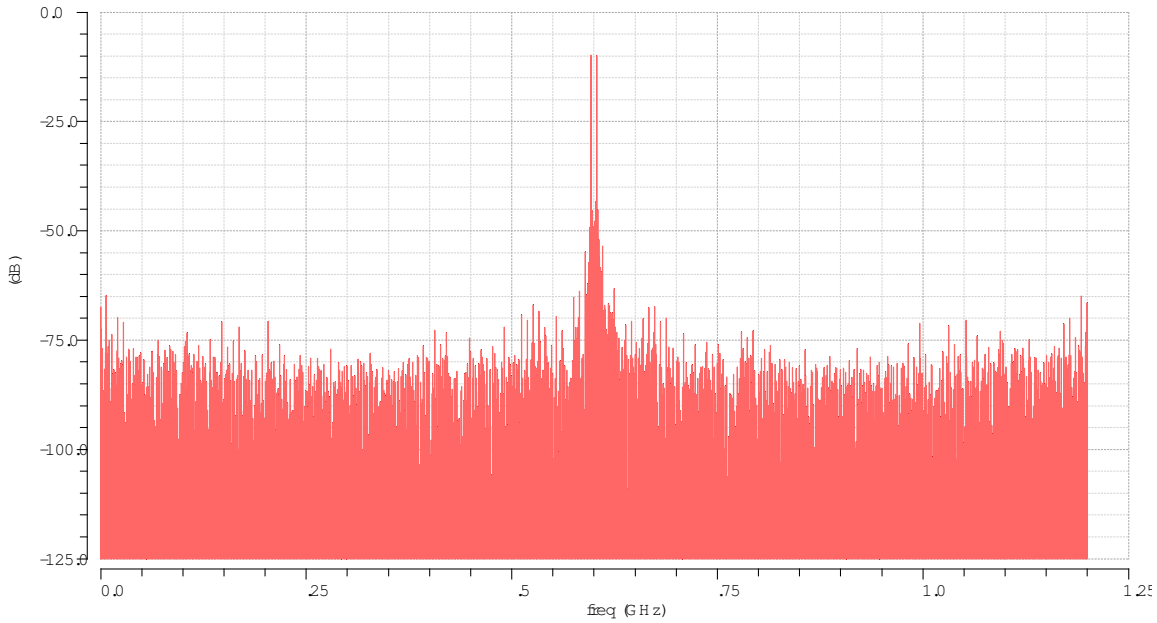

Figure 3.5: Standard DAC with input frequency of 596.48 MHz and large Nyquist image.

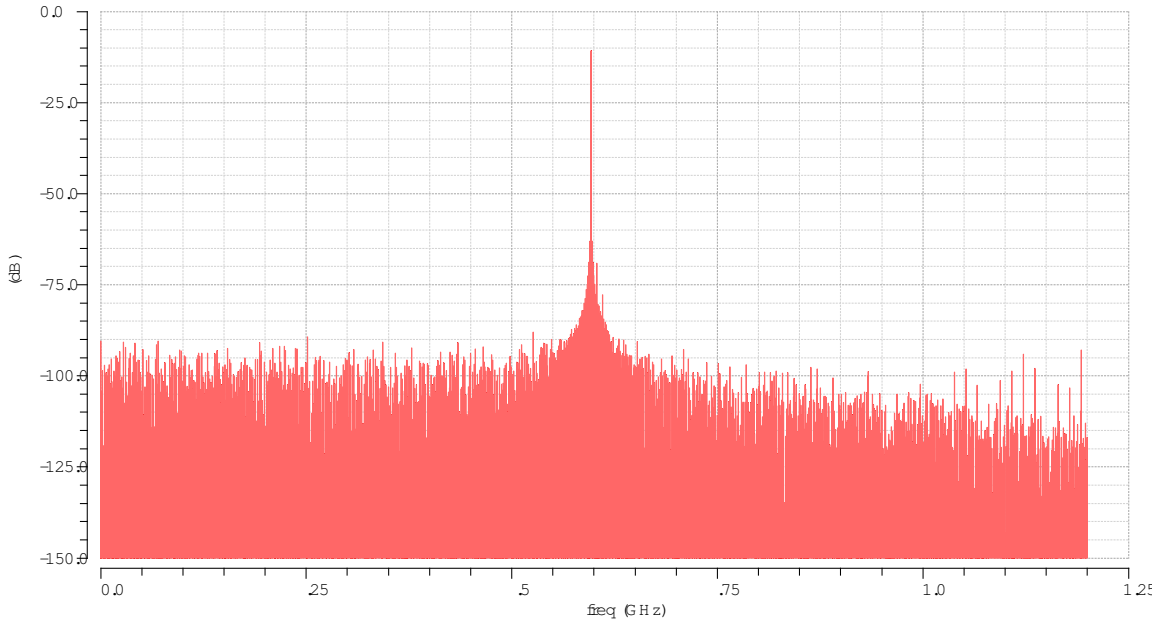

Figure 3.6: Parallel DAC with input frequency of 596.48 MHz and reduced Nyquist image.

Conclusion and Future Work

4.1 Conclusion

This thesis presented a high bandwidth digital to analog converter. The design procedure to ensure the converter is fast and accurate were shown. Each of the sub-circuits, such as the digital logic, current cells, and reconstruction filter were discussed. The following is a list of contributions from this thesis.

- A high bandwidth DAC is designed and implemented in 90 nm technology. Static linearity was comparable with the other works. The DNL and INL being measured at 0.022, and 0.29 respectively. The converter is able to operate at 1.2 GS/s with an input bandwidth up to 600 MHz. The update rate was only 50 GS/s less than the highest sampling rate of the compared works. This converter had the highest SFDR of compared works, measuring at 72.07 dB. The power dissipation is 43 mW, which is about 3 times less power than the converter with the highest sampling rate.

- A 10 order reconstruction filter was implemented. The Sallen-Key low pass active filter architecture was chosen. To obtain 10 filter orders, five second order filters were cascaded. The cutoff frequency of the filter is 430 MHz.

- Interleaving techniques were investigated to improve performance. By summing the outputs of the two parallel DACs, significant reduction in Nyquist images was shown.

4.2 Future Work

A few things could be done to potentially increase performance. The digital sub-circuits could be further optimized for low power and less propagation delay. The use of current mode logic (CML) could be investigated for the digital circuits. This could allow sampling rates approaching 2 GHz to be obtained. Dynamic element matching, and other automated matching techniques could be incorporated in order to improve the static linearity and reduce the impact of process variation. A bandgap voltage reference could be implemented to provide a stable bias voltage to current cells. Finally, interleaved techniques could be further explored to greatly increase the sampling rate of the converter.

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