

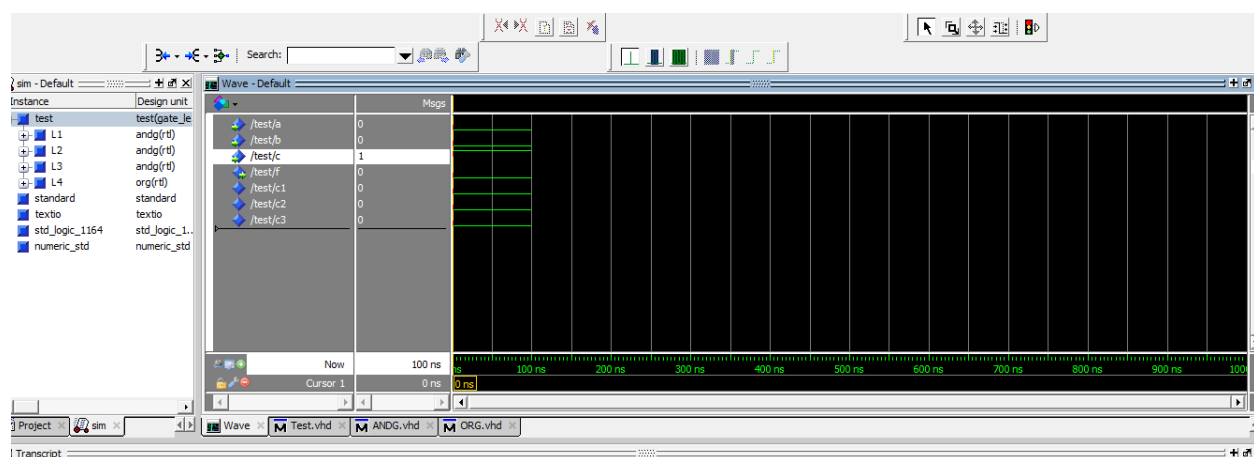
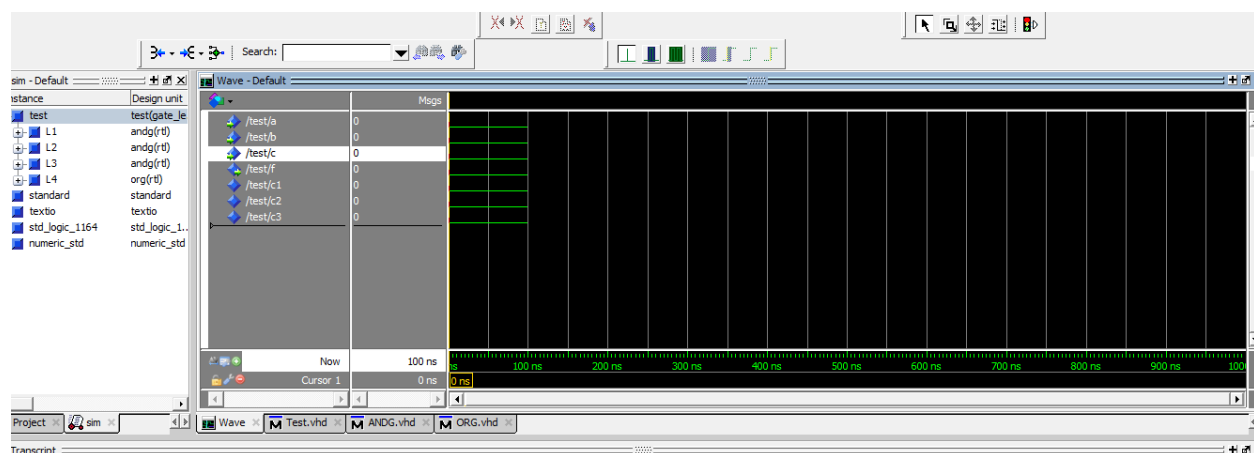
برای طراحی یک سیستم تشخیص اکثریت 3 بیتی، در سطح گیت و با زبان وی اچ دی ال در نرم افزار مدل سیم سه ماژول در نهایت طراحی شد که ماژول اصلی در اینجا "تست" نام گرفته است.

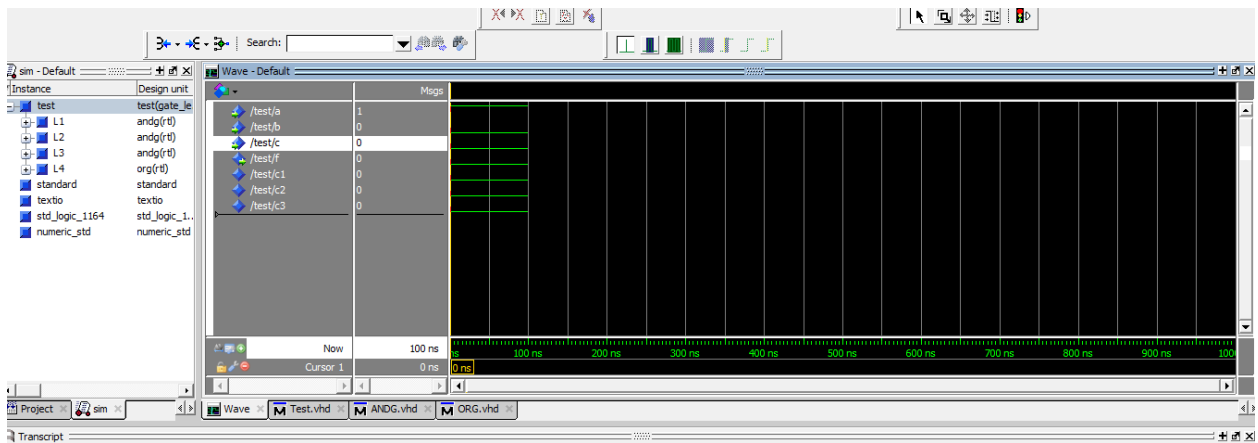
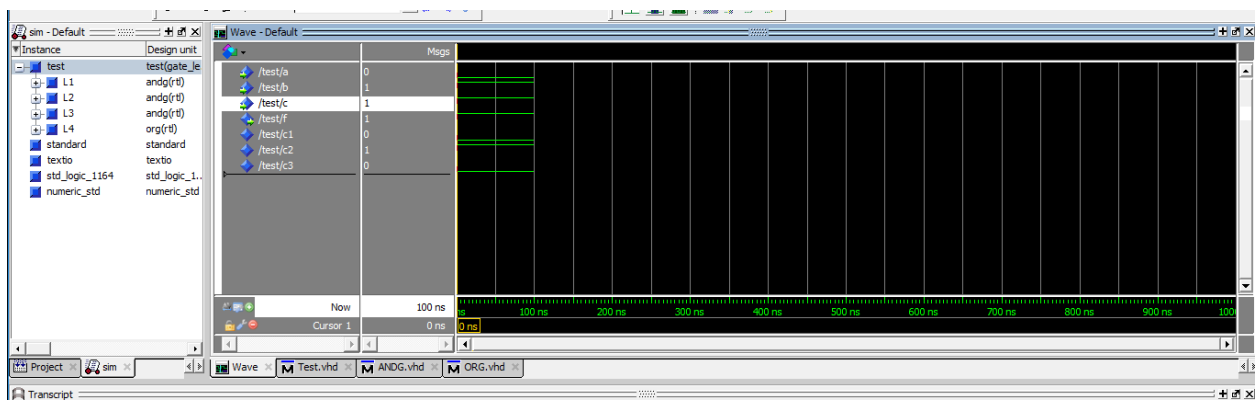
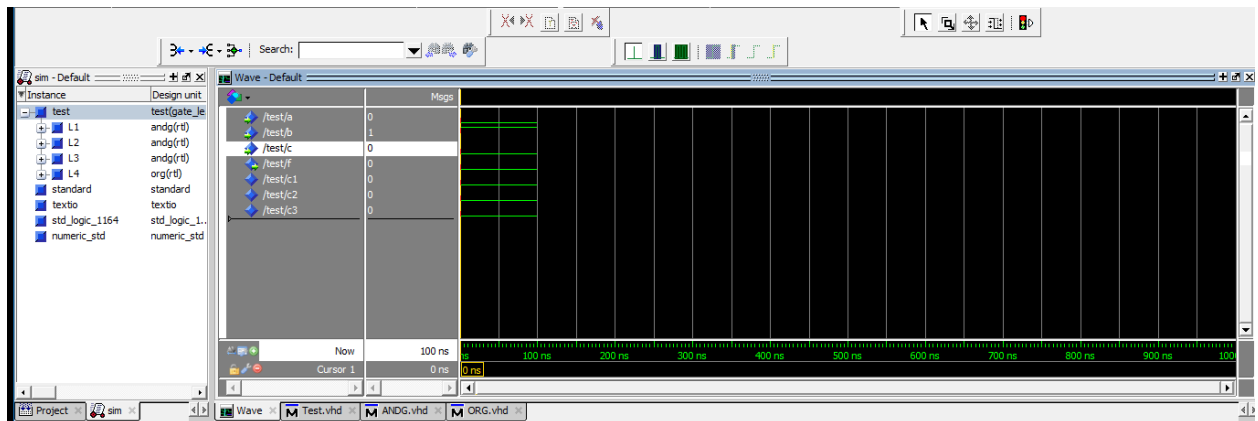
شبیه سازی در هر دو نرم افزار مدل سیم و ویو ادو انجام گرفته است.

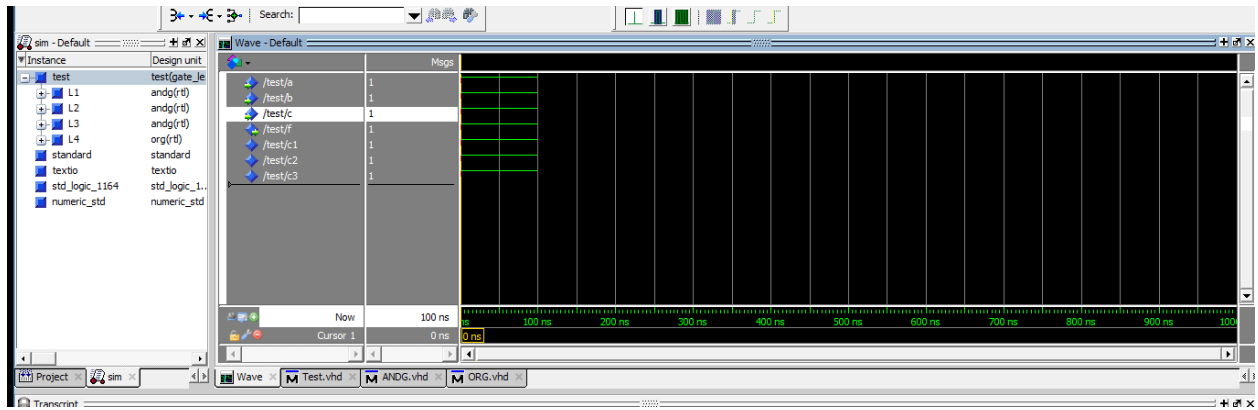
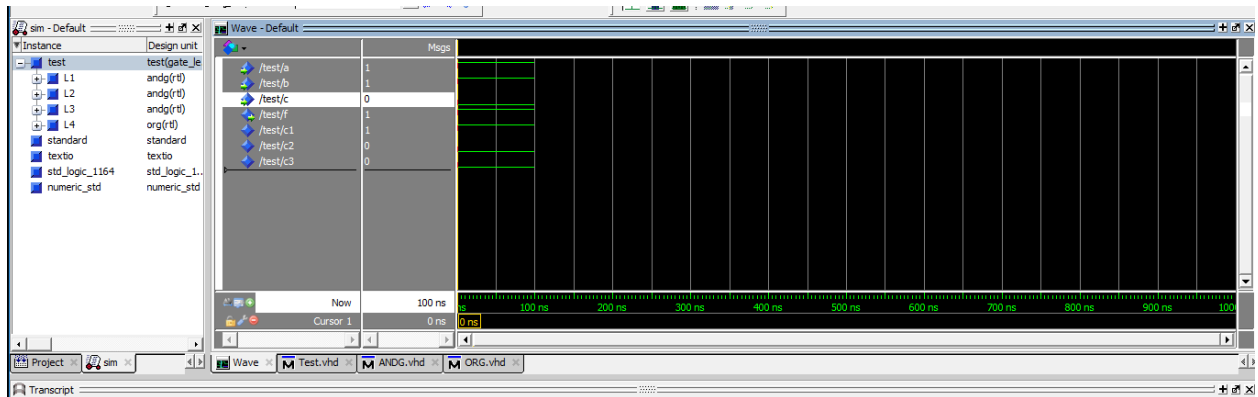
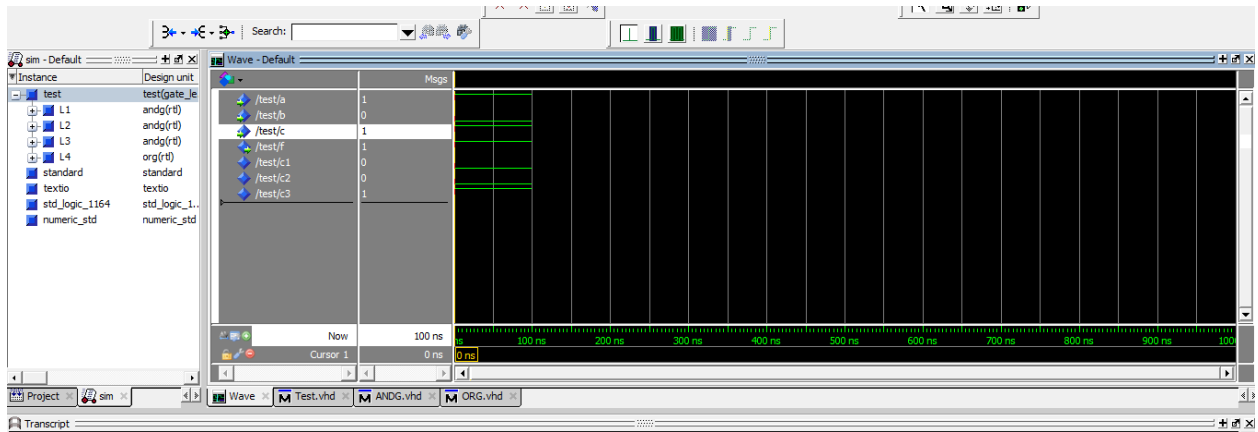
هستند. (Or و AND دو ماژول دیگر گیت های )

نتایج سیگنال های خروجی و ورودی:

شبیه سازی در مدل سیم







## شبیه سازی در نرم افزار ویواندو:\*

project\_1 - [C:/Users/Admin/Desktop/project\_1/project\_1.xpr] - Vivado 2015.4

File Edit Flow Tools Window Layout View Run Help

Implementation Complete

Flow Navigator

- IP Catalog
- IP Integrator
  - Create Block Design
  - Open Block Design
  - Generate Block Design
- Simulation
  - Simulation Settings
  - Run Simulation
- RTL Analysis
  - Elaboration Settings
  - Open Elaborated Design
- Synthesis
  - Synthesis Settings
  - Run Synthesis
  - Open Synthesized Design
- Implementation
  - Implementation Settings
  - Run Implementation
  - Open Implemented Design
- Program and Debug
  - Bitstream Settings
  - Generate Bitstream
  - Open Hardware Manager

Behavioral Simulation Functional - sim\_1 - Test

Scopes

Name	Design Unit	Block Type
Test	Test(GATE_LEV...	VHDL Entity
L1	ANDG(t)	VHDL Entity
L2	ANDG(t)	VHDL Entity
L3	ANDG(t)	VHDL Entity
L4	ORG(t)	VHDL Entity

Objects

Name	Value	Data Type
a	J	Logic
b	U	Logic
c	U	Logic
f	U	Logic
c1	U	Logic
c2	U	Logic
c3	U	Logic

Untitled 1

Name	Value
a	J
b	U
c	U
f	U
c1	U
c2	U
c3	U

Tcl Console

```
# run 1000ns
xsim: Time (s): cpu = 00:00:12 ; elapsed = 00:00:12 . Memory (MB): peak = 898.324 ; gain = 0.000
INFO: [USF-XSim-96] XSim completed. Design snapshot 'Test_behav' loaded.
INFO: [USF-XSim-97] XSim simulation ran for 1000ns
launch_simulation: Time (s): cpu = 00:00:16 ; elapsed = 00:00:38 . Memory (MB): peak = 898.324 ; gain = 0.000
```

Type a Tcl command here

Tcl Console Messages Log

Search the web and Windows

12:45 PM 10/6/2017

:000

project\_1 - [C:/Users/Admin/Desktop/project\_1/project\_1.xpr] - Vivado 2015.4

File Edit Flow Tools Window Layout View Run Help

Implementation Complete

Flow Navigator

- IP Catalog
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  - Create Block Design
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  - Generate Bitstream
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Behavioral Simulation Functional - sim\_1 - Test

Scopes

Name	Design Unit	Block Type
Test	Test(GATE_LEV...	VHDL Entity
L1	ANDG(t)	VHDL Entity
L2	ANDG(t)	VHDL Entity
L3	ANDG(t)	VHDL Entity
L4	ORG(t)	VHDL Entity

Objects

Name	Value	Data Type
a	0	Logic
b	0	Logic
c	0	Logic
f	0	Logic
c1	0	Logic
c2	0	Logic
c3	0	Logic

Untitled 1

Name	Value
a	0
b	0
c	0
f	0
c1	0
c2	0
c3	0

Tcl Console

```
add_force (/Test/a) -radix hex (0 0ns)
add_force (/Test/b) -radix hex (0 0ns)
add_force (/Test/c) -radix hex (0 0ns)
run all
add_force (/Test/c) -radix hex (1 0ns)
```

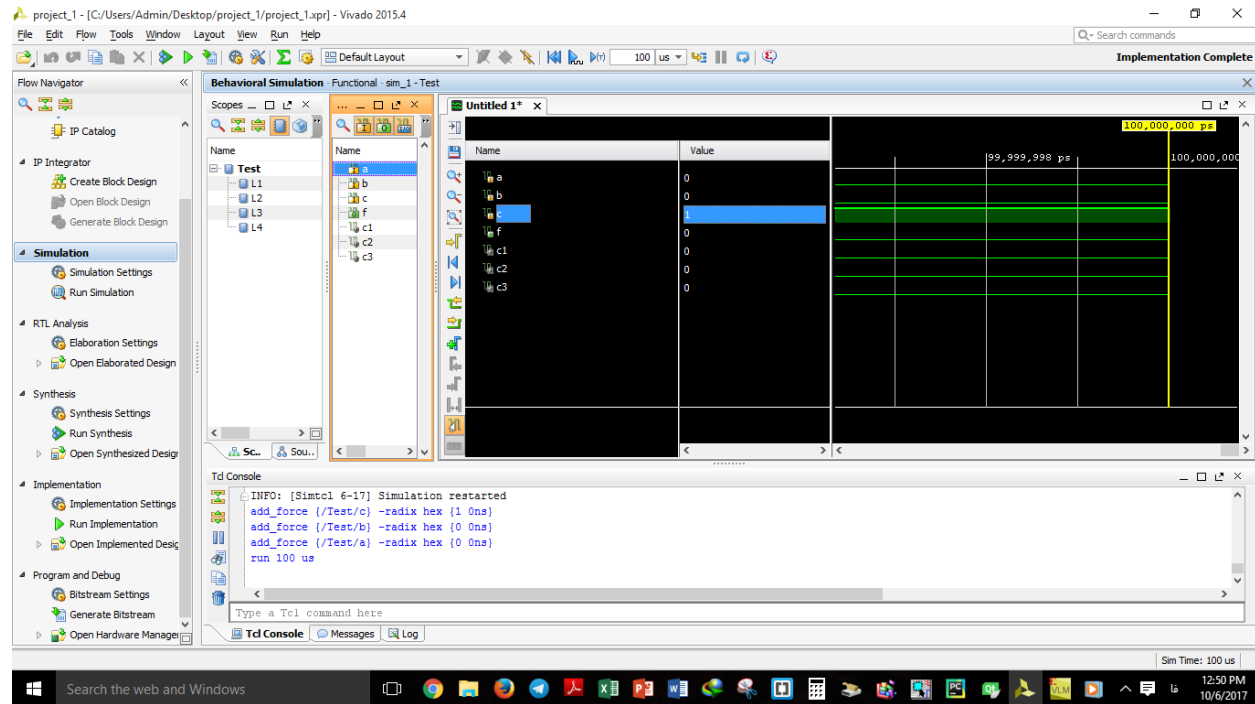
Type a Tcl command here

Tcl Console Messages Log

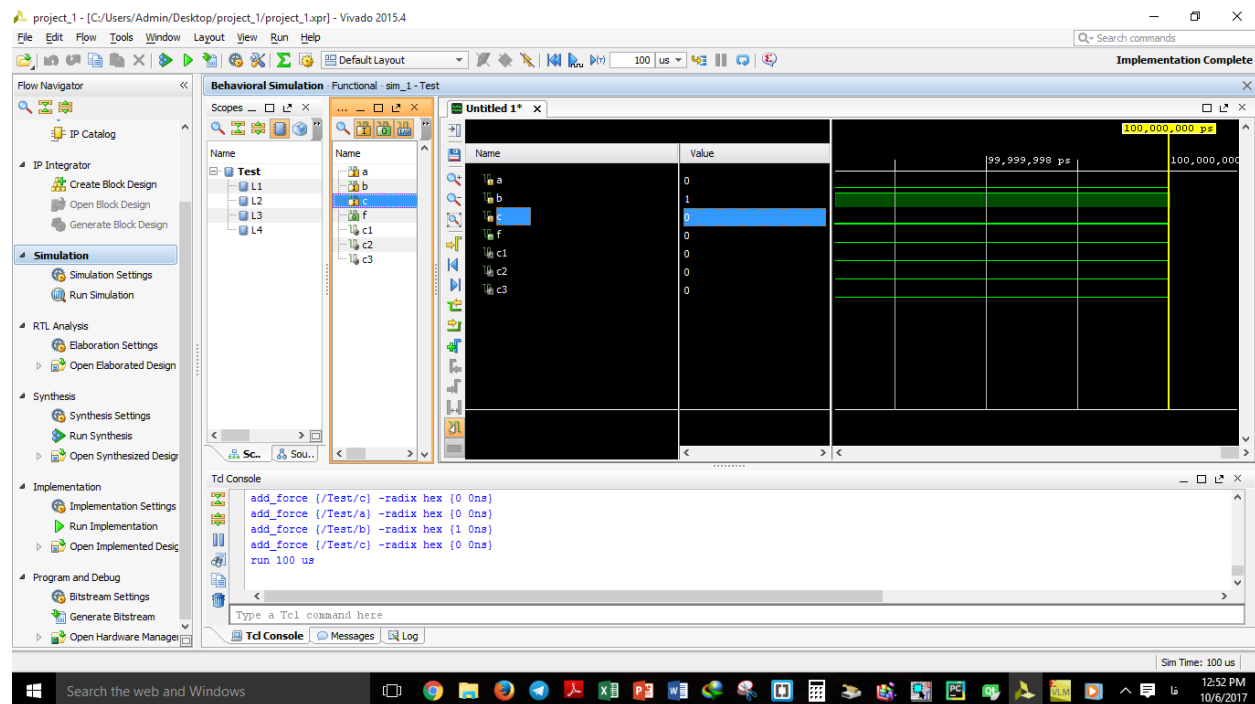
Search the web and Windows

12:49 PM 10/6/2017

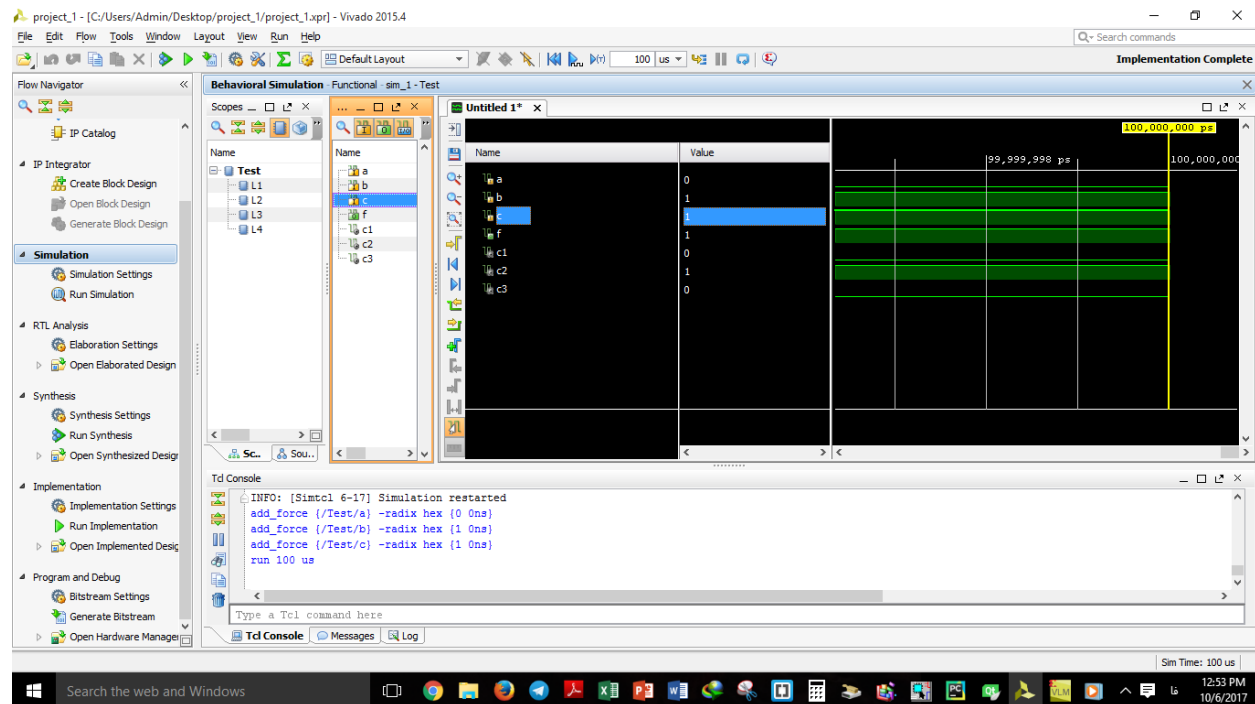
001



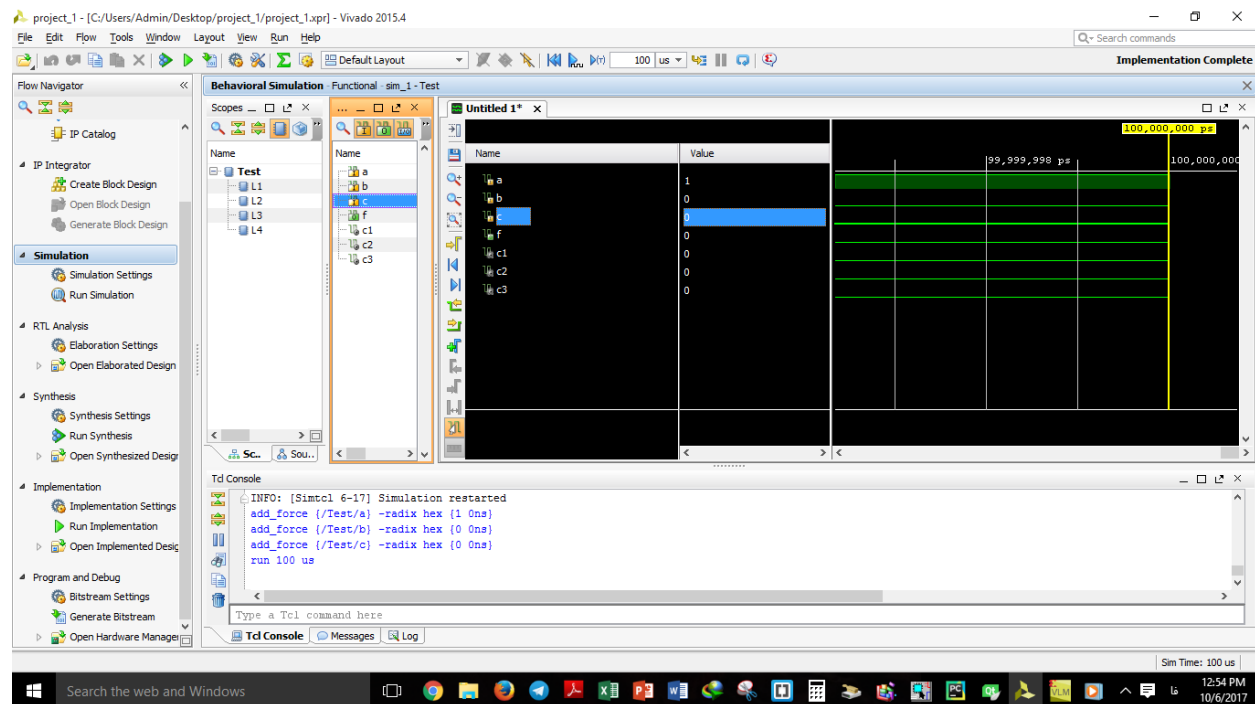
:010



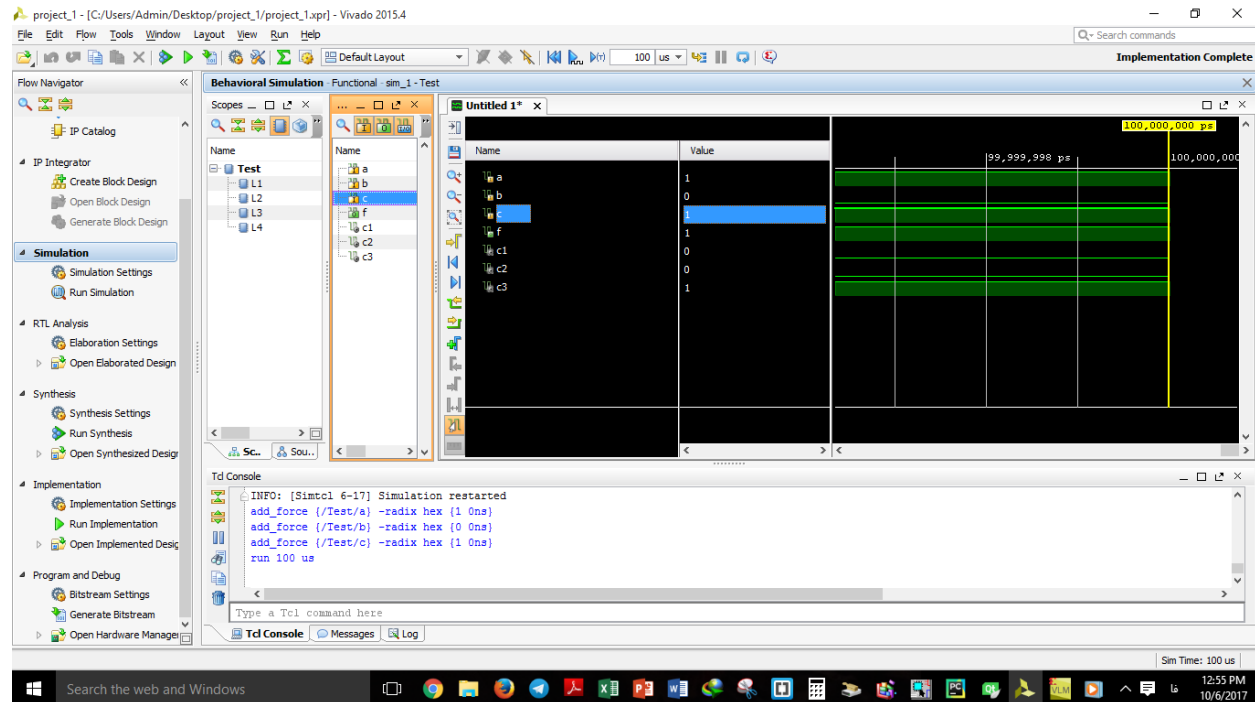
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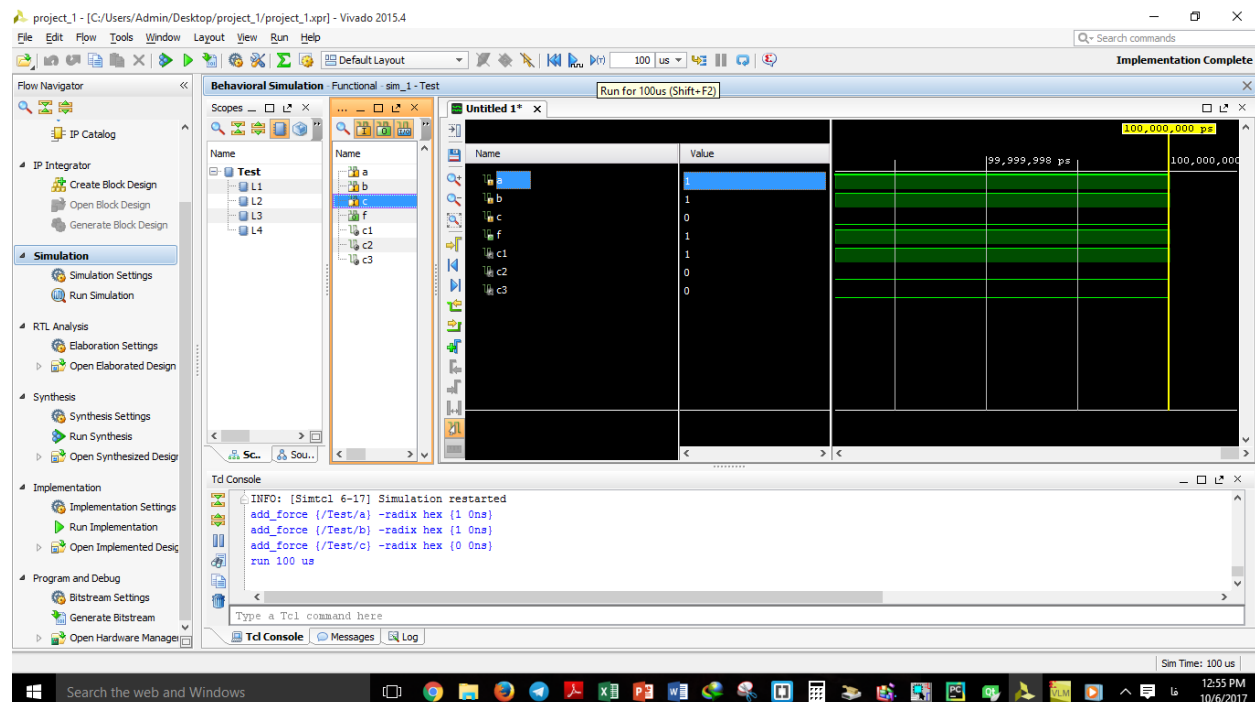
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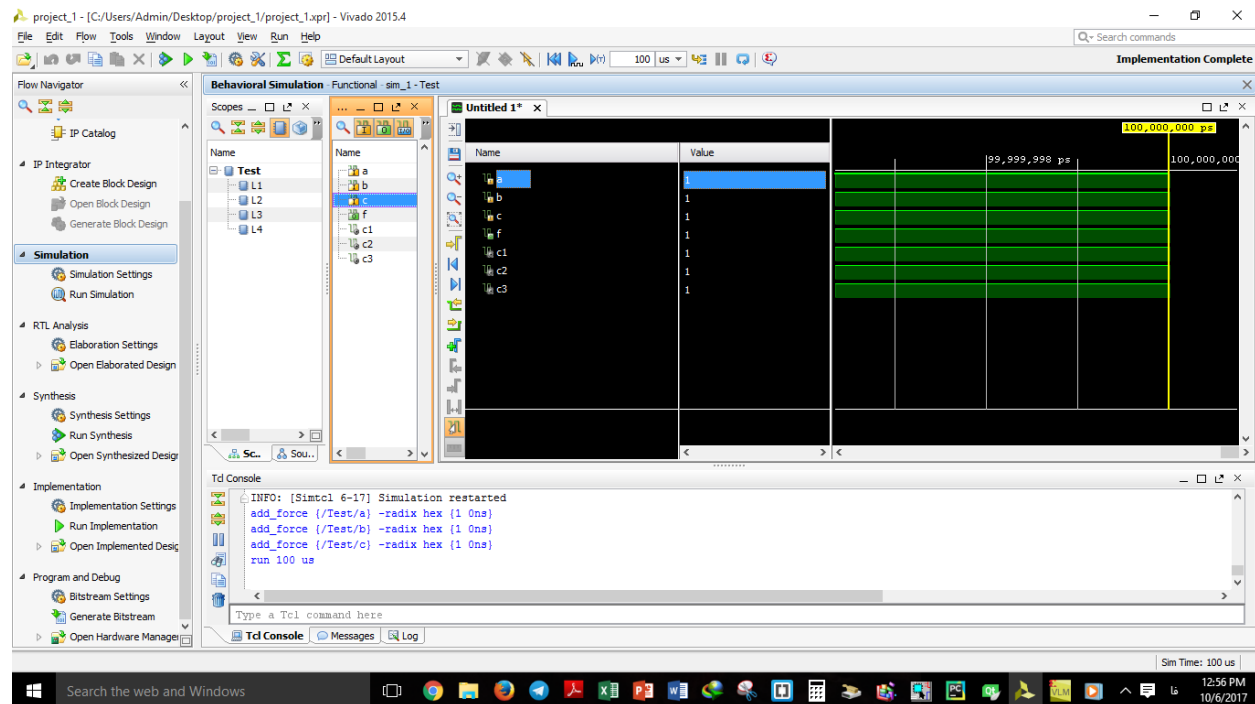
:101



:110



:111



بدین ترتیب طرز کار مدار مشخص میشود و یک سیستم تشخیص اکثریت 3 بیتی طراحی کرده ایم که در حالتی که حداقل دوتا از بیت ها، 1 باشند، خروجی 1 خواهد داد و در غیر این صورت خروجی 0 می دهد.