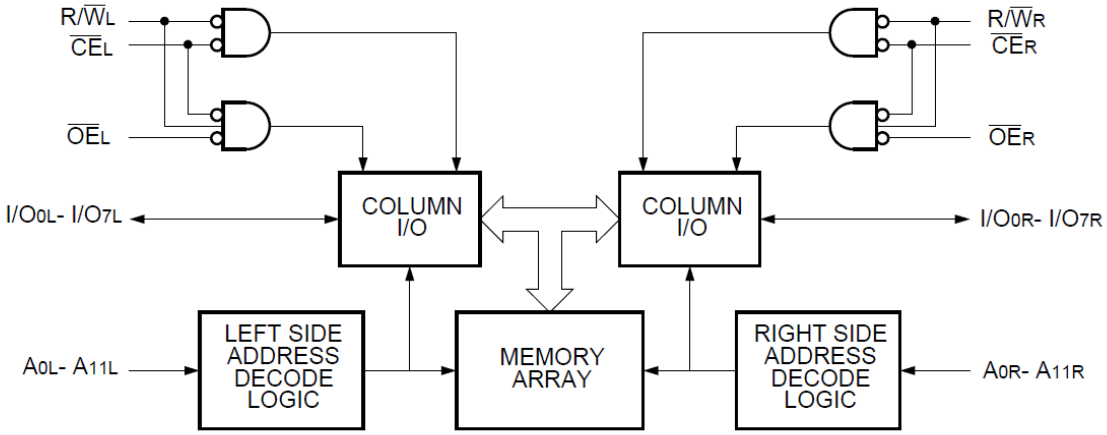
1)

الف)

شکل مربوط به زمانبندی خواندن از حافظه و یافتن پارامترهای زمانی یک تراشه ی Ram ۴ کیلوبایتی را از دیتا شیت آن استخراج کنید.

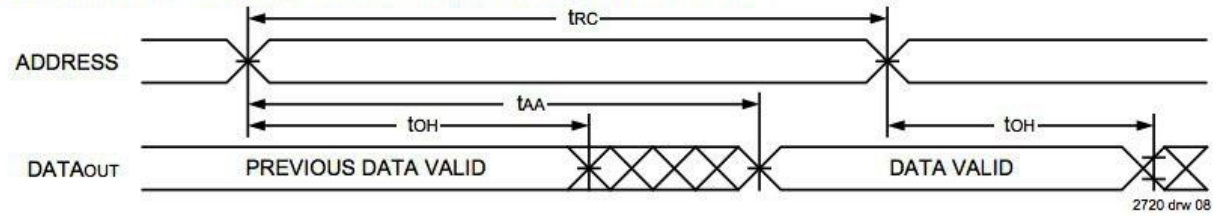
نام تراشه: IDT7134SA/LA

FUNCTIONAL BLOCK DIAGRAM



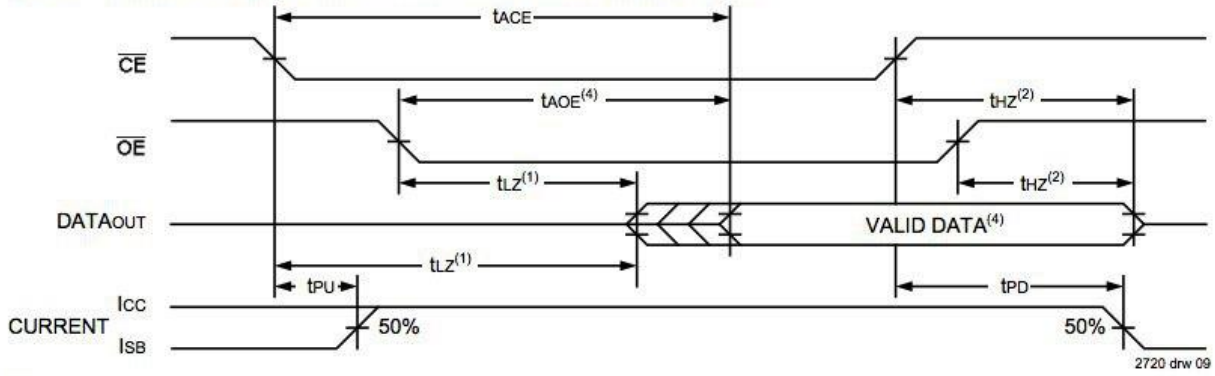
زمانبندی خواندن از حافظه و پارامترهای زمانی:

TIMING WAVEFORM OF READ CYCLE NO. 1, EITHER SIDE(1,2,4)



NOTES:
1. Timing depends on which signal is asserted last, $\overline{OE}$ or $\overline{CE}$.
2. Timing depends on which signal is de-asserted first, $\overline{OE}$ or $\overline{CE}$.
3. R/$\overline{W}$ = VIH.

TIMING WAVEFORM OF READ CYCLE NO. 2, EITHER SIDE(1,3)



NOTES:
1. Timing depends on which signal is asserted last, $\overline{OE}$ or $\overline{CE}$.
2. Timing depends on which signal is de-asserted first, $\overline{OE}$ or $\overline{CE}$.
3. R/$\overline{W}$ = VIH.
4. Start of valid data depends on which timing becomes effective, tAOE, tACE or tAA
5. tAA for RAM Address Access and tSAA for Semaphore Address Access.

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE[3,4]

Symbol	Parameter	7134X20 Com'l Only		7134X25 Com'l & Military		7134X35 Com'l & Military		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t_{RC}	Read Cycle Time	20	—	25	—	35	—	ns
t_{AA}	Address Access Time	—	20	—	25	—	35	ns
t_{ACE}	Chip Enable Access Time	—	20	—	25	—	35	ns
t_{AOE}	Output Enable Access Time	—	15	—	15	—	20	ns
t_{OH}	Output Hold from Address Change	0	—	0	—	0	—	ns
t_{LZ}	Output Low-Z Time[1,2]	0	—	0	—	0	—	ns
t_{HZ}	Output High-Z Time[1,2]	—	15	—	15	—	20	ns
t_{PU}	Chip Enable to Power Up Time[2]	0	—	0	—	0	—	ns
t_{PD}	Chip Disable to Power Down Time[2]	—	20	—	25	—	35	ns

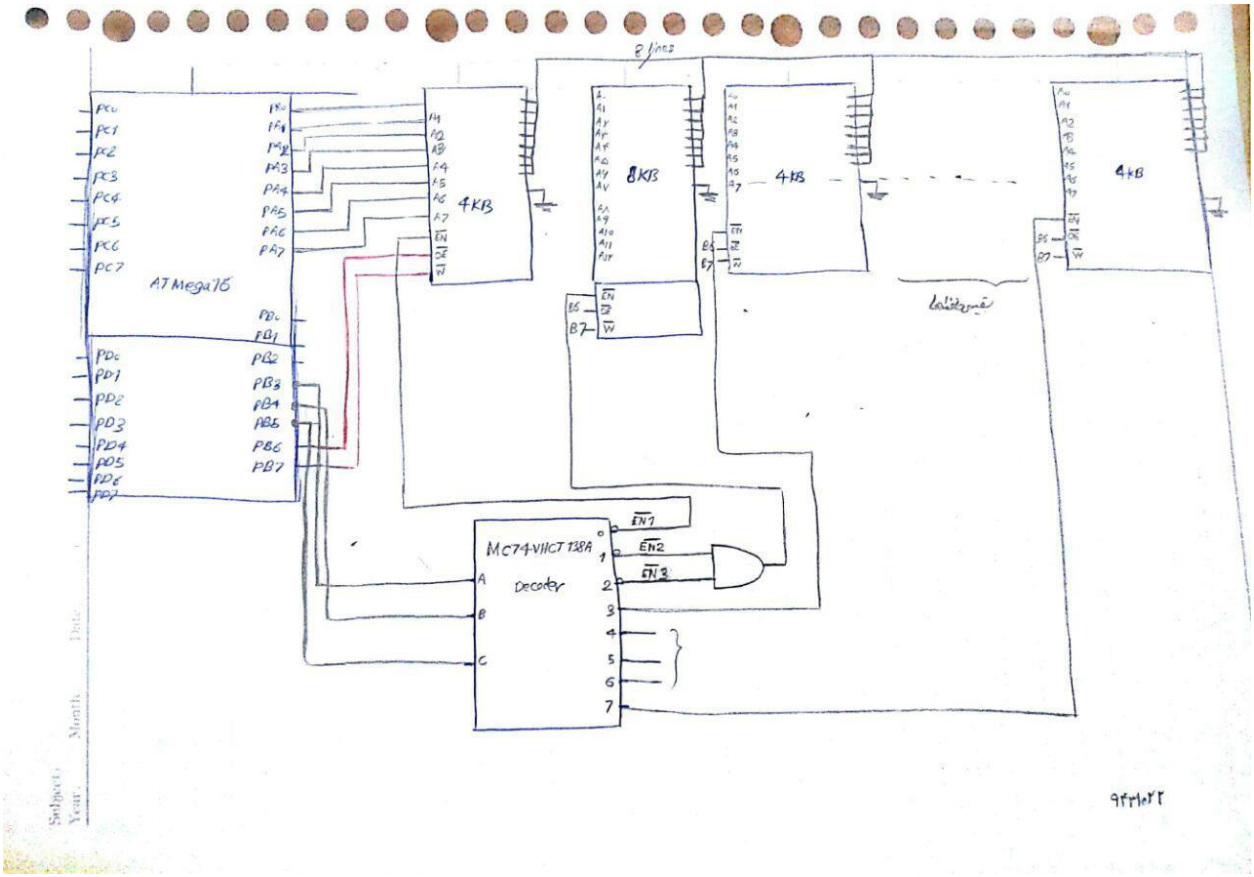
2720 tbl 09a

Symbol	Parameter	7134X45 Com'l & Military		7134X55 Com'l, Ind & Military		7134X70 Com'l & Military		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t_{RC}	Read Cycle Time	45	—	55	—	70	—	ns
t_{AA}	Address Access Time	—	45	—	55	—	70	ns
t_{ACE}	Chip Enable Access Time	—	45	—	55	—	70	ns
t_{AOE}	Output Enable Access Time	—	25	—	30	—	40	ns
t_{OH}	Output Hold from Address Change	0	—	0	—	0	—	ns
t_{LZ}	Output Low-Z Time[1,2]	5	—	5	—	5	—	ns
t_{HZ}	Output High-Z Time[1,2]	—	20	—	25	—	30	ns
t_{PU}	Chip Enable to Power Up Time[2]	0	—	0	—	0	—	ns
t_{PD}	Chip Disable to Power Down Time[2]	—	45	—	50	—	50	ns

2720 tbl 09b

NOTES:
1. Transition is measured ±500mV from Low or High-impedance voltage with the Output Test Load (Figures 1 and 2).
2. This parameter is guaranteed by device characterization, but is not production tested.
3. "X" in part number indicates power rating (SA or LA).
4. Industrial temperature: for other speeds, packages and powers contact your sales office.

دیکودر پیشنهادی باید یک دیکودر ۳ به ۸ باشد که در اینجا مدل MC74VHCT138A را انتخاب کردیم.


ATMega16
4KB
8KB
4KB
4KB
MC74VHCT138A
Decoder
EN1
EN2
EN3

2)

در خصوص انواع و حجم حافظه های موجود در میکروکنترلر STMF32 توضیح دهید.

حافظه ی داخلی:

- Memories:
  - Up to 1 Mbyte of Flash memory
  - Up to 192+4 Kbytes of SRAM including 64-Kbyte of CCM (core coupled memory) data RAM
  - Flexible static memory controller supporting Compact Flash, SRAM, PSRAM, NOR and NAND memories

۱.تا حجم ۲ مگابایت حافظه ی فلش داخلی دارد که در دوبلوک طراحی شده است که قابلیت خواندن و نوشتن دارند.

۵۱۲ کیلوبایت حافظه است که شامل ۱۲۸ کیلوبایت حافظه ی داده +TCM RAM: است
SRAM ۲
(برای داده هایREAL TIME)

۱۶,۳ کیلوبایت دستورات TCM RAM برای critical real-time routines + ۴ کیلوبایت

حافظه ی خارجی کنترلر همراه ۳۲ بیت دیتاباس

+

SRAM, PSRAM, SDRAM/LPSDR SDRAM, NOR/NAND memories

۴. حافظه ی اصلی و حافظه ی کش که دسترسی سریع دارند.

Internal Memories:

•Up to 2 Mbytes of Flash memory organized into two banks allowing read-while-write
•SRAM: 512 Kbytes (including 128 Kbytes of data TCM RAM for critical real-time data)
•+ 16 Kbytes of instruction TCM RAM (for critical real-time routines) + 4 Kbytes of backup SRAM
•Flexible external memory controller with up to 32-bit data bus: SRAM, PSRAM, SDRAM/LPSDR SDRAM, NOR/NAND memories
•Tightly Coupled Memory and cache memory are both fast access memories.
TCM: Tightly Coupled Memory interface PSRAM: Pseudo-static random-access memory SDRAM:

د)

```
;ReadDatafromAddress0500H,SRAMwith20nstAVQV(AddressAccessTime),
ResultinR0
;Propagationdelayof74138decoder:tpd(74ls138)=0ns.

LDIR16,00H;Address:LowByte
LDIR17,07H;Address:HighByte

;CALLMemRead

MemRead:LDIR18,FFH
OUTDDRA,R18 ;PORTAisOutput
OUTDDRB,R18 ;PORTBisOutput
LDIR18,00H
OUTDDRC,R18  ;PORTCisINPUT
OUTPORTA,R16
ANDIR17,BFH;
```

```
;SRAM#1Enabled;OtherSRAMsareDisabled,
;OutputEnabled

ORIR17,80H;;WritePin=1;ReadEnabled
OUTPORTB,R17
NOP
NOP;2NOP=2Clocks=2*62.5ns>tAVQV+1.5Clocks=20ns+1.5*62.5ns

INR0,PINC;ReadDatafromPortC
RET




;WriteDatatoAddress3900H,SRAMwith20nstWLWH(WritePulsewidth),
;12nstDVWH(DataValidToEndofWrite),and0nstWHDX(DataHoldTime),DatainR20
;Propagationdelayof74138decoder:tpd(74ls138)=0ns.

LDIR16,00H;Address:LowByte
LDIR17,40H;Address:HighByte
LDIR20,60H

CALLMemWrite

MemWrite:
LDIR18,FFH
OUTDDRA,R18;  PORTAisOutput
OUTDDRB,R18;  PORTBisOutput
OUTDDRC,R18;  PORTCisOutput
OUTPORTC,R20
OUTPORTA,R16
ANDIR17,7FH;;SRAM#3Enabled;OtherSRAMsareDisabled,
;PinWrite=0     ;WriteEnabled
ORIR17,40H;  ;OutputDisabled
OUTPORTB,R17

NOP;1NOP=1Clock=62.5ns>tWLWH=20ns
SBIPORTB,07;WritePin=1
NOP;1NOP=1Clock=62.5ns>tDVWH=12ns
RET
```