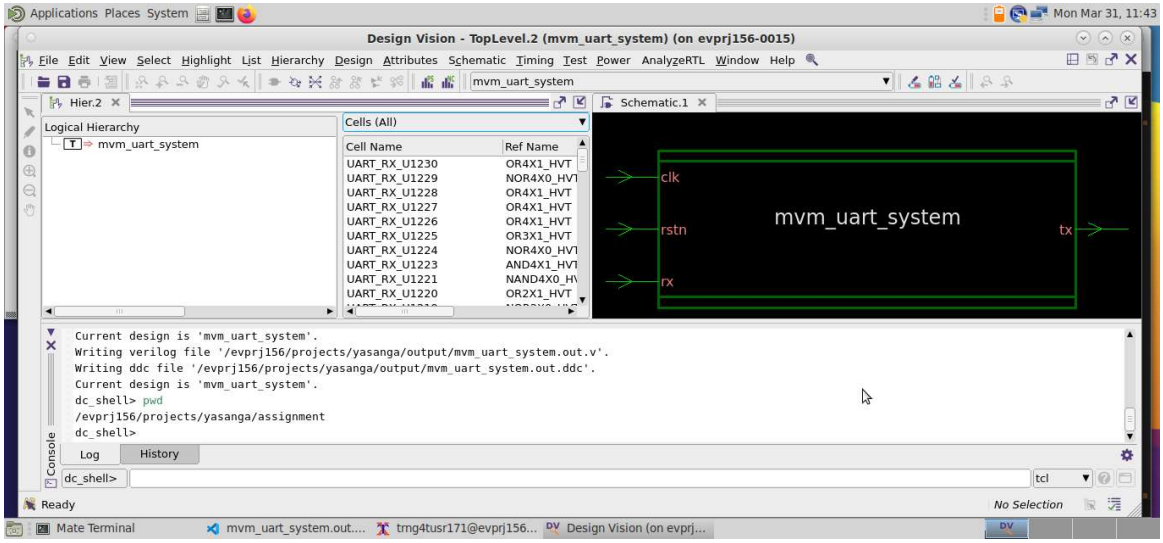
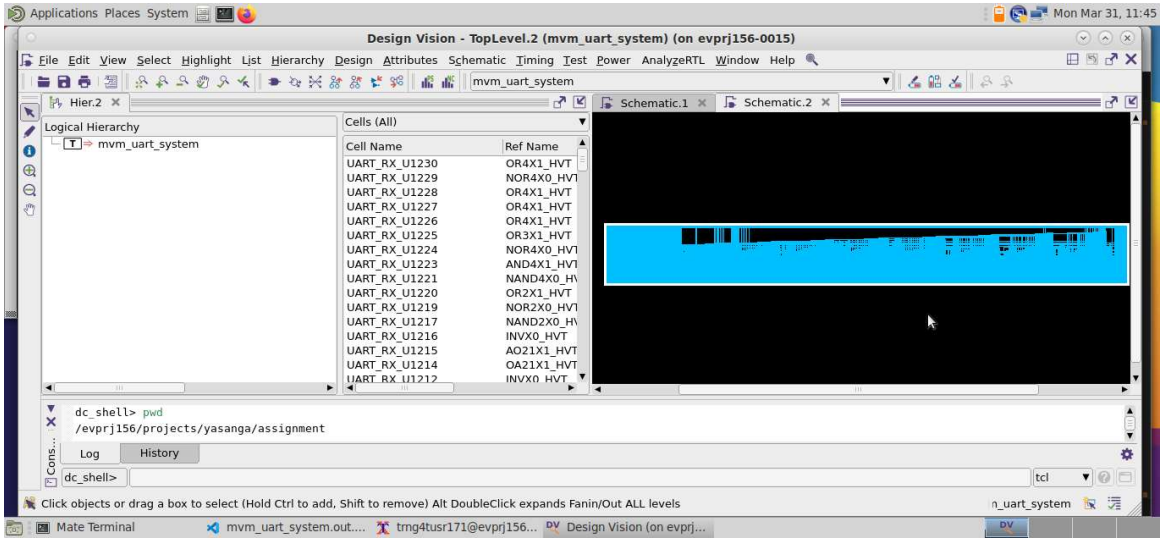
Deliverables

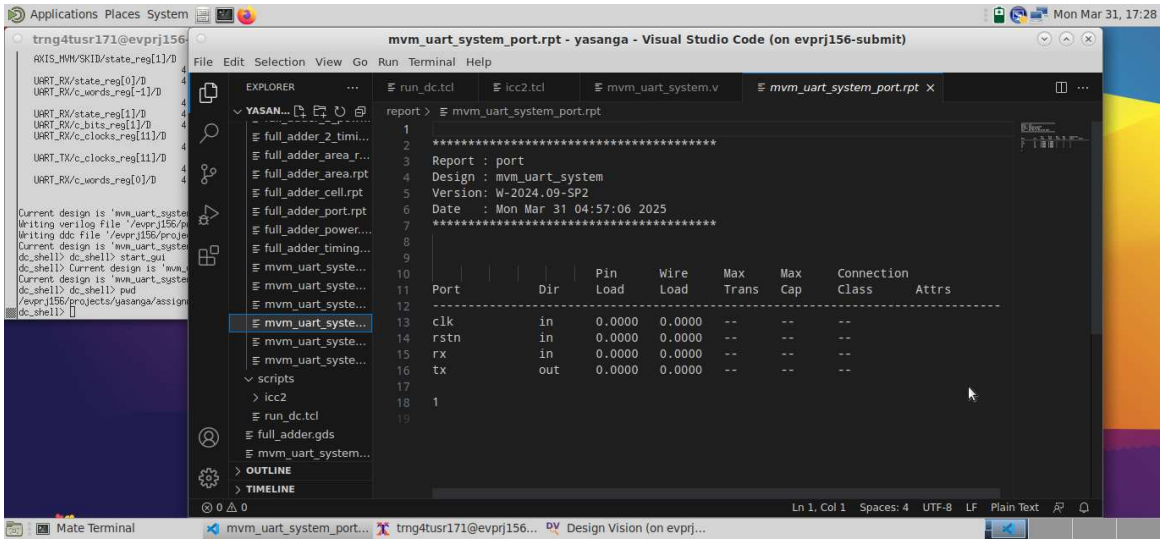
1. The synthesized RTL design schematic visualized in Design Vision of DC



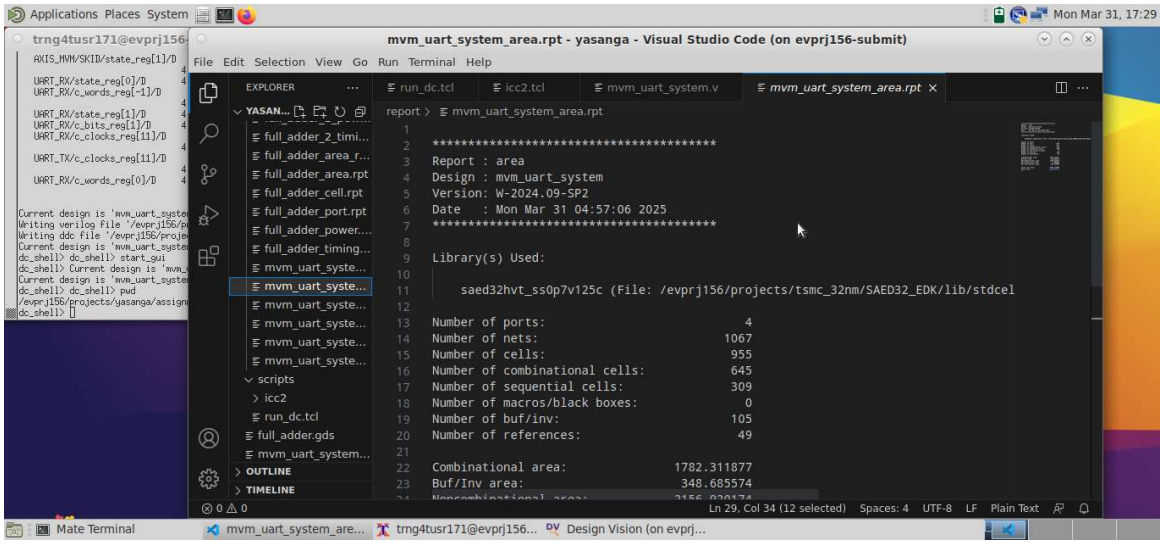


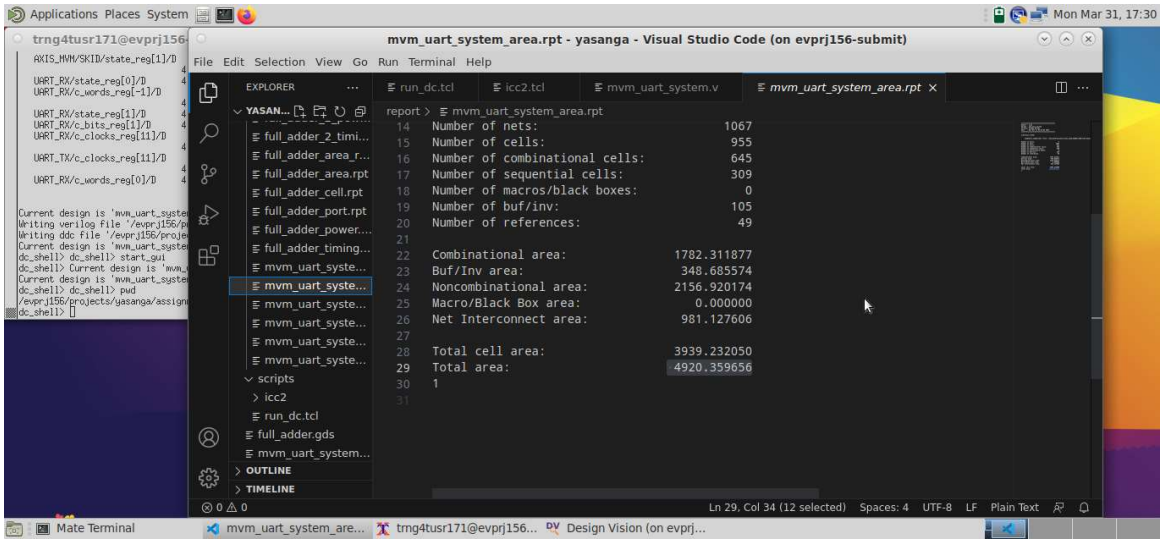
2. Different reports generated during the synthesis process of the mvm_uart_system

a) Ports

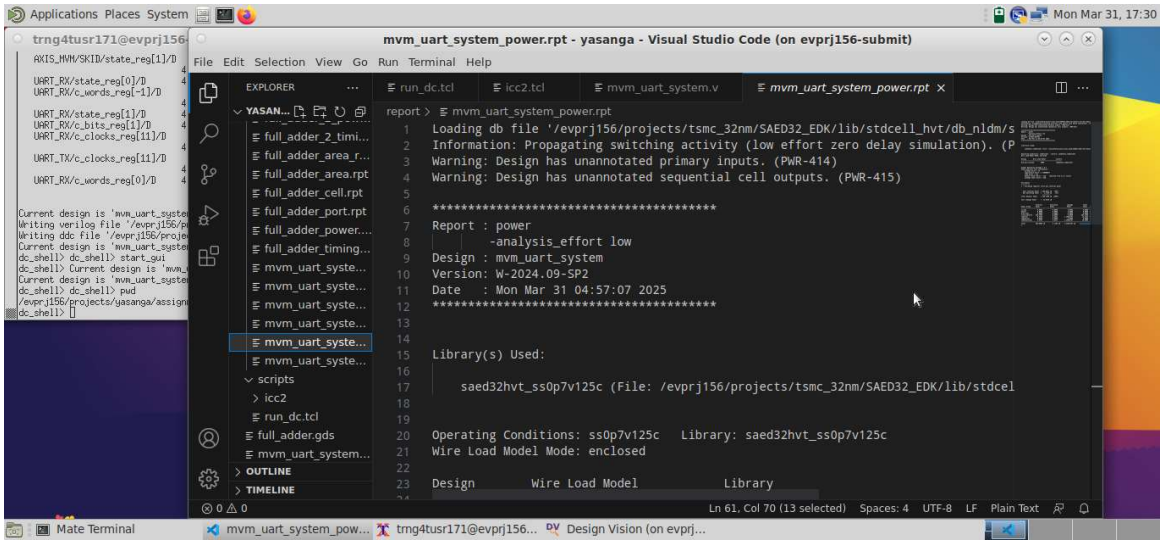


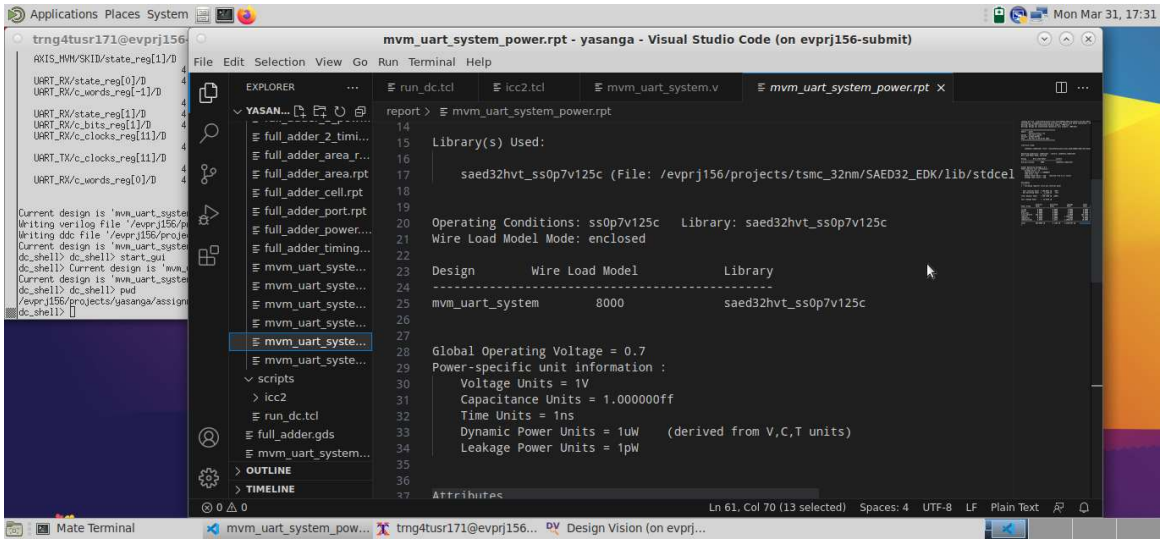
b) Area

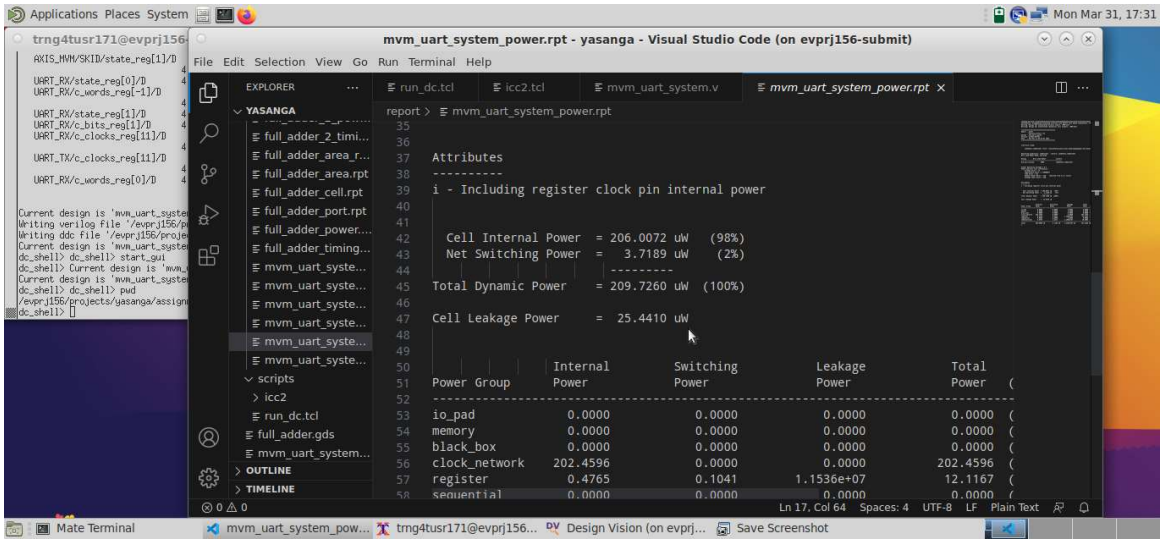


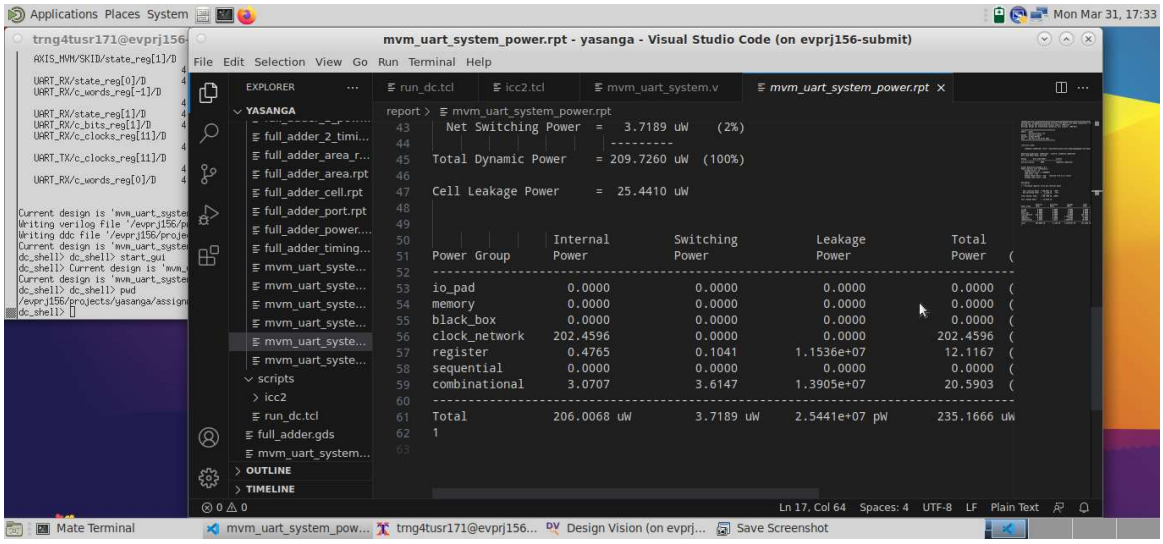

mvm_uart_system_area.rpt - yasanga - Visual Studio Code (on evprj156-submit)
Number of nets: 1067
Number of cells: 955
Number of combinational cells: 645
Number of sequential cells: 309
Number of macros/black boxes: 0
Number of buf/inv: 105
Number of references: 49
Combinational area: 1782.311877
Buf/Inv area: 348.685574
Noncombinational area: 2156.920174
Macro/Black Box area: 0.000000
Net Interconnect area: 981.127606
Total cell area: 3939.232050
Total area: 4920.359656

c) Power


mvm_uart_system_power.rpt - yasanga - Visual Studio Code (on evprj156-submit)
Loading db file '/evprj156/projects/tsmc_32nm/SAED32_EDK/lib/stdcell_hvt/db_nldm/s
Information: Propagating switching activity (low effort zero delay simulation). (P
Warning: Design has unannotated primary inputs. (PWR-414)
Warning: Design has unannotated sequential cell outputs. (PWR-415)
Report : power
-analysis_effort low
Design : mvm_uart_system
Version: W-2024.09-SP2
Date : Mon Mar 31 04:57:07 2025
Library(s) Used:
saed32hvt_ss0p7v125c (File: /evprj156/projects/tsmc_32nm/SAED32_EDK/lib/stdcel
Operating Conditions: ss0p7v125c Library: saed32hvt_ss0p7v125c
Wire Load Model Mode: enclosed
Design Wire Load Model Library

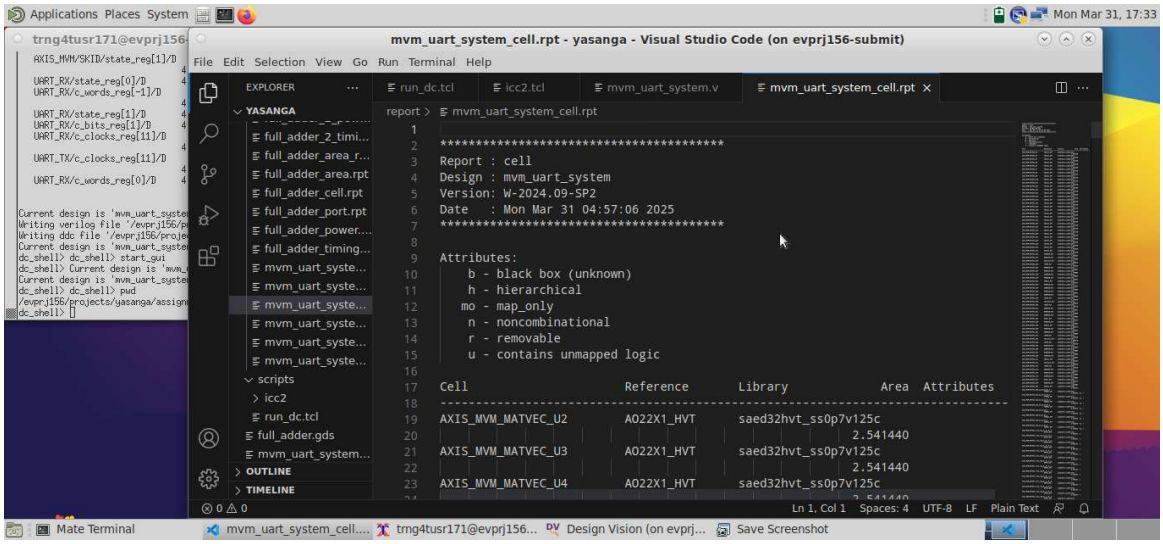

mvm_uart_system_power.rpt - yasanga - Visual Studio Code (on evprj156-submit)
Library(s) Used:
saed32hvt_ss0p7v125c (File: /evprj156/projects/tsmc_32nm/SAED32_EDK/lib/stdcel
Operating Conditions: ss0p7v125c Library: saed32hvt_ss0p7v125c
Wire Load Model Mode: enclosed
Design Wire Load Model Library
mvm_uart_system 8000 saed32hvt_ss0p7v125c
Global Operating Voltage = 0.7
Power-specific unit information :
Voltage Units = 1V
Capacitance Units = 1.000000ff
Time Units = 1ns
Dynamic Power Units = 1uW (derived from V,C,T units)
Leakage Power Units = 1pW

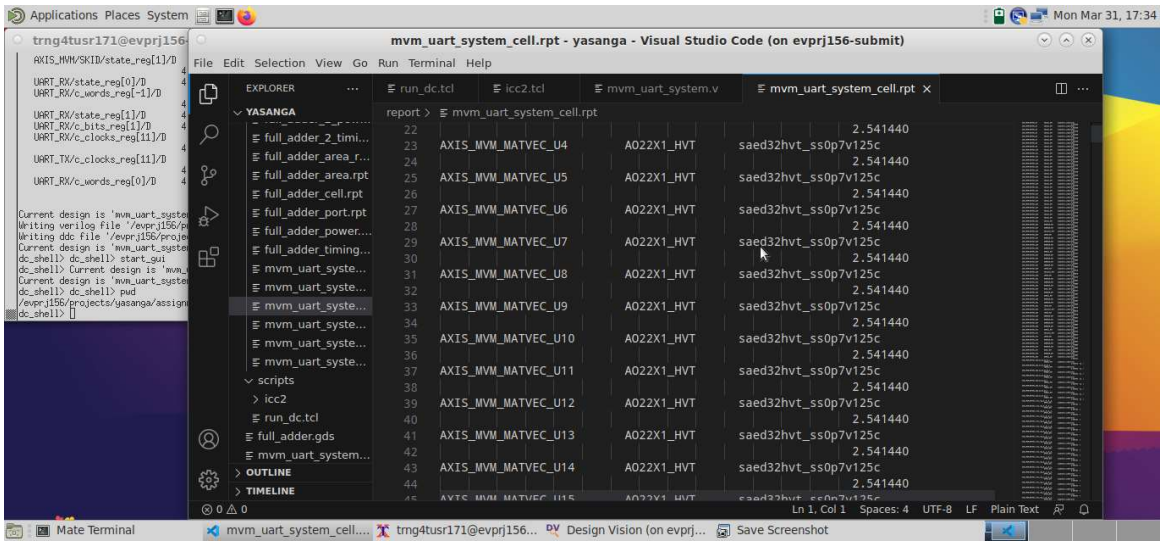




d) Timing e. No. of Cells

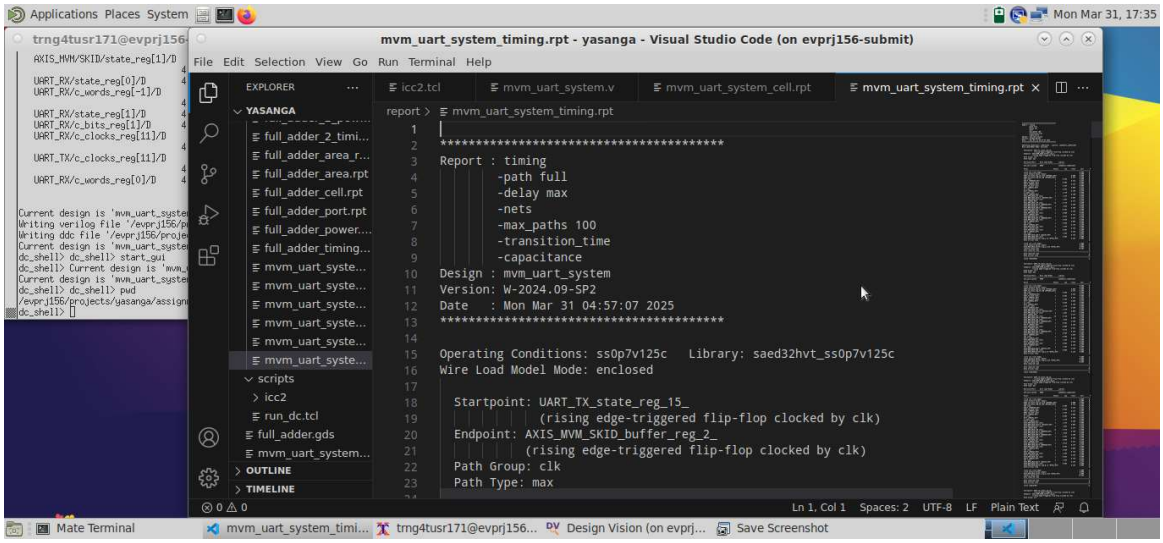
--Cells

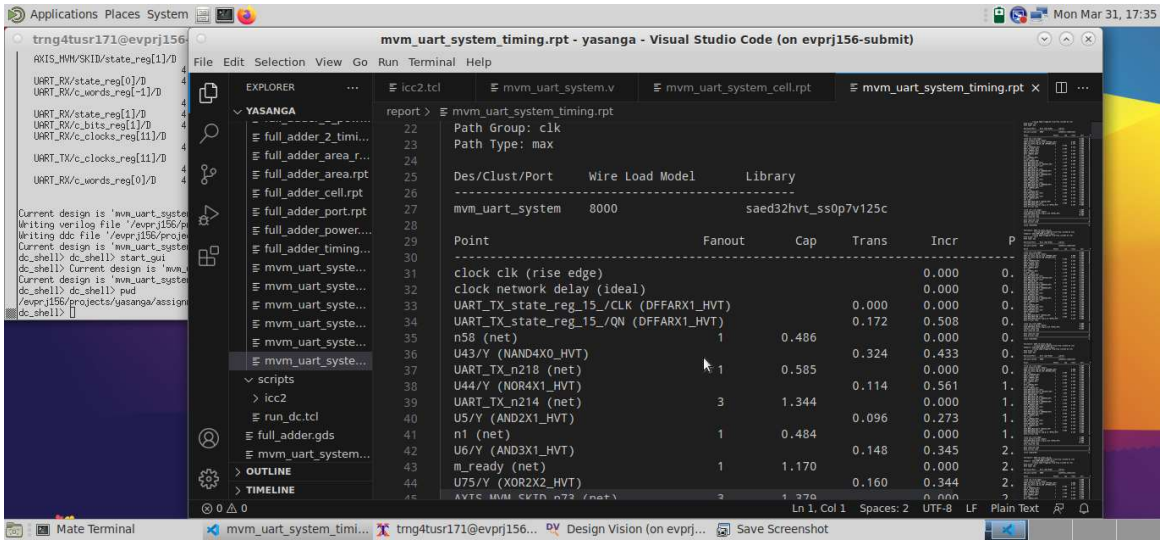


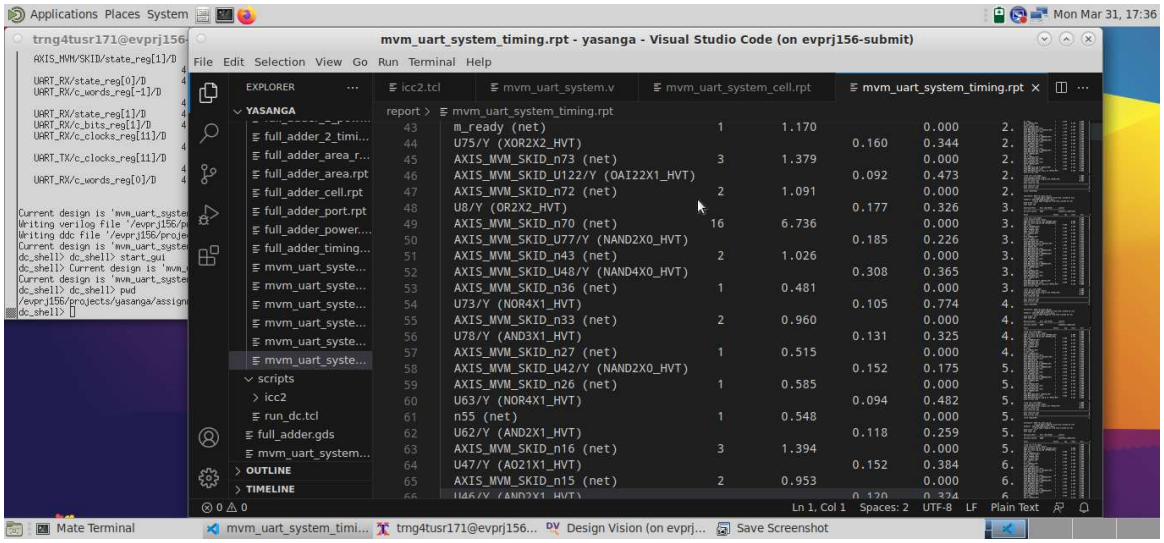


**Many Lines of Cells are here.

--Timing







**Many lines for the timing report are there as well.

3. synthesis step for several combinations of R, C, W_X, W_K parameter values in the top module

Parameter Values in the Top Module				Area	Power
R	C	W_X	W_K		
2	2	2	2	4920.359656	235.1666 uW
4	4	4	4	14942.525177	627.7156 uW
8	8	8	8	107730.521183	2.8218e+03 uW
1	3	5	7	6271.952093	268.8116 uW
2	4	6	8	13088.737178	475.7461 uW

4. The completed PnR layout visualized inside ICC2