Yasas Seneviratne

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SKILLS

■ **Programming Languages:** C/C++, Python, Java

■ Hardware Descriptive Languages: Verilog, SystemVerilog, VHDL

■ Compilers: LLVM

■ Operating Systems: Ubuntu kernel modification for hardware support

■ ISAs Associated: MIPS, x86, RISC-V, ARM

■ Computer Architecture Tools: gem5, PyMTL, zsim

■ Commercial Software: Synopsys SpyGlass, DC Ultra, IC Compiler, Verdi, VCS, Vivado, Vivado HLS, ISE,

Quartus 2, Intel Vtune

■ Open-source tools: Verilator

■ Hands-on FPGAs used: Alveo SN1000 SmartNIC, VCU118, VC707.

FDUCATION

■ Ph.D. Computer Engineering

Department of Computer Engineering University of Virginia (UVA) Advisors | Prof. Kevin Skadron & Prof. Samira Khan Area of Expertise | Computer Architecture Aug 2019 - Present Expected Completion Aug 2025

■ B.Sc. Honors Degree in Electronic & Telecommunication Engineering

Department of Electronic Telecommunication Engineering (ENTC) University of Moratuwa (UOM) Sri Lanka

Thesis | RISC-V base ISA processor design and implementation

Mar 2013 - Apr 2017

EXPERIENCE

■ Google Research | External Collaborator

Jun 2021 - Sep 2022

Hardware design with Google Research Learn to Design Accelerator Team

■ Synopsys | Research and Development Engineer

Apr 2017 - Jun 2019

Hardware accelerator design for Synopsys VCS (Verilog Compiler Simulator)

Nanyang Technological University | Research Intern

Oct 2015 - Apr 2016

Hardware and Embedded Systems Lab (HESL)

PUBLICATIONS

- [P3] Yao Hsiao, Yasas Seneviratne, Tommy Tracy, Kevin Skadron, Caroline Trippel. "Design for Hardware Memory Model Verification", PLARCH, 2023.
- [P2] Yasas Seneviratne, Korakit Seemakhupt, Sihang Liu, and Samira Khan, "NearPM: A Near-memory Processing Prototype for Storage-class Workloads", EuroSys, 2023.
- [P1] Korakit Seemakhupt, Sihang Liu, Yasas Seneviratne, Muhammad Shahbaz, and Samira Khan. "PMNet: In-Network Data Persistence", ISCA, 2021.

OTHER SELECTED PROJECTS

- Design and implementation of a soft processor based on RISC-V ISA. Pipeline design, test platform design and implementation in ZedBoard Zynq-7000 ARM/FPGA SoC Development Board by Digilent.(Four member team Semester 7-8 ENTC, UOM. 2016-2017).
- Design and implementation of an architecture for an embedded neural net accelerator based on Hopfield nets. Matlab simulation of the functionality, RTL simulation of the architecture in Verilog. (*two member team*, *ENTC*, *UOM*. 2016-2017)
- Design, verification, and simulation of a hardware bus supporting 2 Masters & 3 slaves. Design and simulation of Arbiter and Address decoder. (Four member team Semester 8 ENTC, UOM, 2016-2017).
- Design and implementation of an accelerator architecture for a real-time traffic density estimator. C simulation of the functionality, RTL simulation of the architecture in Verilog. Target platform: Virtex-7 FPGA VC707 Evaluation Kit by Xilinx. (*Individual*, NTU, SCE, HESL. 2015-2016)
- Design, simulation and implementation of a JPEG 2000 decoder. RTL simulation of the architecture in Verilog and implementation on Atlys Spartan-6 FPGA Trainer Board by Digilent. (Four member team Semester 5 ENTC, UOM. 2015).
- Designed and implementation of a 16 operand processor using Verilog HDL. Implemented on terasIC DEO-Nano development and education board. (Individual Semester 5 ENTC, UOM. 2015).

ACADEMIC ACHIEVEMENTS. SCHOLARSHIPS & HONORS

- Graduated with **second class upper division** honors from University of Moratuwa, Sri Lanka, 2017.
- Dean's listed in semester 2 (2013) and semester 3 (2013) for academic achievements in the department of Electronic and Telecommunication Engineering University of Moratuwa.
- Received "Pranama" scholarship for being one of the best students among Sri Lanka Insurance policyholders for General Certificate of Education (GCE) Advanced Level (A-level) examination 2011.
- Received "EDCS (Education Employees Co-operative Thrift & Credit Society)" scholarship for achievement in General Certificate of Education (GCE) Advanced Level (A-level) examination 2011.
- Ranked 3rd in the district 121st in Sri Lanka (top 0.5% amongst approximately 30,000 candidates) in the General Certificate of Education (GCE) Advanced Level (A-level) examination in the Physical Science Stream (Mathematics, Chemistry, Physics) conducted by the Department of Examinations of the Ministry of Education Sri Lanka, 2011.
- Received "Pranama" scholarship for being one of the best students among Sri Lanka Insurance policyholders for General Certificate of Education (GCE) Ordinary Level (O-level) examination 2008.

TEACHING EXPERIENCE

■ University of Virginia | Graduate Teaching Assistant

CS 6354 Graduate Computer Architecture

2021 Spring

CS 3330 Computer Architecture

2020 Fall

CS 3330 Computer Architecture

2020 Spring

VOLUNTEER ACTIVITIES

Artifact Reviewer:

54th IEEE/ACM International Symposium on Microarchitecture (MICRO 2021)

Clubs and Societies:

Rotaract Club of University of Moratuwa (2013 – 2017), E-Club University of Moratuwa (2013 – 2017).

Leadership:

Chairperson Gaming Fest computer gaming competition at University of Moratuwa, (2015).

Community Services:

E-Care 2017: Helping to build and repair infrastructure the under develop school Banagoda Vidyalaya, Ratnapura.

Inspirer 2014: English improving workshops conducted for two days at Badulla for Ordinary Level Students.

EXTRA-CURRICULAR ACTIVITIES

- Participated in events "Abina 2014/2015", "Sanda Midula 2015" organized by ENTC, "Hela Kam Kala 2012" as a rhythm guitarist.
- Participated in the Sri Lanka Robotics challenge (SLRC) 2014.
- Participated in the Inter School All-Island Hockey Tournament 2007 Representing the under 16 Hockey team of Central college Anuradhapura.
- Participated in representing Mahinda house in the annual Sports meets of Central College Anuradhapura.

Under 17 (2011): Cricket, Hockey

Under 15 (2009): Cricket, Hockey

Under 13 (2007): Cricket, Football