CSE-5358 MICROPROCESSOR SYSTEMS PROJECT REPORT

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INTRODUCTION

This project aims to interface a Synchronous DRAM (SDRAM MT48LC16M4A2) to an 8086-1 Microprocessor that supports only Asynchronous DRAM. This has been achieved by the design of the following SDRAM Controller using System Verilog.

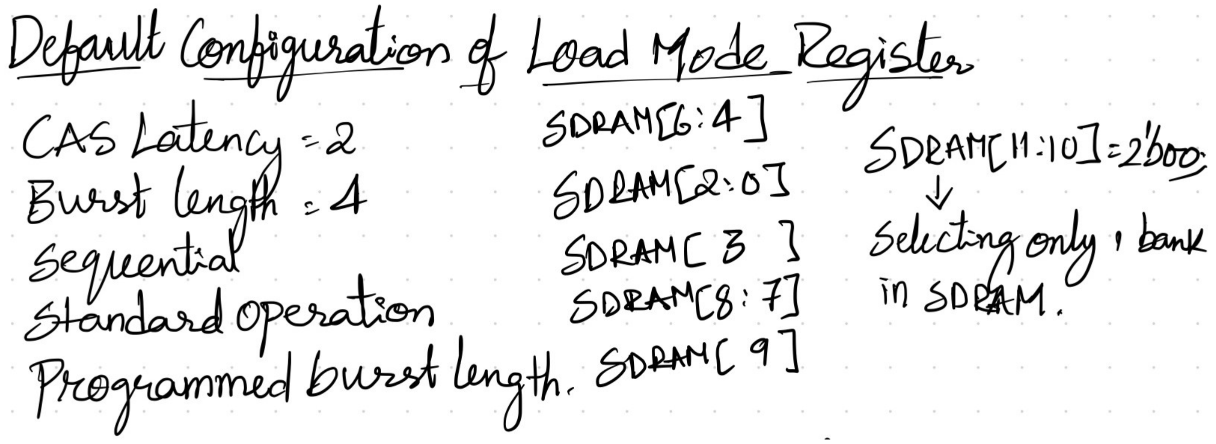
SDRAM SPECIFICATIONS

The SDRAM chip used:	MT48LC16M4A2
Configuration:	4 Meg x 4 x 4 banks
Speed Grade:	-75
Clock Frequency:	100MHz
CAS Latency:	2
Burst Length:	4

Address:

No of Rows:	2^{12}
No of Columns:	2^{10}
No of Memory Banks:	2^{2}
No of Bits from the Banks:	2^{2}
Total Memory Available:	64 MiB of which 512 KiB to be interfaced and used with the 8086.

Configuring the Load Mode Register:

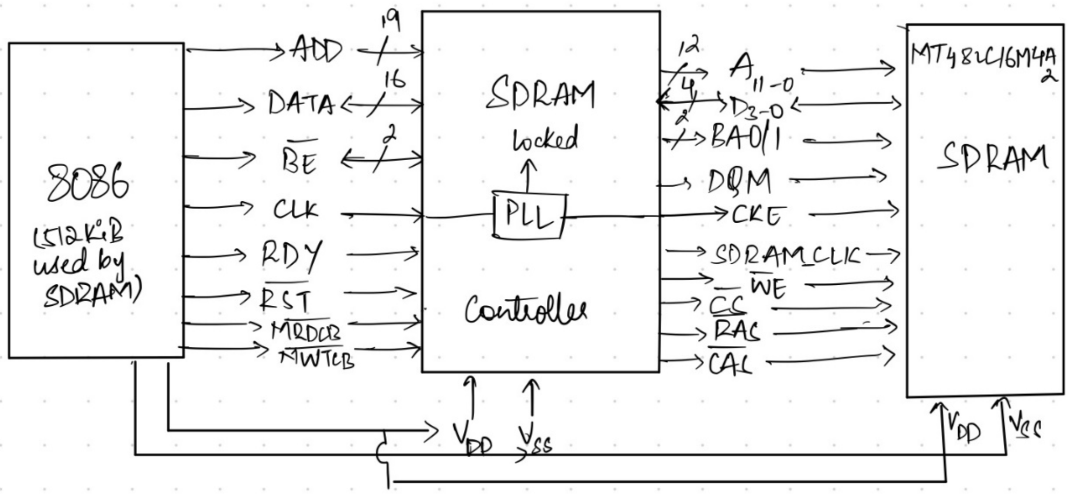


Default Configuration of Load Mode Register

CAS Latency = 2	SDRAM[6:4]
Burst length = 4	SDRAM[2:0]
Sequential	SDRAM[3]
Standard operation	SDRAM[8:7]
Programmed burst length.	SDRAM[9]

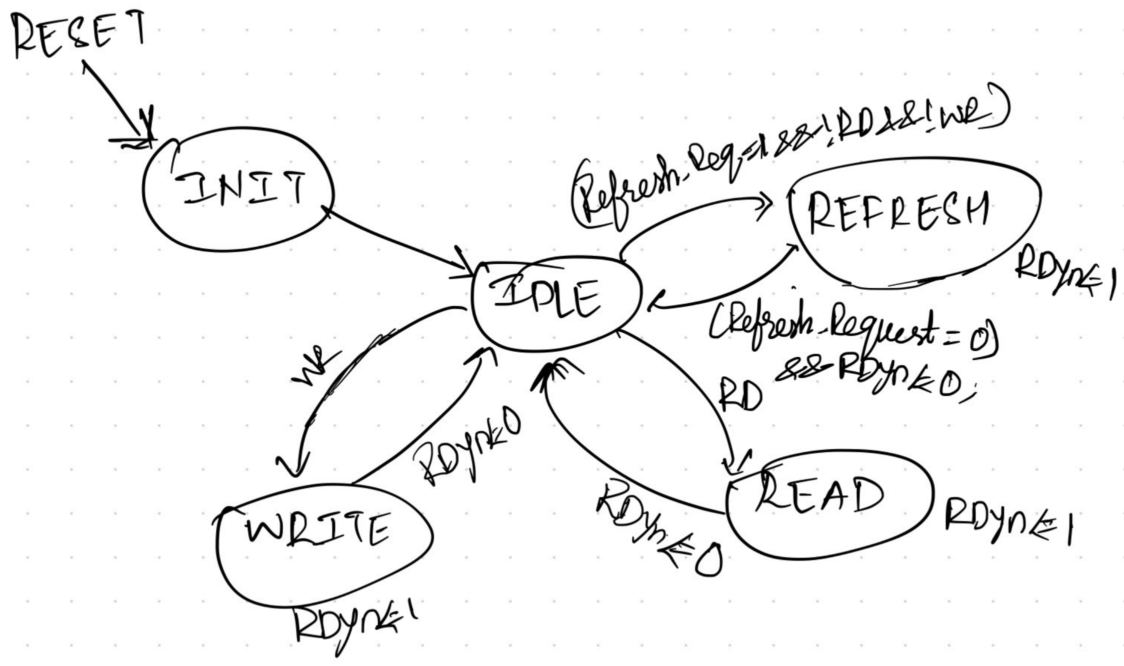
SDRAM[11:10] = 2'b00;
↓
Selecting only 1 bank in SDRAM.

PROCESSOR SUBSYTEM AND INTERFACE DIAGRAM

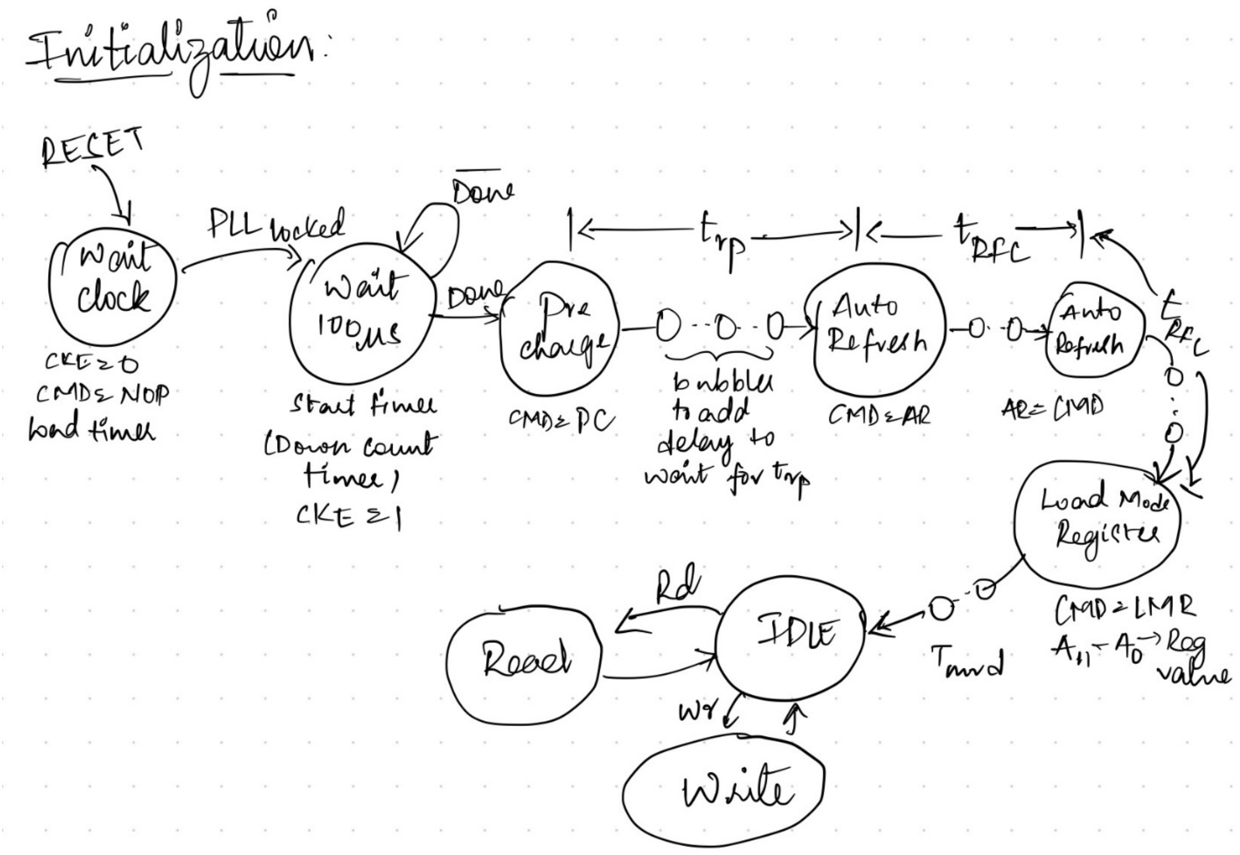


The 8086-1 clock runs at 10 MHz which is clocked up to the SDRAM clock speed of 100 MHz using a phase locked loop implemented in the Verilog code. The state machine for the SDRAM controller runs at the SDRAM clock speed and all the control signals and the data has been adjusted for clock crossing using double flip flops with the respective clocks synchronized to allow for appropriate detection of the said signals during transitions for edge detection.

STATE MACHINE DIAGRAM AND STATE TIMING WAVEFORMS



Initialization Stage



After the Rstn signal is asserted, we go to the next state called wait clock where CKE is 0 with NOP Command. We wait in this state until the clk is phase locked with SDRAM_CLK.

Once the clk is phase locked with the SDRAM clock, the state waits for 100us (wait_100us state) where CKE is 1. If it is done it does the pre charge Command or else, it stays in the same state.

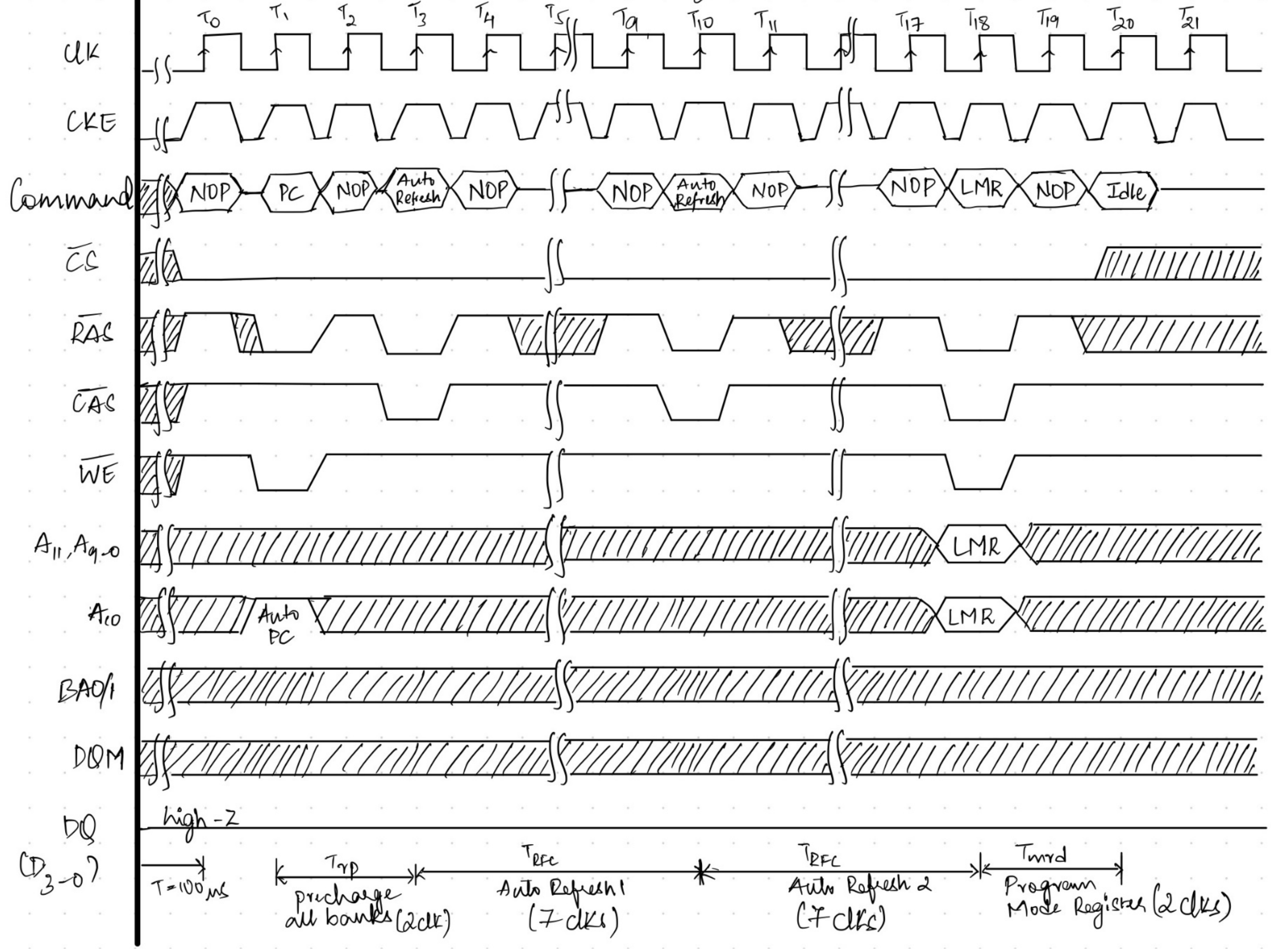
During pre-charge the A10 bit is asserted high in output as a function of state. This Trp will wait for 2clocks with a wait state included in between. Once this state is completed the SDRAM will have precharged all the banks.

After this state we perform two auto refresh states, where each state takes 7clocks (Trfc) to transition from one another. After the second auto refresh it moves to Load Mode Register state where we load the bits into the 12-bit address to configure the SDRAM by default.

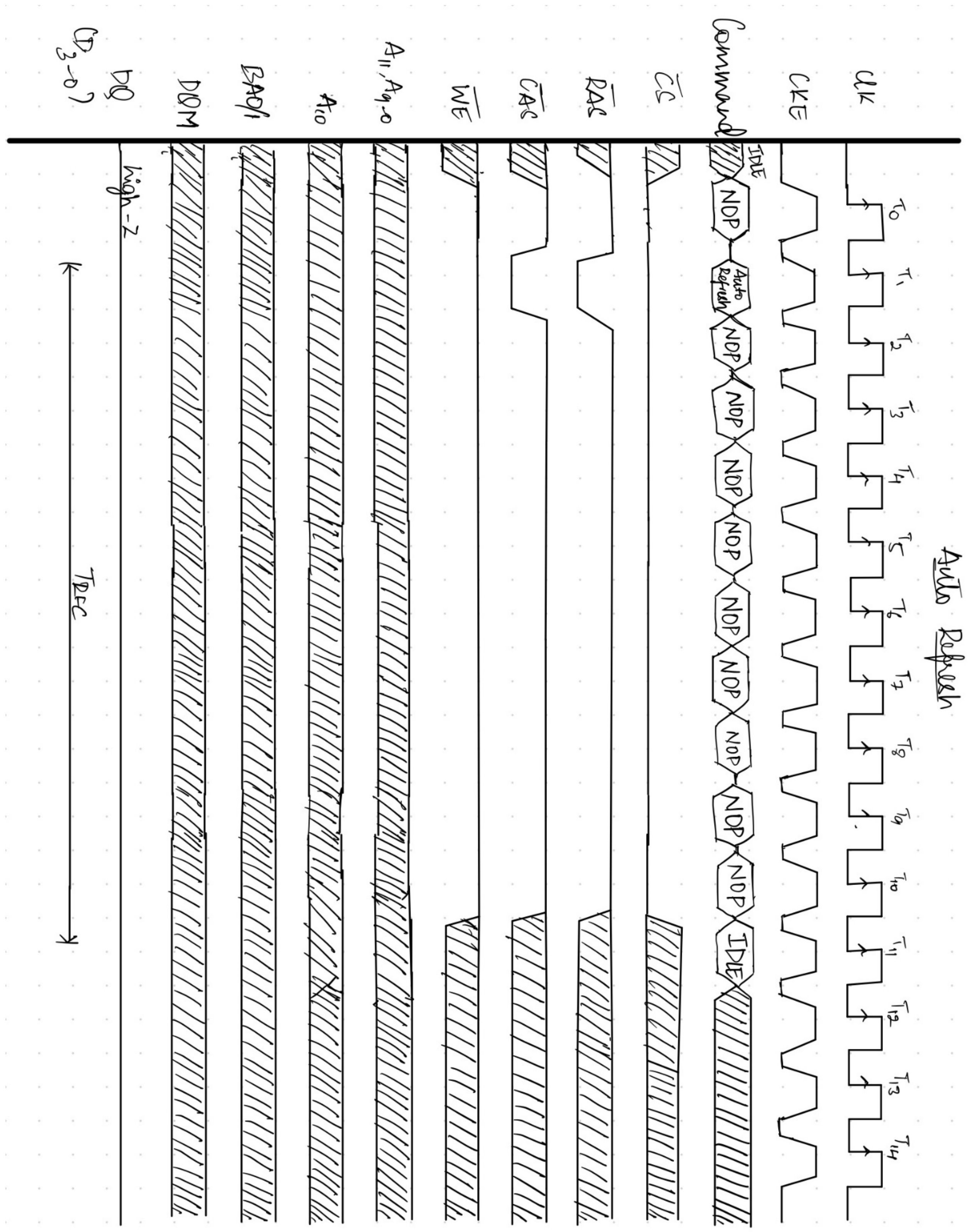
CAS latency =2, Burst length=4, sequential, Standard operation and programmed burst length.

We add a wait state in between the Load state and the idle state as the Tmrd is 2clks and state transition takes a clock altogether.

Initialization



Auto Refresh Stage



When in Idle state we start a down counter for 15.625us which is (64ms/4096 rows), when it reaches zero, we assert a refresh request only when there is no read or write signals coming from the microprocessor.

In the Refresh cycle we add 6 wait states and a wait state transitioning from wait state back to idle. So, the cycle takes 7 clocks. Before going back to the idle state, we clear the refresh request and load the counter, reset the wait states back to 1.

Read Stage:

We use cross clocking using double flip flop when reading data from faster clock to slower clocks. When there is a Read request, we move to read activate state where we wait for 2 clocks Trcd.

The row address is matched from SDRAM Nibble Addresses [21:10] and 2 bank bits [23:22] in the output as a function of state during the Activate read state. Then we move to Read state where we do active low for DQMn bits and wait for 2 clocks Tcl.

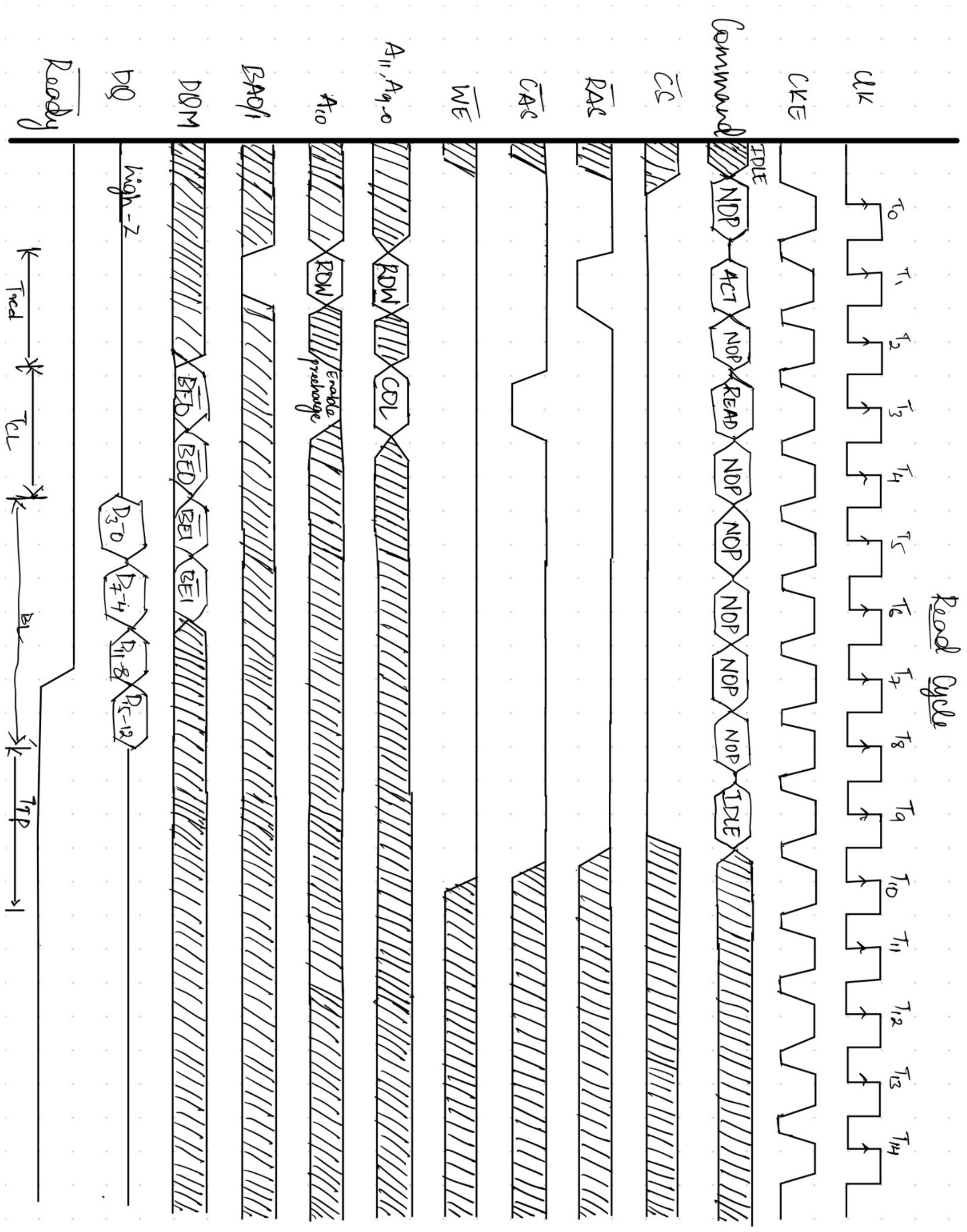
In the read state, the column address is matched from SDRAM Nibble Addresses [9:0] and 2 bank bits [23:22] in the output as a function of state

After this we transfer the data from SDRAM DQ to 8086 data bus at a burst length of 4. Each burst is latched with a 4bit data and all the latched 4*4bits are put in a temporary register and sent to the data bus.

When there is a read request, we immediately assert the ready signal (active low) and during the 4th burst we make it low again.

As we are using auto precharge there’s no reason to wait for another 2 clocks, so we move back to idle state. To auto precharge set A10 bit high in the output as a function of state.

(please flip over for the Read Cycle timing waveform)


Read Cycle
Clk
CKE
$\overline{CS}$
$\overline{RAS}$
$\overline{CAS}$
$\overline{WE}$
A_{11}, A_{9-0}
A_{10}
$BA0/1$
DQM
DQ
$\overline{Ready}$
Command
T_0 T_1 T_2 T_3 T_4 T_5 T_6 T_7 T_8 T_9 T_{10} T_{11} T_{12} T_{13} T_{14}
IDLE
NOP
ACT
NOP
READ
NOP
NOP
NOP
NOP
NOP
IDLE
ROW
COL
ROW
enable precharge
$\overline{BE0}$
$\overline{BE0}$
$\overline{BE1}$
$\overline{BE1}$
high-Z
D_{3-0}
D_{7-4}
D_{11-8}
D_{15-12}
T_{rcd}
T_{CL}
BL
T_{RP}

Write Stage:

We use cross clocking using double flip flop when reading data from faster clock to slower clocks. When there is a write request, we move to read activate state where we wait for 2 clocks Trcd.

The row address is matched from SDRAM Nibble Addresses [21:10] and 2 bank bits [23:22] in the output as a function of state during Active write state. Then we move to the write state where we do active low for DQMn bits.

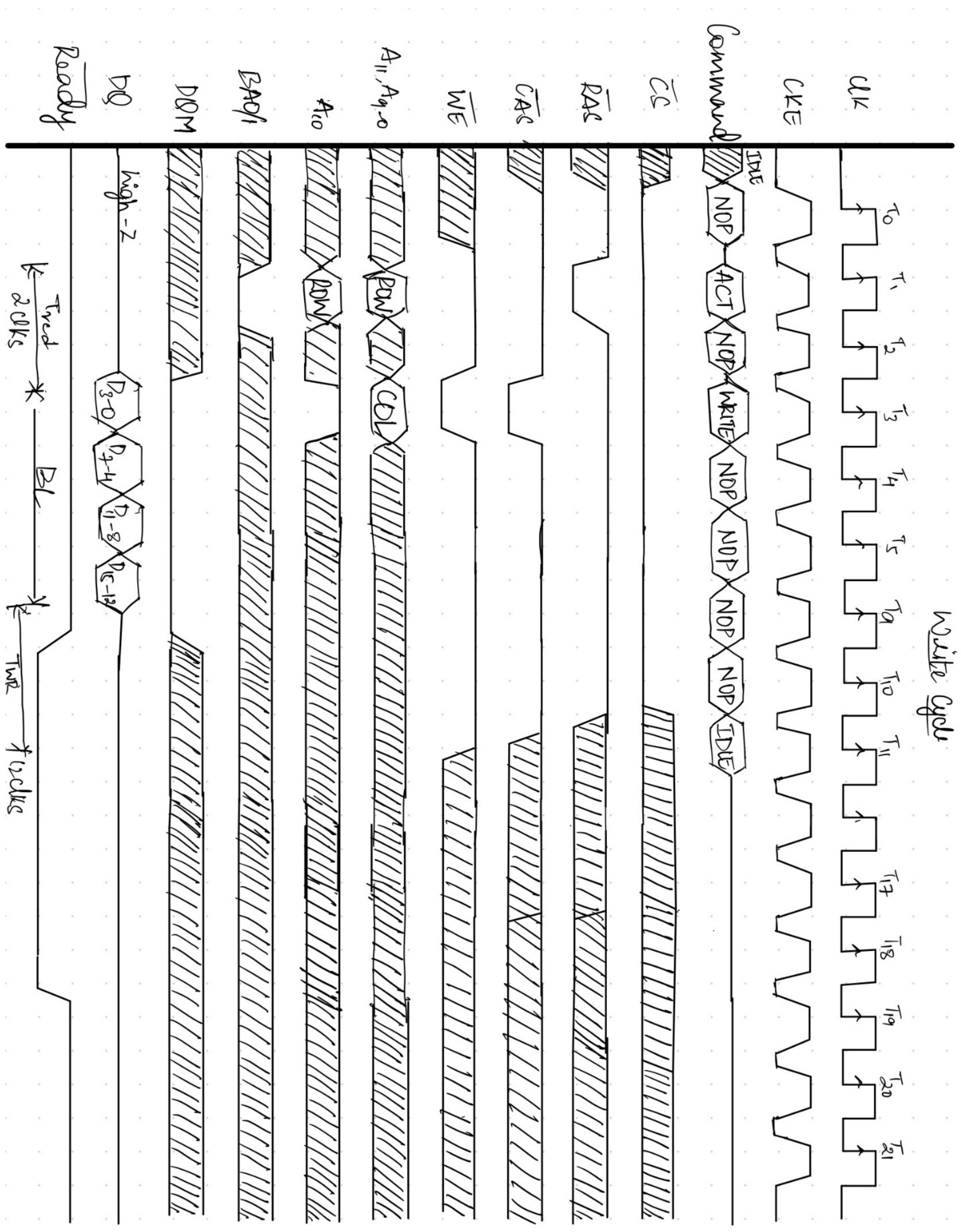
In the write state, the column address is matched from SDRAM Nibble Addresses [9:0] and 2 bank bits [23:22] in the output as a function of state

After this state we transfer the data from SDRAM DQ to 8086 data bus at a burst length of 4.

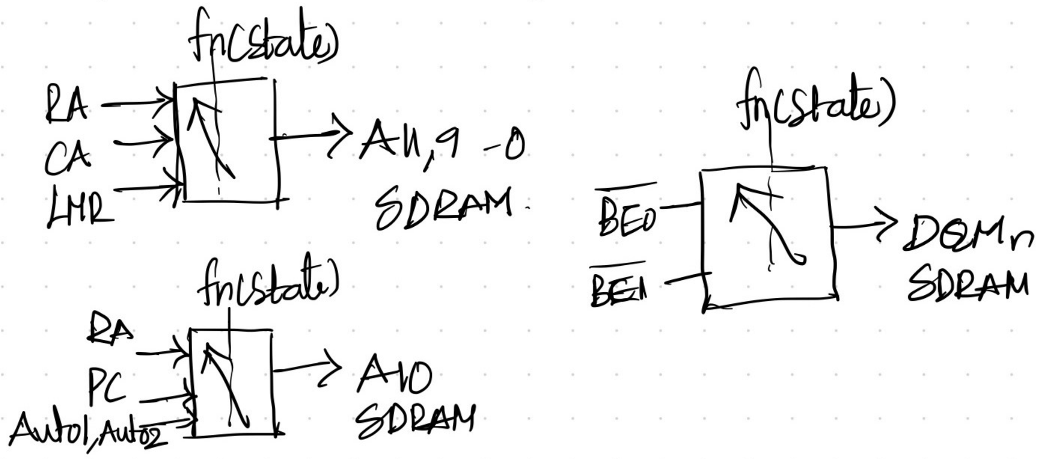
When there is a write request, we immediately assert the ready signal (active low) and after the data transfer we wait for another 2 clocks Twr (write recovery time) and assert the ready signal low.

As we are using auto pre charge there's no reason to wait for another 2 clocks, so we move back to idle state. To auto precharge set A10 bit high in the output as a function of state.

(please flip over for the write cycle timing waveform)


Write Cycle
CLK
CKE
Command
CS
RAS
CAS
WE
A11, A9-0
A10
BA0/1
DQM
DQ
Ready
T0
T1
T2
T3
T4
T5
T9
T10
T11
T17
T18
T19
T20
T21
IDLE
NOP
ACT
NOP
WRITE
NOP
NOP
NOP
NOP
IDLE
ROW
ROW
COL
high-Z
D3-0
D7-4
D11-8
D15-12
Tred
2 clks
BL
TWR
4 clks

Output as a function of state :



Outputs	Equations
SDRAM[0:11] A11,9-0	= f(Read, write, LMR, Read-ACT, Write-ACT)
SD-RAM[10]	= f(Read, write)
DQMn	= f(Read-ACT, Write-ACT, Read, write)
SD-RAM[10]	= f(Precharge, Auto Refresh1, Auto Refresh 2)
CSn, RaSn, CaSn, WEn	= f(NOP, Precharge, Auto Refresh1, AutoRefresh2, Load, Activate, Read, write).

Table For Reference in output as a function of Command.

CMD	CS	RAS	CAS	WE
Nop	L	H	H	H
Active	L	L	H	H
Read	L	H	L	H
write	L	H	L	L
Precharge	L	L	H	L
AutoRefresh	L	L	L	H
LMR	L	L	L	L