

CS223 Laboratory Assignment 2

Full Adder, 2-bit Adder, Lab Calculator on FPGA

Preliminary Work Submission Deadline:

All Sections: 17th Oct, Mon 09:00

Lab dates and times:

Section 1: 17th Oct, Mon 08:30-12:20 in EA-Z04

Section 2: 18th Oct, Tue 08:30-12:20 in EA-Z04

Section 3: 19th Oct, Wed 08:30-12:20 in EA-Z04

Section 4: 17th Oct, Mon 13:30-17:20 in EA-Z04

Section 5: 21st Oct, Fri 08:30-12:20 in EA-Z04

Section 6: 18th Oct, Tue 13:30-17:20 in EA-Z04

Location: EA Z04 (in the EA building, straight ahead past the elevators)

Groups: Each student will do the lab individually. Group size = 1

Preliminary Report (30 pts)

In the previous lab, you implemented a Half Adder using gates on the breadboard. In this lab you will implement very similar circuits, including lab calculator, but this time on the **FPGA**. Today's lab needs considerably advanced preparation. You need to **learn how to work with Xilinx's design toolset** before attending the lab. In addition, **SystemVerilog models and test benches** should be prepared in advance and assembled neatly into a Preliminary Report with a cover page and pages for the SystemVerilog codes. Each page should have a proper heading. The content of the report will be as follows:

- (a) A cover page including course code, course name, and section, the number of the lab, your name-surname, student ID, date.
- (b) Circuit schematic for a half adder.
- (c) Circuit schematic for a half subtractor.
- (d) Circuit schematic for a full adder **(using two half adders as black boxes)**.
- (e) **Circuit schematic for a 2-bit adder (using two full adders as black boxes)**.
- (f) **Circuit schematic for the lab calculator (refer Figure 1-2)**
- (g) Behavioral SystemVerilog module for the half adder and a testbench for it.
- (h) Behavioral SystemVerilog module for the half subtractor and a testbench for it.
- (i) Structural SystemVerilog module for the full adder and a testbench for it. Use the half adder module you wrote in part (g).
- (j) Structural SystemVerilog module for the 2-bit adder and a testbench for it. Use the full adder module you wrote in part (i).
- (k) Structural SystemVerilog module for the lab calculator and a testbench for it. (Use your half-adder, and half subtractor as the building blocks for your highest level module)

Note that the behavioral model describes the function of a module using Boolean equations and continuous assignment statements; whereas structural modeling refers to using and combining simpler pieces of modules (it is an application of hierarchy). You can refer to the slides of Chapter 4 of your textbook while preparing your modules and test benches.

Lab calculator

C	D	module	Y	Z
0	0	XOR	$A \oplus B$	d
0	1	NAND	$\overline{A \cdot B}$	d
1	0	Half Adder	Sum	Carry Out
1	1	Half Subtractor	Difference	Borrow out

Figure 1: Lab calculator (*d* denotes “don’t care”)

C	D	A	B	Y	Z
0	0	0	0	0	d
0	0	0	1	1	d
0	0	1	0	1	d
0	0	1	1	0	d
0	1	0	0	1	d
0	1	0	1	1	d
0	1	1	0	1	d
0	1	1	1	0	d
1	0	0	0	0	0
1	0	0	1	1	0
1	0	1	0	1	0
1	0	1	1	0	1
1	1	0	0	0	0
1	1	0	1	1	1
1	1	1	0	1	0
1	1	1	1	0	0

Figure 2: Truth table of the lab calculator

You will need a copy of your designs and SystemVerilog programs with you to use in the lab. Therefore, you should get a copy of it before you come to the lab, for your own use.

Additional pre-lab work:

You should read the following documents (available on Moodle) to be familiar with steps of design flow (Simulation, Synthesis, Implementation, Bitstream Generation, Downloading to FPGA board), using the Xilinx **Vivado** tool. You can download, install and practice working with Xilinx Vivado on your own computer with a free webpack license.

- Suggestions for Lab Success.
- Basys 3 Vivado Decoder Tutorial.
- Vivado Tutorial.
- Basys 3 FPGA Board Reference Manual.

Implementation on FPGA (70 pts)

In this step, you implement your modules on FPGA board. You don't need to connect your **Basys 3** board to the Beti board. Working with standalone Basys 3 and having it connected to your computer is enough for this lab. There are some switches and LEDs available on Basys 3 which you can use them.

- *Create a new Xilinx Vivado Project. Use appropriate names for files and folders, keeping the project in a directory where you can find it later and erase it (at the end of the lab).*
- (a) Simulation: Implement the half adder module in behavioral style (preliminary [part-g](#)). Then, using the SystemVerilog testbench code you wrote, verify in simulation that your circuit works correctly.
- (b) Simulation: Implement the half subtractor module in behavioral style (preliminary [part-h](#)). Then, using the SystemVerilog testbench code you wrote, verify in simulation that your circuit works correctly.
- (c) Simulation: Implement the full adder module in structural style (preliminary [part-i](#)). Then, using the SystemVerilog testbench code you wrote, verify in simulation that your circuit works correctly.
- (d) Simulation: Implement the 2-bit adder module using two full adders you wrote (preliminary [part-j](#)). Then, using the SystemVerilog testbench code you wrote, verify in simulation that your circuit works correctly.
- (e) Simulation: Implement the lab calculator module using a half adder, a half subtractor, a NAND gate, and an XOR gate in structural style (preliminary [part-k](#)). Then, using the System Verilog testbench code you wrote, verify in simulation that your circuit works correctly.
- (f) When you are convinced that your codes work correctly, show the simulation results to your TA. Be prepared to answer questions that you may be asked.
- (g) Program the FPGA: Now, follow the Xilinx Vivado design flow to synthesize, implement, generate a bitstream file, and program 2-bit adder and lab calculator to Basys 3 FPGA board.
- (h) Test your design: Using the switches and LEDs (on Basys 3) that you have assigned in the constraint file (.xdc), test your designs. When you are convinced that they work correctly, show the physical implementation results to the TA. Be prepared to answer questions that you may be asked.

Submit your code for MOSS similarity testing

Finally, when you are done and before leaving the lab, you need to upload the file StudentID_SectionNumber.txt created in the Implementation on FPGA part. Be sure that the file contains exactly and only the codes which are specifically detailed above. If you have multiple files, just copy and paste them in order, one after another inside text file. Check the specifications! Even if you didn't finish or didn't get the SystemVerilog part working, you must submit your code to the Moodle Assignment for similarity checking. Your codes will be compared against all the other codes in all sections of the class, by the MOSS program, to determine how similar it is (as an indication of plagiarism). So be sure that the code you submit is the code that you actually wrote yourself! All students must upload their code to the 'Moodle Assignment' on the Moodle page specific for their sections. Check submission time and don't miss it before leaving the lab. After taking a backup of your work, don't forget to delete it from the computer. Because students of other sections will work with your system too.

Clean Up

- (1) Clean up your lab station, and return all the parts, wires, the Beti trainer board, etc. Leave your lab workstation for others the way you would like to find it.
- (2) CONGRATULATIONS! You are finished with Lab 2 and are one step closer to becoming a computer engineer.

NOTES

- Advance work on this lab, and all labs, is strongly suggested.
- Be sure to read and follow the Policies for CS223 labs, posted in Moodle.

LAB POLICIES

1. There are three computers in each row in the lab. Don't use middle computers, unless you are allowed by lab coordinator.
2. You borrow a lab-board containing the development board, connectors, etc. in the beginning. The lab coordinator takes your signature. When you are done, return it to his/her, otherwise you will be responsible and lose points.
3. Each lab-board has a number. You must always use the same board throughout the semester.
4. You must be in the lab, working on the lab, from the time lab starts until you finish and leave. (bathroom and snack breaks are the exception to this rule). Absence from the lab, at any time, is counted as absence from the whole lab that day.
5. No cell phone usage during lab. Tell friends not to call during the lab hours--you are busy learning how digital circuits work !
6. Internet usage is permitted only to lab-related technical sites. No Facebook, Twitter, email, news, video games, etc--you are busy learning how digital circuits work !
7. You need to be in lab on time and turn in your preliminary report at the start of the lab.