Course No.: CS224
Lab No. : 6
Section No. : 6
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Lab Experiment Report

Report for Matrix Size 1 (N = 100)

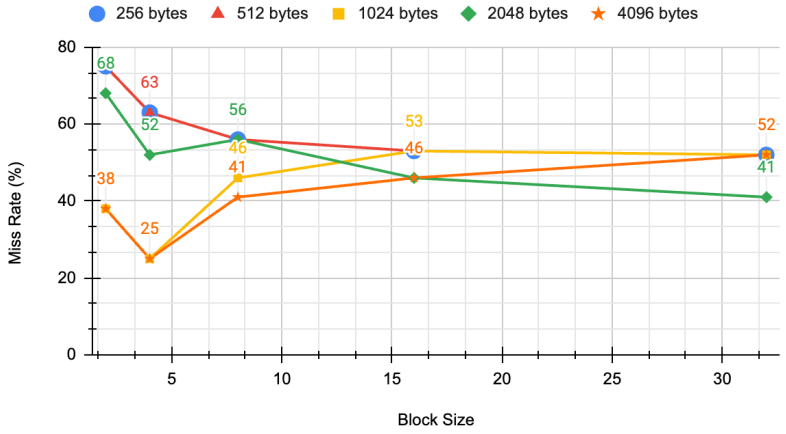
Part a)

1. Row-Major Summation Table

Cache block size (words) →		2	4	8	16	32
Cache size (bytes) ↓	Data Title					
256	Miss rate (%)	75	63	56	53	52
	Number of misses	15113	12609	11355	10729	10417
512	Miss rate (%)	75	63	56	53	52
	Number of misses	15113	12609	11355	10729	10417
1024	Miss rate (%)	68	52	56	53	52
	Number of misses	13763	10584	11355	10729	10417
2048	Miss rate (%)	38	25	46	53	52
	Number of misses	7691	5029	9330	10729	10417
4096	Miss rate (%)	38	25	41	46	52
	Number of misses	7689	5028	8265	9188	10417

Table 1.1: Miss rates and number of misses of row-major summation for direct-mapped cache

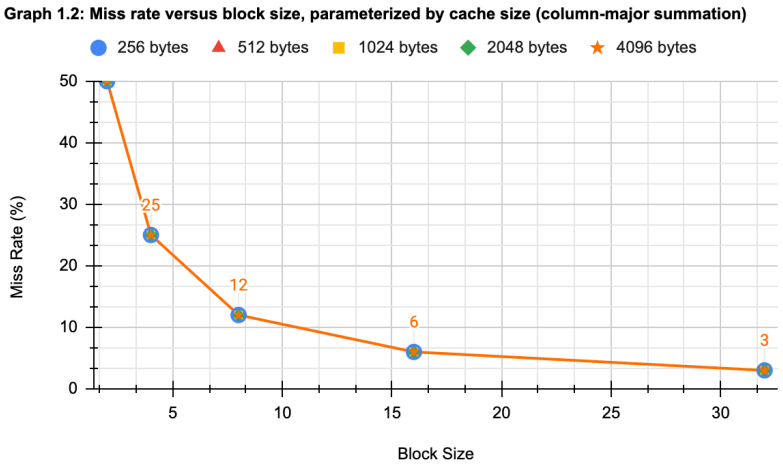
Graph 1.1: Miss rate versus block size, parameterized by cache size (row-major summation)



2. Column-Major Summation Table

Cache block size (words) →		2	4	8	16	32
Cache size (bytes) ↓	Data Title					
256	Miss rate (%)	50	25	12	6	3
	Number of misses	10014	5009	2506	1255	630
512	Miss rate (%)	50	25	12	6	3
	Number of misses	10014	5009	2506	1255	630
1024	Miss rate (%)	50	25	12	6	3
	Number of misses	10014	5009	2506	1255	630
2048	Miss rate (%)	50	25	12	6	3
	Number of misses	10014	5009	2506	1255	630
4096	Miss rate (%)	50	25	12	6	3
	Number of misses	10014	5009	2506	1255	630

Table 1.2: Miss rates and number of misses of column-major summation for direct-mapped cache



Part b)

Choosen hit rate configuration →		Good hit rate Cache size (bytes): 2048 Cache block size (words): 4	Medium hit rate Cache size (bytes): 1024 Cache block size (words): 16	Poor hit rate Cache size (bytes): 512 Cache block size (words): 2
Placement policy ↓	Data Title ↓			
Direct Mapped	Miss rate (%)	25	53	75
	Number of misses	5029	10729	15113
Fully Associative -LRU	Miss rate (%)	25	53	75
	Number of misses	5033	10729	15113
Fully Associative -Random	Miss rate (%)	35	53	69
	Number of misses	6989	10715	13819

Table 1.3: Experimenting miss rates for different cache designs through choosen hit rate configurations from Table 1.1

Part c)

Choosen hit rate configuration →		Good hit rate	Medium hit rate	Poor hit rate
N-way set associative cache set size ↓	Data Title	Cache size (bytes): 2048 Cache block size (words): 4	Cache size (bytes): 1024 Cache block size (words): 16	Cache size (bytes): 512 Cache block size (words): 2
1	Miss rate (%)	25	53	75
	Number of misses	5029	10729	15113
2	Miss rate (%)	25	53	75
	Number of misses	5032	10729	15113
4	Miss rate (%)	25	53	75
	Number of misses	5033	5033	15113
8	Miss rate (%)	25	53	75
	Number of misses	5033	10729	15113
16	Miss rate (%)	25	53	75
	Number of misses	5033	10729	15113

Table 1.4: Experimenting miss rates for N-way caches with different set sizes through choosen hit rate configurations from Table 1.1

Report for Matrix Size 2 (N = 50)

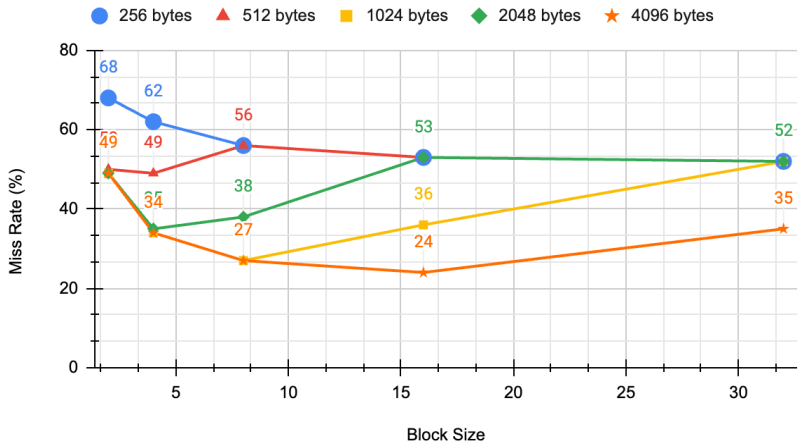
Part a)

1. Row-Major Summation Table

Cache block size (words) →		2	4	8	16	32
Cache size (bytes) ↓	Data Title					
256	Miss rate (%)	68	62	56	53	52
	Number of misses	3488	3184	2868	2711	2633
512	Miss rate (%)	50	49	56	53	52
	Number of misses	2536	2487	2868	2711	2633
1024	Miss rate (%)	49	35	38	53	52
	Number of misses	2528	1785	1923	2711	2633
2048	Miss rate (%)	49	34	27	36	52
	Number of misses	2528	1762	1404	1858	2633
4096	Miss rate (%)	49	34	27	24	35
	Number of misses	2528	1762	1358	1201	1792

Table 2.1: Miss rates and number of misses of row-major summation for direct-mapped cache

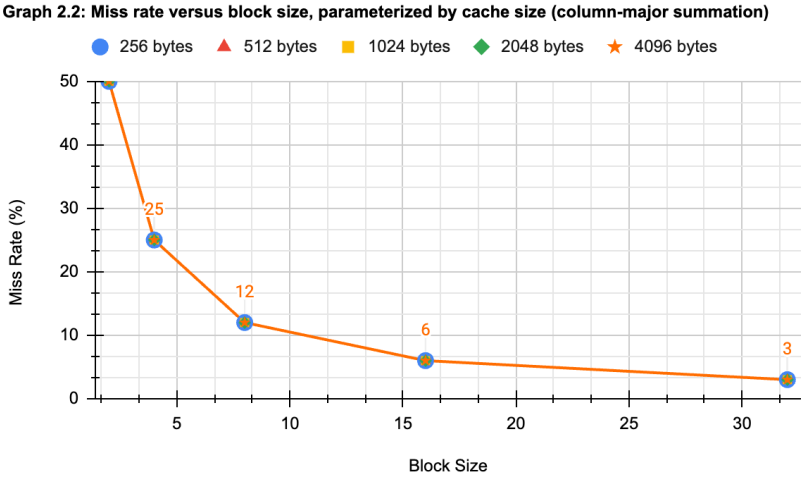
Graph 2.1: Miss rate versus block size, parameterized by cache size (row-major summation)



2. Column-Major Summation Table

Cache block size (words) →		2	4	8	16	32
Cache size (bytes) ↓	Data Title					
256	Miss rate (%)	50	25	12	6	3
	Number of misses	2514	1259	632	319	162
512	Miss rate (%)	50	25	12	6	3
	Number of misses	2514	1259	632	319	162
1024	Miss rate (%)	50	25	12	6	3
	Number of misses	2514	1259	632	319	162
2048	Miss rate (%)	50	25	12	6	3
	Number of misses	2514	1259	632	319	162
4096	Miss rate (%)	50	25	12	6	3
	Number of misses	2514	1259	632	319	162

Table 2.2: Miss rates and number of misses of column-major summation for direct-mapped cache



Part b)

Choosen hit rate configuration →		Good hit rate Cache size (bytes): 4096 Cache block size (words): 16	Medium hit rate Cache size (bytes): 512 Cache block size (words): 4	Poor hit rate Cache size (bytes): 256 Cache block size (words): 2
Placement policy ↓	Data Title ↓			
Direct Mapped	Miss rate (%)	24	49	68
	Number of misses	1201	2487	3488
Fully Associative -LRU	Miss rate (%)	7	62	75
	Number of misses	358	3184	3813
Fully Associative -Random	Miss rate (%)	14	52	68
	Number of misses	703	2634	3477

Table 2.3: Experimenting miss rates for different cache designs through choosen hit rate configurations from Table 2.1

Part c)

Choosen hit rate configuration →		Good hit rate	Medium hit rate	Poor hit rate
N-way set associative cache set size ↓	Data Title	Cache size (bytes): 4096 Cache block size (words): 16	Cache size (bytes): 512 Cache block size (words): 4	Cache size (bytes): 256 Cache block size (words): 2
2	Miss rate (%)	14	60	75
	Number of misses	716	3084	3813
4	Miss rate (%)	13	62	75
	Number of misses	656	3184	3813
8	Miss rate (%)	7	62	75
	Number of misses	356	3184	3813
16	Miss rate (%)	7	62	75
	Number of misses	357	3184	3813
32	Miss rate (%)	7	62	75
	Number of misses	358	3184	3813

Table 2.4: Experimenting miss rates for N-way caches with different set sizes through choosen hit rate configurations from Table 2.1