Analog Course Project

EE301 Analog Circuits

Submitted to : Prof. Mahendra Sakare

By

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Report: Design of Cascode Amplifier using LTspice schematics and Magic tool layout

Objectives:

Design of cascode amplifier and cascode current mirror in schematic and layout using

LTspice or Cadence and Magic/Cadence tools in 180 nm (supply 1.8 V) technology and only schematic of cascode amplifier, beta multiplier and cascode current mirror in 22 nm (supply 0.8 V) technology node to see the effect of lowering the technology node.

The target specifications for designing the cascode amplifier are as follows:

• VDD = 1.8 V

• AV = 20 V/V

• Power dissipation (PD) < 5 mW

• Load Capacitance (CL) = 1 pF

• Unity Gain Bandwidth(UGB) > 500 KHz.

Tools used:

LTSpice software and Magic EDA layout tool

Given:

The block diagram for the single-stage cascode amplifier with required biasing network is shown Fig 1. The cascode amplifier requires a biasing circuit which

includes the beta multiplier and cascode current mirror circuits. The beta multiplier circuit provides the input to the cascode current mirror and cascode amplifier. One capacitor as a load is added at the output of the cascode amplifier. The characteristics due to the cascoding of amplifiers are: the impedances at input and output are high.

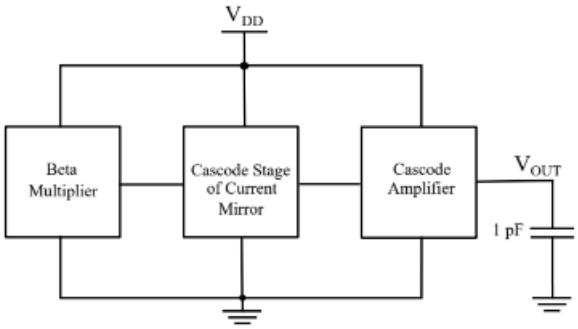


Figure 1: Block diagram of cascode amplifier with other blocks

Circuit Diagram:

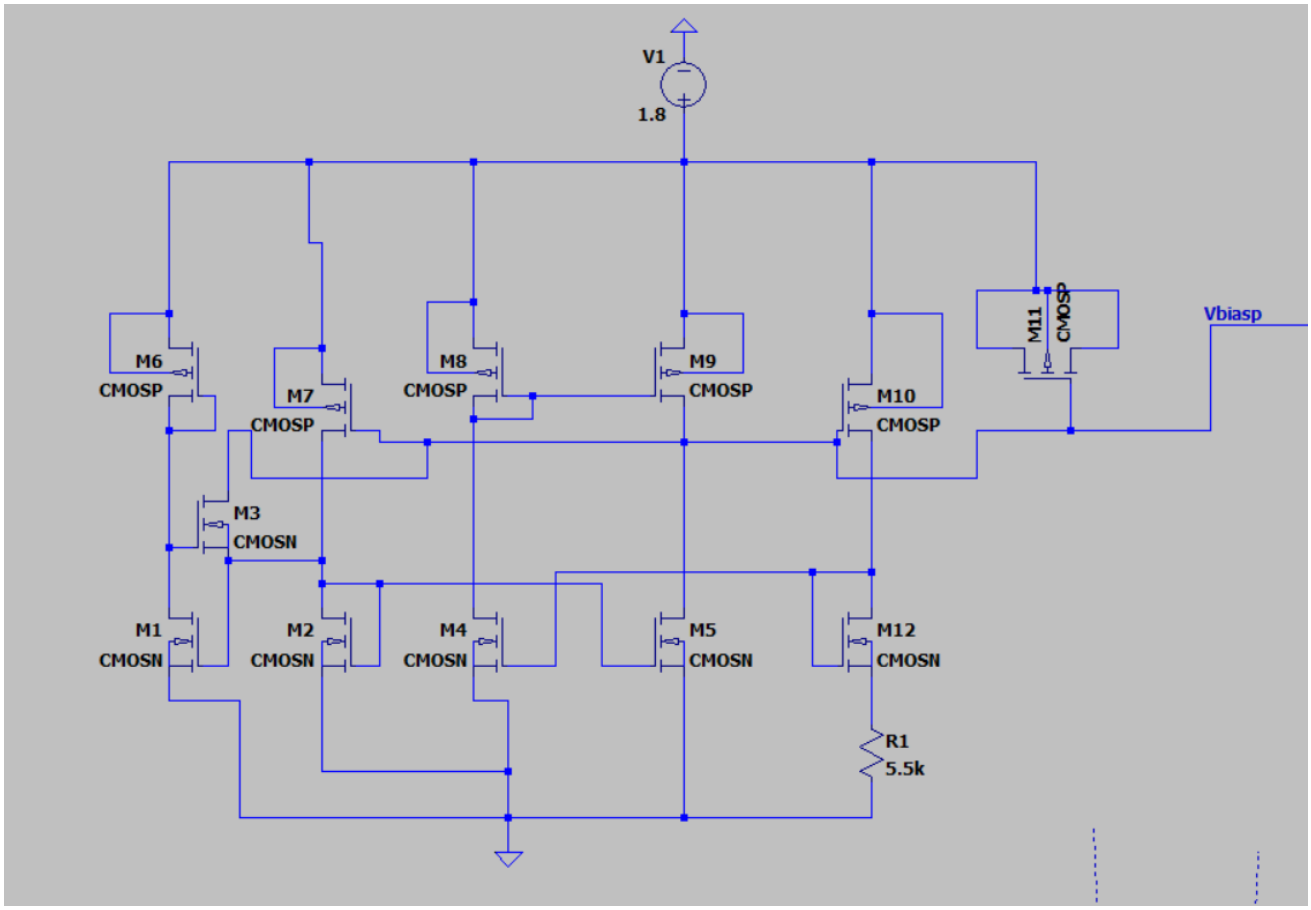


Fig 2. Beta Multiplier for 180nm technology

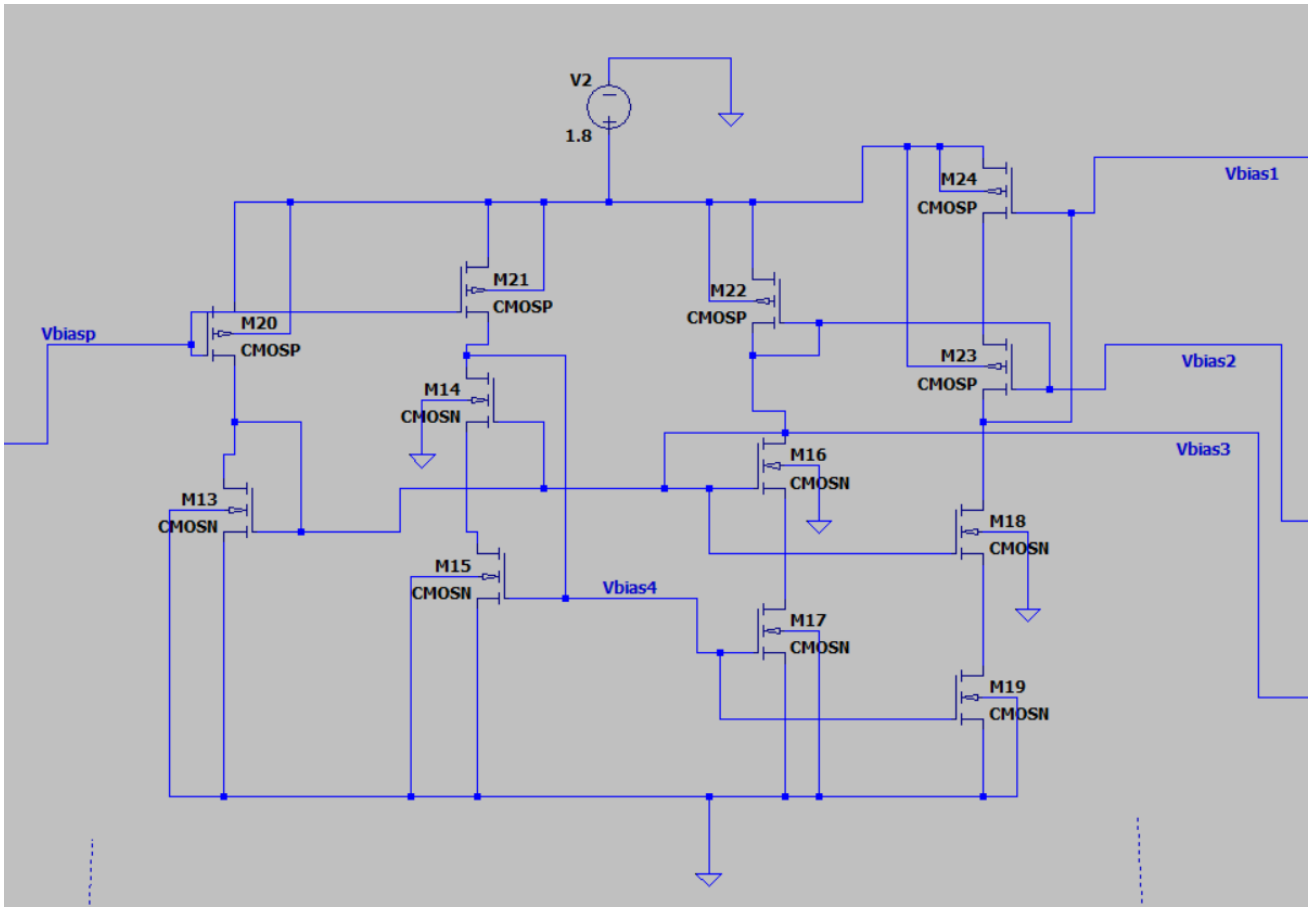


Fig 3. Current mirror biasing cascode amplifier for 180nm technology

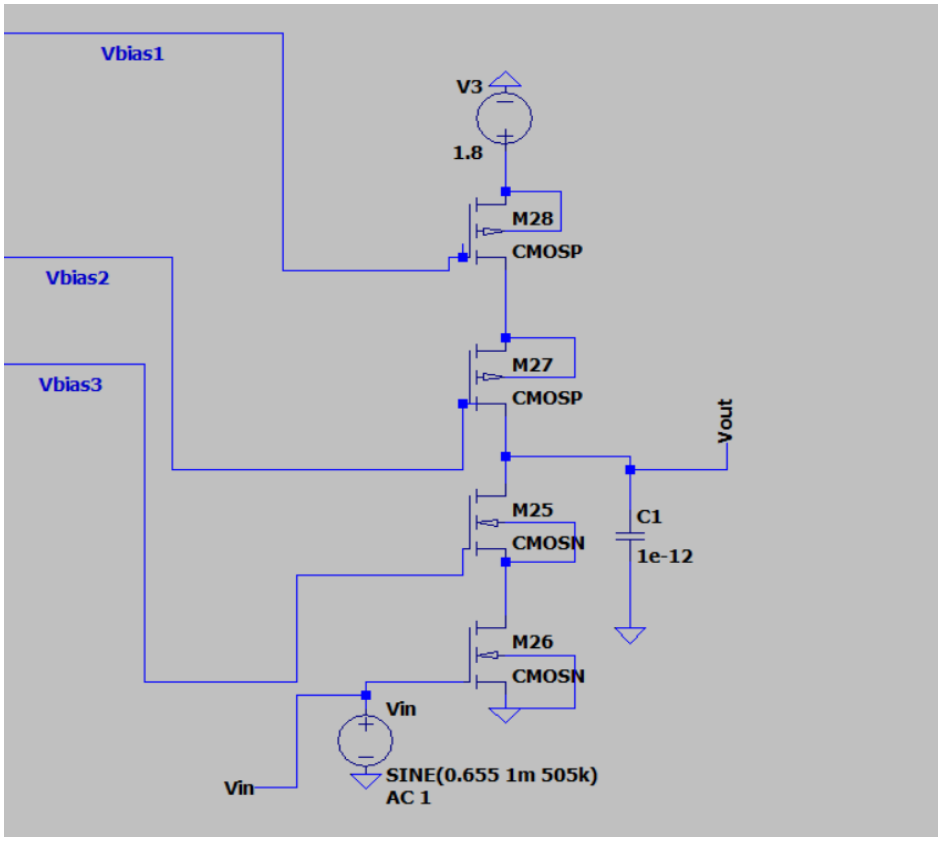


Fig 4. Cascode amplifier for 180nm technology

***(Only Vdd and aspect ratio will change in case of 22nm schematics)*

Calculation:

Calculations :-

(I) For 180nm technology:-

→ Taking frequency $f_0 = 3MHz$ and $I_d = 10\mu A$

Required gain = 20V/V

$f_0 = \frac{1}{2\pi R_{out} C}$

Putting above values, we get $R_{out} = 53051.65\ \Omega$

$A_v = g_m \times R_{out} \Rightarrow g_m = \frac{A_v}{R_{out}} = \frac{20}{53051.65} = 3.14 \times 10^{-4}\ S$

→ $g_m = \sqrt{2 \times I_D \times \mu_n C_{ox} \frac{W}{L}} = \sqrt{2 \times 10\mu \times 270\mu \times \frac{W}{L}}$

$\Rightarrow \left(\frac{W}{L}\right)_{NMOS} = 18.277$

→ For 1st PMOS of Cascode Amplifier

$V_g = V_{bias1} = \underbrace{1.08V}_{\text{This we are getting by cascode CM}}$

$V_s = 1.8V$, $V_{thp} = 0.3906$

$I_d = 0.5 \times \mu_p \times C_{ox} \times \frac{W}{L} \times (V_{gs} - V_{thp})^2$

$\left(\frac{W}{L}\right)_{PMOS} = 4.096$

For NMOS in sat.

$V_{ds} \geq V_{gs} - V_{thn}$

assume $V_{dsat} = 200mV$

For M25 → $200mV \geq V_S - 0.5 \Rightarrow V_S \leq 0.7V$

For M26 → $200mV \geq V_{bias3} - 0.2 - 0.5 \Rightarrow V_{bias3} \leq 0.7V$

For PMOS in sat

$V_{ds} \leq V_{gs} - V_{thp}$

For M27 → $-200mV \leq V_{bias2} - 1.6 + 0.3906$

$V_{bias2} \geq 1.0094V$

For M28 → $-200mV \leq V_{bias1} - 1.8V + 0.3906$

$V_{bias1} \geq 1.2094V$

(II) For 22nm Technology:-

Assuming $I_d = 8\mu A$, $f_0 = 1MHz$

Reqd gain = 20V/V

$f_0 = \frac{1}{2\pi R_{out} C}$ $\Rightarrow$ $R_{out} = 159154.9\ \Omega$

$A_v = g_m \times R_{out}$ $\Rightarrow$ $g_m = 12 \times 10^{-5}$

$g_m = \sqrt{2 \times I_d \times \mu_n \times C_{ox} \frac{W}{L}}$

$\Rightarrow \left(\frac{W}{L}\right)_{NMOS} = 7.5$

For First PMOS in cascode Amplifier

$V_S = 0.8V$ $V_{thp} = 0.44$.

$V_g = V_{bias1} = 0.2481V$

$I_d = 0.5 \times \mu_p \times C_{ox} \times \frac{W}{L} \times (V_{gs} - V_{thp})^2$

$\Rightarrow \left(\frac{W}{L}\right)_{PMOS} = 11.59554$

→ Assuming $V_{dsat} = 200mV$

For M28 → $200mV \geq V_S - 0.5$ $\Rightarrow$ $V_S \leq 0.7V$

For M27 → $200mV \geq V_{bias3} - 0.2 - 0.5$ $\Rightarrow$ $V_{bias3} \leq 0.7V$

For M25 → $-200mV \leq V_{bias2} - 0.6 + 0.46$

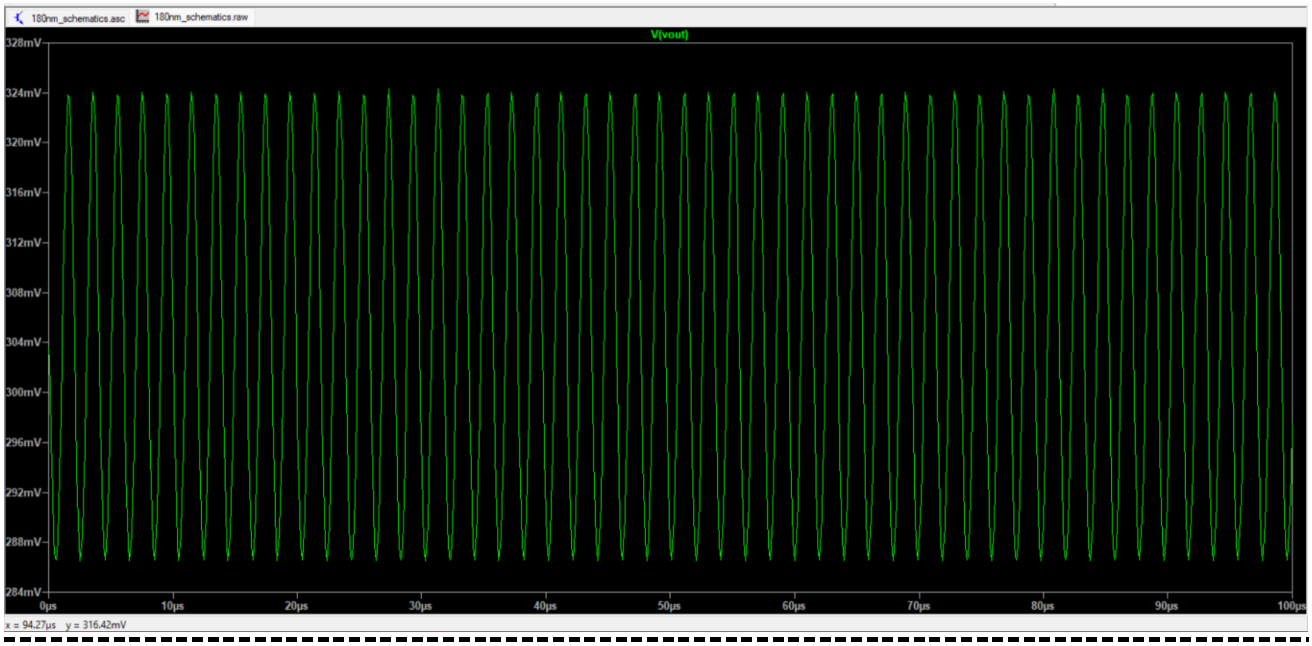
$V_{bias2} \geq -0.06$

For M26 → $-200mV \leq V_{bias1} - 0.8 + 0.3906$

$V_{bias1} \geq 0.14V$

Observations:

For 180nm technology:



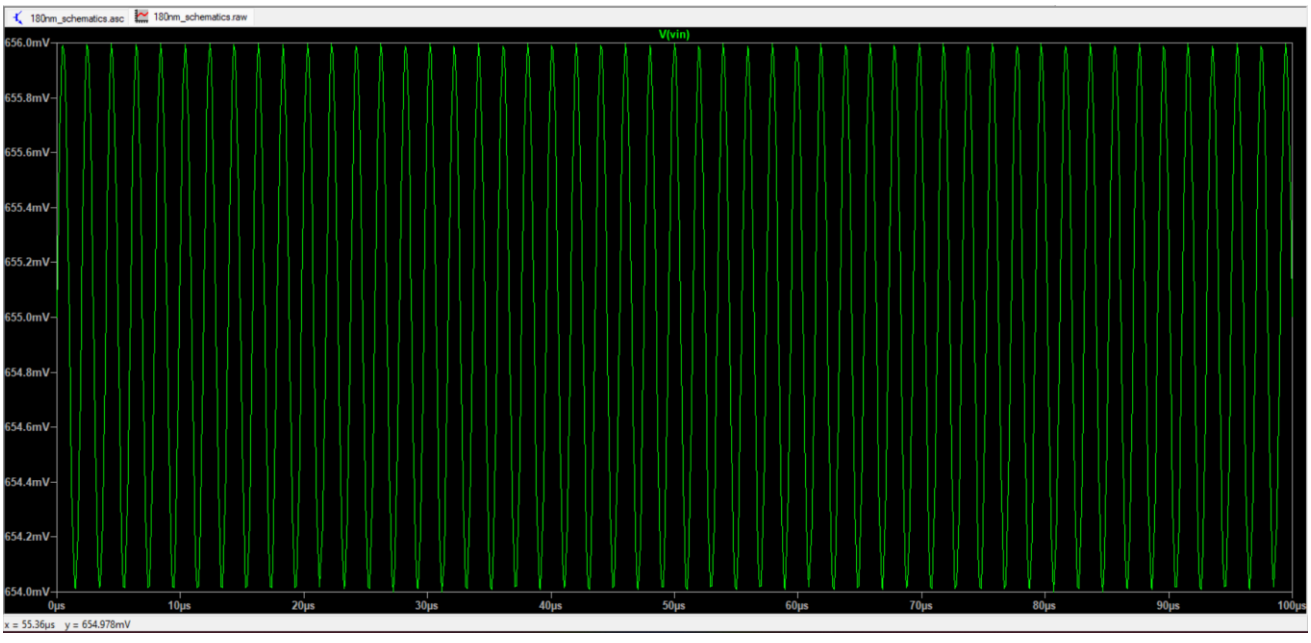


Fig 6. Vout and Vin plot for 180nm technology

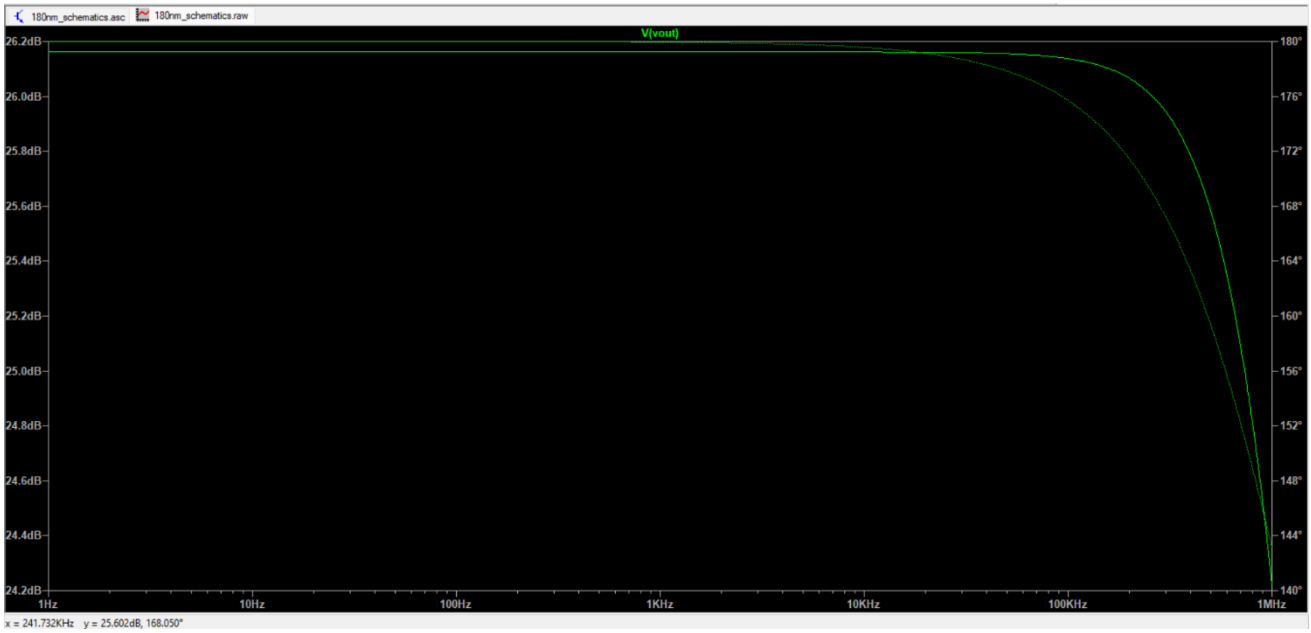
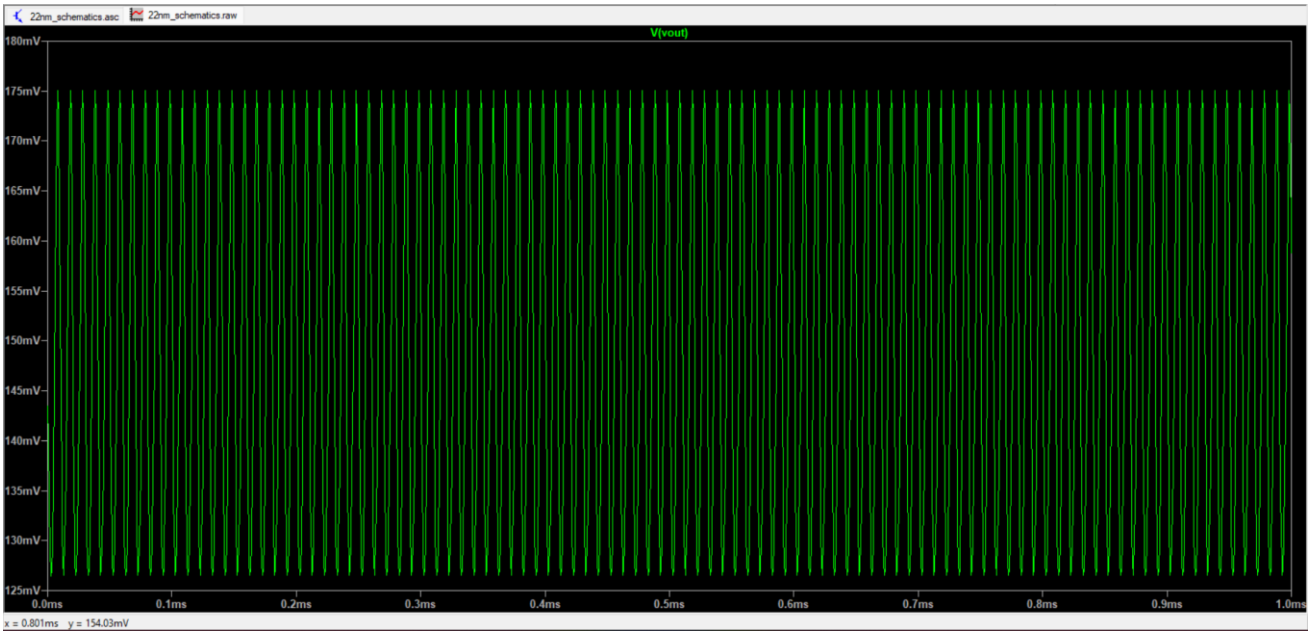


Fig 7. Bode plot for 180nm technology

- Vin=0.655V (DC Bias), Vac=1 mV, f=505kHz
- Output Voltage Swing: (286m to 324m) V = 38mV
- Amplitude of Swing= 38mV
- Gain= 19V/V
- Gain = 26.16dB for F<500kHz
- Pd = 0.2268uW < 5mW

For 22nm technology:



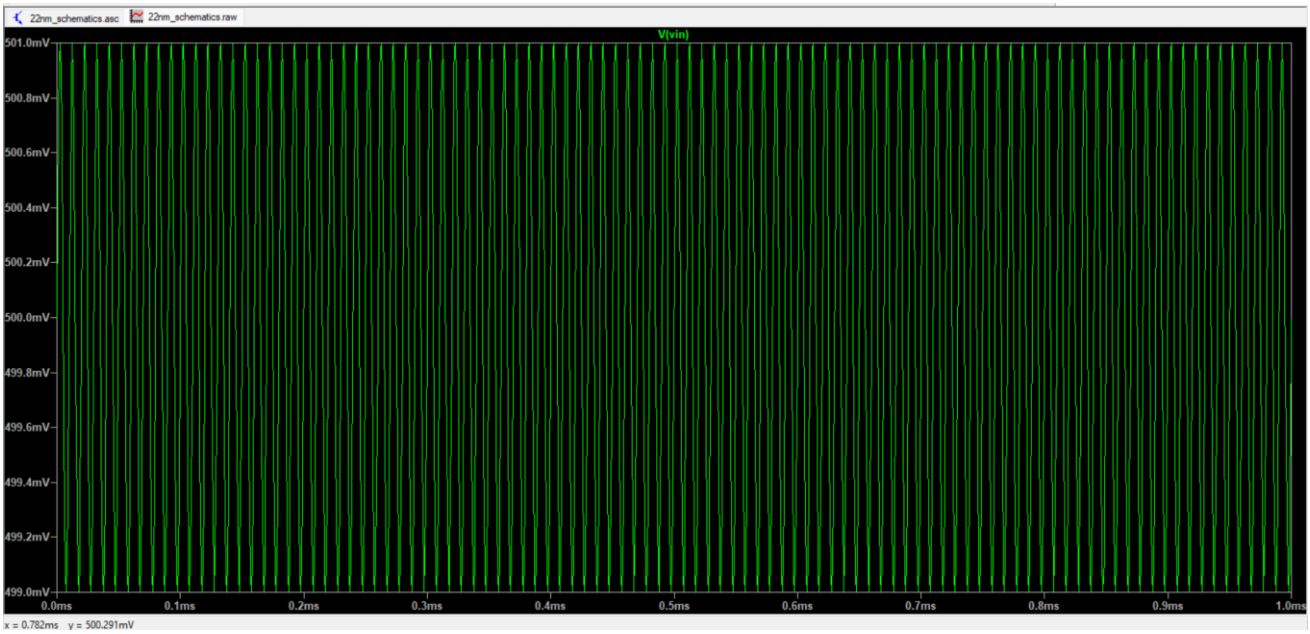


Fig 8. Vout and Vin plot for 22nm technology

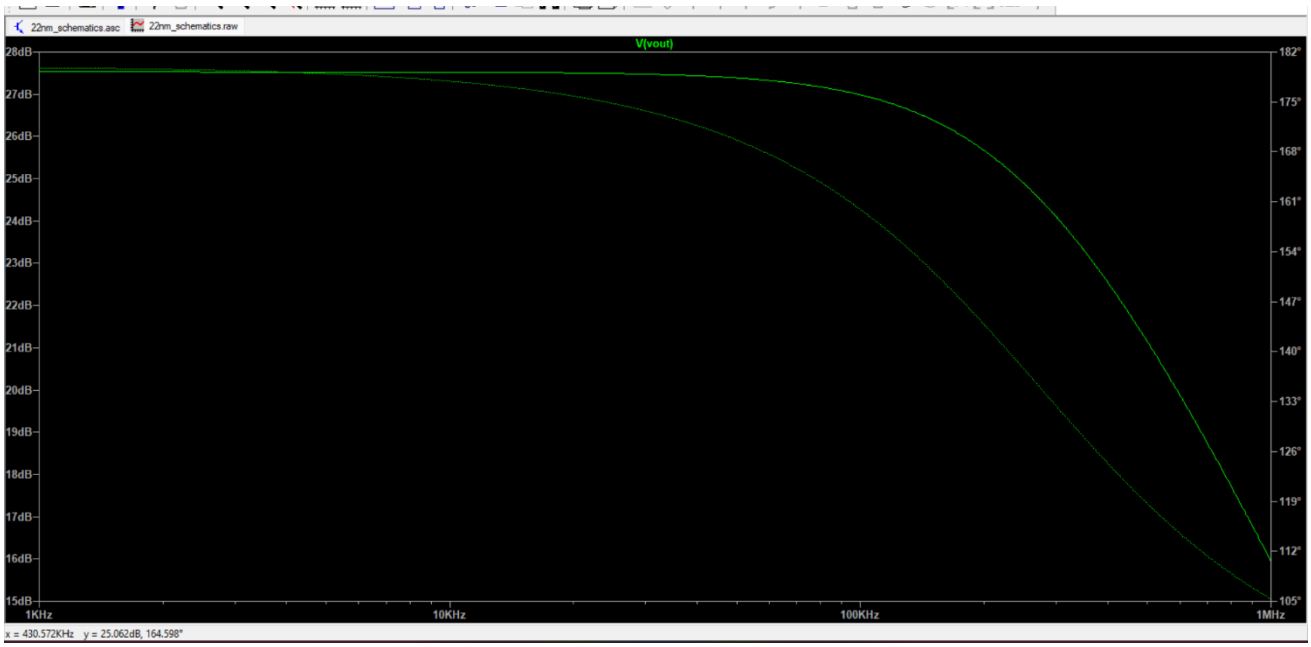


Fig 9. Bode plot for 22nm technology

- Vin=0.50V (DC Bias), Vac=1 mV, f=100kHz
- Output Voltage Swing: (127m to 175m) V = 24mV
- Amplitude of Swing= 24mV
- Gain= 24V/V
- Gain = 27.46dB for F<500kHz
- Pd = 0.0006uW < 5mW

MAGIC layout:

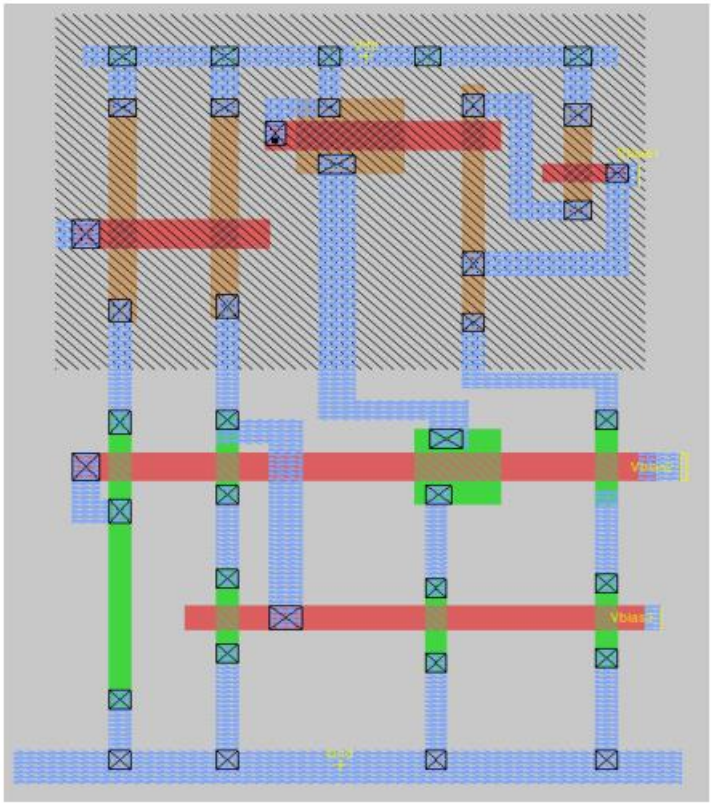


Fig 10. Current mirror layout for 180nm technology

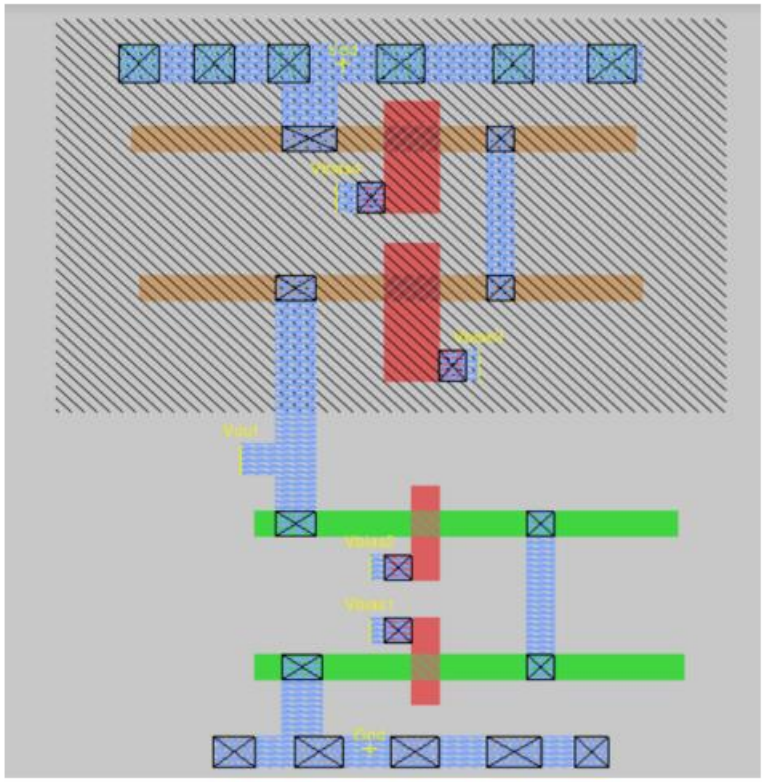


Fig 11. Cascode amplifier layout for 180nm technology

Conclusion:

Simulations and practical calculations were performed for the Beta Multiplier, Cascode Current Mirror, and Cascode Amplifier using LTspice and Magic software. The results from these analyses exhibited strong concordance. The observation tables demonstrate that the estimated, computed, and LTspice values for different parameters fall within similar ranges, affirming that the simulations and practical calculations are in good agreement with each other.