

Performance Degradation of High Voltage LDMOS-FET in the Presence of Total Ionisation Dose Radiation

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by

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Abstract

The successful implementation of high voltage devices in the harsh environments of space and nuclear reactors depends on the total ionisation dose (TID) analysis of those devices. There is currently no literature on the electrical TID response of laterally diffused metal oxide semiconductors (LDMOS) for gamma irradiation (Co-60) with pre- and post-annealing at high temperatures. This report highlights an experimental and simulation examination of the impacts of post-high temperature annealing and TID on LDMOS-FET. Further, we also examined the electrical behaviour of n-channel LDMOS FETs prior to, and after annealing at 168 hours at 100 degrees Celsius with the worst bias conditions. Threshold voltage drift, off-state source to drain leakage current magnitude, transconductance (g_m), and output conductance (g_{ds}) are indicators of a device's radiation tolerance. To illustrate the radiation sensitivity of LDMOS devices, experimental along with simulated test results of input ($I_{DS} - V_{GS}$) and output ($I_{DS} - V_{DS}$) characteristics with drift length are plotted for pre, post, and after annealing. After 400 Krad(Si) TID irradiation, a 20 mV shift in the threshold voltage is found, but the subthreshold leakage current increases by three orders. Electrical data analysis shows that LDMOS devices are extremely vulnerable to TID irradiation; therefore, it is necessary to use proper process and designing strategies to reduce the effects of TID on LDMOS FET. The development of Radhard LDMOS devices is encouraged by this analysis.

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Chapter 1

Introduction to High Voltage MOSFET

The MOSFETs are made for low-to-medium voltage operations between 0.8 to 6 V in digital, analogue, mixed-signal, and RF applications. However, many analogue applications need transistors that can handle currents of several amps and voltages above 20 V. These transistors are known as power and high-voltage transistors. LDMOS (as shown in Fig. 1.1) is a type of power mosfet which is used in many applications such as analog switches, high voltage driver ICs, space satellite systems, military electronic systems, DC-DC converters [1] and power management ICs. LDMOS stands for lateral double-diffused MOS transistor. The D in LDMOS specifies the double diffusion of Boron and Arsenic through the same oxide opening and L (lateral) signifies the current direction which is parallel to the silicon surface.

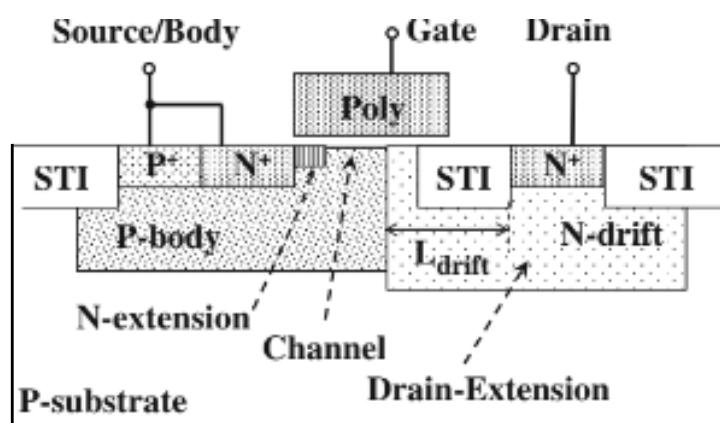


Figure 1.1: N-channel LDMOS

1.1 Drift Region

The drift region (as shown in Fig. 1.2) in LDMOS is an extended lightly doped region of polarity similar to drain. Its purpose is to bifurcate the drain voltage and sustain high voltage on itself. The drift length (L_{drift}) and thickness (t_{drift}), and the doping concentration (N_{drift}) in the drift region are the most important parameters that determine the device characteristics. It should be lightly doped and long enough to support the majority of the drain voltage, keeping the lateral field below the level necessary for avalanche breakdown. The field in oxide should continue to be below the safe operating point. The resistance across the drift region is termed as R_{drift} which is the most significant part of on resistance ($R_{ds(on)}$). The reverse-biased drain-to-substrate/P-well connections are represented by a single "blocking diode." [2]

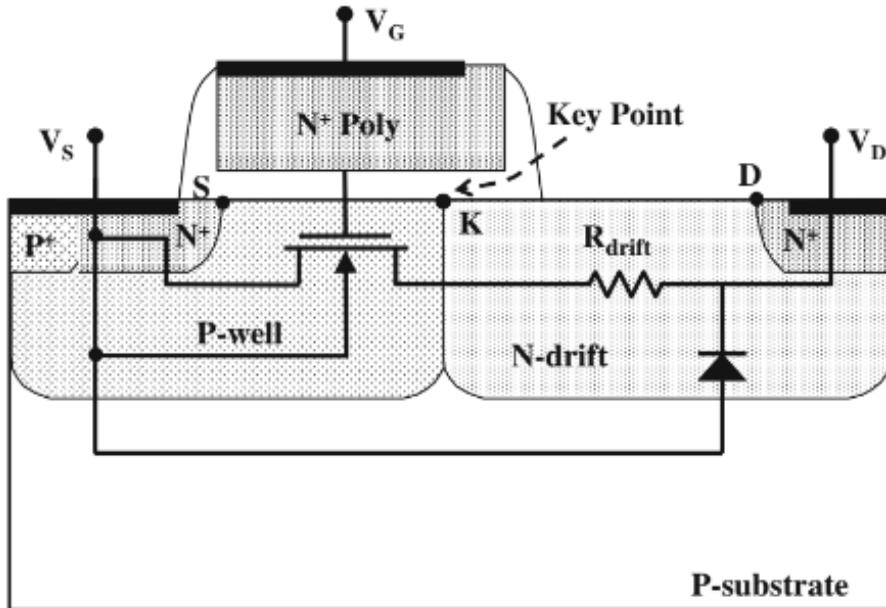


Figure 1.2: N-channel drain-extended transistor [2]

1.2 On State Analysis

1.2.1 On Resistance $R_{ds(on)}$

The drain to source resistance ($R_{ds(on)}$) is an important parameter which is responsible for the power losses and efficiency of LDMOS. In order to reduce the power losses it should be kept low. The $R_{ds(on)}$ is a combination of source/drain resistance, channel resistance and drift resistance (as shown in equation 1.1).

$$R_{DS(on)} = R_{Source} + R_{Drain} + R_{Channel} + R_{Drift} + R_{acc.} \quad (1.1)$$

where, $R_{acc.}$ is the resistance of gate overlapped drift region.

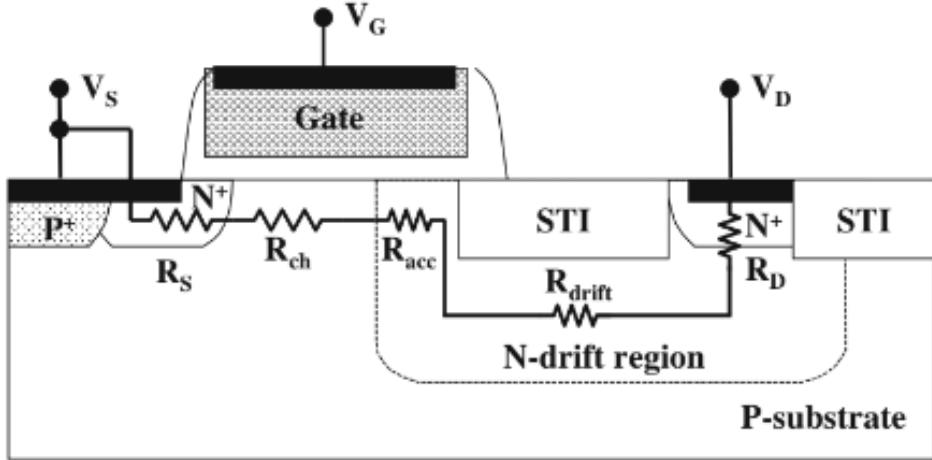


Figure 1.3: LDMOS Resistor components [2]

$$R_{drift} = \frac{1}{(q)(\mu_N)(N_D)(t_{drift} - t_{STI})} \quad (1.2)$$

$$R_{on(specific)} = R_{ds(on)} * DeviceArea \quad (1.3)$$

1.3 Off State Analysis

The breakdown voltage (BV_{DSS}) is the crucial component of off state analysis. When the drain is reverse biased and the body, gate, and source are grounded, the MOSFET is off. In off state most of voltage that is applied to the drain is dropped across drift region. The drain extended region should be uniformly doped.

1.3.1 Analysis of Breakdown Voltage

In off state analysis, drain is reversed biased and the body, gate and source are grounded. Due to this biasing condition the drift region is depleted. The drift region is divided into three parts that are initially assumed to be independent of each other: (1) the MOS region under the gate (2) the lateral junction (3) the vertical junction

Due to the reverse biased, the drain has the ability to deplete the MOS region under the gate, the drift region is vertically exhausted at a distance of X_{dn1} (as shown in Fig.1.4). Notably, just the area beneath the gate is depleted. The vertical junction which is the zone between drift and substrate (X_{dn3} X_{dp3}) as well as the lateral junction between P-well and N-well (Y_{dp2} Y_{dn2}), is also depleted by the reverse bias nature of drift and P-body.

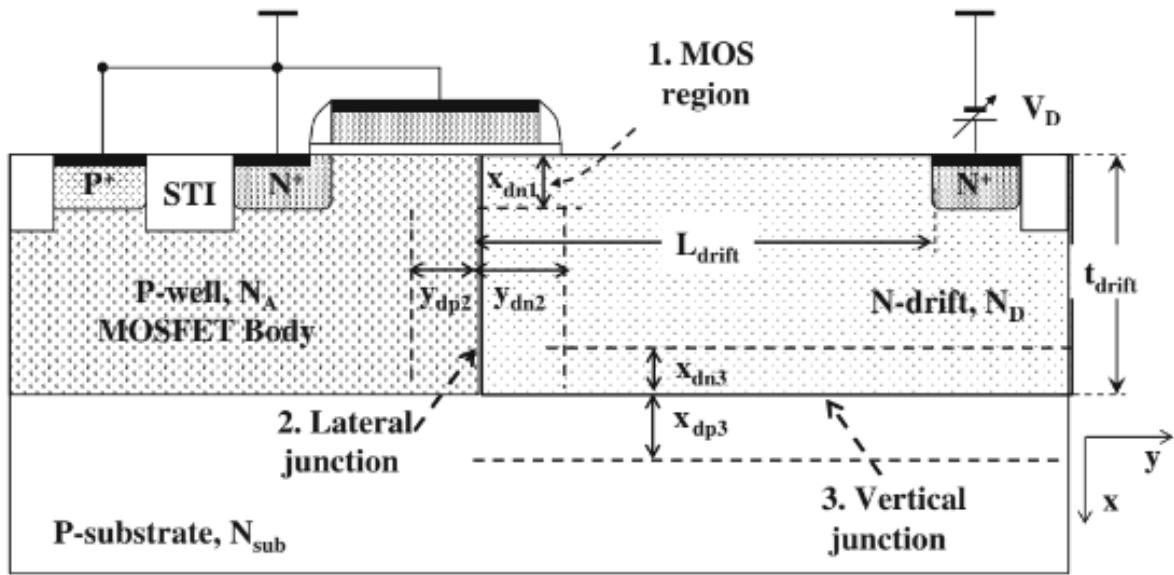


Figure 1.4: Cross-section view of a drain-extended structure with bias applied, showing the key regions for BV_{DSS} analysis [2]

The surface under the gate area keeps growing but cannot invert as the V_{DG} (drain to gate voltage) increases because the gate gets more negative with respect to the drift region. Instead, the surface enters a profound state of deep depletion, and the majority of the drain voltage decreases throughout the depletion area. As a result, MOSFETs can operate at high drain-to-gate voltages and the overall electric field across the gate oxide is reduced.

The charge in the depletion region would let say in X_{dn1} would be :-

$$Q = q(N_D)X_{dn1} \quad (1.4)$$

The electric field in the silicon region corresponding to the depletion width X_{dn1} would be:-

$$E_{si} = \frac{Q}{\epsilon_0 \epsilon_{si}} \quad (1.5)$$

The field in the oxide can be found using continuity equation for the displacement vector:-

$$E_{ox} = Es \frac{esi}{e_{ox}} \quad (1.6)$$

When examined individually, the drift-to-body junction-2 often displays a lower breakdown voltage than the drift-to-substrate junction-3 for a sufficiently long and deep drift area (as shown in Fig. 1.5). This is brought on by the P-body's higher boron content than the substrate. The breakdown voltage of the drift-to-body junction limits the transistor breakdown voltage, BV_{DSS} , under the aforementioned assumptions, where the depletion areas of the two junctions do not interact. [2]

$$BV_{DSS} = e0esi \frac{Ec^2}{2q(N_D)} \quad (1.7)$$

1.3.2 Reduced Surface Field, RESURF

The phenomenon known as RESURF occurs when the depletion regions of various junctions overlap, as shown in the figure(FIG RESURF), causing the depleted charge to be divided amongst those junctions. As a result of charge sharing, the effective electric field is diminished, allowing for the imposition of a high reverse voltage prior to the critical threshold for avalanche breakdown. This reduced electric field is referred to as a REduced SURface Field since it occurs close to the surface. It provides a trade-off between the LDMOS on resistance and breakdown voltage.

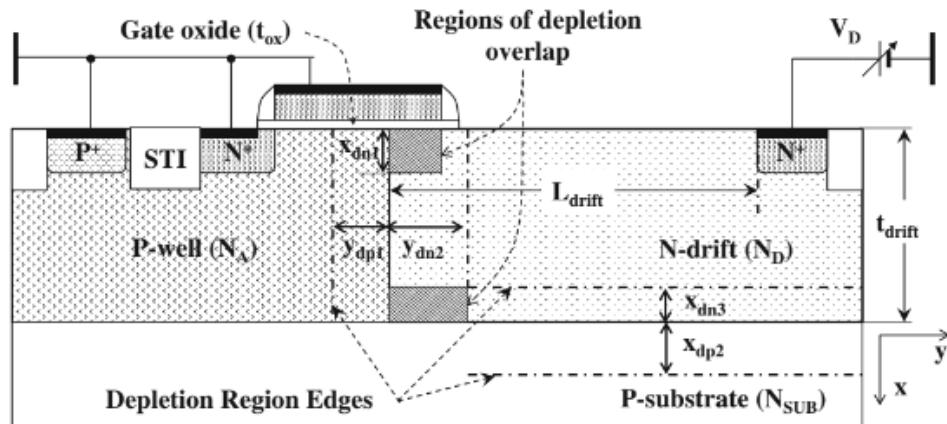


Figure 1.5: Drain-extended structure with overlapping MOS, lateral and vertical depletion regions [2]

1.3.3 Single RESURF Technique

The drift-to-substrate junction, the only junction having a depletion region in the single RESURF approach, interacts with the lateral drift-to-body junction. The thickness of the drift layer affects the breakdown voltage for a particular Nd, Nsub, and P-body concentration.

A small charge is shared between two junctions when t_{drift} is large compared to the thickness of the P-body. The peak field at the drift-to-body (p-well) junction reaches the critical field for avalanche breakdown earlier than at the drift-to-substrate junction because the p-well has a higher concentration than the substrate. Thus the transistor breakdown voltage BV_{DSS} is essentially limited by that of the drift-to-body junction.

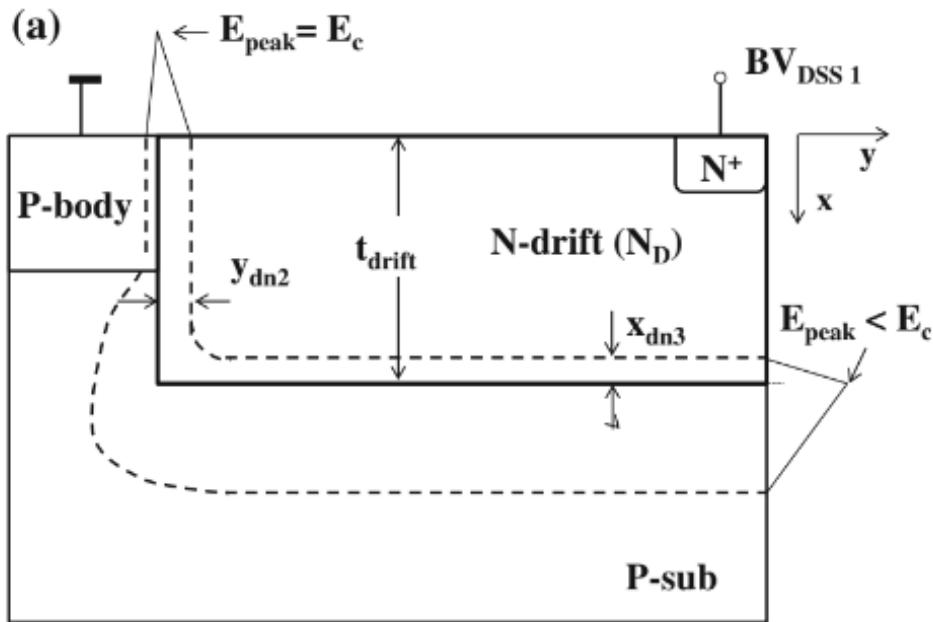


Figure 1.6: Thick t_{drift} so that no interaction with drift-to-pbody depletion region [2]

When t_{drift} is equivalent to X_{dn3} the horizontal drift-to-substrate junction begins to control the majority of the depleted charge (stretches further and approaches the surface. see Fig. 1.6) which reduces the effective ionised concentration in the drift area offered by the p-body. The drift-to-p-body junction (Y_{dn2}) must therefore stretch over a considerable area roughly equivalent to L_{drift} in order to maintain charge balance, which would further reduce the lateral field. Therefore, before the critical electric field is reached, a greater reverse voltage can be delivered to the drain.

The field distribution in drift region exhibits two peak fields, one at drift-body junction and another at drift-drain junction. The breakdown at drift-drain junction can be prevented by

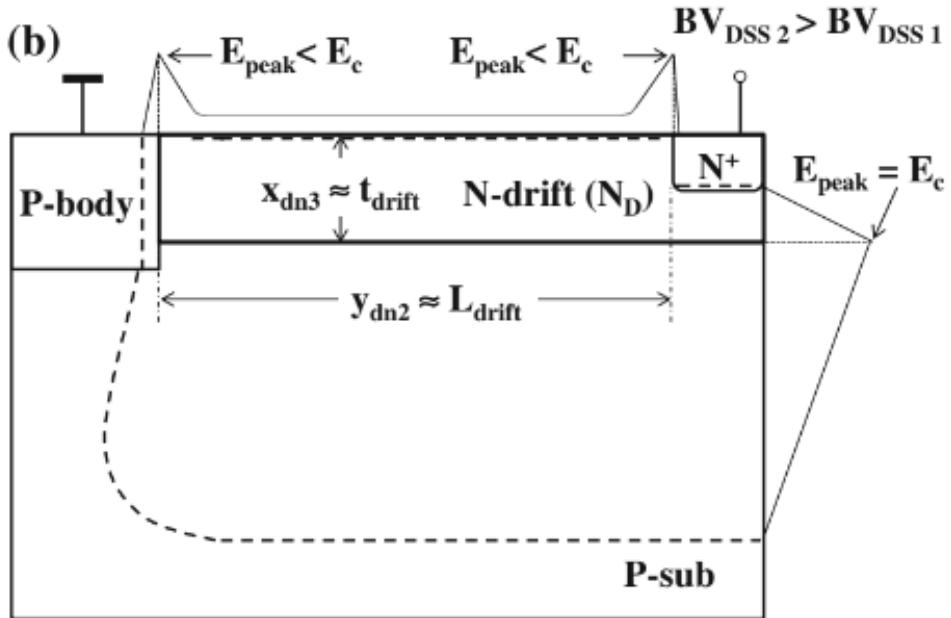


Figure 1.7: Thin t_{drift} , optimised interaction between depletion regions and breakdown occurs at drift-to-substrate junction [2]

increasing the L_{drift} which further increases the on resistance. After optimising the structure, X_{dn3} reaches the surface before the drift-body junction breaks down, that is, before the peak fields reach the critical field E_c .

The RESURF has four parameters for its proper optimization:- (1)N-drift concentration (2)N-drift thickness (3)P-substrate concentration (4)P-body concentration

The basic goal of high-voltage transistor design is to reduce on resistance while maintaining a high breakdown voltage. However, the doping and drift region thickness requirements for these two factors frequently contradict. The product of $N_D \times t_{drift}$ determines the sheet resistance of the drift region. The sheet resistance should be optimized upto its best. Lower N-drift sheet resistance is produced by higher drift region N_D doping concentration and higher substrate doping N_{sub} . This is due to the fact that N_D must be increased in order to retain the same optimized N-drift thickness and N_D/N_{sub} ratio. However, increasing the substrate concentration has a negative impact on the drift-to-substrate junction's breakdown voltage and capacitance. So there is trade-off between on-resistance breakdown voltage.

1.3.4 Double RESURF Technique

To increase the trade-off between on-resistance breakdown voltage, employ the double RESURF approach. In order to maintain the voltage without employing the double RESURF approach, we continuously lengthen the drift, which increases $R_{DS(on)}$. An opposing polarity of RESURF (P_{top} in the N drift zone) is incorporated in the double RESURF approach. The total depletion of the drift region is now caused by the P_{top} and substrate. A new P_{top} -to-drift region junction is added for depletion. Before the lateral breakdown voltage of the N^+ drain-to- P_{top} junction is reached, the P_{top} layer and N_{drift} area must be completely depleted in order for there to be a significant breakdown voltage.

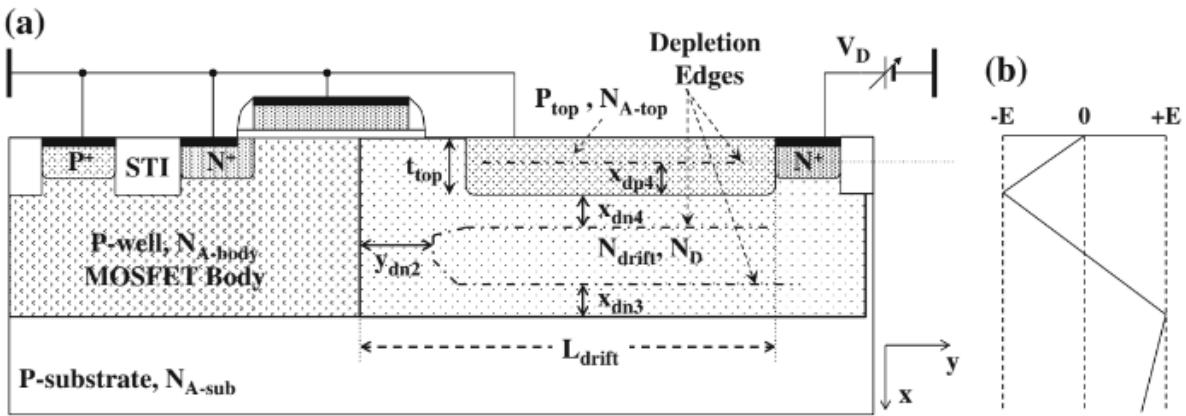


Figure 1.8: Double-RESURF structure. (a) Schematic cross section. (b) Field distribution assuming full depletion [2]

The integrated concentration in the drift zone between the top and bottom junctions can be increased by almost a factor of 2, to around $2.8 \times 10^{12} cm^2$, because the drift region is simultaneously depleted from both the top and bottom junctions, in contrast to a single RESURF structure of the same drift thickness, and still be completely depleted before breakdown takes place. As a result, a significantly lower drift sheet resistance can be attained.

1.3.5 Triple RESURF Technique

The sole distinction between a triple RESURF technique and a double RESURF is that the P_{top} layer is buried deep within the drift region. As a result, before the breakdown voltage of the N^+ -drain-to- P_{top} junction is achieved, another P_{top} -to-drift junction will begin depleting the drift region more quickly. To further reduce the drift sheet resistance and subsequently $R_{DS(on)}$, the

integrated concentration in the drift region can be increased by roughly a factor of three when compared to a single RESURF structure and by a factor of 1.5 when compared to a double RESURF structure.

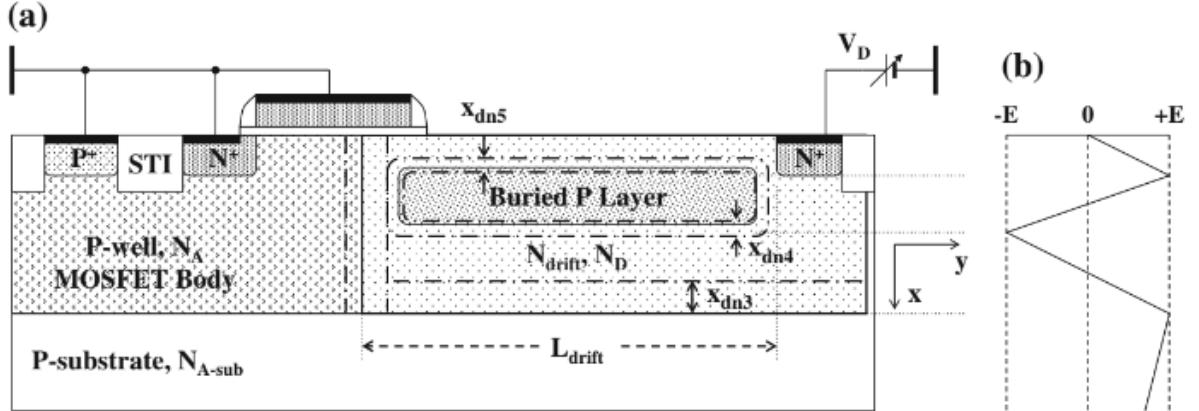


Figure 1.9: Triple-RESURF structure. (a) Schematic cross section. (b) Vertical field distribution at midpoint of L_{drift}, assuming full depletion [2]

1.4 Trade Off between R_{SP} and BV_{DSS}

For designing the high voltage transistors, the main objective is to simultaneously reduce the specific resistance (R_{SP}) and attain the highest breakdown voltage (BV_{DSS}). The dominant part of the specific resistance is drift resistance which reduces while increasing N_D (doping concentration of drift region). Whereas the breakdown voltage is inversely proportional to N_D. While increasing N_D for lowering the specific resistance the corresponding breakdown voltage decreases. Hence there is a trade-off between R_{SP} and BV_{DSS}. [2]

$$R_{SP} = \frac{L_{drift}}{q(u_n)(N_D)} \quad (1.8)$$

$$L_{drift} = \frac{2BV}{E_c} \quad (1.9)$$

Chapter 2

Literature survey

2.1 Radiation on LDMOS

2.1.1 Necessity for the study of Radiation effects on LDMOS

From 24V for portable electronics to 700V for telecommunications and industrial use, LDMOS offers a wide range of applications. Because of its capacity to maintain high voltage, high power transistors are now being used more frequently in power switches and DC-DC converters for satellite systems. High power gadgets that are readily accessible on the market perform poorly in radiation settings. Thus, one of the main objectives of space researchers is the creation of radiation-tolerant LDMOS high voltage FETs. For use in abrasive environments like space, nuclear reactors, and high energy particle physics investigations, LDMOS-FET must have a thorough electrical characterization .

2.1.2 Effects of Radiation on LDMOS

The effects of TID radiation on traditional CMOS devices have been well investigated [3]. The effects of the total ionisation dose in silicon-based devices are primarily brought about by two fundamental occurrences. both the creation of interface state traps at the gate oxide and silicon interface and the trapping of radiation-induced positive fixed charges in oxides. Critical electrical characteristics such drive current (I_{ON}), off-state leakage current (I_{OFF}), and threshold voltage (V_{th}) change as a result of the first. The interface trap charges build up over time and following the irradiation pulse causes a shift in sub threshold swing (SS), whereas the oxide trapped charge has a tendency to anneal out over time.The interface charges eventually

outweigh the fixed oxide charges, which may have consequences like rebound (low and negative V_{th} at first for n-channel MOSFETs, but eventually high and positive) [4], [5]

In addition, the development of interface charges impairs drive current and noise margin. Due to the fact that trapped oxide charges are proportional to oxide thickness (t_{ox}), oxide is the region that is most susceptible to TID radiation. The greater the oxide thickness, the more charges it can trap as well as the radiation's associated consequences, such as high leakage current and V_{th} shift. Additionally, the polarity of interface charges may be positive or negative, and these charges may anneal out over time, showing time-dependent behaviour that makes it even harder to forecast a device's tolerance to radiation.

Chapter 3

LDMOS FET structure and Process Flow

Four sections make up this chapter. The first section discusses the design of the LDMOS device, the second section describes the process flow, the third section highlights the prerad and postrad analysis, and the final section compares the experimental data with simulated data.

3.1 LDMOS FET structure

The architecture of LDMOS FET device is similar to conventional MOSFETs, with additional drain region, also known as drift region (N-LDD) is tailored with additional implants (RESURF, STI, nitride spacers) to sustain appropriate doping concentrations and high drain voltage. Shallow Trench Isolation is a technical term. This method stops electric current from leaking between nearby semiconductor components. To safeguard the gate stack and underlying gate oxide throughout further processing like etching, masking, poly deposition etc., the silicon nitride sidewall spacer is kept in place.

The gate oxide thickness TOX of DUTs under test is 7 nm, used for conventional 3.3V 180 nm CMOS process. For all different device artifacts, the gate length (drawn poly) is fixed at 0.6 μm and gate overlap on drift region LN is 0.15 μm . Important parameters of the device design are overlap of gate poly on ntype drift region(LN) and extension of gate poly on source side (LW), which controls critical device performance like off-state breakdown voltage (B_{VDSS}),on resistance (R_{on}) and drive current (I_{ON}) [6]. Fig. 3.1 shows the device structure and list of critical LDMOS FET parameters

Regarding ionising radiation, the isolation oxide for the n-LDD to drain isolation and the presence of thick oxide in the drift zone are crucial components of the LDMOS device

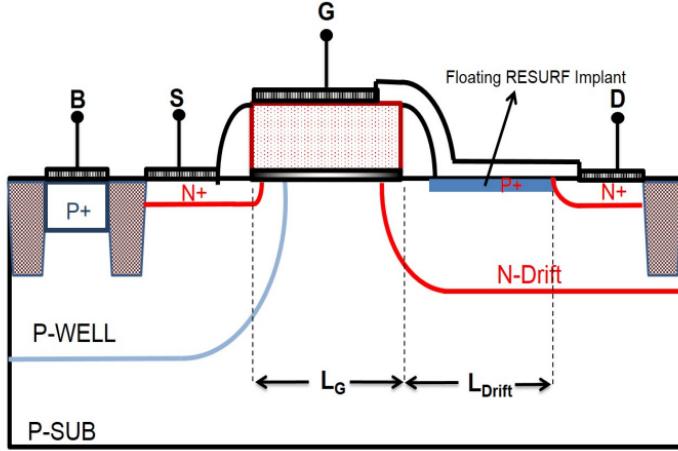


Figure 3.1: LDMOS Device Cross section

LDMOS Gate Length (L_G)	$0.6\mu\text{m}$
Gate Oxide Thickness (G_{OX})	7 nm
Gate Overlap on Drift region L_N	$0.15\mu\text{m}$
Extension of gate poly on source side (L_w)	$0.15\mu\text{m}$
LDMOS drift length (L_{drift})	$1.1\mu\text{m}$
STI depth (STI_d)	$0.43\mu\text{m}$
Gate poly thickness (G_{th})	$0.20\mu\text{m}$
NS Oxide thickness on drain side (NS_{th})	$0.04\mu\text{m}$
Spacer thickness	$0.10\mu\text{m}$
S/D Junction depth	$0.20\mu\text{m}$

Figure 3.2: Device Parameters

architecture. The charge balance in the drift zone of high voltage devices may be altered by the trapped charge in the drift area's oxide and at the interface between oxide and silicon, changing the devices' on resistance and OFF/ON state breakdown voltage. Additionally, these charges produce localised electric fields, which could jeopardise the dependability of a device. So high voltage devices exhibit poor radiation endurance as a result of these extra oxides in key locations.

Use of nitride isolation in place of oxide is one way to get around thick oxide isolation between the gate and drain. However, this nitride isolation necessitates the construction of extra process modules in the traditional process flow with additional mask, ultimately raising the cost and process complexity. Stress under the silicon and the development of silicon flaw sites, which may lead to extra surface leakage, are other problems with nitride.

However, this nitride isolation necessitates the construction of extra process modules in the traditional process flow with additional mask, ultimately raising the cost and process complexity. Stress under the silicon and the development of silicon flaw sites, which may lead to

extra surface leakage, are other problems with nitride.

Due to their low charge trapping capacity, poly buffered oxide or nitride can be employed to fill thick oxide trenches in the drift area of LDMOS device designs. Despite being a process challenge, the filling of trenches with poly buffered oxide/nitride needs to be developed and included as a new process module in the current CMOS baseline process. Such devices are more vulnerable to radiation-induced leakages because to the inadequate rounding of trench corners in drift regions. As a longer polish time reduces the radiation tolerance of these devices, the trench polish time must also be tuned for improved rad hard performance [7]. Therefore, these extra process modules and process adjustments are necessary for the construction of radiation-tolerant high-voltage devices using the baseline process.

3.2 Process Flow

The high voltage process flow starting substrate is argon annealed p-type wafer with resistivity of 1.5 ohm-cm followed by shallow trench isolation unit process module. Subsequent to this Well module integration starts where retrograde n-well and p-well formed with multiple sequence of implants. High quality gate oxide of thickness 70 Å is grown in two step process, where initially 50 Å is partially grown in first step and remaining oxide in subsequent steps. Both MUV and DUV lithography is used to pattern various layers. Shallow S/D extension region is formed and additional mask is used to pattern and implant drift region. After this source/drain (S/D) implantation is carried out and before S/D anneal RESURF implantation of opposite nature of doping than drift is also carried out. Standard Salicidation was followed to this to have low contact resistance and improved circuit speed. At last BEOL module, using undoped silicon di-oxide as ILD and composite layers of oxide and nitride for final passivation was completed.

So, in conclusion high voltage process follows the baseline standard CMOS process flow up-to gate poly patterning with modular process modules dedicated for high voltage process integration. After gate module additional mask is used for drift region implantation and same is used for RESURF region implantation after nitride spacer side wall and source/drain implant. This floating RESURF region is covered with thick oxide to avoid short with source/drain during salicidation. It requires one additional masks, two implants, few additional deposition and etch process for integration. After that standard fabrication sequence of contact pattern, etch

metallization and passivation. The layout of the LDMOS FET device created in the Synopsys Sentaurus TCAD Sdevice is shown in Fig. 3.3.

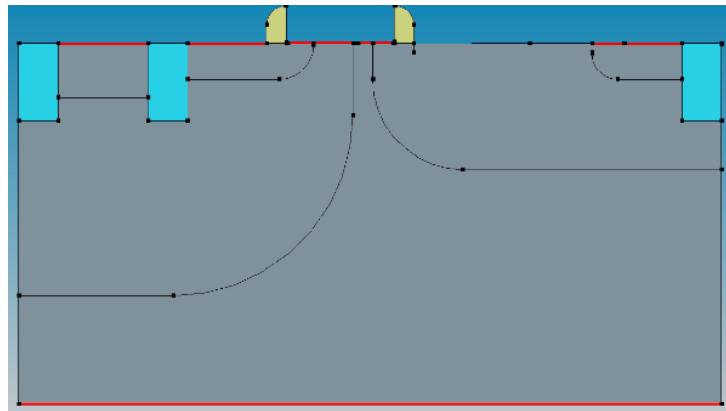


Figure 3.3: LDMOS Device layout in Sentaurus TCAD Sdevice

The doping concentrations for the above device is as follows:-

- Substrate = $1e15/cm^3$ (p-type)
- Pwell = $1e18/cm^3$ (p-type)
- Nwell = $2e17/cm^3$ (n-type)
- Body = $1e15/cm^3$ (p-type)
- Source = $1e20/cm^3$ (n-type)
- Drain = $1e20/cm^3$ (n-type)
- RESURF = $5e13/cm^3$ (p-type)

3.3 Pre Radiation and Post Radiation Analysis

3.3.1 Pre Radiation Analysis

Applying bias voltages $V_{DG} = 0.1V$ and $V_{GS} = 3.3V$ output characteristics of LDMOS FET is observed whose $V_{th} = 0.7$ V off current $I_{OFF} = 1e-12 A/\mu m$ and on current $I_{ON} = 1e-5 A/\mu m$.

The $I_{DS} - V_{GS}$ characteristics is shown in Fig 3.4

Note that the above curve is plotted in semilog scale where Y-axis is logarithmic.

The breakdown analysis is also done by applying drain bias voltage a DC sweep of 30V. Fig 3.5 shows the breakdown curve which is between Id and Vd. In figure itself it is observed that the drain current Id shoots up rapidly at Vd = 20V which depicts its breakdown voltage.

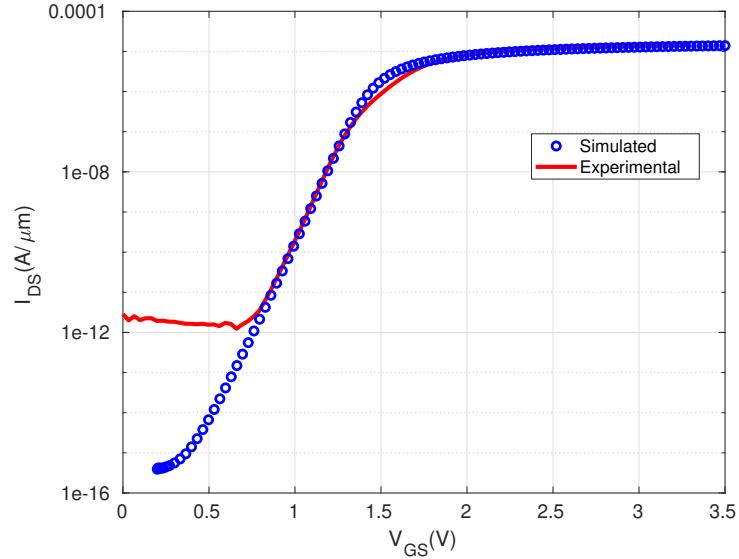


Figure 3.4: Experimental and simulation analysis of transfer characteristics of LDMOS-FET.

3.3.2 Post Radiation Analysis

As mentioned in the sections above, radiation causes fixed and trap charges to form in the gate oxide as well as trap charges at the oxide–silicon contact. It raises I_{OFF} and changes the threshold voltage V_{th} . As the trap concentration or radiation dose rises, the I_{OFF} current does too. At varied concentrations, level type trap charges of 0.50 and 0.55 eV from the conduction band were inserted into the silicon/oxide contact.

- 100K rad/sec corresponds to $5e14 /cm^3$
- 200K rad/sec corresponds to $1.5e15 /cm^3$
- 300K rad/sec corresponds to $3e16 /cm^3$
- 400K rad/sec corresponds to $2e17 /cm^3$

Fig. 3.5 shows the deviation of output characteristics (Id-Vg) from its pre radiation trend.

The breakdown analysis when trap charges are applied at the silicon/oxide interface is shown in Fig. 3.5. As the radiation exposure rises, the breakdown voltage shows an upward trend.

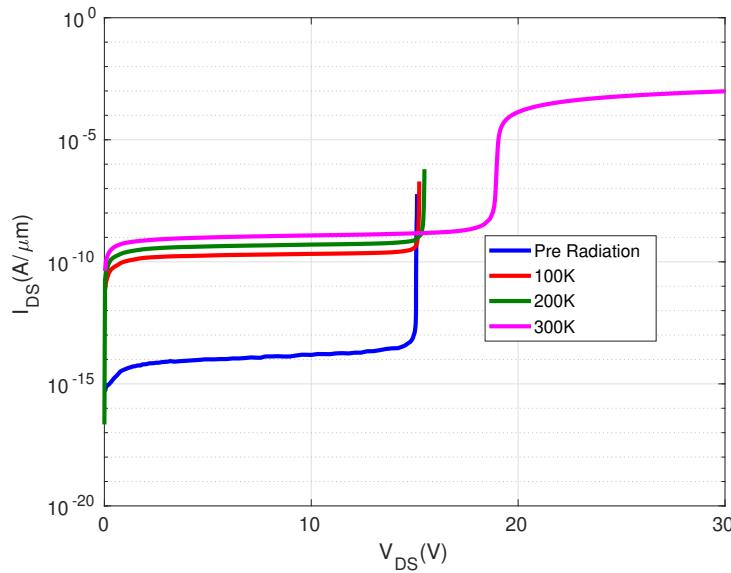


Figure 3.5: Breakdown Analysis at varying dose rate (Id-Vd) characteristics

3.3.3 TID effects on Digital Performance of LDMOS transistor

The basic building block of any digital circuit is inverter. Major effects on digital circuits of TID is on switching speed and on static/dynamic power consumption. In conventional inverters total dose reduces switching speed and increases static and dynamic power consumption. The major parametric changes on LDMOS devices due to 400krad(Si) irradiation is given in Table 3.1.

Table 3.1: Parameteric Variation of LDMOS-FET

Threshold voltage reduction, V_{TH}	20(mV)
Off- state leakage current increase, I_{OFF}	3 orders
Drive current increase, $I_{D,SAT}$	4%
On resistance decrease, R_{ON}	8%

From Table 3.1 it is clear that threshold voltage shift is very minimal for LDMOS devices whereas the off-state leakage current increases significantly by 3 orders. Increase in the saturation current can also be correlated with V_{th} and enhancement in the leakage current. The On resistance (R_{ON}) is also slightly down by 8 percent which also attributed to increase in drive current. So in conclusion, we observed that for 400krad(Si) TID there is no significant adverse effect on digital performance metrics of devices. As off-state breakdown voltage (BV_{DSS}) is also one of the critical parameters of device there is nominal reduction in BV_{DS}

up to 400krad(Si) TID dose and devices can be used for 10V V_{DS} operation. However the sub-threshold slope (SS) do not retrieves to its prerad condition, showing presence of interface states in devices. So, it may be concluded that high temperature annealing may anneals out oxide trap charges but interface state traps remain there and degrade the device performance.

3.3.4 TID effects on Analog Performance of LDMOS Transistor

For analog and mixed circuit performance analog performance parameters such as gm and gds are critical. Pre and post-irradiation gm and gds are plotted up to 400krad(Si) @100krad steps are shown in Fig. 3.6 and Fig.3.7, not much significant change is observed in the characteristics. So up to 400krad (Si) TID irradiation the devices analog performance parameters are well within the limit.

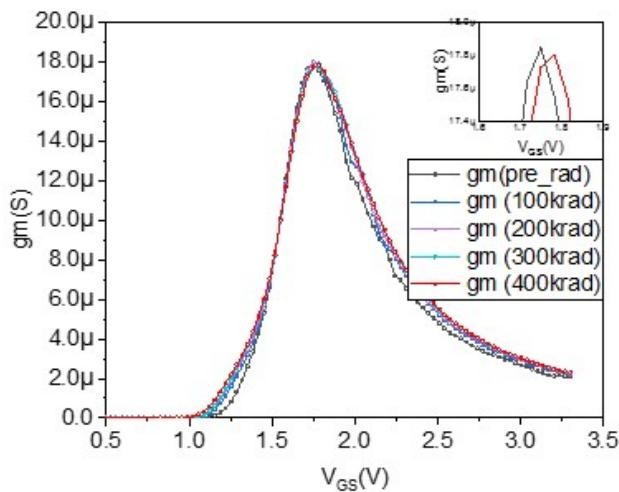


Figure 3.6: Transconductance of pre- and post-radiation of LDMOS-FET.

3.4 Comparing experimental results with simulated results

The Co-60 source and the 10 keV X-Ray source are two frequently utilised sources of total ionising dose. Gamma radiation from the Co-60 gamma cell has an average energy of 1.25 eV. When intense gamma rays contact with silicon devices, they can produce thousands of e-h pairs, and the creation of these e-h pairs results in total dose effects. Compton scattering is the main physical event. According to MIL-Std-883, Test Method 1019, testing must be done at radiation rates between 50 and 300 rad(Si)/s to qualify the devices.

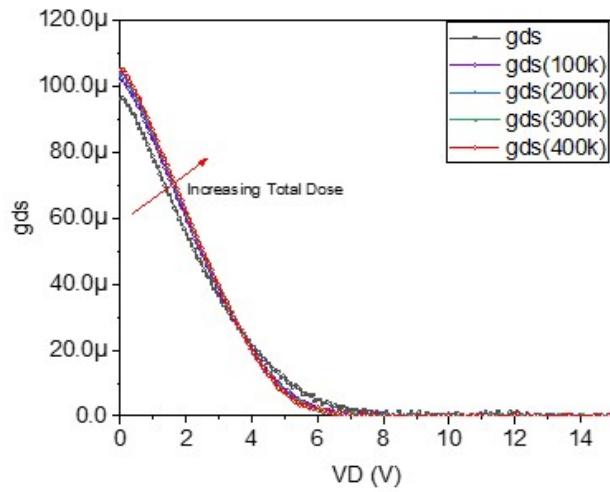


Figure 3.7: Output conductance of pre- and post-radiation of LDMOS-FET.

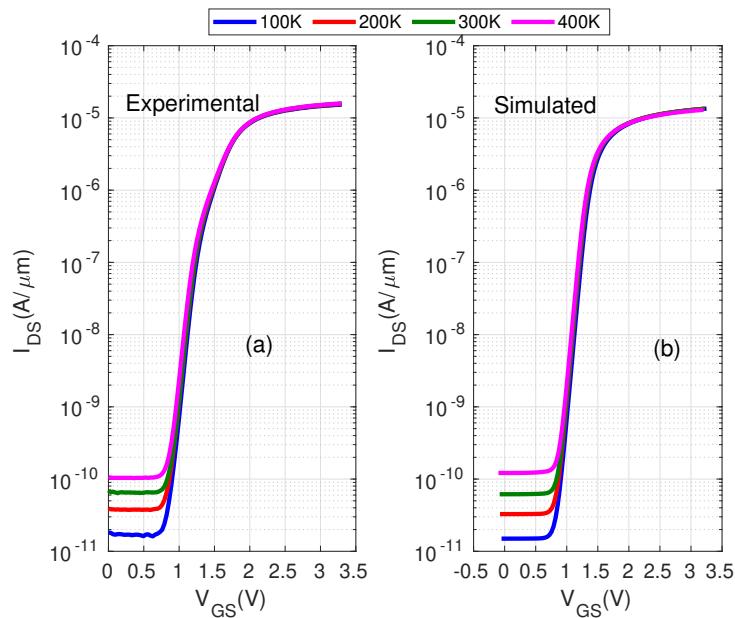


Figure 3.8: Post Radiation Output Characteristics ($I_{DS} - V_{GS}$):(a) Experimental, and (b) Simulated

In this test procedure, the devices are exposed to radiation at room temperature (24.6°C) at any dose rate between 50 and 200 rad(Si)/s for a predetermined dose. All electrical measurements must be made at room temperature because TID effects are also temperature-sensitive. The minimum allowable time between irradiating the device and performing an electrical characterisation is one hour. Under the worst bias situation (Gate=3.3V, source, drain, and body 0V), Total Ionisation Dose (TID) testing are carried out at the package level. Device input

and output characteristics are also measured, and critical device parameters are recorded prior to and throughout each intermediate irradiation phase.

The experimental outcomes after exposure to a Co-60 radiation source at varied dose rates between 100k rad/sec and 400k rad/sec are shown in Fig. 3.8.

Chapter 4

Conclusion

In order to provide high voltage modules for high voltage I/O circuits and dc-dc converters to be employed in space satellite systems, a high voltage LDMOS device is incorporated into the 180nm baseline CMOS process. This study examines the TID behaviour of High Voltage LDMOS before, after, and after annealing up to 400 krad(Si) using a Co-60 Gamma source under the worst bias situation. Although there has been little change in the devices, V_{th} , I_{dSAT} , BV_{DSS} , and R_{ON} , there has been a considerable change in their I_{OFF} , which is bad news for solar-powered battery-operated systems.

LDMOS devices' post-anneal IV characteristics measurement shows noticeable alterations in SS, although I_{OFF} . has returned to its pre-irradiation level. This decrease in the SS shows that gate oxide traps are removed by high temperature annealing, yet interface states brought on by TID irradiation are having an impact on device performance. The cumulative dosage for these LDMOS devices is 100krad(Si). As in this work, displacement damage and single event effects are solely covered for the TID response of LDMOS for Co-60 gamma irradiation.

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