

END TERM EXAMINATION

FIFTH SEMESTER [B.TECH/M.TECH] DECEMBER-JANUARY 2018

Paper Code: IT 305

Time : 3 Hours

Subject: Computer Architecture

Maximum Marks : 75

Note: Attempt any five questions including Q.NO. 1 which is compulsory.
Select one question from each unit.

Q1. Answer the following:

(5x5=25)

- Perform the following decimal numbers to the bases indicated:
7652 to octal and binary
1938 to hexadecimal to binary
175 to binary
- Explain BSA direct addressing, indirect addressing, Immediate addressing and Register addressing.
- Write a program to add two 8 bit numbers using 8085 instruction set.
- Write a short note on micro coded CPU.
- An instruction is stored at location 300 with its address field at location 301. The address field has the value 400. A processor register R1 contains the number 200. Evaluate the effective address if the addressing mode of the instruction is:
 - Direct
 - Immediate
 - Relative

Unit-I

Q2. a) Register A holds the 8 bit binary 11011001. Determine the b operation and the logic microoperation to be perform in order to change the value in A to (4)

i) 01101101

ii) 11111101

b) Explain IEEE 754 floating point standard. (4)

c) Perform the arithmetic operation $(+42)+(-13)$ and $(+42)-(-13)$ in binary using signed 2's complement representation for negative numbers. (4.5)

Q3. a) Show the block diagram of the hardware that implement the following register transfer statement: (5)

$y \leftarrow R_2 \leftarrow R_1, R_1 \rightarrow R_2$

b) Draw a diagram for 4 bit binary adder. (5)

c) What is selective complement operation? (2.5)

Unit-II

Q4. a) Draw a diagram showing basic computer registers connected to a common bus. (8.5)

b) Consider a stack where SP=000000, calculate how many items are there in the stack of: (4)

i) FULL = 1 and EMTY = 0

ii) FULL = 0 and EMTY = 1

Q5. a) Draw a flowchart for showing how an Interrupt is handled by the computer. (6)

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- b) What is the difference between a direct and an indirect address instruction? How many references to memory are needed for each type of instruction to bring an operand into a processor register? (6.5)

Unit-III

Q6. a) What is the difference between hardwired control and microprogrammed control? (3)

b) Explain in details the instruction cycle state diagram with interrupt. (6)

c) What is data bus, Control bus and address bus? (3.5)

Q7. a) A relative mode branch type of instruction is stored in memory at an address equivalent to decimal 750. The branch is made to an address equivalent to decimal 500.

i) What should be the value of the relative address field of the instruction (in decimal)?

ii) Determine the relative address value in the binary using 12 bits. (Why must the no. be in 2's complement?)

iii) Determine the binary value in PC after the fetch phase and calculate binary value of 500. (8)

b) Draw design of accumulator logic. (4.5)

Unit-IV

Q8. Write short notes of the following:

a) DMA (3)

b) A synchronous data transfer (3)

c) RS 422 standard (3)

d) UART (3.5)

END TERM EXAMINATION

FIFTH SEMESTER [B.TECH/M.TECH] DECEMBER-JANUARY 2018

Paper Code: IT 305

Time : 3 Hours

Subject: Computer Architecture

Maximum Marks : 60

Note: Attempt any five questions including Q.NO. 1 which is compulsory.
Select one question from each unit.

(4x5=20)

Q1. Answer the following:

- Perform the following decimal numbers to the bases indicated:
7652 to octal and binary
1938 to hexadecimal to binary
175 to binary
- Explain BSA direct addressing, indirect addressing, Immediate addressing and Register addressing.
- Write a program to add two 8 bit numbers using 8085 instruction set.
- Write a short note on micro coded CPU.
- An instruction is stored at location 300 with its address field at location 301. The address field has the value 400. A processor register R1 contains the number 200. Evaluate the effective address if the addressing mode of the instruction is:
 - Direct
 - Immediate
 - Relative

Unit-I

Q2. a) Register A holds the 8 bit binary 11011001. Determine the b operation and the logic microoperation to be perform in order to change the value in A to

(3)

i) 01101101

ii) 11111101

b) Explain IEEE 754 floating point standard.

(3)

c) Perform the arithmetic operation $(+42)+(-13)$ and $(+42)-(-13)$ in binary using signed 2's complement representation for negative numbers.

(4)

Q3. a) Show the block diagram of the hardware that implement the following register transfer statement:

(4)

y^t: R2 \leftarrow R1, R1 \rightarrow R2

b) Draw a diagram for 4 bit binary adder.

(4)

c) What is selective complement operation?

(2)

Unit-II

Q4. a) Draw a diagram showing basic computer registers connected to a common bus.

(7)

b) Consider a stack where SP=000000, calculate how many items are there in the stack of:

(3)

i) FULL = 1 and EMTY = 0

ii) FULL = 0 and EMTY = 1

Q5. a) Draw a flowchart for showing how an Interrupt is handled by the computer.

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- b) What is the difference between a direct and an indirect address instruction? How many references to memory are needed for each type of instruction to bring an operand into a processor register? (5)

Unit-III

Q6. a) What is the difference between hardwired control and microprogrammed control? (2)

b) Explain in details the instruction cycle state diagram with interrupt. (5)

c) What is data bus, Control bus and address bus? (3)

Q7. a) A relative mode branch type of instruction is stored in memory at an address equivalent to decimal 750. The branch is made to an address equivalent to decimal 500.

i) What should be the value of the relative address field of the instruction (in decimal)?

ii) Determine the relative address value in the binary using 12 bits.
(Why must the no. be in 2's complement?)

iii) Determine the binary value in PC after the fetch phase and calculate binary value of 500. (7)

b) Draw design of accumulator logic. (3)

Unit-IV

Q8. Write short notes of the following: (2.5)

a) DMA (2.5)

b) A synchronous data transfer (2)

c) RS 422 standard (3)

d) UART

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END TERM EXAMINATION

FIFTH SEMESTER [B.TECH] DECEMBER-2014-JANUARY 2015

Paper Code: IT-305

Time: 3 Hours

Subject: Computer Architecture

Maximum Marks: 60

Note: Attempt any five questions including Q.no. 1 which is compulsory.
Select one question from each Unit.

- Q1 Answer the following questions:- (10x2=20)
- (a) Differentiate between Hardwired control and Microprogrammed Control.
 - (b) Explain the cause of Stack overflow.
 - (c) ABCD- seven segment decoder/driver is connected to an LED display. Which segments are illuminated for the input code DCBA = 0001.
 - (d) What is pipeline register?
 - (e) How many 128*8 RAM chips are needed to provide a memory capacity of 2048 bytes?
 - (f) What is Excess 3 code?
 - (g) What is advantage of using Cache memory?
 - (h) What features designate 8085 as an 8 bit processor?
 - (i) What is shift register?
 - (j) What is the basic difference between computer organization and computer architecture.

Unit-I

- Q2 (a) Register A holds the 8-bit binary 11011001. Determine the B operand and the logic micro-operation to be performed in order to change the value in A to:
(i) 01101101 (ii) 11111101. (6)
- (b) Subtract the following using 2's complement.
(i) 1000011 from 10101010 (ii) 72532 from 3250. (2x2=4)

- Q3 (a) Design 4-bit common bus to transfer the contents of one register to other. (6)
(b) Explain IEEE 754 floating point standard with example. (4)

Unit-II

- Q4 (a) Explain 8085 instruction set architecture. (5)
(b) What do you understand by Fetch cycle, instruction cycle and machine cycle? (5)
- Q5 (a) Write a program to evaluate the arithmetic statement. (6)
$$X = (A + B) * (C + D).$$

(i) Using an accumulator type computer with one address instruction.
(ii) Using two and three address instructions and
(iii) Using stack-organized computer with zero address instructions.

- (b) Draw a block diagram of associative memory. (4)

Unit-III

- Q6 (a) Explain stack organization with an example. (5)
(b) What do you mean by indexed addressing mode? (5)

- Q7 (a) What is parallelism and pipelining in computer architecture? (6)
(b) Write a note on Pentium Processor. (4)

Unit-IV

- Q8 (a) Draw a block diagram of associative memory. (5)
(b) What do you mean by memory hierarchy? Briefly discuss. (5)

- Q9 (a) What do you mean by Software and Hardware interrupts? How these are used in microprocessors? (6)
(b) Explain RS-232-C. (4)

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END TERM EXAMINATION

FIFTH SEMESTER [B.TECH./M.TECH.] DECEMBER 2010

Paper Code: IT307

Subject: Digital Signal Processing

Paper ID: 15307

Time : 3 Hours

Maximum Marks : 60

Note: Attempt any five questions.

- Q1** Define (a) linearity (b) shift-invariance (c) causality and (d) stability of a discrete time system. Verify these conditions for the following systems:- (12)

$$(i) T[x(n)] = \sum_{k=n_0}^n x(k)$$

$$(ii) T[x(n)] = \sum_{k=n-n_0}^{n+n_0} x(k)$$

$$(iii) T[x(n)] = x(n - n_0)$$

$$(iv) T[x(n)] = e^{x(n)}$$

- Q2** (a) Define z-transform. Determine the z-transform of the following sequences and give their region of convergence:- (6)

$$(i) \left(\frac{1}{2}\right)^n u(n) \quad (ii) \left(\frac{1}{2}\right)^n (u(n) - u(n-10))$$

- (b) Discuss the z-transform theorems and properties. (6)

- Q3** (a) Explain DFT. Give matrix relations for computing DFT and IDFT. (6)

- (b) Define circular convolution. Evaluate circular convolution of the following sequences- $x(n)=\{1\ 3\ 4\ 2\ 1\}$ and $h(n)=\{2\ 0\ 1\ 0\ 1\}$. (6)

- Q4** (a) Explain the Overlap-Add method for evaluating convolution of infinite length sequence with finite length sequence. (6)

- (b) Give the symmetry property of the DFT of a complex sequence and explain them. (6)

- Q5** (a) Give and explain the network structures for IIR filters. (6)

- (b) Discuss the polyphase realization of FIR filters. (6)

- Q6** (a) How digital filter specifications are given? Explain with the help of magnitude response specifications. (4)

- (b) Explain the process of IIR filter design using bilinear transformation. (8)

- Q7** What are the approaches for decreasing the computational complexity of the DFT? Explain decimation-in-time FFT algorithm with the help of an example. (12)

- Q8** (a) Compare IIR and FIR filters. (4)

- (b) Describe procedure for designing FIR filters using windows. (8)

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END TERM EXAMINATION

FIFTH SEMESTER [B.TECH./M.TECH.] - DECEMBER 2010

Subject: Computer Architecture

Paper Code: IT305

Paper ID: 15305

Time : 3 Hours

Maximum Marks : 60

Note: Attempt any five questions.

- Q1** What do you mean by micro-operations? State their significance. What are the various types? Illustrate the implementation of each category of micro-operations through its block diagram(s). **(12)**
- Q2** (a) Write a short note on microprogrammed control unit architecture. **(7)**
 (b) Write a short note on DMA. **(5)**
- Q3** (a) Why do we require addressing modes? Explain autoincrement, implied and relative addressing mode. **(6)**
 (b) Discuss the difference between RAM and ROM. Explain the various types of RAM used in computer. **(6)**
- Q4** (a) What are the different stages of an instruction cycle? **(5)**
 (b) What are I/O processors? What is their role? Show CPU-IOP communication? **(7)**
- Q5** (a) List and explain the various ports/pins of 8085 microprocessor. **(5)**
 (b) Design parallel priority interrupt hardware for a system with six interrupt sources. **(7)**
- Q6** (a) With the help of an example, perform the multiplication of two unsigned numbers, using shift and add method. **(7)**
 (b) What are the advantages and disadvantage of 2's complement representation over sign magnitude representation? **(5)**
- Q7** (a) Differentiate between programmed versus interrupt driven I/O. **(5)**
 (b) Define Virtual memory. How is it implemented? Explain in detail. **(7)**
- Q8** Write short notes on any three of the following:- **(3x4=12)**
 (a) RS-232-C
 (b) Bus Arbitration Logic
 (c) High Speed Memories
 (d) Levels of programming languages

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END TERM EXAMINATION

FIFTH SEMESTER [B.TECH(CSE/IT)] NOVEMBER-DECEMBER 2018

Paper Code: IT-305

Subject: Computer Architecture

Time: 3 Hours

Maximum Marks: 75

Note: Attempt five questions in all including Q.no.1 which is compulsory.
Select one question from each unit.

- Q1 Answer the following: (10x2.5=25)
- (a) Explain unsigned numbers. Give its notation
 - (b) Explain IEEE 754 floating point standard.
 - (c) Mention any four functions of arithmetic logic shift unit.
 - (d) Explain the features of high speed memory.
 - (e) Give the standard of RS-422.
 - (f) Explain the role of strobe control and handshaking in asynchronous data transfer.
 - (g) Draw microprogrammed sequencer for control memory.
 - (h) Explain register organization and stack organization.
 - (i) Explain the features of first pass and second pass related to assembler.
 - (j) Explain various phases of instruction cycle.

UNIT-I

- Q2 (a) Explain arithmetic and logic microoperation. Give an example for each. (4)
- (b) Perform the subtraction for the following unsigned binary numbers by taking the 2's complement of the subtrahend: $11010 - 10000$. (4.5)
- (c) Explain the following for floating point representation: (4)
(i) mantissa
(ii) exponent
(iii) fraction
(iv) normalization

OR

- Q3 (a) Explain three-state bus buffer. Give an example to illustrate bus and memory transfer instructions. (2+2)
- (b) Starting from an initial value of $R = 11011101$, determine the sequence of binary values in R after a logical shift-left, followed by a circular shift-right, following by a logical shift-right and a circular shift-left. (4)
- (c) Explain bus arbitration with an example. (4.5)

UNIT-II

- Q4 (a) Draw the flow chart of interrupt cycle. (4)
- (b) Mention the features of machine language and assembly language. (4)
- (c) Explain timing and control with an example. (4.5)

OR

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- Q5 (a) Give any two examples of register references instructions and memory reference instructions. (4)
- (b) Give the classification of 8085 instruction set. (4)
- (c) A computer uses a memory unit with 256K words of 32 bits each. A binary instruction code is stored in one word of memory. The instruction has four parts: an indirect bit, an operation code, a register code part to specify one of 64 registers, and an address part.
- (i) How many bits are there in the operation code, the register code part, and the address part? (4)
 - (ii) Draw the instruction word format and indicate the number of bits in each part. (4)
 - (iii) How many bits are there in the data and address inputs of the memory? (4)

UNIT-III

- Q6 (a) Explain the design and implementation of simple CPU. (4)
- (b) Draw the architecture of 8085. (4)
- (c) An instruction is stored at location 300 with its address field at location 301. The address field has the value 400. A processor register R1 contains the number 200. Evaluate the effective address if the addressing mode of the instruction is (a) relative, (b) register indirect and (c) index with R1 as the index register. (4.5)

OR

- Q7 (a) Compare hardwired control and microprogrammed control. Give their applications. (2.5)
- (b) Explain address sequencing in microprogrammed control. Draw the block diagram of selection of address for control memory. (3+3)
- (c) A computer has 16 registers, an ALU (arithmetic logic unit) with 32 operations, and a shifter with eight operations, all connected to a common bus system.
- (i) Formulate a control word for a microoperation. (4)
 - (ii) Specify the number of bits in each field of the control word and give a general encoding scheme. (4)

UNIT-IV

- Q8 (a) Explain the following modes of transfer:
- (i) Programmed I/O (6)
 - (ii) Interrupt-initiated I/O
 - (iii) Direct memory access
- (b) Explain the process of character-oriented and bit-oriented data transfer in serial communication. (3)
- (c) Draw the block diagram of universal asynchronous receiver transmitter. (3.5)

OR

- Q9 (a) Explain the process of address mapping using pages in virtual memory. Give an illustration. (4.5)
- (b) An address space is specified by 24 bits and the corresponding memory space by 16 bits. Answer the following:
- (i) How many words are there in the address space? (3)
 - (ii) How many words are there in the memory space?
- (c) Draw the block diagram of RAM and ROM chips. (5)

END TERM EXAMINATION

FIFTH SEMESTER [B.TECH/M.TECH] DECEMBER 2013

Paper Code: IT-305

Subject: Computer Architecture

Time : 3 Hours

Maximum Marks : 60

Note: Attempt any five questions, including Q.no. 1 is compulsory. Select one question from each Unit.

- Q1 Answer the following questions:- (10x2=20)
- (a) Convert $(215)_{10}$ in BCD.
 - (b) What is Logic Micro Operation.
 - (c) What is Indirect Address.
 - (d) What is Program Counter.
 - (e) Explain an Instruction Format.
 - (f) Differentiate between Hardwired & Microprogramme control unit.
 - (g) Convert the following arithmetic expression from reverse polish notation to infix notation:-
$$ABC * / D - EF / +$$
 - (h) What is set- associative mapping?
 - (i) Differentiate between synchronous and asynchronous data transfer.
 - (j) What is hit ratio?

UNIT-I

- Q2 (a) Explain IEEE 754 floating point representation in detail with the help of an example. (5)
- (b) Perform the subtraction with the following unsigned binary number by taking 2's complement:- (5)
- (i) $11010 - 10000$
 - (ii) $100 - 110000$

OR

- Q3 (a) Show the block diagram of the hardware that implement the following register transfer statement:- (5)
 $y^{T_2} : R_2 \leftarrow R_1, R_1 \leftarrow R_2$
- (b) Draw a diagram for 4-bit binary adder. (5)

UNIT-II

- Q4 Explain different types of basic computer registers and memory with their functions and draw a diagram showing basic computer registers connected to a common bus. (10)

OR

- Q5 (a) Draw a timing diagram assuming that SC is cleared to zero at Time T_3 if control signal C_7 is active. $C_7 T_3 : SC \leftarrow 0$ (5)
- C_7 is activated with positive clock transition associated with T_1 . (5)
- (b) What are input/output interrupts? (5)

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UNIT-III

Q6 (a) Define the following:-

- (i) Micro Operation
- (ii) Micro Instruction
- (iii) Micro Program
- (iv) Micro Code

(5)

(b) What do you mean by decoding of micro operation fields.

OR

(5)

Q7 (a) Consider in a stack $SP = 000000$ ($SP = \text{Stack Point Register}$), then many items are there in the stack if:

- (i) FULL = 1 and EMTY = 0 ?
- (ii) FULL = 0 and EMTY = 1 ?

(5)

(b) What are the basic differences between a branch instruction, a call subroutine instruction, and program interrupt? (5)

UNIT-IV

Q8 Define following **(any two)**:

(5x2=10)

- (a) RS - 232 - C & RS - 422 standard.
- (b) Auxiliary Memory.
- (c) What is Associative Mapping, Direct Mapping, Set- Associative Mapping?

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END TERM EXAMINATION

FIFTH SEMESTER [B.TECH./M.TECH.] DECEMBER 2016

Paper Code: IT-305

Subject: Computer Architecture

Time: 3 Hours

Maximum Marks: 60

Note: Attempts any five questions including Q no. 1 which is compulsory.
Select one question from each unit.

- Q1 Answer the following:- (10x2=20)
- (a) Calculate the sum of $(-28)_{10}$ and $(52)_{10}$ using 2's complement.
 - (b) Write 4040000016 in IEEE 32 BIT FORMAT.
 - (c) What are the reasons for using Virtual Memory?
 - (d) How many cycles a serial adder needs to add two n bit number?
 - (e) What are the two instructions needed in the basic computer in order to set the E flip flop to 1?
 - (f) What do you mean by direct Address? Explain with example.
 - (g) What is a micro instruction?
 - (h) Describe briefly various operations of stack.
 - (i) What do you mean by the instruction $R2 \leftarrow R1$? Explain type of instruction.
 - (j) What are the disadvantages of memory mapped Processor.

UNIT-I

- Q2 (a) If a register holds a value of 10101010, determine its value after the following shift operations: (5)
(i) Arithmetic shift left by 1, circular shift right by 1 and followed by a logical shift left by 1.
(ii) Arithmetic shift right by 1, , circular shift left by 1 and followed by a logical shift right by 1.
(b) Construct a 5-to - 32 line decoder with four 3-to-8 line decoders with enable and one 2-to-4 line decoder. Draw the necessary block diagram. (5)
- Q3 (a) Design an 8 bit combinatorial circuit. (6)
(b) Explain the principle of operation for a carry save adder with examples. (4)

UNIT-II

- Q4 (a) What are the special registers in a computer? Explain their purpose in details. (8)
(b) Explain the various classifications of parallel structures. (2)
- Q5 (a) What are memory reference instructions? (2)
(b) Describe bus and memory transfer with example. (8)

UNIT-III

- Q6 With a neat flow chart, explain the internal control structure of the control unit using- (10)
(i) Hard-wired Control
(ii) Micro programmed Control

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- Q7 (a) An instruction is stored at location 300 with its address field at location 301. The address field has the value 400. A processor register R1 contains the number 200. Evaluate the effective address if the addressing mode of the instruction is: (5)
- (i) Direct
 - (ii) Immediate
 - (iii) Relative
 - (iv) Register Indirect
 - (v) Index with R1 as the index register.
- (b) Explain 8085 instruction set architecture (5)

UNIT-IV

- Q8 (a) Explain the reading and writing operation of a basis static RAM cell. (5)
- (b) A computer has 512 KB cache memory and 2MB main memory. If the block size is 64 bytes, then find out the sub fields for: (5)
- (i) Direct mapped cache
 - (ii) Associative
- Q9 Write short notes on **any two** of the following:- (5x2=10)
- (a) Programmed I/O techniques
 - (b) DMA
 - (c) Vector Interrupt
- *****

END TERM EXAMINATION

FIFTH SEMESTER [B.TECH] DECEMBER 2015

Paper Code: IT-305

Subject: Computer Architecture

Time: 3 Hours

Maximum Marks: 60

Note: Attempt all questions as directed. Internal choice is indicated.

Q1 Answer the following:

- (a) Represent decimal no. 6234 in (i) BCD (ii) Excess 3 code formats.
(b) What is Microprogramming?
(c) Compare logical shift and circular shift with the help of an example.
(d) What is pipeline register?
(e) What are the two instruction needed in the basic computer in order to set the E flip flop to 1?
(f) What do you mean by Indirect Address? Explain with example.
(g) Draw a logic circuit of XOR gate.
(h) Describe briefly various operation of stack.
(i) Explain IEEE 754 floating point standard.
(j) What are memory reference instructions?

(10x2=20)

Unit-I

- Q2 (a) An 8 bit register contains the binary value 10011100. What is the register value after arithmetic shift right? Starting from the initial number 10011100, determine the register value after an arithmetic shift left, and state whether there is an overflow. (5)
(b) Write a short note on Floating point representation with example. Represent the number (+76.8)₁₀ as a floating point number with 24 bits. The normalized fraction mantissa has 16 bits and exponent has 8 bits. (5)

OR

- Q3 (a) Describe bus and memory transfer with example. (8)
(b) Compare and contrast microoperation and microinstruction. (2)

Unit-II

- Q4 (a) Describe various types of basic computer instruction formats showing their opcode combinations with example. (6)
(b) Explain 8085 instruction set architecture. (4)

OR

- Q5 What are interrupts? Explain different types of interrupts. (10)

Unit-III

- Q6 (a) An instruction is stored at location 300 with its address field at location 301. The address field has the value 400. A processor register R1 contains the number 200. Evaluate the effective address if the addressing mode of the instruction is:
(i) Direct
(ii) Immediate
(iii) Relative
(iv) Register indirect
(v) Index with R1 as the index register (5)

- (b) For Microprogrammed control organization discuss the function of control address register, sequencer, pipeline and subroutine register. (5)

OR

- Q7 (a) Give an example to illustrate time and control logic for CPU instruction. (5)
(b) Give an example to illustrate the following:
(i) Three address instruction (ii) RISC instruction. (5)

Unit-IV

(5x2=10)

Q8 Write short notes on any two:

- (a) Virtual Memory
(b) Asynchronous data transfer
(c) RS 422 standard

END TERM EXAMINATION

FIFTH SEMESTER [B.TECH(IT)] DECEMBER- 2019

Paper Code: IT-305

Subject: Computer Architecture

Time : 3 Hours

Maximum Marks :75

Note: Attempt any five questions including Q. No.1 which is compulsory.

- Q1 Explain following in brief:- any five (5x5=25)
- (a) What is Cyclic Stealing? Why it is required?
 - (b) What is opcode, operand and opcode mnemonic? Give example.
 - (c) Why is cache memory faster than RAM?
 - (d) What is in memory cache?
 - (e) Why RAM is not suitable for permanent storage?
 - (f) Explain virtual memory in brief.
- Q2 (a) How the data is transferred between accumulator, bus and memory? What is the role of PC, IR, MBR and MAR during this process? Do they work as multiplexer or decoder? Explain. (6)
(b) Explain Arithmetic micro operations in detail with suitable example. (6.5)
- Q3 Explain following micro operations using example: any five (5x2.5=12.5)
- (a) Selective set and Selective complement
 - (b) Mask Operations
 - (c) Insert Operation
 - (d) Clear Operations
 - (e) Arithmetic Shift left Micro operation and Arithmetic Shift Right Micro operation.
AND, OR and NOT, NAND and NOR, ExOR and Ex-NOR operations
 - (f)
- Q4 (a) Draw and explain instruction cycle and interrupt cycle. (6)
(b) What is Bus arbitration? Explain four types of bus arbitration? Differentiate between centralized bus arbitration and inter-processor arbitration? (6.5)
- Q5 (a) Explain Interrupt Driven I/O Basic Operation. What is Input Output Multiple Interrupts and how they are handled? Discuss the input output modes of transfer in brief. (6)
(b) Distinguish between Programmed I/O and DMA and gives Disadvantage and advantages of each method. What is the role of DMA controller? (6.5)
- Q6 (a) What is the instruction format in computer architecture? What are the types of operands? Discuss its parts and explain different types of instruction format? (6)
(b) Discuss Addressing modes and elaborate the difference between Absolute addressing, Base addressing, Relative addressing and Indirect addressing. (6.5)
- Q7 (a) Differentiate between hardwired control unit and Micro programmed control unit. (6)
(b) Which kind of memories are considered as high speed memory and why? Can a computer run without cache memory? What are the different types of cache memory available in industry? Where is cache memory located? Differentiate between cache and RAM memory in brief. (6.5)
- Q8 Write short note on following: (5x2.5=12.5)
- (a) UART
 - (b) RS-232 and RS-422 standard
 - (c) First pass and second pass assembler
 - (d) IEEE 754 floating point standard
 - (e) Signed and unsigned notations

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END TERM EXAMINATION

FIFTH SEMESTER [B.TECH./M.TECH.] DECEMBER 2016

Paper Code: IT-305

Subject: Computer Architecture

Time: 3 Hours

Maximum Marks: 60

Note: Attempts any five questions including Q no. 1 which is compulsory.
Select one question from each unit.

Q1 Answer the following:-

(10x2=20)

- (a) Calculate the sum of $(-28)_{10}$ and $(52)_{10}$ using 2's complement.
- (b) Write 4040000016 in IEEE 32 BIT FORMAT.
- (c) What are the reasons for using Virtual Memory?
- (d) How many cycles a serial adder needs to add two n bit number?
- (e) What are the two instructions needed in the basic computer in order to set the E flip flop to 1?
- (f) What do you mean by direct Address? Explain with example.
- (g) What is a micro instruction?
- (h) Describe briefly various operations of stack.
- (i) What do you mean by the instruction $R2 \leftarrow R1$? Explain type of instruction.
- (j) What are the disadvantages of memory mapped Processor.

UNIT-I

- Q2 (a) If a register holds a value of 10101010, determine its value after the following shift operations: (5)
(i) Arithmetic shift left by 1, circular shift right by 1 and followed by a logical shift left by 1.
(ii) Arithmetic shift right by 1, , circular shift left by 1 and followed by a logical shift right by 1.
(b) Construct a 5-to - 32 line decoder with four 3-to-8 line decoders with enable and one 2-to-4 line decoder. Draw the necessary block diagram. (5)

- Q3 (a) Design an 8 bit combinatorial circuit. (6)
(b) Explain the principle of operation for a carry save adder with examples. (4)

UNIT-II

- Q4 (a) What are the special registers in a computer? Explain their purpose in details. (8)
(b) Explain the various classifications of parallel structures. (2)
- Q5 (a) What are memory reference instructions? (2)
(b) Describe bus and memory transfer with example. (8)

UNIT-III

- Q6 With a neat flow chart, explain the internal control structure of the control unit using- (10)
(i) Hard-wired Control
(ii) Micro programmed Control

P.T.O.

IT-305

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[-2 -]

- Q7 (a) An instruction is stored at location 300 with its address field at location 301. The address field has the value 400. A processor register R1 contains the number 200. Evaluate the effective address if the addressing mode of the instruction is: (5)
- (i) Direct
 - (ii) Immediate
 - (iii) Relative
 - (iv) Register Indirect
 - (v) Index with R1 as the index register.
- (b) Explain 8085 instruction set architecture (5)

UNIT-IV

- Q8 (a) Explain the reading and writing operation of a basis static RAM cell. (5)
- (b) A computer has 512 KB cache memory and 2MB main memory. If the block size is 64 bytes, then find out the sub fields for: (5)
- (i) Direct mapped cache
 - (ii) Associative
- Q9 Write short notes on **any two** of the following:- (5x2=10)
- (a) Programmed I/O techniques
 - (b) DMA
 - (c) Vector Interrupt

Q

Q4

END TERM EXAMINATION

FIFTH SEMESTER [B.TECH./M.TECH.] DECEMBER 2016

Paper Code: IT-305

Subject: Computer Architecture

Time: 3 Hours

Maximum Marks: 60

Note: Attempts any five questions including Q no. 1 which is compulsory.

Select one question from each unit.

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- (a) Calculate the sum of $(-28)_{10}$ and $(52)_{10}$ using 2's complement.
 - (b) Write 4040000016 in IEEE 32 BIT FORMAT.
 - (c) What are the reasons for using Virtual Memory?
 - (d) How many cycles a serial adder needs to add two n bit number?
 - (e) What are the two instructions needed in the basic computer in order to set the E flip flop to 1?
 - (f) What do you mean by direct Address? Explain with example.
 - (g) What is a micro instruction?
 - (h) Describe briefly various operations of stack.
 - (i) What do you mean by the instruction $R2 \leftarrow R1$? Explain type of instruction.
 - (j) What are the disadvantages of memory mapped Processor.

UNIT-I

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(i) Arithmetic shift left by 1, circular shift right by 1 and followed by a logical shift left by 1.
(ii) Arithmetic shift right by 1, , circular shift left by 1 and followed by a logical shift right by 1.
(b) Construct a 5-to - 32 line decoder with four 3-to-8 line decoders with enable and one 2-to-4 line decoder. Draw the necessary block diagram. (5)
- Q3 (a) Design an 8 bit combinatorial circuit. (6)
(b) Explain the principle of operation for a carry save adder with examples. (4)

UNIT-II

- Q4 (a) What are the special registers in a computer? Explain their purpose in details. (8)
(b) Explain the various classifications of parallel structures. (2)
- Q5 (a) What are memory reference instructions? (2)
(b) Describe bus and memory transfer with example. (8)

UNIT-III

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(i) Hard-wired Control
(ii) Micro programmed Control

P.T.O.

IT-305

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[-2 -]

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- (i) Direct
 - (ii) Immediate
 - (iii) Relative
 - (iv) Register Indirect
 - (v) Index with R1 as the index register.
- (b) Explain 8085 instruction set architecture **(5)**

UNIT-IV

- Q8 (a) Explain the reading and writing operation of a basic static RAM cell. **(5)**
- (b) A computer has 512 KB cache memory and 2MB main memory. If the block size is 64 bytes, then find out the sub fields for: **(5)**
- (i) Direct mapped cache
 - (ii) Associative
- Q9 Write short notes on **any two** of the following:- **(5x2=10)**
- (a) Programmed I/O techniques
 - (b) DMA
 - (c) Vector Interrupt

END TERM EXAMINATION

FIFTH SEMESTER [B.TECH(CSE/IT)] NOVEMBER-DECEMBER 2018

Paper Code: IT-305

Subject: Computer Architecture

Time: 3 Hours

Maximum Marks: 75

Note: Attempt five questions in all including Q.no. 1 which is compulsory.
Select one question from each unit.

- Q1 Answer the following: (10x2.5=25)
- (a) Explain unsigned numbers. Give its notation
 - (b) Explain IEEE 754 floating point standard.
 - (c) Mention any four functions of arithmetic logic shift unit.
 - (d) Explain the features of high speed memory.
 - (e) Give the standard of RS-422.
 - (f) Explain the role of strobe control and handshaking in asynchronous data transfer.
 - (g) Draw microprogrammed sequencer for control memory.
 - (h) Explain register organization and stack organization.
 - (i) Explain the features of first pass and second pass related to assembler.
 - (j) Explain various phases of instruction cycle.

UNIT-I

- Q2 (a) Explain arithmetic and logic microoperation. Give an example for each. (4)
- (b) Perform the subtraction for the following unsigned binary numbers by taking the 2's complement of the subtrahend: $11010 - 10000$. (4.5)
- (c) Explain the following for floating point representation: (4)
(i) mantissa
(ii) exponent
(iii) fraction
(iv) normalization

OR

- Q3 (a) Explain three-state bus buffer. Give an example to illustrate bus and memory transfer instructions. (2+2)
- (b) Starting from an initial value of $R = 11011101$, determine the sequence of binary values in R after a logical shift-left, followed by a circular shift-right, following by a logical shift-right and a circular shift-left. (4)
- (c) Explain bus arbitration with an example. (4.5)

UNIT-II

- Q4 (a) Draw the flow chart of interrupt cycle. (4)
- (b) Mention the features of machine language and assembly language. (4)
- (c) Explain timing and control with an example. (4.5)

OR

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- Q5 (a) Give any two examples of register references instructions and memory reference instructions. (4)
- (b) Give the classification of 8085 instruction set. (4)
- (c) A computer uses a memory unit with 256K words of 32 bits each. A binary instruction code is stored in one word of memory. The instruction has four parts: an indirect bit, an operation code, a register code part to specify one of 64 registers, and an address part. (4.5)
- (i) How many bits are there in the operation code, the register code part, and the address part?
- (ii) Draw the instruction word format and indicate the number of bits in each part.
- (iii) How many bits are there in the data and address inputs of the memory?

UNIT-III

- Q6 (a) Explain the design and implementation of simple CPU. (4)
- (b) Draw the architecture of 8085. (4)
- (c) An instruction is stored at location 300 with its address field at location 301. The address field has the value 400. A processor register R1 contains the number 200. Evaluate the effective address if the addressing mode of the instruction is (a) relative, (b) register indirect and (c) index with R1 as the index register. (4.5)

OR

- Q7 (a) Compare hardwired control and microprogrammed control. Give their applications. (2.5)
- (b) Explain address sequencing in microprogrammed control. Draw the block diagram of selection of address for control memory. (3+3)
- (c) A computer has 16 registers, an ALU (arithmetic logic unit) with 32 operations, and a shifter with eight operations, all connected to a common bus system. (4)
- (i) Formulate a control word for a microoperation.
- (ii) Specify the number of bits in each field of the control word and give a general encoding scheme.

UNIT-IV

- Q8 (a) Explain the following modes of transfer: (6)
- (i) Programmed I/O
 - (ii) Interrupt-initiated I/O
 - (iii) Direct memory access
- (b) Explain the process of character-oriented and bit-oriented data transfer in serial communication. (3)
- (c) Draw the block diagram of universal asynchronous receiver transmitter. (3.5)

OR

- Q9 (a) Explain the process of address mapping using pages in virtual memory. Give an illustration. (4.5)
- (b) An address space is specified by 24 bits and the corresponding memory space by 16 bits. Answer the following: (3)
- (i) How many words are there in the address space?
 - (ii) How many words are there in the memory space?
- (c) Draw the block diagram of RAM and ROM chips. (5)

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END TERM EXAMINATION

FIRST SEMESTER [MCA(SE)] DEC.2014 – JAN.2015

Paper Code: IT-603**Subject: Computer Architecture****Time : 3 Hours****Maximum Marks :60****Note: Attempt any five questions including Q.no.1 which is compulsory.**
Select one question from each unit.

- Q1** Explain briefly the following:- (2)
 (a) Prove that NOR gate is universal gate. (2)
 (b) Discuss VON - Neumann Model. (2)
 (c) What is decoder? Explain 2-bit decoder with the help of a diagram. (2)
 (d) What is locality of reference? (2)
 (e) What is the difference between isolated I/O and memory mapped I/O? (2)
 (f) Define microinstruction and micro operation. (2)
 (g) Explain Excess – 3 code & BCD code. (2)
 (h) Describe any one peripheral device. (2)
 (i) Explain Error detection code. (2)
 (j) What is encoder? (2)

UNIT-I

- Q2** Design 4 – bit bidirectional shift register with parallel load. (10)

- Q3** Design 2 – bit count down counter. This is a sequential circuit with 2 flip flops & one input x . When $x=0$, the state of the flip flops does not change. When $x=1$, the state sequence is 11, 10, 01, 00, 11 & repeat. (10)

UNIT-II

- Q4** An instruction is started at location 300 with its address field at location 301. The address field has the value 400. A processor register R1 contains the number 200. Evaluate the effective address if the addressing mode of the instruction is (a) Direct (b) Immediate (c) Relative (d) Register indirect (e) Index with R1 as the index register. (10)

- Q5** The content of PC in the basic computer is 3AF (all numbers are in hexadecimal). The content of AC is 7EC3. The content of memory at address 3AF is 932E. The content of memory at address 32E is 09AC. The content of memory at address 9AC is 8B9F. (10)
 (a) What is the instruction that will be fetched and executed next?
 (b) Show the binary operation that will be performed in the AC when the instruction is executed.
 (c) Give the contents of registers PC, AR, DR, AC and IR in hexadecimal and the values of E, I and the sequence counter SC in binary at the end of the instruction cycle.

UNIT-III

- Q6** Show the hardware to be used for the addition & subtraction of two decimal numbers in signed – magnitude representation and signed – 2's complement representation. Indicate how an overflow is detected? (10)

- Q7** Show the hardware to be used for the addition & subtraction of fixed point binary data in signed magnitude representation & signed 2's complement. Indicate how an overflow is detected? (10)

UNIT-IV

- Q8** What is Asynchronous data transfer? Explain strobe control and handshaking techniques. (10)
- Q9** What is segmented – page mapping? Draw a neat diagram and explain logical to physical address mapping and mapping in segmented page memory management unit.(10)

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END TERM EXAMINATION

FIFTH SEMESTER [B.TECH] DECEMBER-2014-JANUARY 2015

Paper Code: IT-305

Subject: Computer Architecture

Time: 3 Hours

Maximum Marks: 60

Note: Attempt any five questions including Q.no. 1 which is compulsory.
Select one question from each Unit.

- Q1 Answer the following questions:- (10x2=20)
- (a) Differentiate between Hardwired control and Microprogrammed Control.
 - (b) Explain the cause of Stack overflow.
 - (c) ABCD- seven segment decoder/driver is connected to an LED display. Which segments are illuminated for the input code DCBA = 0001.
 - (d) What is pipeline register?
 - (e) How many 128*8 RAM chips are needed to provide a memory capacity of 2048 bytes?
 - (f) What is Excess 3 code?
 - (g) What is advantage of using Cache memory?
 - (h) What features designate 8085 as an 8 bit processor?
 - (i) What is shift register?
 - (j) What is the basic difference between computer organization and computer architecture.

Unit-I

- Q2 (a) Register A holds the 8-bit binary 11011001. Determine the B operand and the logic micro-operation to be performed in order to change the value in A to:
(i) 01101101 (ii) 11111101. (6)
- (b) Subtract the following using 2's complement.
(i) 1000011 from 10101010 (ii) 72532 from 3250. (2x2=4)

- Q3 (a) Design 4-bit common bus to transfer the contents of one register to other. (6)
(b) Explain IEEE 754 floating point standard with example. (4)

Unit-II

- Q4 (a) Explain 8085 instruction set architecture. (5)
(b) What do you understand by Fetch cycle, instruction cycle and machine cycle? (5)

- Q5 (a) Write a program to evaluate the arithmetic statement. (6)
$$X = (A + B) * (C + D).$$

(i) Using an accumulator type computer with one address instruction.
(ii) Using two and three address instructions and
(iii) Using stack-organized computer with zero address instructions.

- (b) Draw a block diagram of associative memory. (4)

Unit-III

- Q6 (a) Explain stack organization with an example. (5)
(b) What do you mean by indexed addressing mode? (5)

- Q7 (a) What is parallelism and pipelining in computer architecture? (6)
(b) Write a note on Pentium Processor. (4)

Unit-IV

- Q8 (a) Draw a block diagram of associative memory. (5)
(b) What do you mean by memory hierarchy? Briefly discuss. (5)

- Q9 (a) What do you mean by Software and Hardware interrupts? How these are used in microprocessors? (6)
(b) Explain RS-232-C. (4)

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END TERM EXAMINATION

FIFTH SEMESTER [B.TECH(IT)] DECEMBER- 2019

Paper Code: IT-305

Subject: Computer Architecture

Time : 3 Hours

Maximum Marks :75

Note: Attempt any five questions including Q. No.1 which is compulsory.

- Q1 Explain following in brief:- any five (5x5=25)
- (a) What is Cyclic Stealing? Why it is required?
 - (b) What is opcode, operand and opcode mnemonic? Give example.
 - (c) Why is cache memory faster than RAM?
 - (d) What is in memory cache?
 - (e) Why RAM is not suitable for permanent storage?
 - (f) Explain virtual memory in brief.
- Q2 (a) How the data is transferred between accumulator, bus and memory? What is the role of PC, IR, MBR and MAR during this process? Do they work as multiplexer or decoder? Explain. (6)
(b) Explain Arithmetic micro operations in detail with suitable example. (6.5)
- Q3 Explain following micro operations using example: any five (5x2.5=12.5)
- (a) Selective set and Selective complement
 - (b) Mask Operations
 - (c) Insert Operation
 - (d) Clear Operations
 - (e) Arithmetic Shift left Micro operation and Arithmetic Shift Right Micro operation.
AND, OR and NOT, NAND and NOR, ExOR and Ex-NOR operations
 - (f)
- Q4 (a) Draw and explain instruction cycle and interrupt cycle. (6)
(b) What is Bus arbitration? Explain four types of bus arbitration? Differentiate between centralized bus arbitration and inter-processor arbitration? (6.5)
- Q5 (a) Explain Interrupt Driven I/O Basic Operation. What is Input Output Multiple Interrupts and how they are handled? Discuss the input output modes of transfer in brief. (6)
(b) Distinguish between Programmed I/O and DMA and gives Disadvantage and advantages of each method. What is the role of DMA controller? (6.5)
- Q6 (a) What is the instruction format in computer architecture? What are the types of operands? Discuss its parts and explain different types of instruction format? (6)
(b) Discuss Addressing modes and elaborate the difference between Absolute addressing, Base addressing, Relative addressing and Indirect addressing. (6.5)
- Q7 (a) Differentiate between hardwired control unit and Micro programmed control unit. (6)
(b) Which kind of memories are considered as high speed memory and why? Can a computer run without cache memory? What are the different types of cache memory available in industry? Where is cache memory located? Differentiate between cache and RAM memory in brief. (6.5)
- Q8 Write short note on following: (5x2.5=12.5)
- (a) UART
 - (b) RS-232 and RS-422 standard
 - (c) First pass and second pass assembler
 - (d) IEEE 754 floating point standard
 - (e) Signed and unsigned notations

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END TERM EXAMINATION

FIFTH SEMESTER [B.TECH] DECEMBER 2015

Paper Code: IT-305

Subject: Computer Architecture

Time: 3 Hours

Maximum Marks: 60

Note: Attempt all questions as directed. Internal choice is indicated.

Q1 Answer the following:

- (a) Represent decimal no. 6234 in (i) BCD (ii) Excess 3 code formats.
- (b) What is Microprogramming?
- (c) Compare logical shift and circular shift with the help of an example.
- (d) What is pipeline register?
- (e) What are the two instruction needed in the basic computer in order to set the E flip flop to 1?
- (f) What do you mean by Indirect Address? Explain with example.
- (g) Draw a logic circuit of XOR gate.
- (h) Describe briefly various operation of stack.
- (i) Explain IEEE 754 floating point standard.
- (j) What are memory reference instructions?

(10x2=20)

Unit-I

- Q2 (a) An 8 bit register contains the binary value 10011100. What is the register value after arithmetic shift right? Starting from the initial number 10011100, determine the register value after an arithmetic shift left, and state whether there is an overflow. (5)
- (b) Write a short note on Floating point representation with example. Represent the number (+76.8)₁₀ as a floating point number with 24 bits. The normalized fraction mantissa has 16 bits and exponent has 8 bits. (5)

OR

- Q3 (a) Describe bus and memory transfer with example. (8)
(b) Compare and contrast microoperation and microinstruction. (2)

Unit-II

- Q4 (a) Describe various types of basic computer instruction formats showing their opcode combinations with example. (6)
(b) Explain 8085 instruction set architecture. (4)

OR

- Q5 What are interrupts? Explain different types of interrupts. (10)

Unit-III

- Q6 (a) An instruction is stored at location 300 with its address field at location 301. The address field has the value 400. A processor register R1 contains the number 200. Evaluate the effective address if the addressing mode of the instruction is: (5)
- (i) Direct
 - (ii) Immediate
 - (iii) Relative
 - (iv) Register indirect
 - (v) Index with R1 as the index register

- (b) For Microprogrammed control organization discuss the function of control address register, sequencer, pipeline and subroutine register. (5)

OR

- Q7 (a) Give an example to illustrate time and control logic for CPU instruction. (5)
(b) Give an example to illustrate the following: (5)
(i) Three address instruction (ii) RISC instruction.

Unit-IV

(5x2=10)

Q8 Write short notes on any two:

- (a) Virtual Memory
- (b) Asynchronous data transfer
- (c) RS 422 standard

END TERM EXAMINATION

FIFTH SEMESTER [B.TECH./M.TECH.] DECEMBER 2016

Paper Code: IT-305

Subject: Computer Architecture

Time: 3 Hours

Maximum Marks: 60

Note: Attempts any five questions including Q no. 1 which is compulsory.
Select one question from each unit.

- Q1 Answer the following:- (10x2=20)
- (a) Calculate the sum of $(-28)_{10}$ and $(52)_{10}$ using 2's complement.
 - (b) Write 4040000016 in IEEE 32 BIT FORMAT.
 - (c) What are the reasons for using Virtual Memory?
 - (d) How many cycles a serial adder needs to add two n bit number?
 - (e) What are the two instructions needed in the basic computer in order to set the E flip flop to 1?
 - (f) What do you mean by direct Address? Explain with example.
 - (g) What is a micro instruction?
 - (h) Describe briefly various operations of stack.
 - (i) What do you mean by the instruction $R2 \leftarrow R1$? Explain type of instruction.
 - (j) What are the disadvantages of memory mapped Processor.

UNIT-I

- Q2 (a) If a register holds a value of 10101010, determine its value after the following shift operations: (5)
(i) Arithmetic shift left by 1, circular shift right by 1 and followed by a logical shift left by 1.
(ii) Arithmetic shift right by 1, , circular shift left by 1 and followed by a logical shift right by 1.
(b) Construct a 5-to - 32 line decoder with four 3-to-8 line decoders with enable and one 2-to-4 line decoder. Draw the necessary block diagram. (5)
- Q3 (a) Design an 8 bit combinatorial circuit. (6)
(b) Explain the principle of operation for a carry save adder with examples. (4)

UNIT-II

- Q4 (a) What are the special registers in a computer? Explain their purpose in details. (8)
(b) Explain the various classifications of parallel structures. (2)
- Q5 (a) What are memory reference instructions? (2)
(b) Describe bus and memory transfer with example. (8)

UNIT-III

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(i) Hard-wired Control
(ii) Micro programmed Control

P.T.O.

IT-305
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- Q7 (a) An instruction is stored at location 300 with its address field at location 301. The address field has the value 400. A processor register R1 contains the number 200. Evaluate the effective address if the addressing mode of the instruction is: (5)
- (i) Direct
 - (ii) Immediate
 - (iii) Relative
 - (iv) Register Indirect
 - (v) Index with R1 as the index register.
- (b) Explain 8085 instruction set architecture (5)

UNIT-IV

- Q8 (a) Explain the reading and writing operation of a basis static RAM cell. (5)
- (b) A computer has 512 KB cache memory and 2MB main memory. If the block size is 64 bytes, then find out the sub fields for: (5)
- (i) Direct mapped cache
 - (ii) Associative
- Q9 Write short notes on **any two** of the following:- (5x2=10)
- (a) Programmed I/O techniques
 - (b) DMA
 - (c) Vector Interrupt
- *****

END TERM EXAMINATION

FIFTH SEMESTER [B.TECH/M.TECH] DECEMBER 2013

Paper Code: IT-305

Subject: Computer Architecture

Time : 3 Hours

Maximum Marks : 60

Note: Attempt any five questions, including Q.no. 1 is compulsory. Select one question from each Unit.

- Q1 Answer the following questions:- (10x2=20)
- (a) Convert $(215)_{10}$ in BCD.
 - (b) What is Logic Micro Operation.
 - (c) What is Indirect Address.
 - (d) What is Program Counter.
 - (e) Explain an Instruction Format.
 - (f) Differentiate between Hardwired & Microprogramme control unit.
 - (g) Convert the following arithmetic expression from reverse polish notation to infix notation:-
$$ABC * / D - EF / +$$
 - (h) What is set- associative mapping?
 - (i) Differentiate between synchronous and asynchronous data transfer.
 - (j) What is hit ratio?

UNIT-I

- Q2 (a) Explain IEEE 754 floating point representation in detail with the help of an example. (5)
- (b) Perform the subtraction with the following unsigned binary number by taking 2's complement:- (5)
- (i) $11010 - 10000$
 - (ii) $100 - 110000$

OR

- Q3 (a) Show the block diagram of the hardware that implement the following register transfer statement:- (5)
 $y^{T_2} : R_2 \leftarrow R_1, R_1 \leftarrow R_2$
- (b) Draw a diagram for 4-bit binary adder. (5)

UNIT-II

- Q4 Explain different types of basic computer registers and memory with their functions and draw a diagram showing basic computer registers connected to a common bus. (10)

OR

- Q5 (a) Draw a timing diagram assuming that SC is cleared to zero at Time T_3 if control signal C_7 is active. $C_7 T_3 : SC \leftarrow 0$ (5)
- C_7 is activated with positive clock transition associated with T_1 . (5)
- (b) What are input/output interrupts? (5)

P.T.O.

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UNIT-III

Q6 (a) Define the following:-

- (i) Micro Operation
- (ii) Micro Instruction
- (iii) Micro Program
- (iv) Micro Code

(5)

(b) What do you mean by decoding of micro operation fields.

OR

(5)

Q7 (a) Consider in a stack $SP = 000000$ ($SP = \text{Stack Point Register}$), then many items are there in the stack if:

- (i) FULL = 1 and EMTY = 0 ?
- (ii) FULL = 0 and EMTY = 1 ?

(5)

(b) What are the basic differences between a branch instruction, a call subroutine instruction, and program interrupt? (5)

UNIT-IV

Q8 Define following **(any two)**:

(5x2=10)

- (a) RS - 232 - C & RS - 422 standard.
- (b) Auxiliary Memory.
- (c) What is Associative Mapping, Direct Mapping, Set- Associative Mapping?

R.P.E

Please write your Exam Roll No.)

Exam Roll No.

END TERM EXAMINATION

FIFTH SEMESTER [B.TECH(CSE/IT)] NOVEMBER-DECEMBER 2018

Paper Code: IT-305

Subject: Computer Architecture

Time: 3 Hours

Maximum Marks: 75

Note: Attempt five questions in all including Q.no.1 which is compulsory.
Select one question from each unit.

- Q1 Answer the following: (10x2.5=25)
- (a) Explain unsigned numbers. Give its notation
 - (b) Explain IEEE 754 floating point standard.
 - (c) Mention any four functions of arithmetic logic shift unit.
 - (d) Explain the features of high speed memory.
 - (e) Give the standard of RS-422.
 - (f) Explain the role of strobe control and handshaking in asynchronous data transfer.
 - (g) Draw microprogrammed sequencer for control memory.
 - (h) Explain register organization and stack organization.
 - (i) Explain the features of first pass and second pass related to assembler.
 - (j) Explain various phases of instruction cycle.

UNIT-I

- Q2 (a) Explain arithmetic and logic microoperation. Give an example for each. (4)
- (b) Perform the subtraction for the following unsigned binary numbers by taking the 2's complement of the subtrahend: $11010 - 10000$. (4.5)
- (c) Explain the following for floating point representation: (4)
(i) mantissa
(ii) exponent
(iii) fraction
(iv) normalization

OR

- Q3 (a) Explain three-state bus buffer. Give an example to illustrate bus and memory transfer instructions. (2+2)
- (b) Starting from an initial value of $R = 11011101$, determine the sequence of binary values in R after a logical shift-left, followed by a circular shift-right, following by a logical shift-right and a circular shift-left. (4)
- (c) Explain bus arbitration with an example. (4.5)

UNIT-II

- Q4 (a) Draw the flow chart of interrupt cycle. (4)
- (b) Mention the features of machine language and assembly language. (4)
- (c) Explain timing and control with an example. (4.5)

OR

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- Q5 (a) Give any two examples of register references instructions and memory reference instructions. (4)
- (b) Give the classification of 8085 instruction set. (4)
- (c) A computer uses a memory unit with 256K words of 32 bits each. A binary instruction code is stored in one word of memory. The instruction has four parts: an indirect bit, an operation code, a register code part to specify one of 64 registers, and an address part.
- (i) How many bits are there in the operation code, the register code part, and the address part? (4)
 - (ii) Draw the instruction word format and indicate the number of bits in each part. (4)
 - (iii) How many bits are there in the data and address inputs of the memory? (4)

UNIT-III

- Q6 (a) Explain the design and implementation of simple CPU. (4)
- (b) Draw the architecture of 8085. (4)
- (c) An instruction is stored at location 300 with its address field at location 301. The address field has the value 400. A processor register R1 contains the number 200. Evaluate the effective address if the addressing mode of the instruction is (a) relative, (b) register indirect and (c) index with R1 as the index register. (4.5)

OR

- Q7 (a) Compare hardwired control and microprogrammed control. Give their applications. (2.5)
- (b) Explain address sequencing in microprogrammed control. Draw the block diagram of selection of address for control memory. (3+3)
- (c) A computer has 16 registers, an ALU (arithmetic logic unit) with 32 operations, and a shifter with eight operations, all connected to a common bus system.
- (i) Formulate a control word for a microoperation. (4)
 - (ii) Specify the number of bits in each field of the control word and give a general encoding scheme. (4)

UNIT-IV

- Q8 (a) Explain the following modes of transfer: (6)
- (i) Programmed I/O
 - (ii) Interrupt-initiated I/O
 - (iii) Direct memory access
- (b) Explain the process of character-oriented and bit-oriented data transfer in serial communication. (3)
- (c) Draw the block diagram of universal asynchronous receiver transmitter. (3.5)

OR

- Q9 (a) Explain the process of address mapping using pages in virtual memory. Give an illustration. (4.5)
- (b) An address space is specified by 24 bits and the corresponding memory space by 16 bits. Answer the following: (3)
- (i) How many words are there in the address space?
 - (ii) How many words are there in the memory space?
- (c) Draw the block diagram of RAM and ROM chips. (5)

END TERM EXAMINATION

FIFTH SEMESTER [B.TECH./M.TECH.] - DECEMBER 2010

Subject: Computer Architecture

Paper Code: IT305

Paper ID: 15305

Time : 3 Hours

Maximum Marks : 60

Note: Attempt any five questions.

- Q1** What do you mean by micro-operations? State their significance. What are the various types? Illustrate the implementation of each category of micro-operations through its block diagram(s). **(12)**
- Q2** (a) Write a short note on microprogrammed control unit architecture. **(7)**
 (b) Write a short note on DMA. **(5)**
- Q3** (a) Why do we require addressing modes? Explain autoincrement, implied and relative addressing mode. **(6)**
 (b) Discuss the difference between RAM and ROM. Explain the various types of RAM used in computer. **(6)**
- Q4** (a) What are the different stages of an instruction cycle? **(5)**
 (b) What are I/O processors? What is their role? Show CPU-IOP communication? **(7)**
- Q5** (a) List and explain the various ports/pins of 8085 microprocessor. **(5)**
 (b) Design parallel priority interrupt hardware for a system with six interrupt sources. **(7)**
- Q6** (a) With the help of an example, perform the multiplication of two unsigned numbers, using shift and add method. **(7)**
 (b) What are the advantages and disadvantage of 2's complement representation over sign magnitude representation? **(5)**
- Q7** (a) Differentiate between programmed versus interrupt driven I/O. **(5)**
 (b) Define Virtual memory. How is it implemented? Explain in detail. **(7)**
- Q8** Write short notes on any three of the following:- **(3x4=12)**
 (a) RS-232-C
 (b) Bus Arbitration Logic
 (c) High Speed Memories
 (d) Levels of programming languages

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(Please write your Exam Roll No.)

Exam Roll No.

END TERM EXAMINATION

FIFTH SEMESTER [B.TECH] DECEMBER-2014-JANUARY 2015

Paper Code: IT-305

Time: 3 Hours

Subject: Computer Architecture

Maximum Marks: 60

Note: Attempt any five questions including Q.no. 1 which is compulsory.
Select one question from each Unit.

- Q1 Answer the following questions:- (10x2=20)
- (a) Differentiate between Hardwired control and Microprogrammed Control.
 - (b) Explain the cause of Stack overflow.
 - (c) ABCD- seven segment decoder/driver is connected to an LED display. Which segments are illuminated for the input code DCBA = 0001.
 - (d) What is pipeline register?
 - (e) How many 128*8 RAM chips are needed to provide a memory capacity of 2048 bytes?
 - (f) What is Excess 3 code?
 - (g) What is advantage of using Cache memory?
 - (h) What features designate 8085 as an 8 bit processor?
 - (i) What is shift register?
 - (j) What is the basic difference between computer organization and computer architecture.

Unit-I

- Q2 (a) Register A holds the 8-bit binary 11011001. Determine the B operand and the logic micro-operation to be performed in order to change the value in A to:
(i) 01101101 (ii) 11111101. (6)
- (b) Subtract the following using 2's complement.
(i) 1000011 from 10101010 (ii) 72532 from 3250. (2x2=4)

- Q3 (a) Design 4-bit common bus to transfer the contents of one register to other. (6)
(b) Explain IEEE 754 floating point standard with example. (4)

Unit-II

- Q4 (a) Explain 8085 instruction set architecture. (5)
(b) What do you understand by Fetch cycle, instruction cycle and machine cycle? (5)
- Q5 (a) Write a program to evaluate the arithmetic statement. (6)
$$X = (A + B) * (C + D).$$

(i) Using an accumulator type computer with one address instruction.
(ii) Using two and three address instructions and
(iii) Using stack-organized computer with zero address instructions.

- (b) Draw a block diagram of associative memory. (4)

Unit-III

- Q6 (a) Explain stack organization with an example. (5)
(b) What do you mean by indexed addressing mode? (5)

- Q7 (a) What is parallelism and pipelining in computer architecture? (6)
(b) Write a note on Pentium Processor. (4)

Unit-IV

- Q8 (a) Draw a block diagram of associative memory. (5)
(b) What do you mean by memory hierarchy? Briefly discuss. (5)

- Q9 (a) What do you mean by Software and Hardware interrupts? How these are used in microprocessors? (6)
(b) Explain RS-232-C. (4)

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END TERM EXAMINATION

FIFTH SEMESTER [B.TECH/M.TECH] DECEMBER-JANUARY 2018

Paper Code: IT 305

Time : 3 Hours

Subject: Computer Architecture

Maximum Marks : 75

Note: Attempt any five questions including Q.NO. 1 which is compulsory.
Select one question from each unit.

Q1. Answer the following:

(5x5=25)

- Perform the following decimal numbers to the bases indicated:
7652 to octal and binary
1938 to hexadecimal to binary
175 to binary
- Explain BSA direct addressing, indirect addressing, Immediate addressing and Register addressing.
- Write a program to add two 8 bit numbers using 8085 instruction set.
- Write a short note on micro coded CPU.
- An instruction is stored at location 300 with its address field at location 301. The address field has the value 400. A processor register R1 contains the number 200. Evaluate the effective address if the addressing mode of the instruction is:
 - Direct
 - Immediate
 - Relative

Unit-I

Q2. a) Register A holds the 8 bit binary 11011001. Determine the b operation and the logic microoperation to be perform in order to change the value in A to (4)

i) 01101101

ii) 11111101

b) Explain IEEE 754 floating point standard. (4)

c) Perform the arithmetic operation $(+42)+(-13)$ and $(+42)-(-13)$ in binary using signed 2's complement representation for negative numbers. (4.5)

Q3. a) Show the block diagram of the hardware that implement the following register transfer statement: (5)

$y \leftarrow R_2 \leftarrow R_1, R_1 \rightarrow R_2$

b) Draw a diagram for 4 bit binary adder. (5)

c) What is selective complement operation? (2.5)

Unit-II

Q4. a) Draw a diagram showing basic computer registers connected to a common bus. (8.5)

b) Consider a stack where SP=000000, calculate how many items are there in the stack of: (4)

i) FULL = 1 and EMTY = 0

ii) FULL = 0 and EMTY = 1

Q5. a) Draw a flowchart for showing how an Interrupt is handled by the computer. (6)

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- b) What is the difference between a direct and an indirect address instruction? How many references to memory are needed for each type of instruction to bring an operand into a processor register? (6.5)

Unit-III

Q6. a) What is the difference between hardwired control and microprogrammed control? (3)

b) Explain in details the instruction cycle state diagram with interrupt. (6)

c) What is data bus, Control bus and address bus? (3.5)

Q7. a) A relative mode branch type of instruction is stored in memory at an address equivalent to decimal 750. The branch is made to an address equivalent to decimal 500.

i) What should be the value of the relative address field of the instruction (in decimal)?

ii) Determine the relative address value in the binary using 12 bits. (Why must the no. be in 2's complement?)

iii) Determine the binary value in PC after the fetch phase and calculate binary value of 500. (8)

b) Draw design of accumulator logic. (4.5)

Unit-IV

Q8. Write short notes of the following:

a) DMA (3)

b) A synchronous data transfer (3)

c) RS 422 standard (3)

d) UART (3.5)

END TERM EXAMINATION

FIFTH SEMESTER [B.TECH/M.TECH] DECEMBER-JANUARY 2018

Paper Code: IT 305

Time : 3 Hours

Subject: Computer Architecture

Maximum Marks : 60

Note: Attempt any five questions including Q.NO. 1 which is compulsory.
Select one question from each unit.

(4x5=20)

Q1. Answer the following:

- Perform the following decimal numbers to the bases indicated:
7652 to octal and binary
1938 to hexadecimal to binary
175 to binary
- Explain BSA direct addressing, indirect addressing, Immediate addressing and Register addressing.
- Write a program to add two 8 bit numbers using 8085 instruction set.
- Write a short note on micro coded CPU.
- An instruction is stored at location 300 with its address field at location 301. The address field has the value 400. A processor register R1 contains the number 200. Evaluate the effective address if the addressing mode of the instruction is:
 - Direct
 - Immediate
 - Relative

Unit-I

Q2. a) Register A holds the 8 bit binary 11011001. Determine the b operation and the logic microoperation to be perform in order to change the value in A to

(3)

i) 01101101

ii) 11111101

b) Explain IEEE 754 floating point standard.

(3)

c) Perform the arithmetic operation $(+42)+(-13)$ and $(+42)-(-13)$ in binary using signed 2's complement representation for negative numbers.

(4)

Q3. a) Show the block diagram of the hardware that implement the following register transfer statement:

(4)

y^t: R2 \leftarrow R1, R1 \rightarrow R2

b) Draw a diagram for 4 bit binary adder.

(4)

c) What is selective complement operation?

(2)

Unit-II

Q4. a) Draw a diagram showing basic computer registers connected to a common bus.

(7)

b) Consider a stack where SP=000000, calculate how many items are there in the stack of:

(3)

i) FULL = 1 and EMTY = 0

ii) FULL = 0 and EMTY = 1

Q5. a) Draw a flowchart for showing how an Interrupt is handled by the computer.

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- b) What is the difference between a direct and an indirect address instruction? How many references to memory are needed for each type of instruction to bring an operand into a processor register? (5)

Unit-III

- Q6. a) What is the difference between hardwired control and microprogrammed control? (2)

- b) Explain in details the instruction cycle state diagram with interrupt. (5)

- c) What is data bus, Control bus and address bus? (3)

- Q7. a) A relative mode branch type of instruction is stored in memory at an address equivalent to decimal 750. The branch is made to an address equivalent to decimal 500.

- i) What should be the value of the relative address field of the instruction (in decimal)?

- ii) Determine the relative address value in the binary using 12 bits.
(Why must the no. be in 2's complement?)

- iii) Determine the binary value in PC after the fetch phase and calculate binary value of 500. (7)

- b) Draw design of accumulator logic. (3)

Unit-IV

- Q8. Write short notes of the following: (2.5)

- a) DMA (2.5)

- b) A synchronous data transfer (2)

- c) RS 422 standard (3)

- d) UART (3)

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