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END TERM EXAMINATION

FIFTH SEMESTER [B.TECH./M.TECH.] DECEMBER 2015

Paper Code: IT303   Subject: Analog & Digital Communication

Time: 3 Hours   Maximum Marks: 60

Note: Attempt any five questions including Q no.1 which is compulsory. Internal choice is indicated.

Q1   Answer the following:-
(a) What are the basic signals? Explain. Also find the Fourier transform of unit step signal.   (4)
(b) What do you mean by modulation index? Explain how bandwidth is dependent on the modulation index in FM.   (3)
(c) What is quantization noise? Explain the different type of quantization noise in communication system.   (4)
(d) Explain the Shannon's channel capacity theorem.   (3)
(e) What is the need of modulation in communication system? Explain using examples.   (3)
(f) A signal is transmitted over a medium with bandwidth of 4 KHz. If signal power is 64 Watts and a white Gaussian noise is added to the signal in medium is of power 2Watt. Find the required capacity of the medium.   (3)

Q2   (a) Compare the different scheme AM, DSBSC and SSBSC. Explain which one is power efficient.   (5)
(b) What do you mean Auto Correlation and Cross Correlation of the signals? What is the significance of Correlation functions in communication system?(5)

                              OR

Q3   (a) Explain the various communication systems using block diagram.   (5)
(b) Draw Fourier spectrum of DSBSC and also find the power spectral density.(5)

Q4   (a) What is the difference between narrow band and wideband FM?   (5)
(b) Explain the PWM scheme. How PWM and PPM signals are generated? Explain.   (5)

                              OR

Q5   (a) Explain the sampling theorem. What is significance of Nyquist theorem at receiver in communication systems?   (5)
(b) Compare the FM and PM scheme.   (5)

Q6   (a) Explain the ADM scheme. What are the advantages of ADM over DM?   (5)
(b) What are the steps for generation of digital signal from an analog signal? Explain the advantages of encoding of the signals.   (5)

                              OR

Q7   (a) What do you mean by multiplexing? What are the advantages of multiplxing in communication system?   (5)
(b) Find the probability of error for ASK, PSK, and FSK. Also draw the constellation diagram for each.   (5)

Q8   (a) Compare the Shannon's and Huffman's coding scheme using an example. Which one is better?   (5)
(b) A DMS X has five symbols x1, x2, x3, x4, and x5 with $p(x1) = 0.4$, $p(x2) = 0.19$, $p(x3) = 0.16$, $p(x4) = 0.15$ and $p(x5) = 0.1$.   (5)
(i) Construct a Shannon Fano Code for X and calculate the efficiency of the code.
(ii) Repeat for the Huffman code and compare the results.

                              OR

Q9   (a) What is the difference between source coding and channel coding? Define entropy and rate of information.   (5)
(b) What are convolution codes? How are they different from block codes?   (5)

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END TERM EXAMINATION

FIFTH SEMESTER [B.TECH./M.TECH.] DECEMBER 2015

Paper Code: IT307 **Subject: Digital Signal Processing**

Time : 3 Hours **Maximum Marks :60**

Note: Attempt any five questions. Use of calculator is permitted.

Q1. Let $x[n]$, $y[n]$ and $w[n]$ denote three arbitrary sequences. Show that: (6+6)
 (a) Discrete convolution is commutative, i.e.,
  $x[n] * y[n] = y[n] * x[n]$
 (b) Discrete convolution is associative, i.e.,
  $x[n] * (y[n] * w[n]) = (x[n] * y[n]) * w[n]$

Q2. For each of the following systems, determine whether or not the system is (1) stable), (2) (2x6) casual, (3) linear, and (4) shift-invariant:
 (a) $y[n] = g[n] x[n]$ (d) $y[n] = x[n\text{-}n_0]$

 (b) $y[n]= \displaystyle\sum_{k=n_0}^{n} x[k]$ (e) $y[n]=e^{x[n]}$

 (c) $y[n]= \displaystyle\sum_{k=n-n_0}^{n+n_0} x[k]$ (f) $y[n] = ax[n] + b$ where $a,b > 0$

Q3 Find the z-transform of the following: (6+6)
 (a) $x[n]=a^n \sin(\omega n)u[n]$ (b) $x[n]=a^n u[n]-b^n u[-n-1]$, (a and b) <1, b>a

Q4 Determine the impulse response of the FIR filter whose impulse response is (6+6) $h[n] = \{1,-2,3\}$ and the input signal is $x[n] = \{1,-2,3,-4,5,-6,7,-8,9\}$. Use any method for calculation of the concerned DFT and then use the following method for calculation of the linear convolution:
 (a) Overlap Save (b) Overlap Add

Q5 A system is described by the difference equation (4x3) $y[n] - (3/4) y[n\text{-}1] + (1/2) y[n\text{-}2] = x[n] + (1/2) x[n\text{-}1]$
 Draw a signal flow graph to implement this system in each of the following forms:
 (a) Direct form I,
 (b) Direct for II,
 (c) Cascade and
 (d) Parallel

Q6 Design a digital lowpass Butterworth filter worth a passband magnitude characteristic that (12) is constant within 0.75 dB for a frequency below $w = 0.2613\pi$ and stopband attenuation of at least 20dB for frequencies between $w = 0.4018\pi$ and π. Use the Impulse Invariant Design Method.

Q7a Determine the DFT of the signal $x[n] = \{2,1,4,6,5,8,3,9\}$ by decimation in time FFT. (8)

Q7b What is the time complexity of the (naive) DFT algorithm, and the time complexity of the (4) radix-2 Decimation in time FFT algorithm.

Q8 Write short notes on any two of the following: (6+6)
 (a) Sampling Theorem
 (b) FIR filter design with windows
 (c) Bi-linear transformation for Filter design

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END TERM EXAMINATION

FIFTH SEMESTER [B.TECH/M.TECH] DECEMBER 2015-JANUARY 2016

Paper Code: IT-309   Subject: Object Oriented Software Engineering

Time: 3 Hours   Maximum Marks: 60

Note: Attempt any five questions including Q.no.1 which is compulsory.

Q1 Write short note on the followings (any four):   (4x5=20)
  (a) Unit testing
  (b) Entity class, interface class and control class.
  (c) Discuss the V model of testing.
  (d) Dimensions of Analysis Model.
  (e) Software measurements and software metrics.
  (f) Defects density and Defect removal.

Q2 (a) Explain spiral model of software development life cycle in detail with the help of neat diagram.   (5)
  (b) What are the drawbacks of waterfall model? How they are overcome by other SDLC models? Discuss in brief.   (5)

Q3 (a) What are the various methods for requirement elicitation? List all of them and explain any one in detail.   (5)
  (b) SRS document is created after the requirement elicitation. List various characteristics of good SRS design.   (5)

Q4 (a) What is use-case model? Why is the use-case modeling useful in analysis?   (5)
  (b) Draw a neat USE-CASE diagram for ATM cash withdrawal mechanism. Make assumptions if necessary but clearly state them. (5)

Q5 (a) Identify various types of relationship might exists between objects. How the association is different from aggregation?   (5)
  (b) What are the various standards commonly followed during software development life cycle models?   (5)

Q6 (a) Compare and contrast object-oriented analysis with the conventional approach of structured analysis during the software development process.   (5)
  (b) Make a class diagram for the student schema in University automation system. Give class representation along with attribute type and visibility classifiers.   (5)

Q7 Explain all UML diagram in brief. Take an example of Hospital Management System or University Automation System and draw UML diagrams for the case study in brief. Just make one UML diagram for each type.   (10)

Q8 (a) How the test cases are derived from Use-Case? Explain five step process in detail.   (5)
  (b) Consider a Use-Case diagram of "Login" in to the system. Generate test cases for it.   (5)

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END TERM EXAMINATION

FIFTH SEMESTER [B.TECH/M.TECH] DECEMBER 2015-JANUARY 2016

Paper Code: IT-311   Subject: Digital Design Using VHDL

Time: 3 Hours   Maximum Marks: 60

Note: Attempt any five questions including Q.no.1 which is compulsory.
Select one question from each Unit.

Q1 Explain following in brief. Use block diagram when necessary.
(a) Explain Gajski's 'Y' chart.   (5)
(b) Discuss delay in VHDL.   (5)
(c) Explain RTC.   (5)
(d) Define signal attribute to VHDL.   (5)

Unit-I

Q2 (a) Design a 3:8 Decoder using VHDL.   (4)
(b) Design a 5:32 Decoder using a macro of 2:4 and 3:8 decoder with VHDL.   (6)

Q3 (a) Design a full adder using VHDL.   (4)
(b) Design a 4-Bit Adder using a macro of full adder with Generate Statement.   (6)

Unit-II

Q4 (a) Design a behavioral model of 3-Bit asynchronous counter.   (5)
(b) Differentiate between signal and variable.   (5)

Q5 (a) Design a 4-Bit serial-in-serial-out shift Register.   (5)
(b) Design a S-R flip flop using VHDL.   (5)

Unit-III

Q6 Design a 4-Bit serial Adder using VHDL.   (10)

Q7 Explain state diagram of 4 x 4 Bit multiplier circuit.   (10)

Unit-IV

Q8 Explain design of Bus architecture using MUX.   (10)

Q7 Design a RAM using VHDL.   (10)

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END TERM EXAMINATION

FIFTH SEMESTER [B.TECH] DECEMBER 2015

Paper Code: IT-305   Subject: Computer Architecture

Time: 3 Hours   Maximum Marks: 60

Note: Attempt all questions as directed. Internal choice is indicated.

Q1 Answer the following: (10x2=20)
  (a) Represent decimal no. 6234 in (i) BCD (ii) Excess 3 code formats.
  (b) What is Microprogramming?
  (c) Compare logical shift and circular shift with the help of an example.
  (d) What is pipeline register?
  (e) What are the two instruction needed in the basic computer in order to set the E flip flop to 1?
  (f) What do you mean by Indirect Address? Explain with example.
  (g) Draw a logic circuit of XOR gate.
  (h) Describe briefly various operation of stack.
  (i) Explain IEEE 754 floating point standard.
  (j) What are memory reference instructions?

Unit-I

Q2 (a) An 8 bit register contains the binary value 10011100. What is the register value after arithmetic shift right? Starting from the initial number 10011100, determine the register value after an arithmetic shift left, and state whether there is an overflow.   (5)
  (b) Write a short note on Floating point representation with example. Represent the number $(+76.8)_{10}$ as a floating point number with 24 bits. The normalized fraction mantissa has 16 bits and exponent has 8 bits.   (5)

OR

Q3 (a) Describe bus and memory transfer with example.   (8)
  (b) Compare and contrast microperation and microinstruction.   (2)

Unit-II

Q4 (a) Describe various types of basic computer instruction formats showing their opcode combinations with example.   (6)
  (b) Explain 8085 instruction set architecture.   (4)

OR

Q5 What are interrupts? Explain different types of interrupts.   (10)

Unit-III

Q6 (a) An instruction is stored at location 300 with its address field at location 301. The address field has the value 400. A processor register R1 contains the number 200. Evaluate the effective address if the addressing mode of the instruction is: (5)
  (i) Direct
  (ii) Immediate
  (iii) Relative
  (iv) Register indirect
  (v) Index with R1 as the index register
  (b) For Microprogrammed control organization discuss the function of control address register, sequencer, pipeline and subroutine register.   (5)

OR

Q7 (a) Give an example to illustrate time and control logic for CPU instruction.   (5)
  (b) Give an example to illustrate the following: (5)
  (i) Three address instruction   (ii) RISC instruction.

Unit-IV

Q8 Write short notes on **any two**:   (5x2=10)
  (a) Virtual Memory
  (b) Asynchronous data transfer
  (c) RS 422 standard

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