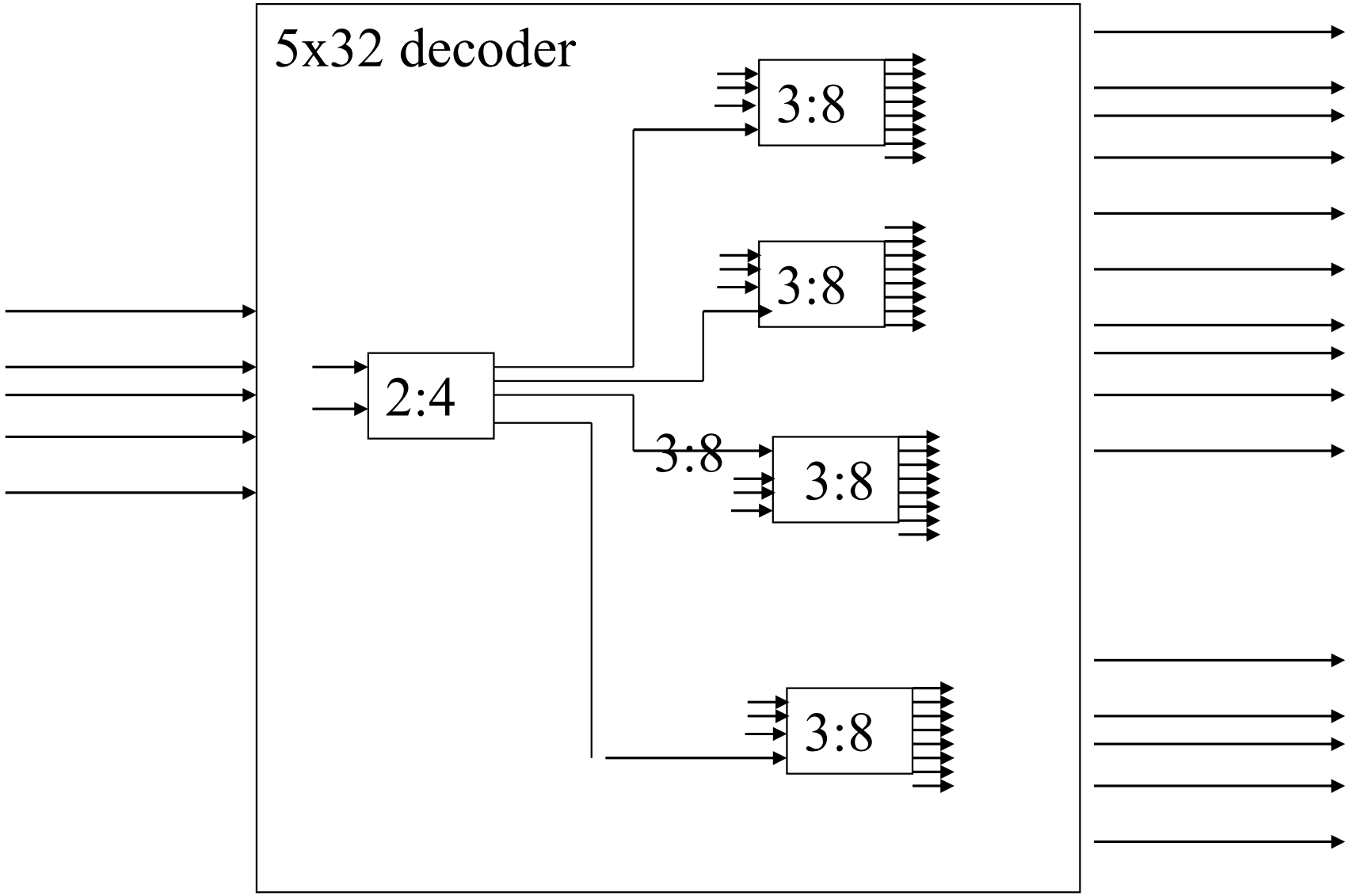
5x32 decoder
3:8
3:8
2:4
3:8
3:8
3:8

VHDL code for 2:4 Decoder

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
entity Decoder2_4 is
    Port ( x : in  STD_LOGIC_VECTOR (1 downto 0);
           y : out  STD_LOGIC_VECTOR (3 downto 0);
           en : in  STD_LOGIC);
end Decoder2_4;
architecture Behavioral of Decoder2_4 is
signal temp : std_logic_vector (3 downto 0);
begin
                    temp <=         "0001" when x = "00" else
                                            "0010" when x = "01" else
                                            "0100" when x = "10" else
                                            "1000" when x = "11";

y <= temp when en = '1' else "0000";

end Behavioral;
```

VHDL code for Decoder 3:8

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
entity decoder3_8 is
    Port ( w : in  STD_LOGIC_VECTOR (2 downto 0);
           u : out  STD_LOGIC_VECTOR (7 downto 0);
           en_3 : in  STD_LOGIC);
end decoder3_8;
architecture Behavioral of decoder3_8 is
signal temp_3 : std_logic_vector(7 downto 0);
begin
                    temp_3 <= "00000001" when w = "000" else
                     "00000010" when w = "001" else
                     "00000100" when w = "010" else
                     "00001000" when w = "011" else
                     "00010000" when w = "100" else
                     "00100000" when w = "101" else
                     "01000000" when w = "110" else
                     "10000000";
u <= temp_3 when en_3 = '1' else "00000000";
end Behavioral;
```

VHDL coder for Decoder 5:32

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
entity decoder5_32 is
    Port ( m : in  STD_LOGIC_VECTOR (4 downto 0);
           n : out  STD_LOGIC_VECTOR (31 downto 0);
           en5 : in  STD_LOGIC);
                  end decoder5_32;
architecture Behavioral of decoder5_32 is
                  component Decoder2_4 is
                                Port ( x : in  STD_LOGIC_VECTOR (1 downto 0);
                                y : out  STD_LOGIC_VECTOR (3 downto 0);
                                en : in  STD_LOGIC);
                  end component Decoder2_4;
                  component decoder3_8 is
                                  Port ( w : in  STD_LOGIC_VECTOR (2 downto 0);
                                              u : out  STD_LOGIC_VECTOR (7 downto 0);
                                                      en_3 : in  STD_LOGIC);
                  end component decoder3_8;
                  signal temp5 : std_logic_vector (3 downto 0);
```

```
begin

a2_4 : Decoder2_4 port map (x(1)=>m(4), x(0)=>m(3), y(3)=>temp5(3), y(2)=>temp5(2), y(1)=>temp5(1),
y(0)=>temp5(0),en=>en5);

a3_8_0 : decoder3_8 port map (w(2)=>m(2), w(1)=>m(1), w(0) => m(0), en_3=>temp5(0),u(7)=>n(7), u(6)=>n(6),
u(5)=>n(5), u(4)=>n(4), u(3)=>n(3), u(2)=>n(2), u(1)=>n(1), u(0)=>n(0));

a3_8_1 : decoder3_8 port map (w(2)=>m(2), w(1)=>m(1), w(0) => m(0), en_3=>temp5(1),u(7)=>n(15), u(6)=>n(14),
u(5)=>n(13), u(4)=>n(12), u(3)=>n(11), u(2)=>n(10), u(1)=>n(9), u(0)=>n(8));

a3_8_2 : decoder3_8 port map (w(2)=>m(2), w(1)=>m(1), w(0) => m(0), en_3=>temp5(2),u(7)=>n(23), u(6)=>n(22),
u(5)=>n(21), u(4)=>n(20), u(3)=>n(19), u(2)=>n(18), u(1)=>n(17), u(0)=>n(16));
a3_8_3 : decoder3_8 port map (w(2)=>m(2), w(1)=>m(1), w(0) => m(0), en_3=>temp5(3),u(7)=>n(31), u(6)=>n(30),
u(5)=>n(29), u(4)=>n(28), u(3)=>n(27), u(2)=>n(26), u(1)=>n(25), u(0)=>n(24));

end Behavioral;
```