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END TERM EXAMINATION

FIFTH SEMESTER [B.TECH] JANUARY-FEBRUARY 2023

Paper Code: IT301 ***Subject: Theory of Computation***

Time: 3 Hours ***Maximum Marks: 75***

Note: Attempt all questions Q.No.1 which is compulsory. Attempt one question from each unit.

Q1 Attempt **Any Five** questions: **[5x5=25]**

a) Show difference in the transition relation of DFA and NDFA

b) What is the key difference in between probabilistic Turing machine and Non-deterministic Turing machine

c) Whether this statement is true of false "*Some problems in NP complete can not be transformed into satisfiability problem in Polynomial time*" [Give reason also]

d) Define parsing. What is 'k' in LL(k) parsing?

e) Give a counterexample to show that context free languages are not closed under intersection

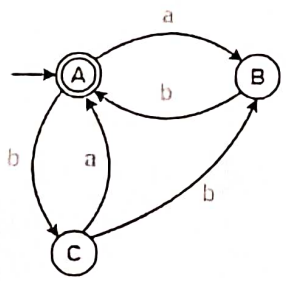
f) What is poly-time reduction?

g) What is the relation in between SPACE and NSPACE complexity classes?

h) What is an undecidable problem?

UNIT-I

Q2 Define Regular expression. Find regular expression for the following Finite Automata **[12.5]**



Q3 Show that regular languages are closed under complementation. Suppose L1 is the collection of binary strings with an even number of 0's, and L2 the collection of binary strings with an even number of 1's. Design a finite automata to recognise the language L1 – L2. **[12.5]**

UNIT-II

Q4 Explain pumping lemma for the context free languages. Let L be the language $\{ a^i b^j c^k \mid 0 \le i \le j \le k \}$.. Show that this language is not a CFL. **[12.5]**

P.T.O.

IT301

P 1/2

Q5 Define deterministic and non-deterministic pushdown automata. Construct PDA for the given CFG, and test whether **010^4** is acceptable by this PDA.
Given grammar: **$S \rightarrow 0BB$; $B \rightarrow 0S \mid 1S \mid 0$** **[12.5]**

UNIT-III

Q6 Define Church-Turing Thesis. Explain any two variants of Turing Machine through examples. **[12.5]**

Q7 Define Recursively enumerable and recursive languages. Prove that Halting problem is undecidable. **[12.5]**

UNIT-IV

Q8 Define key ingredients of an interactive proof system. A graph G is 3-colorable if the vertices of a given graph can be colored with only three colors, such that no two vertices of the same color are connected by an edge. Develop an IPS protocol to show that the given graph is 3-colorable. **[12.5]**

Q9 Define Oracle Turing Machine. What could be the benefit of relativized computation. Check whether followings are **True or False** **[12.5]**
(I) NP $\subseteq$ P^{NP}
(ii) $P^{NP} \subseteq P^{SAT}$

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END TERM EXAMINATION

FIFTH SEMESTER [B.TECH.] JANUARY-FEBRUARY 2023

Paper Code: IT303 ***Subject: Analog and Digital Communication***

Time: 3 Hours ***Maximum Marks: 75***

Note: Attempt five questions in all including Q.No.1 which is compulsory.

Q.1 (a) What is the need for Modulation? **(3)**

(b) With a block diagram, explain electrical communication system. **(3)**

(c) Find the Fourier transform of an impulse signal $x(t) = \delta(t)$ **(3)**

(d) Discuss QAM. **(3)**

(e) Explain the terms **(3)**

(i) S/N ratio

(ii) Noise temperature

(iii) Noise figure

Q.2 (i) Explain the following **(any two)** **(3x2=6)**

(a) Power Spectral Density

(b) Auto Correlation

(c) Convolution

(ii) Explain with the help of block diagram generation and demodulation of AM. **(9)**

Q.3 Explain Sampling Theorem. Find the Nyquist rate and the Nyquist interval for the following signal. **(15)**

$m(t) = 5 \cos 1000\pi t \cos 4000\pi t$

Q.4 Explain **(any two)** **(15)**

(a) Frequency and Phase Modulation

(b) Narrowband and Wideband FM

(c) PAM, PWM & PPM

(d) Multiplexing

Q.5 Give the differences between Coherent and Non-Coherent detection techniques? Explain ASK, FSK, PSK. **(15)**

P.T.O.

Q.6 With block diagram explain PCM. The output signal-to-quantizing noise ratio $(SNR)_0$ in a PCM system is defined as the ratio of average signal power to average quantizing noise power. For a full scale sinusoidal modulating signal with amplitude A, Show that

$$(SNR)_0 = \left(\frac{S}{Nq}\right)_0 = \frac{3}{2} L^2$$

where L is the number of quantizing levels.

Q.7 (a) What are error detection and correction code? **(7)**

(b) Explain Block Codes and Convolution Codes. **(8)**

Q.8 Explain the significance of **(15)**

(i) Rate of Information
(ii) Entropy
(iii) Coding Efficiency

Q.9 (i) Using a suitable example compare Shannon Fano and Huffman Coding. **(9)**

(ii) Consider a telegraph source having two symbols, dot and dash. The dot duration is 0.28. The dash duration is 3 times the dot duration. The probability of the dot's occurring is twice that of the dash and the time between symbols is 0.28. calculate the information rate of the telegraph source. **(6)**

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END TERM EXAMINATION

FIFTH SEMESTER [B.TECH] JANUARY-FEBRUARY 2023

Paper Code: IT-307 **Subject: DIGITAL SIGNAL PROCESSING**

Time: 3 Hours **Maximum Marks: 75**

Note: Attempt five questions in all including Q.No. 1 which is compulsory.

Q.1 Attempt **any five** **(5x5=25)**

(a) Find the Fourier Coefficient of the signal $f(t) = \sin \omega_0 t$

(b) Verify following system for Linearity and Time Invariance:

i) $y(t) = x^2(t)$, ii) $y(t) = \sin t.x(t)$, iii) $y(t) = x(at)$, and iV) $y(t) = \log x(t)$

(c) What is the difference between Causal System or Non-Causal System.

(d) Prove that discrete time harmonics are not always periodic in frequency.

(e) Find the Fourier Coefficient of the signal which is full wave rectifier signal.

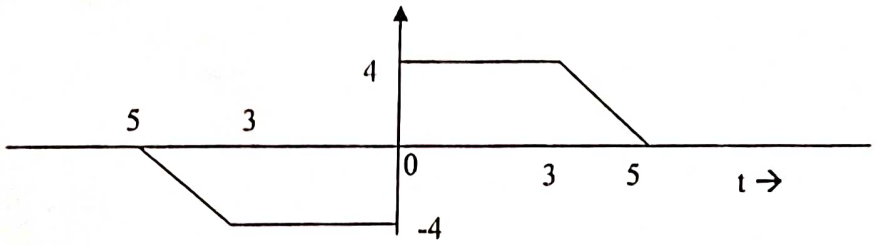
(f) Write a short note on filter bank.

(g) Compare IIR and FIR.

(h) Explain the need of low pass filter with a decimator and mathematically prove that $\omega_x = \omega_y D$

(i) Short note on Frequency Sampling realization FIR filters.

Q2. (a) Signal f(t) is defined as below:- **(6+6.5=12.5)**

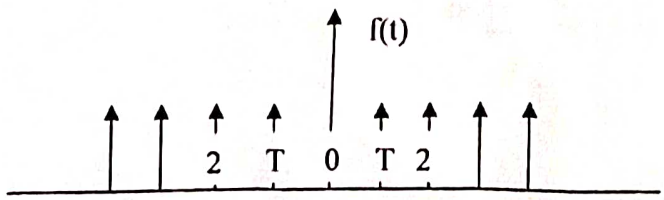


A signal g(t) is realized by multiplying f(t) with $\partial(t+4)+\partial(t-4)$ is the integral of the signal or power signal. Hence find the Energy or Power.

(b) Find the response of discrete time LTI system having the input and impulse responses as given below $f[n] = a^n u[n]$, $h[n] = a^n u[n]$.

Q3. (a) Derive the relationship between Trigonometric Fourier Series and Exponential Fourier Series.

(b) Draw the Complex Spectrum of the given below and also find the Fourier series



(6+6.5=12.5)

Q4. (a) Find the Fourier Transform of the signal **(i)** $f(t)=\frac{1}{\pi t}$, **(ii)** $f(t)=t\left(\frac{\sin t}{\pi t}\right)^2$

(b) Find the number of complex additions and complex multiplications required to find DFT for 16 point signal. Compare them with number of computations required, If FFT algorithm is used. **(6+6.5=12.5)**

Q5. (a) Compute DFT of a sequence, $x(n)=\{1,2,2,2,1,0,0,0\}$ using DIF-FFT algorithm. Sketch its magnitude spectrum.

(b) Find 8-point FFT of , $x(n)=\{1,2,2,2,1\}$ using signal flow graph of Radix-2 Decimation in frequency FFT. **(6+6.5=12.5)**

Q6. Derive the Expression for impulse invariance technique for obtaining transfer function of digital filter from analog filter. Derive the necessary equation for relationship between frequency of analog and digital filter. **(12.5)**

Q7. Compare various windows used for designing FIR filters. **(12.5)**

Q8. Perform the filter realizations using direct form I and direct form II for the following tranfer function. **(12.5)**

$H(Z)=0.5(1-Z^{-2})/(1+1.3Z^{-1}+0.3Z^{-2})$.

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END TERM EXAMINATION

FIFTH SEMESTER [B.TECH] JANUARY-FEBRUARY 2023

Paper Code: IT-309 **Subject: Object Oriented Software Engineering**

Time: 3 Hours **Maximum Marks: 75**

Note: Attempt five questions in all including Q.No.1 which is compulsory. Select one question from each unit.

Q1. (a) Discuss types of mutation testing. What is mutation score? **(5)**
(b) Explain the four main components of the State Transition Model. **(5)**
(c) Discuss the steps for developing a statechart from a use case. **(5)**
(d) What are control classes? List their properties. **(5)**
(e) What is a use case? Discuss four objects of use case diagram. **(5)**

UNIT-I

Q2. Explain the waterfall model. Discuss its advantages and disadvantages. **(12.5)**

Q3. What is software requirement? Discuss any three types of requirements elicitation techniques. **(12.5)**

UNIT-II

Q4. Explain dimensions, objects used in Analysis model. Discuss, how the requirement model is structured in analysis model. **(12.5)**

Q5. Discuss the essential elements of a class diagram. **(12.5)**

UNIT-III

Q6. Explain steps in the design stage. List design model contents. Discuss components of sequence diagram. Draw sequence diagram for cash withdrawl from an ATM machine. **(12.5)**

Q7. What are activity diagrams used for? Drawing activity diagrams explain how decisions and concurrent activities are depicted. Using an E-commerce site list the steps for purchase of an item on the internet and draw activity diagram for the same. **(12.5)**

UNIT-IV

Q8. For 'Login' use case make (i) Basic and Alternate flows (ii) use case scenario matrix (iii) identification of variables (iv) test case matrix with actual data values. **(12.5)**

Q9. What is mutation testing? Explain the steps to execute mutation testing. Discuss the techniques to create the mutant program. What are advantages and disadvantages of mutation testing? **(12.5)**

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END TERM EXAMINATION

FIFTH SEMESTER [B.TECH] FEBRUARY 2023

Paper Code: IT-311 ***Subject: Digital Design using VHDL***

Time: 3 Hours ***Maximum Marks: 75***

Note: Attempt any five questions in all including Q. No.1 which is compulsory. Internal choice is indicated.

(25)

Q1 Attempt **all** questions:-

(a) Define HDL.

(b) Differentiate between Structural and Behavioural modelling.

(c) Explain Synthesizer and Compiler.

(d) Define FPGA and CPLD.

(e) Explain Delta and inertial delay.

Q2 Design 4-bit adder using a macro of half adder and full adder. **(12.5)**

OR

Q3 Design and 5:32 Decoder using a component of 2:4 and 3:8 Decoder. **(12.5)**

Q4 (a) Explain Attributes. **(6)**

(b) Design 3-bit binary asynchronous counter. **(6.5)**

OR

Q5 (a) Design an universal shift register using VHDL. **(6)**

(b) Explain the bus structure implemented using Mux. **(6.5)**

Q6 Explain a design of serial adder using State machine. **(12.5)**

OR

Q7 Explain RTL for state machine design. **(12.5)**

Q8 Design a shift-and-add multiplier using state machine. **(12.5)**

OR

Q9 Design 8-bit SRAM using VHDL. **(12.5)**

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END TERM EXAMINATION

FIFTH SEMESTER [B.TECH (IT)] FEBRUARY 2023

Paper Code: IT-305 **Subject: Computer Architecture**

Time: 3 Hours **Maximum Marks: 75**

Note: Attempt five questions in all including Q. No.1 which is compulsory.

Q1 Give the answer of the following questions:- **(5x5=25)**

(a) What are signed and unsigned binary notations?

(b) What are different instruction code formats?

(c) What are hardwired & micro programmed control unit?

(d) What is virtual memory? Explain

(e) What is interrupt? Explain mask and unmask interrupt.

Q2 What is instruction cycle? Draw a flowchart for instruction cycle of a basic Computer and explain it. **(12.5)**

Q3 (a) Explain the IEEE 754 floating point standard with example. **(6)**

(b) What different types of addressing mode? Explain. **(6.5)**

Q4 What is arithmetic micro-operation? Draw a logic circuit of arithmetic micro- operations and its function table. **(12.5)**

Q5 What are different types of CPU organization? Explain the Stack organization CPU in details. **(12.5)**

Q6 What is an associative memory? Explain the hardware organization of associative memory. **(12.5)**

Q7 What is asynchronous data transfer? Explain strobe and handshaking method of asynchronous data transfer. **(12.5)**

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