

Half Adder and Full Adder

<https://www.androiderode.com/vhdl-code-for-half-adder-and-full-adder-and-simulate-the-code/>

Half and Full Subtractor

<https://www.androiderode.com/half-subtractor-and-full-subtractor-vhdl-simulation-code/>

4 Bit Multiplexer

<https://allaboutfpga.com/vhdl-4-to-1-mux-multiplexer/>

Serial Adder with Accumulator

Page No. 151

BCD to 7 Segment Decoder

<https://allaboutfpga.com/bcd-to-7-segment-decoder-vhdl-code/>

D Flip Flop

<https://www.engineersgarage.com/vhdl-tutorial-16-design-a-d-flip-flop-using-vhdl/>

Synchronous Counter

<https://technobyte.org/vhdl-code-synchronous-upcounter-behavioral/>

4 Bit PIPO Shift Register

<https://allaboutfpga.com/vhdl-code-for-4-bit-shift-register/>

4 Bit ALU

<https://allaboutfpga.com/vhdl-code-for-4-bit-alu/>

4 Bit Carry Look Ahead Adder

<https://allaboutfpga.com/carry-look-ahead-adder-vhdl-code/>

32 Bit Adder

<http://vhsichdl.blogspot.com/2015/04/vhdl-code-to-add-two-32-bit-numbers.html>

4X4 Binary Multiplier

https://en.wikibooks.org/wiki/VHDL_for_FPGA_Design/4-Bit_Multiplier

4 Bit Adder Using Full Adder

<https://allaboutfpga.com/4-bit-ripple-carry-adder-vhdl-code/#:~:text=The%20Main%20operation%20of%20Ripple,Port%20Mapping%204%20Full%20Adder>

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All Flip Flops

<https://allaboutfpga.com/vhdl-code-flipflop-d-t-jk-sr/>

Universal Shift Register

<https://www.electronics-tutorial.net/VHDL/Shift-Registers/Universal-shift-register/>

3:8 Decoder

<https://www.engineersgarage.com/vhdl-tutorial-13-design-3x8-decoder-and-8x3-encoder-using-vhdl/>

2:4 Decoder

<https://allaboutfpga.com/vhdl-code-for-2-to-4-decoder/>

4 Bit Serial Adder

<https://www.isabekov.pro/four-bit-serial-adder-subtractor/>

8:1 Multiplexer

Similar to 4:1 Multiplexer

3 Bit Asynchronous Counter

<https://www.ques10.com/p/32994/write-vhdl-code-for-3-bit-up-counter/>

4 Bit Serial In Serial Out Shift Register

<https://vhdbynaresh.blogspot.com/2013/07/design-of-4-bit-serial-in-serial-out.html>