

Basic Computer Organization and Design

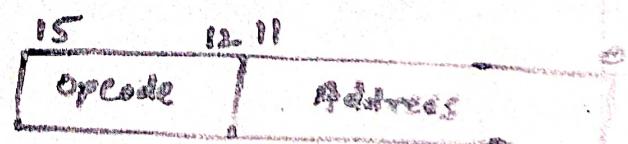
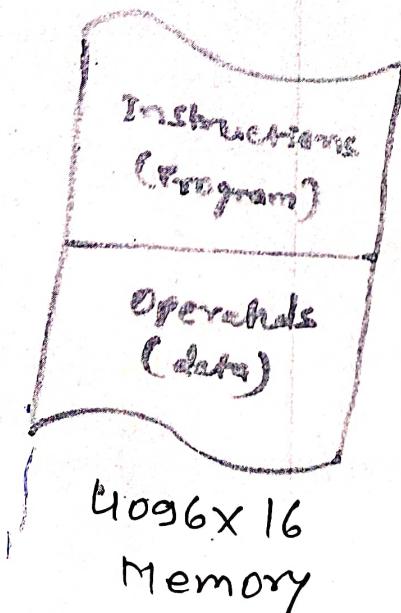
- The organization of the computer is defined by its:
 - internal registers
 - the timing and control structure
 - and the set of instructions.

Instruction code:- An instruction code is a group of bits that instruct the computer to perform a specific operation.

Stored Program Organization:- A simple computer have one processor register and an instruction code formed with two parts.

I	Opcode Address	II part
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- The memory address find an operand in memory.
- The instructions are stored in one section of memory and data in another.



Instruction format

$$2^{12} = 4096$$

$2^4 = 16 \rightarrow$ Possible operations



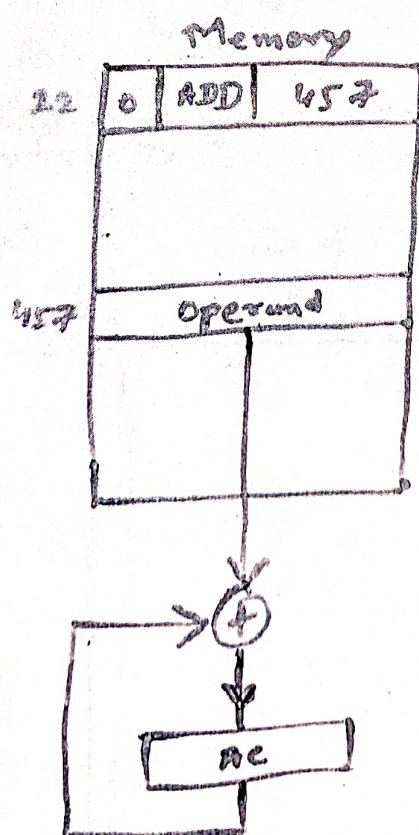
Accumulator (AC):- Accumulator is a processor register.

The operation is performed with the memory operand and the content of AC

e.g. ADD B means $\rightarrow AC \leftarrow AC + B$

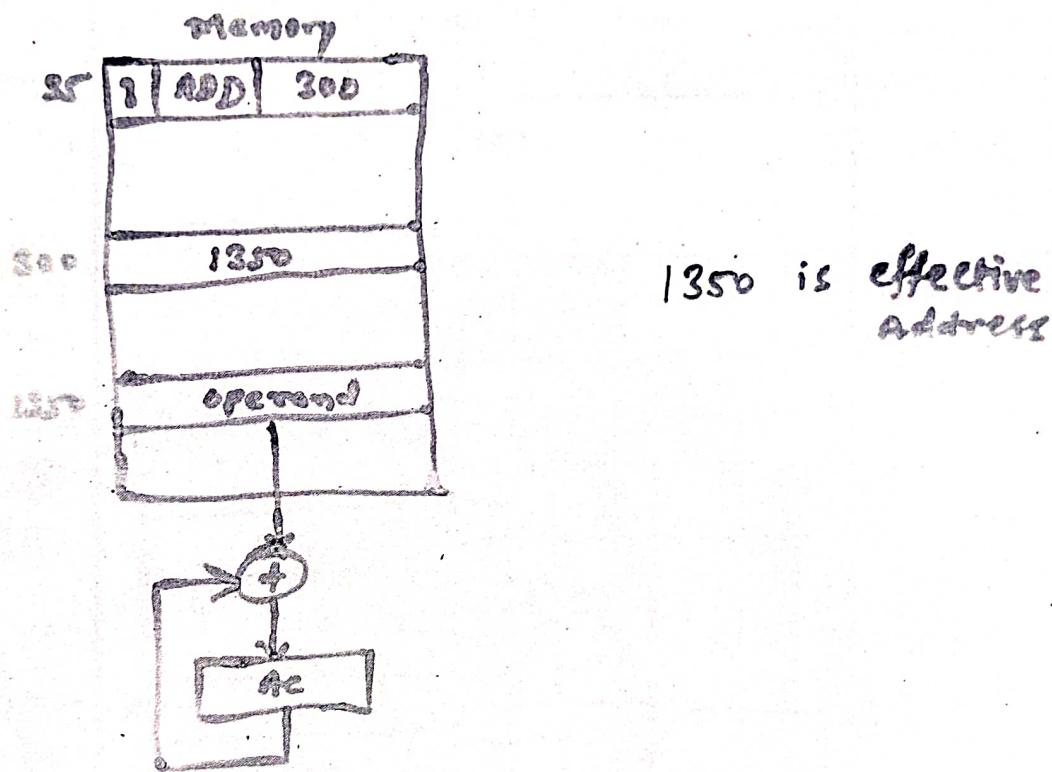
Immediate instruction:- When the second part of an instruction code specifies an operand, the instruction is said to have an immediate operand.

Direct Address:- When the second part of an instruction code specifies the address of an operand, the instruction is said to have a direct address.



if $I=0$ Direct address
 $I=1$ Indirect address

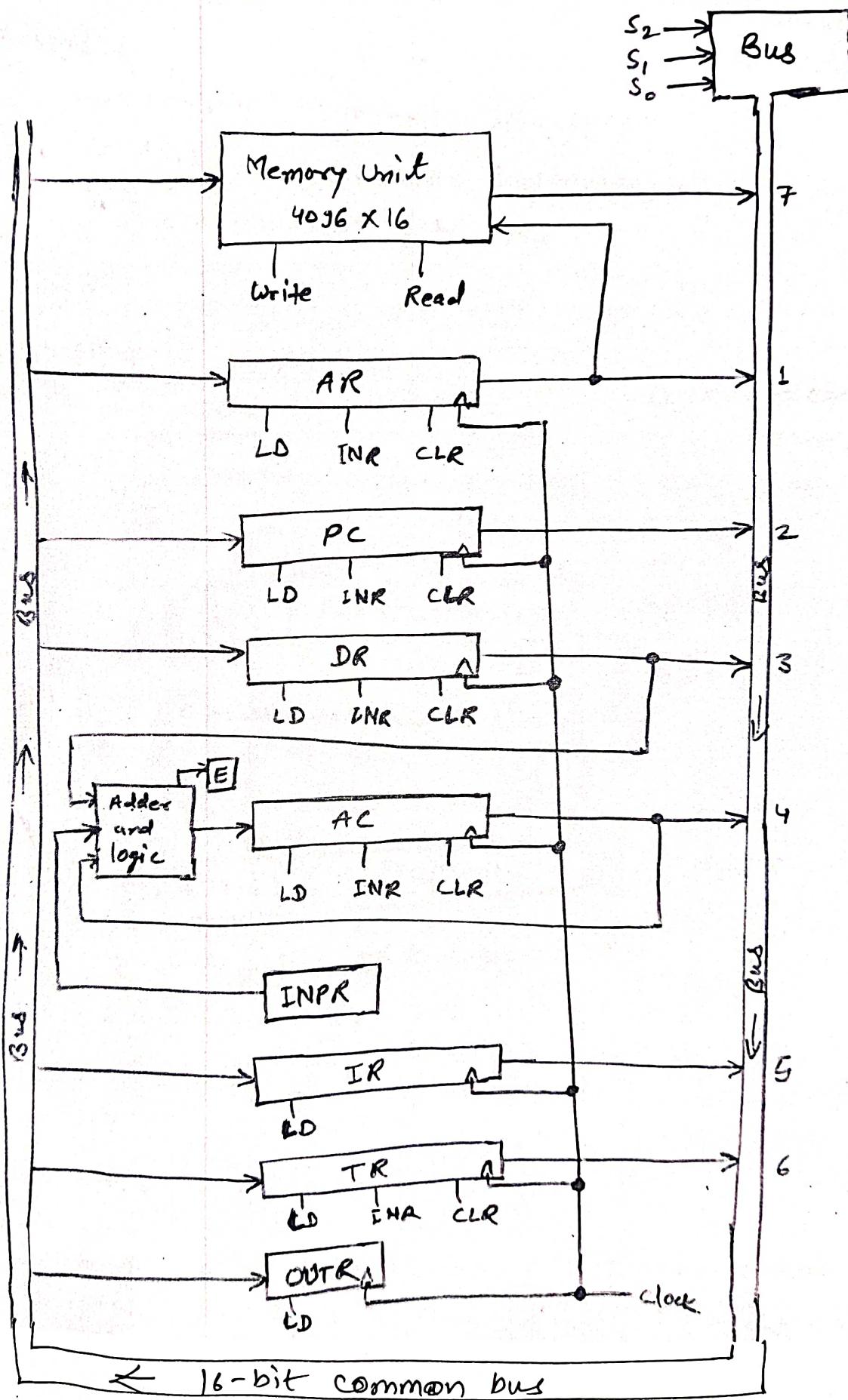
Indirect Address:- when the bits in the second part of the instruction designate an address of a memory word in which the address of the operand is found.



Computer Registers (for basic computer)

Register symbol	No. of bits	Register name
DR	16	Data Register
AR	12	Address Register
AC	16	Accumulator
IR	16	Instruction Register
PC	16	Program Counter
TR	16	Temporary Reg.
INPR	≈ 8	Input Reg.
OUTR	8	Output Reg.

Basic Computer registers connected to common bus.



Computer Instructions

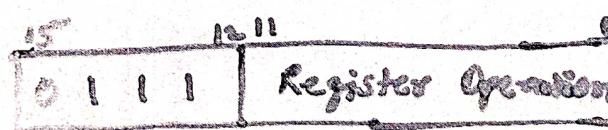
The basic computer has three instruction code formats:

- Memory-reference instruction
- Register-reference instruction
- Input-output instruction



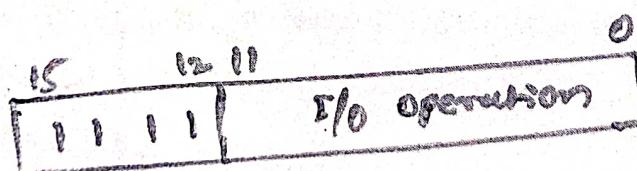
Memory-reference Ins.

Opcode = 000 to 110
 $I=0$ (direct addr)
 $I=1$ (indirect addr)



Register-reference Ins.

Opcode = 111, $I=0$



Input-output instruction

Opcode = 111, $I=1$

Instructions

AND - AND memory word to AC

ADD - add memory word to AC

LDA - Load memory word to AC

STA - Store content of AC in memory

BUN - Branch Unconditionally

B&R - Branch and save return address

ISZ - Increment and skip if zero

CLA - Clear AC

CLG - Clear E

CMA - Complement AC

CIR - Circulate right AC

CLR - Circulate left AC

INC - Increment AC

SPI - skip next instruction if AC positive

SPIA - " " " negative

SZP - skip next instruction if AC zero

HLT - Halt computer

INP - Input character to AC

OUT - Output character from AC

SKI - Skip on input flag

SKO - skip on output flag

ION - Interrupt on

IOF - Interrupt off

Timing and Control

The timing for all registers in the basic computer is controlled by a Master clock generator. The clock pulses are applied to all flip-flops and registers in the system. The control signals are generated in the control unit and provide control inputs for the multiplexers in the common bus, control inputs in processor register, and microoperations for the accumulator.

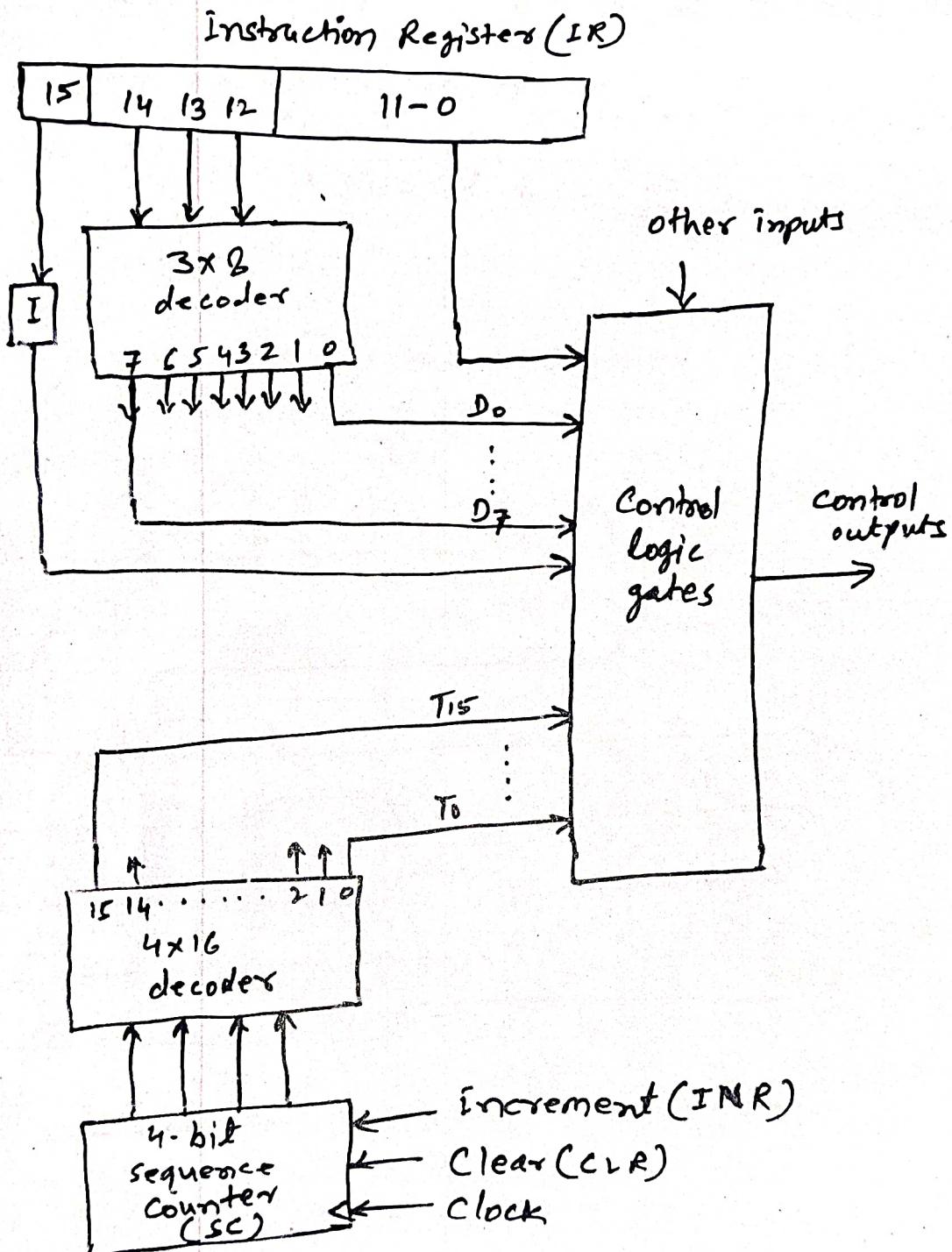
There are two major types of control organization:

- hardwired control
- microprogrammed control

Hardwired control: The control logic is implemented with gates, flip-flops, decoders, and other digital Circuits.

Microprogrammed control: The control information is stored in a control memory. The control memory is programmed to initiate the required sequence of microoperations.

Control Unit:



(control unit of Basic Computer)

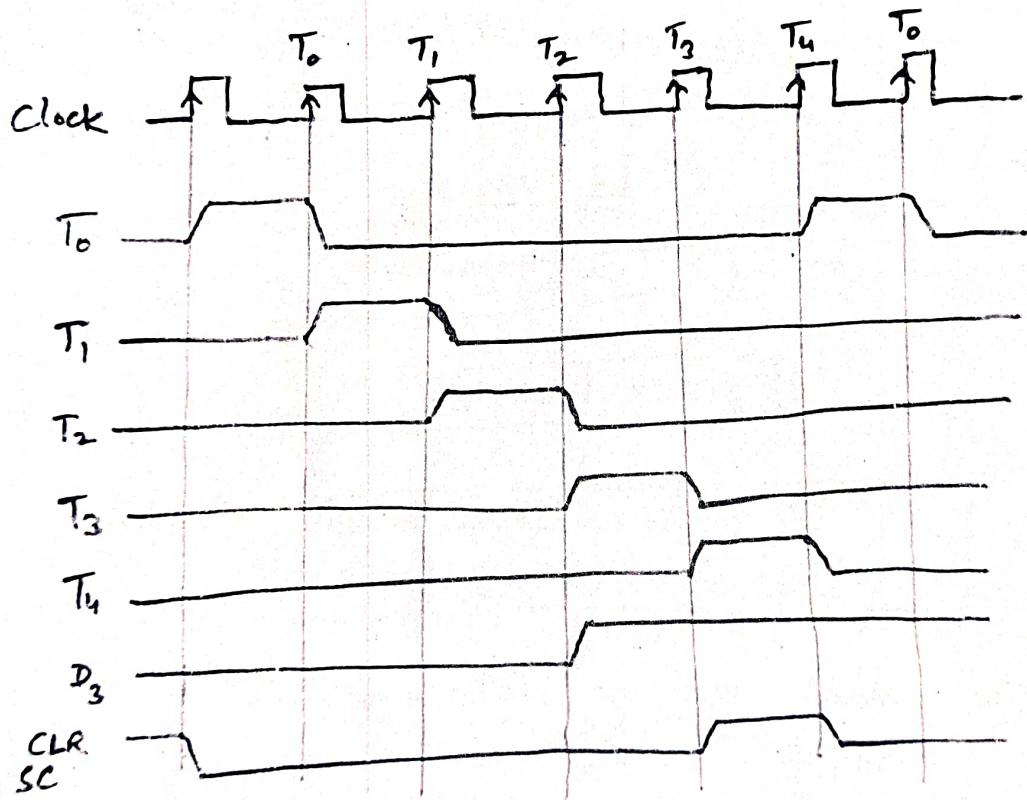
Control timing signals

Example: Consider the case where SC is incremented

→ provide timing signals T_0, T_1, T_2, T_3 , and T_4 in sequence.

At time T_4 , SC is cleared to 0 if decoder output D_3 is active, i.e.

$$D_3 T_4 : SC \leftarrow 0$$

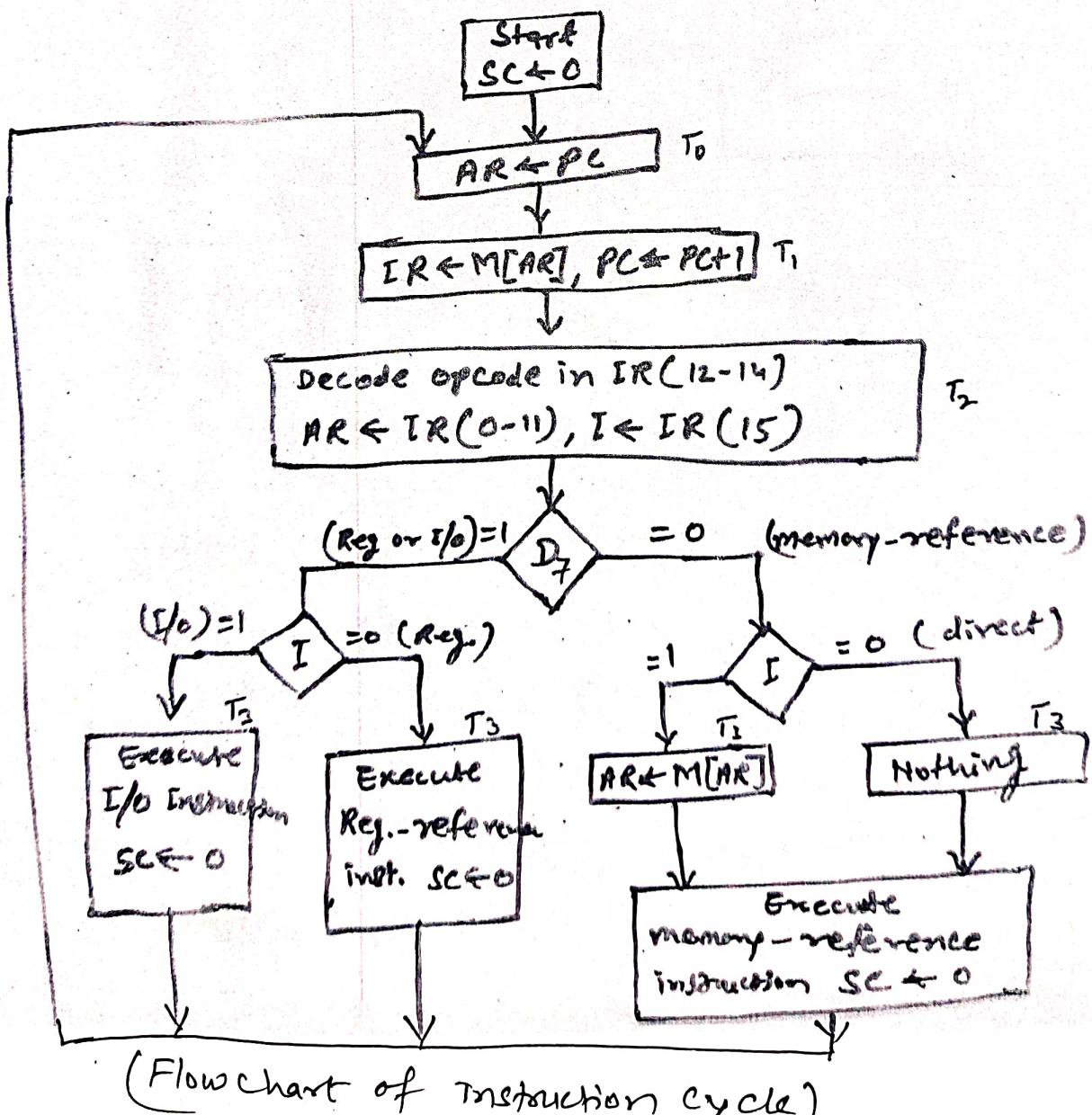


The SC is cleared when $D_3 T_4 = 1$. Output D_3 from the operation decoder becomes active at the end of timing signal T_2 . When T_4 becomes active, the output of the AND gate ($D_3 T_4$) becomes active, and signal applied to the CLR input of SC.

Instruction Cycle

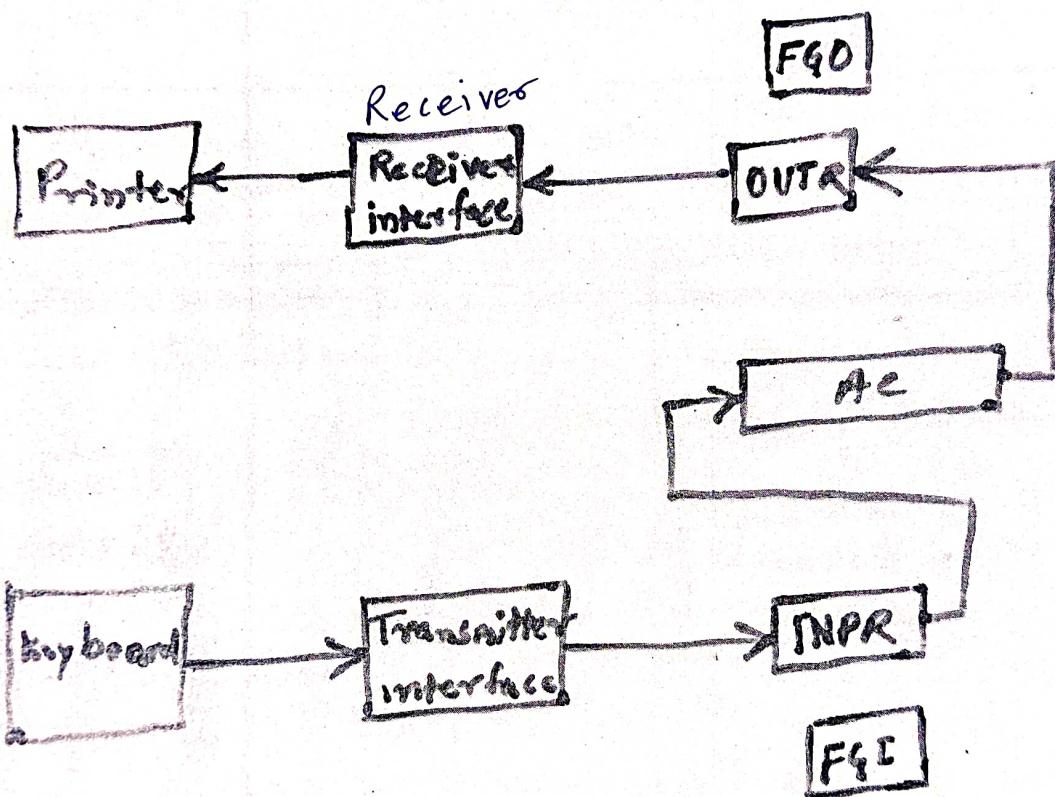
A Computer ~~consisting~~ in the memory unit of the computer consists of a sequence of instructions. The program is executed in the computer by going through a cycle for each instruction.

1. Fetch an instruction from memory
2. Decode the instruction.
3. Read the effective address from memory
4. Execute the instruction (Fetch operand)



Input-Output Configuration

The terminal sends and receives serial info. Each quantity of information has eight bits of an alphanumeric code.



Where:

INPR - Input Register

OUTR - Output Register

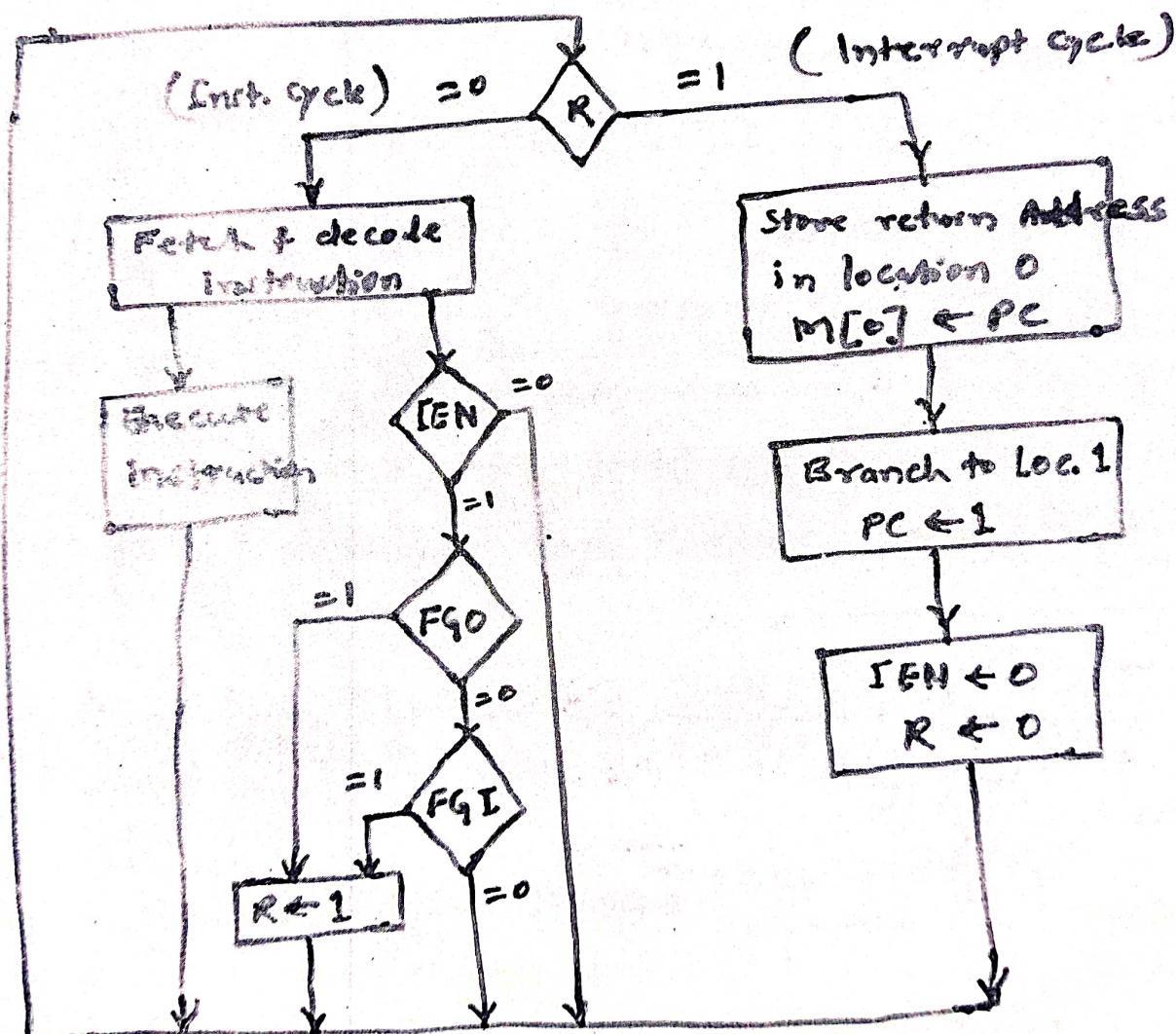
AC - Accumulator

FGI - Input Flag (initial value is 0)

FGO - Output flag (initial value is 1)

Interrupt:

The external device informs the computer when it is ready for the transfer. In the meantime the computer can be busy with other ~~task~~ tasks. This type of transfer uses the interrupt facility.



(Flowchart for interrupt cycle)

where

[EN] - interrupt enable flip-flop

R - interrupt flip-flop

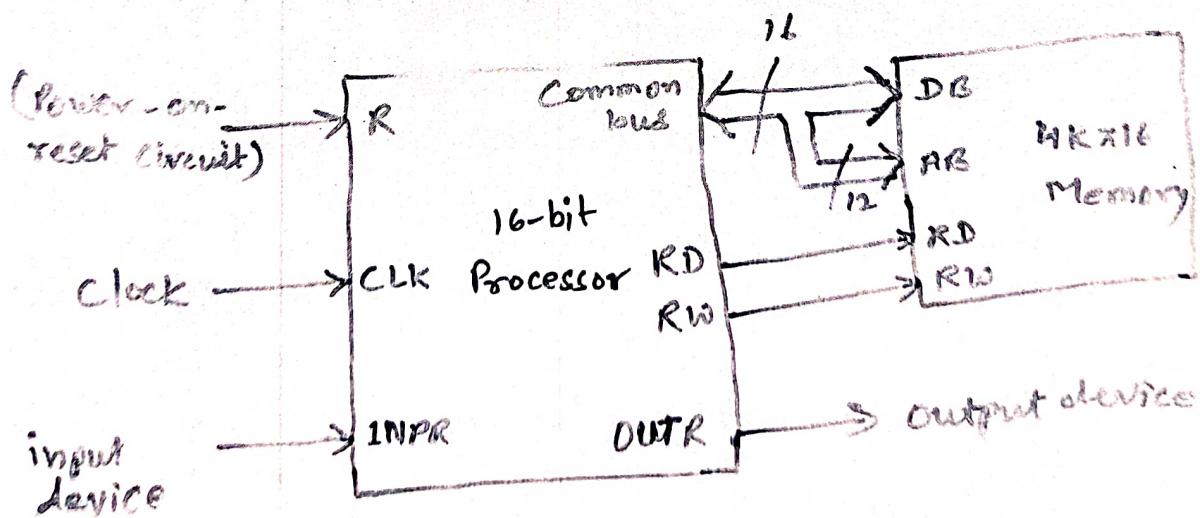
FGI - Input flag.

FGO - Output flag.

Design of Basic Computer

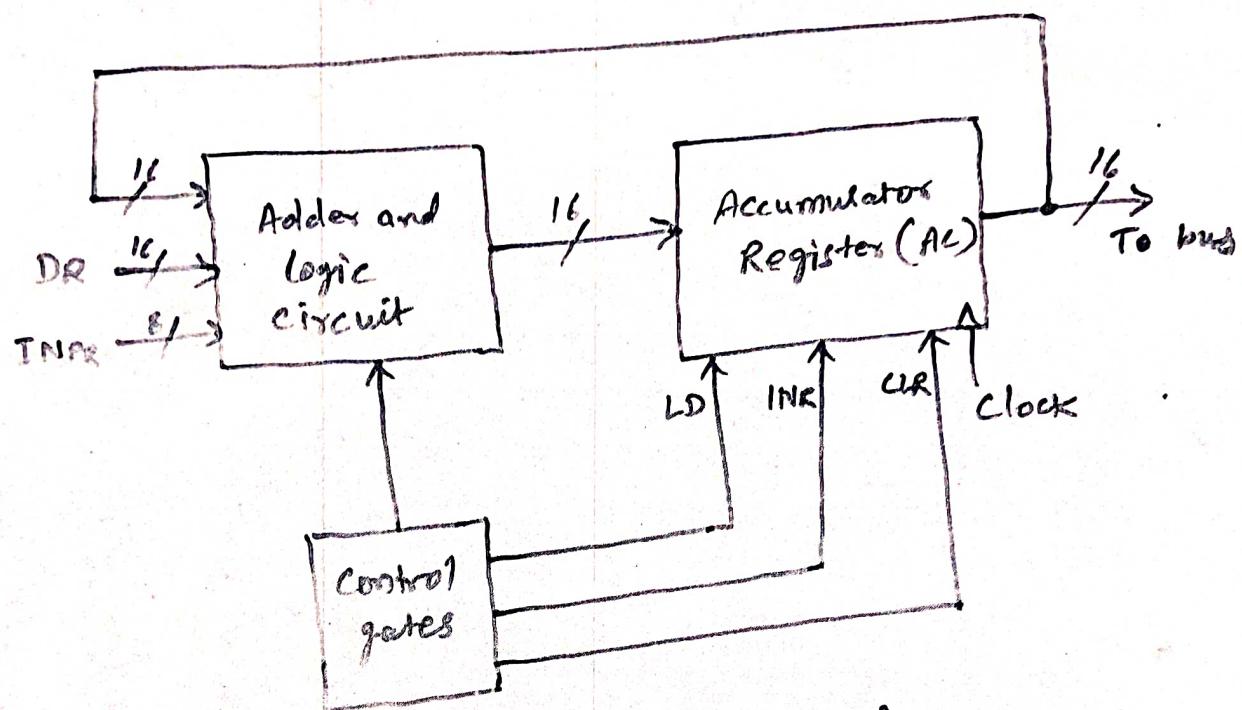
The basic computer consists of the following hardware components:

1. A memory unit with 4096 words of 16 bits each.
2. Nine registers: AR, PC, DR, AC, IR, TR, OUTR, INPR, and SC.
3. Seven flip-flops: I, S, E, R, IEN, FGE, and FGO
4. Two decoders: 3×8 operation decoder and a 4×16 timing decoder
5. A 16-bit common bus
6. Control logic gates
7. Adder and logic circuit connected to the input of AC



(Block diagram of Basic comp.)

Design of Accumulator Logic



(circuit associated with AC)