(Please write your Exam Roll No.) Exam Roll No. .....

END TERM EXAMINATION

FIFTH SEMESTER [B.TECH] DECEMBER 2016 – JANUARY 2017

Paper Code: IT-301 **Subject: Theory of Computation**

Time: 3 Hours **Maximum Marks: 60**

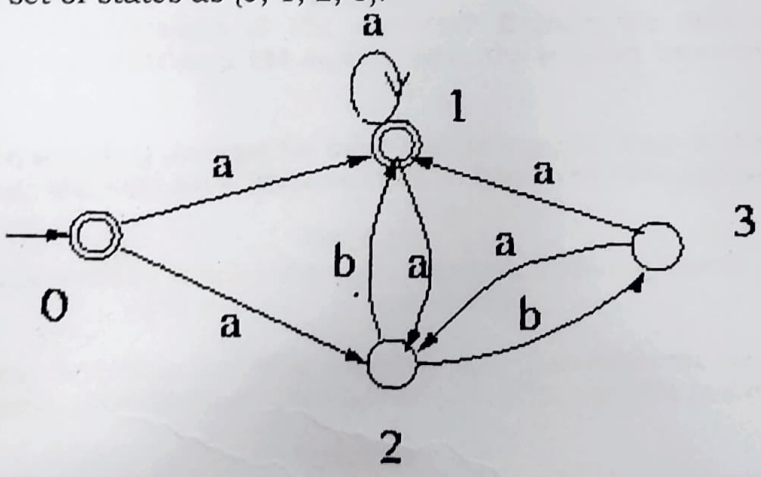
Note: Attempt any five questions including Q.no.1 which is compulsory. Select one question from each Unit.

Q1 (a) Write formal statement of kleen's theorem. **(2.5x8=20)**
(b) Define pumping lemma for context free language?
(c) Define Chomsky normal form of a CFG?
(d) What is LL(2) grammar? How is it different from LL(1).
(e) What is halting problem?
(f) Define Oracle turing Machine.
(g) What is time hierarchy theorem?
(h) Define probabilistic computation and BPP complexity class.

Unit-I

Q2 (a) State Pumping property followed by a regular language and prove that $L = \{a^n b^{2n} \mid n>=1\}$ is non-regular. **(5)**
(b) Prove by construction that regular languages are closed under intersection. **(5)**

Q3 (a) Prove or Disprove the validity of the following statement "Every NDFA (Non-deterministic Finite Automata) can be converted into DFA (deterministic Finite Automata) by increasing the number of states". **(5)**
(b) Find the equivalent regular expression of following Finite Automata with set of states as {0, 1, 2, 3}: **(5)**



Unit-II

Q4 (a) Show that context free languages are closed under union and concatenation. **(5)**
(b) Prove that intersection of regular and context free language will always be context free. **(5)**

Q5 (a) Design a Pushdown Automata to recognize language $L = \{a^n b^{2n} \mid n>=1\}$. **(5)**
(b) Describe the mechanism to find equivalent CFG of a given PDA. **(5)**

P.T.O.

IT-301
P1/2
57/

Unit-III

Q6 How can we combine different Turing machines. Design a Turing Machine to recognize a language L = {SS | S $\in$ {a, b} * }. **(10)**

Q7 Discuss any two variant of the standard Turing machine. Design a Turing Machine to Compute F(n) = 1 + 2 + ... + n (represent n in unary) i.e F(3) = 6. **(10)**

Unit-IV

Q8 Write your comment on the implications of knowing an exact relationship that is "equality" or "Non-equality" in between P and NP complexity classes. Briefly outline the proof of Cook's Theorem. **(10)**

Q9 Define SPCAE and NSPCAE Complexity classes. Prove that PSPCAE is equivalent to NPSPACE. **(10)**

****

(Please write your Exam Roll No.) Exam Roll No. .....

END TERM EXAMINATION

FIFTH SEMESTER [B.TECH./M.TECH.] DECEMBER 2016

Paper Code: IT-303 **Subject: Analog and Digital Communication**

Time: 3 Hours **Maximum Marks: 60**

Note: Attempts any five questions including Q no.1 which is compulsory. Select one question from each unit.

Q1 (a) What is difference between time – division multiplexing. (TDM) and Frequency division multiplexing (FDM). **(4)**

(b) Give the advantages of digital communication. List some practical applications of such communication. **(4)**

(c) Explain the terms: **(4)**
(i) Noise temperature (T_e)
(ii) Noise figure (F)
(iii) S/N ratio (SNR)

(d) What is the need of representation of any signal in terms of Fourier transform in communication? Give typical examples. **(4)**

(e) What is the effect of Quantization in digital communication? What is meant by base-band digital signal? **(4)**

UNIT-I

Q2 Using block/functional diagram, explain a typical method of generation and demodulation of AM-DSB/SC signal. **(10)**

Q3 A signal is given by **(10)**
$X(t) = A \cos\omega_c t$
Find (i) auto – correlation function (ACF)
(ii) power spectral density (PSD)
(iii) power contained in the signal

UNIT-II

Q4 What are the advantages of FM over AM? Explain the difference between narrowband and wideband FM signals. Give the relation between FM and PM signals. **(10)**

Q5 Explain the sampling theorem for band-limited signals. What is the Nyquist rate of sampling? List important features of PAM, PWM and PPM signals. **(10)**

UNIT-III

Q6 Compare the features of following digital communication systems: **(10)**
(i) PCM (ii) DM (iii) ADPCM

Q7 Explain the difference between coherent and non-coherent demodulation of digital signals. Give the basic principle of ASK, FSK and PSK systems. **(10)**

UNIT-IV

Q8 What are various error detection and correction codes? Using typical examples, explain the application of block codes and convolution codes. **(10)**

Q9 Explain the significance of:- **(10)**
(a) Rate of information
(b) Entropy
(c) Coding efficiency.
Using typical examples, explain the difference between Shannon-Fano and Huffman coding.

****

P 572

(Please write your Exam Roll No.) Exam Roll No. .....

END TERM EXAMINATION

FIFTH SEMESTER [B.TECH./M.TECH.] DECEMBER 2016

Paper Code: IT-305 **Subject: Computer Architecture**

Time: 3 Hours **Maximum Marks: 60**

Note: Attempts any five questions including Q no.1 which is compulsory. Select one question from each unit.

Q1 Answer the following:- **(10x2=20)**

(a) Calculate the sum of $(-28)_{10}$ and $(52)_{10}$ using 2's complement.
(b) Write 4040000016 in IEEE 32 BIT FORMAT.
(c) What are the reasons for using Virtual Memory?
(d) How many cycles a serial adder needs to add two n bit number?
(e) What are the two instructions needed in the basic computer in order to set the E flip flop to 1?
(f) What do you mean by direct Address? Explain with example.
(g) What is a micro instruction?
(h) Describe briefly various operations of stack.
(i) What do you mean by the instruction R2← R1? Explain type of instruction.
(j) What are the disadvantages of memory mapped Processor.

UNIT-I

Q2 (a) If a register holds a value of 10101010, determine its value after the following shift operations: **(5)**
(i) Arithmetic shift left by 1, circular shift right by 1 and followed by a logical shift left by 1.
(ii) Arithmetic shift right by 1, , circular shift left by 1 and followed by a logical shift right by 1.
(b) Construct a 5-to – 32 line decoder with four 3-to-8 line decoders with enable and one 2-to-4 line decoder. Draw the necessary block diagram. **(5)**

Q3 (a) Design an 8 bit combinatorial circuit. **(6)**
(b) Explain the principle of operation for a carry save adder with examples. **(4)**

UNIT-II

Q4 (a) What are the special registers in a computer? Explain their purpose in details. **(8)**
(b) Explain the various classifications of parallel structures. **(2)**

Q5 (a) What are memory reference instructions? **(2)**
(b) Describe bus and memory transfer with example. **(8)**

UNIT-III

Q6 With a neat flow chart, explain the internal control structure of the control unit using- **(10)**
(i) Hard-wired Control
(ii) Micro programmed Control

P.T.O.

IT-305
573 P1/2

Q7 (a) An instruction is stored at location 300 with its address field at location 301. The address field has the value 400. A processor register R1 contains the number 200. Evaluate the effective address if the addressing mode of the instruction is: **(5)**

(i) Direct
(ii) Immediate
(iii) Relative
(iv) Register Indirect
(v) Index with R1 as the index register.

(b) Explain 8085 instruction set architecture **(5)**

UNIT-IV

Q8 (a) Explain the reading and writing operation of a basis static RAM cell. **(5)**

(b) A computer has 512 KB cache memory and 2MB main memory. If the block size is 64 bytes, then find out the sub fields for: **(5)**

(i) Direct mapped cache
(ii) Associative

Q9 Write short notes on **any two** of the following:- **(5x2=10)**

(a) Programmed I/O techniques
(b) DMA
(c) Vector Interrupt

****

(Please write your Exam Roll No.) Exam Roll No. .....

END TERM EXAMINATION

FIFTH SEMESTER [B.TECH.] DECEMBER 2016

Paper Code: IT-307 **Subject: Digital Signal Processing**

Time: 3 Hours **Maximum Marks: 60**

Note: Attempt any five questions including Q no.1 which is compulsory. Assume suitable missing data, if any.

Q1 (a) Check the system $y(n)=a^n u(n)$ for stability. **(3)**

(b) Check $y(n)=\sin(n)x(2n-5)$ for Time-Invariance and $y(n)=\sin(n+3)x(n-4)+x(n+2)$ for Causality. **(3)**

(c) Find IR of system $y(n)+4y(n-1)+4y(n-2)=r(n-2)$ **(3)**

(d) Perform convolution of two periodic sequences $x_1(n)=\{1,2,3,4\}$ and $x_2(n)=\{5,6,7,8\}$ using Circular convolution. **(3)**

Q2 (a) The IR of a FIR filter, $h(n)=\delta(n)+\frac{1}{4}\delta(n-1)+\frac{1}{16}\delta(n-2)$. Find the response of this filter to $x(n)=\sin\left(\frac{n\pi}{2}\right)u(n)$ **(6)**

(b) Frequency response of a FIR filter is given as $H(e^{jw})=e^{-3Jw}[2+1.8\cos 3\omega t+1.2\cos 2\omega t+0.5\cos \omega t]$ Find IR of filter and identify filter type based on its passband. **(6)**

Q3 (a) Prove Initial Value Theorem of Z Transform. **(6)**

(b) Two systems having IR $h_1(n)=\left(\frac{1}{4}\right)^n u(n)$. And $h_2(n)=\left(\frac{1}{2}\right)^n u(n)$ are connected in cascade find the next IR. **(6)**

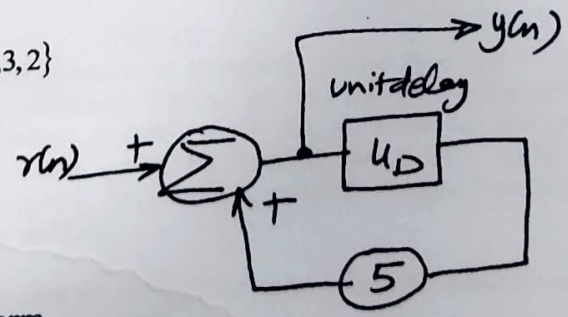
Q4 (a) Show that the magnitude response of an FIR filter at DC can be obtained as $|H(0)|=\left|\sum_{n=0}^{N-1}h(n)\right|$ and at frequency $w=\pi$ as $|H(\pi)|=\left|\sum_{n=0}^{N-1}\cos n\pi h(n)\right|$. **(6)**

(b) For the DTS shown, find **(6)**

(i) LDE

(ii) IR

(iii) Output if $r(n)=\{1,3,2\}$



Q5 Discuss-

(a) Properties of z-transform. **(6)**

(b) Linear convolution using DFT. **(6)**

Q6 The TF of a DT Causal system is $H(z)=\dfrac{1-\frac{1}{2}z^{-1}}{1-z^{-1}+\frac{3}{16}z^{-2}}$ obtain **(12)**

(a) Difference Equation.

P.T.O.

IT-307

57 Pl2

(b) Show DF-I, DF-II, Cascade and Parallel realization of this system.
(c) Find IR, step response and response to input

(i) $x(n)=\left(\frac{1}{2}\right)^n u(n)$ [an exponential excitation]

(ii) $x(n)=2\sin\left(\frac{\pi n}{3}-\frac{\pi}{5}\right)$ [a sinusoidal excitation]

Q7 Derive & explain the decimation in Time & Decimation in Frequency techniques for evaluating FFT. **(12)**

Q8 (a) The signal $f(t)=(0.8)^t u(t)$ is discretized to $f(n)=(0.8)^n u(n)$ having infinite length. Find the DFT of this signal, may be evaluated through an 8-point rectangular window. **(6)**
(b) Write short note on IIR filters. **(6)**

****

(Please write your Exam Roll No.)

Exam Roll No. .....

END TERM EXAMINATION

FIFTH SEMESTER [B.TECH/M.TECH] DECEMBER 2016 JANUARY 2017

Paper Code: IT-309 **Subject: Object Oriented Software Engineering**

Time : 3 Hours **Maximum Marks :60**

Note: Attempt all questions as directed. Internal choice is indicated.

Q1 Answer the following questions: **(10x2=20)**

(a) Why is analysis required for a difficult task?
(b) What are the challenges in designing with inheritance?
(c) What is Random Testing?
(d) What is Guard Condition?
(e) Give examples of Composition and Aggregation.
(f) What are the difference between pattern and framework?
(g) What are Identifying Actors?
(h) What are objects in Analysis and Process?
(i) Differentiate between method and Process.
(j) What are the limitations of state transition table?

Unit-I

Q2 (a) What are the software engineering development activities? Briefly explain each of activities in detail. **(8)**

(b) Differentiate between ISO 9001 and SEI – CMM quality standards. **(2)**

OR

Q3 What is the need of requirement elicitation? What are the Techniques for requirements elicitation? **(10)**

Unit-II

Q4 (a) Draw a Requirement model for online hotel reservation. **(5)**

(b) Differentiate between different types analysis objects for a University Examination System. **(5)**

OR

Q5 (a) What is Analysis Model? For a hospital System make Analysis Model and Design Model. **(5)**

(b) Draw a use case diagram for the admission process in a college where management decides whether to grant admission to a student or not. **(5)**

Unit-III

Q6 (a) What are structural and behavioral things in UML? Explain **(5)**

(b) A publisher publishes different books. An author can write different books but for the same publisher. A contract is signed between the publisher and the author. Reports such as the number of books sold, number of complimentary copies given, Royalty amount to be paid to the author etc. are generated from the system.

Draw a class diagram and an object diagram for the above case. **(5)**

OR

Q7 Discuss the activities performed during the design phase. Explain with the help of an example. **(10)**

Unit-IV

Q8 Write short notes on **any two**: **(5x2=10)**

(a) Fault Based Testing
(b) Object Modeling Techniques
(c) Testing process

****

P 525

(Please write your Exam Roll No.)

Exam Roll No. .....

END TERM EXAMINATION

FIFTH SEMESTER [B.TECH/M.TECH] DECEMBER 2016 – JANUARY 2017

Paper Code: IT-311 **Subject: Digital Design using VHDL**

Time: 3 Hours **Maximum Marks: 60**

Note: Attempt any five questions including Q.no.1 which is compulsory. Select one question from each Unit.

Q1 (a) What is the difference between the literals 16 # 23 DF # and X " 23 DF ". (2)
(b) Define attribute. (2)
(c) Define RTL. (2)
(d) Differentiate between procedure and function. (2)
(e) Explain following: (2)
(i) S' delayed (5 ns)
(ii) S' Last active
(iii) S' event
(iv) S' transduction
(f) Compare signals and variables. (2)
(g) Draw circuit for carry ripple adder. (2)
(h) Explain implicit and explicit sequencing. (2)
(j) Write VHDL code for signed multiplier. (4)

Unit-I

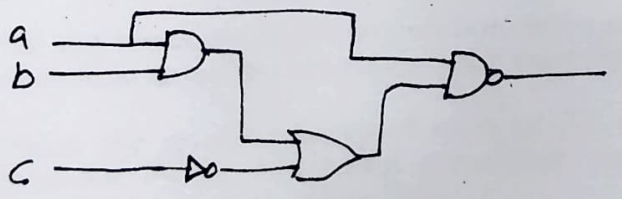
Q2 (a) Explain Behanard, Data flow and structural modeling in detail. (5)
(b) Give VHDL code to design 4-bit binary up counter. (5)

Q3 (a) Design 4-bit multiplexer circuit using VHDL. (5)
(b) Explain Microprogrammed controller. (5)

Unit-II

Q4 (a) Draw block diagram of 4-bit binary multiplier. Explain it. (5)
(b) Design 2:4 and 3:8 decoder circuit using VHDL. (5)

Q5 (a) Write VHDL code for following circuit: (6)



(b) Write a short note on field programming gate array logic. (FPGAs). (4)

Unit-III

Q6 Design FSM of BCD counter. (10)

Q7 (a) Explain Delta, Transport and initial delay with example. (5)
(b) Write short note on design of SRAM. (5)

Unit-IV

Q8 (a) Explain micro instruction sequencing in brief. (5)
(b) Design half adder using VHDL code. How do you implement floating point adder circuit in VHDL. (5)

Q9 (a) Explain Mealy-type FSH for serial adder. (5)
(b) Explain design of Arbiter. (5)

****

P576