FIFTH SEMESTER [B.TECH] DE

| pape       |  | Subject: Computer A   |  |
|------------|--|---|--|
| -1-076     | S Moure  |   | 1 60   |
| Not        | e: Attempt any five question   | Maximum s including Q.no.1 which is constitution from each Unit.  | ompulsory.   |
| Q1         | (c) ABCD- seven segment de   | vired control and Microprogrammed overflow.   |  |
|            | (d) What is pipeline register?   | coder/driver in connected to an attend for the input code DCBA = 000 aps are needed to provide a memoral position of the input code at the code provide a memoral position. | 11.  |
|            | (f) What is Excess 3 code?   |   | ry capacity of   |
|            | (g) What is advantage of using (h) What features designate 80.                                       | Cache memory?<br>85 as an 8 bit processor?  |  |
|            | <ul><li>(i) What is shift register?</li><li>(j) What is the basic difference architecture.</li></ul> | ce between computer organization a  | and computer   |
|            |  | Unit-I  |  |
| Q2         | (a) Register A holds the 8-bit<br>the logic micro-operation to:                                      | binary 11011001. Determine the Bo be performed in order to change   | operand and the value in A   |
|            | (i) 01101101 (ii) 11111110<br>(b) Subtract the following usin  | g 2's complement.   | (6)  |
|            | (i) 1000011 from 1010101   | 0 (ii) 72532 from 3250.   | (2x2=4)  |
| Q3         | (a) Design 4-bit common bus to (b) Explain IEEE 754 floating   | to transfer the contents of one regist point standard with example.  Unit-II  | ter to other. (6)<br>(4)   |
| Q4         | (a) Explain 8085 instruction s   | et architecture.  | (5)  |
|            | (b) What do you understand<br>cycle?   | by Fetch cycle, instruction cycle   | and machine (5)  |
| Q5         | (a) Write a program to evaluat $X = (A + B) * (C + B)$   | - D).   | (6)  |
|            | (ii) Using two and three ad  | type computer with one address ins<br>dress instructions and<br>computer with zero address instruc  |  |
|            | (b) Draw a block diagram of a  | ssociative memory. Unit-III   | (4)  |
| Q6         | <ul><li>(a) Explain stack organization</li><li>(b) What do you mean by inde</li></ul>                | with an example. exed addressing mode?  | (5)<br>(5)   |
| Q7         | (a) What is parallelism and pi<br>(b) Write a note on Pentium P                                      | pelining in computer architecture? rocessor. Unit-IV  | (6)  |
| 8 <i>Q</i> | (a) Draw a block diagram of a (b) What do you mean by men  |   | (5)  |
| Q9         |  | oftware and Hardware interrupts?  | How these are (6)  |
|            | (b) Explain RS-232-C.  |   | AND DESCRIPTION OF THE PARTY OF |

FIFTH SEMESTER [B.TECH./M.TECH.] DECEMBER 2014-JANUARY-2015

Subject: Theory of Computation Paper Code: IT301 Maximum Marks:60 Time: 3 Hours

Note: Attempt any five questions including Q.no.1 which is compulsory.

- (a) Discuss the applications of regular expressions. Q1
  - (b) With the help of examples define Pumping lemma.
  - (c) Explain the disadvantages of ambiguous grammar.
  - (d) Define halting problem.
  - (4x5=20)(e) Differentiate between NP complete and NP hard problem.
- (a) Explain Chomsky classification using example for each classification.(5)  $Q_2$ (b) Discuss the steps to convert a NFA to DFA. Provide example to
  - (5) support the steps.
- (5) (a) Discuss the closure properties of CFL. Q3
  - (b) Differentiate between LL(1) and LL(2) grammar. Provide example for (5)both LL(1) and LL(2) grammar.
- (a) Differentiate between Push down automata and Turing machine. (5)Q4
  - (b) Verify that the language  $L = \{ \omega \in a^n \ b^n \ c^{2n} \}$  is context free or not. (5)
- Define Decidability. What are the factors to determine the decidability? Q5 How does turing machine helpful for decidability? Explain using an (10)example.
- (a) Define hierarchy theorem. Explain using an example. (5)Q6
  - (b) Discuss and explain the various complexity classes. (5)
- Construct the regular expression for the following languages:-(5x2=10)Q7
  - (a) Language that accepts exactly one combination of 0 and 1.
  - (b) Language that accepts any number of 1s at the starting of the language.
- (5x2=10)Write short notes on any two of the following:-Q8
  - (a) Recursion Theorem
  - (b) Non-deterministic turing machine
  - (c) Interactive proof systems

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FIFTH SEMESTER [B.TECH./M.TECH.] DEC. 2014-JAN. 2015 Paper Code: IT303 Subject: Analog & Digital Communications

Time: 3 Hours

Note: Attempt any five questions including Q.no.1 which is compulsory. Maximum Marks :60

Select one question from each unit.

(a) Differentiate between Analog and Digital signals. Discuss pros and cons of Q1 these signals. Give atleast two application of each.

(b) Draw the Spectrum of Frequency Modulated signal and express the relation

(c) How do you avoid aliasing effect in sampled signals and show this effect

(d) List the major demerits of Delta modulation and how these can overcome?

(e) What is entropy of a source, give the formula and explain the significance of this term in information theory? (4x5=20)

UNIT-I

- Explain one of the methods to generate Standard AM signal (DSB, Full carrier), Q2 deduce the relation for bandwidth and represent the signal in time domain and frequency domain. (10)
- Discuss about the following two entities used for statistical analysis of Random Q3

(a) Power Spectral Density (PDF)

(b) Autocorrelation Function How these two parameters are interrelated?

(10)

UNIT-II

- Q4 Describe Armstrong method to generate frequency modulated signal. Draw its spectrum. Discuss about bandwidth requirement of Narrowband and wideband FM signals.
- Describe the generation and detection of Pulse width Modulation (PWM) signal. Q5 Draw all the relevant waveforms. (10)

UNIT-III

- What is quantization and quantization error? Obtain the relation for signal to Q6 Quantization noise ratio of uniform quantizer that is used to make the signal discrete in amplitude domain. Why non-uniform quantization is preferred over (10)uniform quantization?
- Draw and explain the block diagram to Generate QPSK signals over Binary Q7 PSK (BPSK) signals. Draw the constellation diagram for BPSK and QPSK.

UNIT-IV

- A discrete Memory less source has an alphabet of eight letters with Q8 probabilities 0.25, 0.20, 0.15, 0.12, 0.10, 0.08, 0.05, 0.05. Use the Huffman encoding procedure to determine the binary code for the source output.
- Write short notes on any two of the following:-Q9

(2×5=10)

- (a) Block codes
- (b) Convolutional codes
- (c) Significance of S/N ratio and Noise figure.

FIFTH SEMESTER [B.TECH./M.TECH.] DEC. 2014-JAN. 2015

Paper Code: IT307 Subject: Digital Signal Processing Time: 3 Hours Maximum Marks:60 Note: Attempt any five questions including Q.no.1 which is compulsory. Explain the following briefly:-Q1 (2x10=20)(a) Give the properties of Z-transformation. (b) What is signal processing? (c) Give some properties of DFT. (d) Differentiate between FIR and IIR. (e) Define Convolution. (f) Why do we need FFT algorithms? (g) What are the computational saving in using N point FFT algorithm? (h) What are the advantages of FIR filters? (i) Differentiate between DIT and DIF. (j) Give some applications of DSP. (a) What are typical signals? Give some examples of typical signal. (5)Q2(b) Explain the time-domain LTI system with an example. (5) (a) Discuss the design procedure of FIR filter using frequency sampling Q3 (6)method. (b) Give the block diagram representation of digital filter. (4) (a) Derive the butterfly diagram of 8 point radix 2 DIF FFT algorithm and (6)Q4 fully label it. (4) (b) How can we classify signals? (a) Compute linear convolution of the two sequence  $x(n)=\{1,2,2,2\}$  and (6) Q5 (4) (b) Derive expressions to relate z-transfer and DFT.  $h(n)=\{1,2,3,4\}.$ (a) State and explain the scaling and time delay properties of z (5)Q6 (5)(b) Describe different types of sampling methods. transform. (4) (a) Explain the classification of discrete signals. (b) Determine the response of LTI system when the input sequence is  $x(n)=\{-1,1,2,1,-1\}$  using radix 2 DIF FFT. The impulse response is Q7 $h(n) = \{-1, 1, -1, 1\}.$ (a) Give some approaches of reducing the computation of an algorithm. (4) (b) An 8 point sequence is given by  $x(n)=\{2,2,2,2,1,1,1,1\}$ . Compute 8 Q8 point DFT of x(n) by radix DIT-FFT method.

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FIFTH SEMESTER [B.TECH./M.TECH.] DEC. 2014-JAN.-2015

| Paper Code: IT309 |   |  | Subject: Object Oriented Software   |  |
|-------------------|---|--|-------------------------------------|--|
|                   | : 3 Hours   | Maxim  | um Marks :60                        |  |
| Note              | e: Attempt any five question  | ns including Q.no.1 which is   | compulsory.                         |  |
| Q1                | Write short notes on any five (a) System testing (b) Analysis model (c) Software Development L (d) Software quality assurant (e) Software Metrics (f) Requirement Model-Active  | ife cycle  | (4x5=20)                            |  |
| Q2                |   | involved during OOA phase? H<br>red analysis? Provide the gui  |                                     |  |
| Q3                | For hospital management s (a) Draw use-case model. (b) Draw a sequence diagra (c) Explain component diag (d) Write use-case description   | um for any one use case.<br>gram.  | (2.5x4=10)                          |  |
| Q4                | detail.   | performed during requirement<br>oupling and cohesion in detail.  | at elicitation in (5) (5)           |  |
| Q5                | requirements? Give exa  | iate between function and mples of each. terface class and control class                               | (5)                                 |  |
| Q6                | <ul><li>(a) Describe various diagra</li><li>(b) What is an entity class structure?</li></ul>  | ams we make in UML with exames? How it can be used in design   | nple. (8)<br>igning database<br>(2) |  |
| Q7                | <ul> <li>(a) How do we identify the</li> <li>(b) Explain following relation</li> <li>(i) Association</li> <li>(ii) Aggregation</li> <li>(iii) Composition</li> <li>(iv) Dependency</li> <li>(v) Generalization</li> </ul> | relationship between the entiti<br>onships with example:-  | ies? (5)<br>(5)                     |  |
| Q8                | as id, name, phone, em  | for an employee having various<br>nail, street, city, basic sal, HRA<br>lass diagram and object diagra | , TA, DA. (5)                       |  |
| Q9                | Discuss Testing process,  | Testing activities and Techniqu  | ies. (10)                           |  |

FIFTH SEMESTER [B.TECH./M.TECH.] DECEMBER 2014- January 2015

Paper Code: IT311

Subject: Digital Design Using VHDL

Time: 3 Hours

**Maximum Marks:60** 

Note: Attempt any five questions including Q.no.1 which is compulsory. Select one question from each unit.

(a) Briefly outline the purpose of following VHDL modeling constructs:-Q1

(i) Entity Declaration (ii) Process statement

(b) Write variable declaration for a counter, initialized to 0; a status flag used to indicate whether a module is busy and a standard-logic value used to store a temporary results.

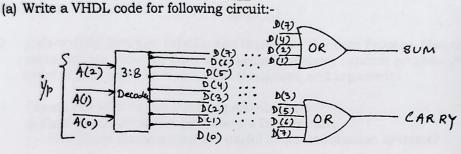
(c) Write a Wait Statement that suspends a process until a signal "ready" changes to '1' or until a maximum of 5ms has elapsed.

(d) Define state machine.

(5x4=20)

UNIT-I Q2

(5)



(b) Write an entity declaration and a behavioural architecture body for a twoinput multiplexer with input parts 'a', 'b' and 'set' and an output port 'z'. If the set input is '0' the value of 'a' shold be copied to 'z', otherwise the value of 'b' should be copied to 'z'. Write a VHDL code to implement the circuit. (5)

(a) Explain Generic and blocks construct. Q3

(5)(5)

UNIT-II

(b) Design an 8:1 MUX using with-select statement.

- (a) Write an 'if' statement that sets a variable 'odd' to '1' if an integer 'n' is odd, **Q4** or to '0' if it is even.
  - (b) Write a loop statement that samples a bit input 'd' when a clock input 'clk' changes to '1'. So long as 'd' is 'zero', the loop continues executing. When 'd' (5)is '1' the loop exits.

OR

(a) Differentiate between signal and variable. Q5

(5)

(b) Design a binary asynchronous counter.

(5)

UNIT-III Design and explain serial Adder suing FSM. Q6

(10)

Q7 Explain RTL.

(10)

UNIT-IV Q8 Design and explain Shift-And-Add Multiplier.

(10)

Q9 Explain Delta, Inertial and transport delay with example. (10)