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END TERM EXAMINATION

FIFTH SEMESTER [B.TECH./M.TECH.] DECEMBER 2013

Paper Code: IT301 **Subject: Theory of Computation**

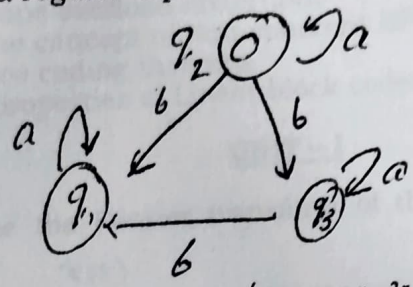
Time : 3 Hours **Maximum Marks :60**

Note: Attempt any five questions including Q.no.1 which is compulsory.

Q1 Explain briefly the following:- **(3x4=12)**

(a) Differentiate between NFA and DFA.
(b) Differentiate between context free grammar and regular grammar.
(c) Differentiate between P and NP problem.
(d) Explain the structure of a Turing machine.

Q2 (a) Construct a regular expression for the language accepted by DFA- **(6)**



(b) Show that the language $L = \{\omega \in a^n b^n c^{2n}\}$ is not context free. **(6)**

Q3 (a) Discuss the closure properties of CFLs. **(6)**
(b) State Pumping Lemma. Illustrate the pumping Lemma using an example. **(6)**

Q4 Consider the following grammar $E \rightarrow E+T/T$, $T \rightarrow a/b$. Determine- **(12)**

(a) SLR parsing table.
(b) LL(I) grammar/parsing table.

Q5 (a) Design a Turing machine, that accepts all the language of all palindrome over the alphabet {a,b}. **(8)**
(b) Justify the 5(a) turing machine on the string (i) babb (ii) bab. **(4)**

Q6 Construct a PDA to accept all strings generated by the language $\{a^n b^m a^n | m, n \geq 1\}$. **(12)**

Q7 (a) Differentiate NP complete and NP Hard problems. Explain NP complete and NP hard problems with some example. **(6)**
(b) Discuss and explain Hierarchy Theorem. **(6)**

Q8 Write short notes on **any two** of the following:- **(6x2=12)**

(a) Halting problem
(b) Decidability
(c) Chomsky Classification

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END TERM EXAMINATION

FIFTH SEMESTER [B.TECH./M.TECH.] DECEMBER-2013

Paper Code: IT-303 **Subject: Analog & Digital Communication**

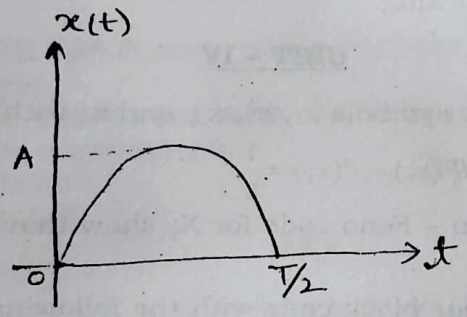
Time : 3 Hours **Maximum Marks :60**

Note: Attempt five questions including Q.No.1 which is compulsory. Select one question from each unit.

Q.1 (a) Explain the need for modulation in communication system. (2)
(b) Compare energy spectral density function and power spectral density function. (2)
(c) Show that the maximum power efficiency of an AM modular is 50%. (2)
(d) What do you mean by Hilbert transfer and inverse Hilbert transform. (2)
(e) Draw the block diagram to show the process of generation of FM using phase modulator. (2)
(f) What is aliasing and how it is reduced? (2)
(g) What is slope overload distortion? (2)
(h) Explain the concept of Non-coherent BPSK. (2)
(i) State source coding theorem. (2)
(j) State the properties of Linear block codes. (2)

UNIT – I

Q.2 (a) Determine the Fourier transform of the sinusoidal pulse shown in Fig.1. (5)



(b) Prove that the convolution of a function x(f) with an unit impulse function results the function itself. (5)

OR

Q.3 (a) Explain the square-law diode modulation method for AM generation. (5)

(b) Compare the three main system of SSB generation by drawing up a table of the outstanding characteristics of each system. (5)

UNIT – II

Q.4 A baseband or modulating signal $x(t) = 5\cos 2\pi 15x10^3 t$ angle modulates a carrier signal $A\cos\omega_c t$ (10)

(i) Determine the modulation index and band width for (a) FM System (b) PM System

(ii) find the change in the bandwidth and modulation index for both FM and PM if modulating frequency fm is reduced to 5KHZ. Assume $K_f = K_p = 15$ KHz/Volt

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OR

Q.5 (a) Find the Nyquist rate and the Nyquist internal for the signal. (5)

$$x(t) = \frac{1}{2\pi}\cos(4000\pi t)\cos(1000\pi t)$$

(b) Write short notes on **any two** (2.5X2=5)

(i) Asynchronous Multiplexing
(ii) FDM
(iii) PWM detector

UNIT – III

Q.6 (a) Explain the quantization error and derive an expression for maximum signal to noise ratio in PCM system that uses Linear quantization. (5)

(b) With the help of neat diagram explain the transmitter and receiver of PCM. (5)

OR

Q.7 (a) Draw the block diagram of DPSK modulator and explain how synchronization problem is avoided for its detection. (5)

(b) What is QPSK. Draw the block diagram of generation of QPSK system and explain its working. (5)

UNIT – IV

Q.8 (a) A DMS X has four symbols x_1, x_2, x_3, and x_4 with (5)

$$P(x_1) = \frac{1}{2}, P(x_2) = \frac{1}{4} and P(x_3) = P(x_4) = \frac{1}{8}.$$

Construct a Shannon – Feno code for X; show that the code efficiency is 100 percent.

(b) Given a (6,3) Linear block code with the following parity-check matrix H; (5)

$$H = \begin{bmatrix} 101100 \\ 011010 \\ 111001 \end{bmatrix}$$

(i) Find the generator matrix
(ii) Find the code word for the data bit 101.

OR

Q.9 Write short notes on **any two** (5X2=10)

(a) Convolution Codes
(b) Entropy and information rate
(c) Noise temperature and Noise figure.

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END TERM EXAMINATION

FIFTH SEMESTER [B.TECH/M.TECH] DECEMBER 2013

Paper Code: IT-305 **Subject: Computer Architecture**

Time : 3 Hours **Maximum Marks :60**

Note: Attempt any five questions, including Q.no.1 is compulsory. Select one question from each Unit.

Q1 Answer the following questions:- **(10x2=20)**

(a) Convert $(215)_{10}$ in BCD.
(b) What is Logic Micro Operation.
(c) What is Indirect Address.
(d) What is Program Counter.
(e) Explain an Instruction Format.
(f) Differentiate between Hardwired & Microprogramme control unit.
(g) Convert the following arithmetic expression from reverse polish notation to infix notation:-
ABC * / D – EF / +
(h) What is set- associative mapping?
(i) Differentiate between synchronous and asynchronous data transfer.
(j) What is hit ratio?

UNIT-I

Q2 (a) Explain IEEE 754 floating point representation in detail with the help of an example. **(5)**

(b) Perform the subtraction with the following unsigned binary number by taking 2's complement:- **(5)**
(i) 11010 - 10000
(ii) 100 – 110000

OR

Q3 (a) Show the block diagram of the hardware that implement the following register transfer statement:- **(5)**

y^{T_2} : R2 ← R1, R1 ← R2

(b) Draw a diagram for 4-bit binary adder. **(5)**

UNIT-II

Q4 Explain different types of basic computer registers and memory with their functions and draw a diagram shouting basic computer registers connected to a common bus. **(10)**

OR

Q5 (a) Draw a timing diagram assuming that SC is cleared to zero at Time T_3 if control signal C_7 is active. $C_7\ T_3$: SC ← O

C_7 is activated with positive clock transition associated with T_1. **(5)**

(b) What are input/output interrupts? **(5)**

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UNIT-III

Q6 (a) Define the following:-
(i) Micro Operation
(ii) Micro Instruction
(iii) Micro Program
(iv) Micro Code (5)

(b) What do you mean by decoding of micro operation fields. (5)

OR

Q7 (a) Consider in a stock SP = 000000 (SP = Stack Point Register), then many items are there in the stack if:
(i) FULL = 1 and EMTY = 0 ?
(ii) FULL = 0 and EMTY = 1 ? (5)

(b) What are the basic differences between a branch instruction, a call subroutine instruction, and program interrupt? (5)

UNIT-IV

Q8 Define following **(any two)**:- **(5x2=10)**
(a) RS – 232 – C & RS – 422 standard.
(b) Auxiliary Memory.
(c) What is Associative Mapping, Direct Mapping, Set- Associative Mapping?

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END TERM EXAMINATION

FIFTH SEMESTER [B.TECH./M.TECH.] DECEMBER 2013

Paper Code: IT307 **Subject: Digital Signal Processing**

Time : 3 Hours **Maximum Marks :60**

Note: Attempt any five questions. Usage of calculators is allowed.

Q1. Attempt any four parts. (3x4)

(i) Explain one-dimensional signal with suitable examples.

(ii) Distinguish between continuous time and discrete time signals.

(iii) Explain periodic signals.

(iv) Define the term "stability" for a linear time invariant system.

(v) Determine the *z*-transform as well as the Region of Convergence for $x[n]=(\frac{1}{2})^n u[n]$.

(vi) State and establish the circular – shift property for the Discrete Fourier Transform (DFT).

Q2. Attempt any three parts. (4x3)

(i) Consider the discrete time Linear Time Invariant (Linear Shift Invariant) system with input *x*[n] and output is *y*[n] for which *y*[n-1] – (10/9)*y*[n]+*y*[n+1] = *x*[n]. Determine the unit-response in *z*-domain.

(ii) Find the *z*-transform of the following:

(a) $x[n] = -n\, a^n\, u[-n-1]$

(b) $x[n] = a^n \sin(w\, n)\, u[n]$

(iii) Find the inverse *z*-transform of , $X(z)=\frac{1+z^{-1}+2z^{-2}}{(1-\frac{1}{2}z^{-1})(1-\frac{1}{3}z^{-1})(1-\frac{1}{4}z^{-1})}; |z|>\frac{1}{2}$

(iv) Given that the *z*-transform of x[n] is X(z), find the *z*-transform of x[n] – x[n-1]. Establish your result.

Q3. Attempt any three parts. (4x3)

(a) Determine the output of the linear filter whose impulse response is h[n] = {1,-2,3} and the input signal is x[n] = {-1,2,-3,4,-5,6,-8} using either overlap-save or overlap-add method. State the method used.

(b) State and establish the Parseval's property/theorem for DFT.

(c) If the DFT of two N point sequences x[n] and y[n] is X[k] and Y[k], respectively. What is the DFT of x[n]y[n].

(d) Find the circular convolution of the given sequences: x[n] = {1,3,5,7} and y[n] = {2,4,6,8}.

Q4. Attempt all parts: (9+3)

(a) Determine the DFT of the given data sequence: x[n] = {2,1,4,6,5,8,3,9} using decimation in time FFT.

(b) What is the computational complexity of the FFT algorithm. Write a brief note.

Q5. For the system described by the difference equation: (6+6)

$y[n] - (13/12)\, y[n-1] - (1/24)\, y[n-3] = x[n]+2x[n-1]$

obtain the following realizations:

i. Direct Form I

ii. Parallel

Q6. Obtain the direct form structure and the cascade structure form for: (6+6)

$H(z) = 1 + 8z^{-1} + 21z^{-2} + 35z^{-3} + 28z^{-4} + 15z^{-5}$.

Q7. Attempt any 3 parts. (4x3)

i. Determine the impulse invariant digital filter transfer function corresponding to the transfer function for an anlaog filter given by

$$H(s)=\frac{s+2}{(s+2)^2+4}$$

ii. Compare and contrast IIR and FIR filters.

iii. Write short note on the sampling theorem. Determine the Nyquist rate / sampling rate for the given signal:
$x(t) = 2\cos(50\pi t) + 3\sin(150\pi t) - 4\cos(300\pi t)$

iv. Write short note on linear phase filter.

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END TERM EXAMINATION

FIFTH SEMESTER [B.TECH/M.TECH] DECEMBER 2013

Paper Code: IT-309 **Subject: Object Oriented Software Engineering**

Time: 3 Hours **Maximum Marks: 60**

Note: Attempt any five questions, including Q.no.1 is compulsory. Select One question from each Unit.

Q1 Answer the following questions:- (10x2=20)

(a) Walk Through.
(b) Reusability.
(c) Cohesion.
(d) Discuss advantages of incremental model.
(e) What is the need of SRS?
(f) What is an abstract class?
(g) What is the difference between scenario and use case?
(h) What is polymorphism testing?
(i) When should we choose an object oriented database?
(j) How do we identify the Actor's in a particular system?

UNIT-I

Q2 (a) What are different standards for developing life cycle models? (7)
(b) Is there ever a case when the generic phases of software engineering process do not apply? If so, describe it. (3)

OR

Q3 (a) Describe the activities involved in requirement elicitation in detail. (8)
(b) Distinguish between functional and non-functional requirements. (2)

UNIT-II

Q4 Discuss the issues related to managing the analysis in a multi-team development project. (10)

OR

Q5 (a) Explain how OOA model is translated to OOD model. (5)
(b) What are the main features of Test Model? (5)

UNIT-III

Q6 (a) How is use case related to a system? (5)
(b) What are building blocks of UML? Discuss with an example. (5)

OR

Q7 Develop a complete use case for using your debit card for a meal at restaurant. (10)

UNIT-IV

Q8 Explain any two of the following:- (2x5=10)

(a) Various Testing Activities.
(b) System Testing.
(c) Object Oriented Component Testing.

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END TERM EXAMINATION

FIFTH SEMESTER [B.TECH/M.TECH] DECEMBER 2013

Paper Code: IT-311 **Subject: Digital System Design using VHDL**

Time : 3 Hours **Maximum Marks :60**

Note: Attempt any five questions, including Q.no.1 is compulsory. Select one question from each Unit.

Q.No.1 (a) Discuss design flow and synthesis process in VHDL.
(b) What are the Moore and Mealy machines? Compare them. (5*4=20)
(c) What is process statement and how it is used in VHDL? Give example.
(d) What is a resolution function in VHDL? Discuss.
(e) What is port mapping? How port mapping is used in VHDL language?

UNIT-I

Q. No. 2 (a) Discuss different data types used in VHDL? Explain with examples. (5)
(b) What is meant by operator overloading? Give an example. (5)
Q. No.3 Write VHDL codes for 2: 4 decoder and 4:1 multiplexer using behavioral modeling style. (10)

UNIT-II

Q. No.4 Write down the truth table and VHDL code for the 4-bit up/down counter. Draw the circuit and output waveforms. (10)
Q. No.5 Write down the truth table and VHDL code for the 4-bit left to right shift register. Draw the circuit and output waveforms. (10)

UNIT-III

Q. No.6. Write state table and draw the state diagram for D flip-flop, T flip flop, JK flip-flop. Also write the VHDL code for these flip-flops. (10)
Q. No.7 Design a clocked sequential circuit and that operates according to the given state table. Use D flip flops. Also write the VHDL code. (10)

Present state (AB)	Input (X)	Next state(AB)	Output (Y)
00	0	00	0
00	1	01	1
01	0	10	0
01	1	01	0
10	0	10	0
10	1	11	1
11	0	11	0
11	1	00	0

UNIT-IV

Q. No. 8 (a) Explain the inertial and transport delay model in VHDL. (5)
(b) How can a multiplier circuit be defined in synthesis? (5)
Q. No.9 Explain in detail the ASM technique of designing a sequential circuit. (10)

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