

END TERM EXAMINATION

FIFTH SEMESTER [B.TECH.] DECEMBER 2017

Paper Code: IT-301

Subject: Theory of Computation

Time: 3 Hours

Maximum Marks: 60

Note: Attempt any five questions including Q.No 1 which is compulsory. Select one question from each unit.

Q1 Answer the following questions: (2x10=20)

- (a) State kleen's theorem. what is a regular expression.
- (b) Define top down parsing and LL(1) grammar.
- (c) Write your comment on "Can a machine produce itself?
- (d) Define PSPACE and NSPACE complexity classes.
- (e) Prove that language $L=\{a^n b^n | n > 0\}$ is not regular.
- (f) State Pumping lemma for context free language.
- (g) What is a parse tree
- (h) Differentiate between polynomial time reduction and Logarithmic space reduction
- (i) Define Pushdown automata. Give example.

UNIT-I

Q2 Prove that regular languages are closed under union and intersection. Let M1 and M2 be the two Finite automata's accepting the language L1 and L2 respectively. Design automaton to recognize the language. (10)

- (a) $L_1 \cup L_2$
- (b) $L_1 - L_2$
- (c) $L_1 \cap L_2$

Where $L_1 = \{\text{No. of } a's \text{ in the string defined over } a, b \text{ is even}\}$

And $L_2 = \{\text{no of } b's \text{ in the string defined over } a, b \text{ is odd}\}$

Q3 Define Nondeterministic automata. Explain the mechanism to convert NDFA into DFA. (10)

UNIT-II

Q4 Define Pushdown automata. What is instantaneous descriptor. Design a pushdown automata to recognize the language $L=\{a^n b^{2n} | n > 1\}$ (10)

Q5 Prove that context free languages are closed under union and concatenation. Also prove that intersection of a Context free language and regular language will be a context free language. (10)

UNIT-III

Q6 What is Un-decidability problem? Prove that Halting Problem is Undecidable. (10)

Q7 Prove that Multitape Multihead Turing is computationally equivalent to a Standard Turning Machine. Design a turning Machine to accept the language $L=\{a^n b^n | n > 0\}$. (10)

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UNIT-IV

Q8 Write your views on the following "Every P-class problem is an NP-class problem". Also Prove that clique problem is NP complete. (10)

Q9 Prove that a problem solvable in the space of $O(f(n))$ requires worst case time of the order of $O(2^{f(n)})$ [Make necessary assumptions]. State and Prove Savitch theorem.

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END TERM EXAMINATION

FIFTH SEMESTER [B.TECH.] DECEMBER 2017

Paper Code: IT-301

Time: 3 Hours

Subject: Theory of Computation

Maximum Marks: 75

Note: Attempt any five questions including Q.No 1 which is compulsory. Select one question from each unit.

- Q1 Answer the following questions: (2.5x10=25)
- (a) State Kleen's theorem. what is a regular expression.
 - (b) Define top down parsing and LL(1) grammar.
 - (c) Write your comment on "Can a machine produce itself?
 - (d) Define PSPACE and NSPACE complexity classes.
 - (e) Prove that language $L=\{a^n b^n | n > 0\}$ is not regular.
 - (f) State Pumping lemma for context free language.
 - (g) What is a parse tree
 - (h) Differentiate between polynomial time reduction and Logarithmic space reduction
 - (i) Define Pushdown automata. Give example.

UNIT-I

- Q2 Prove that regular languages are closed under union and intersection. Let M1 and M2 be the two Finite automata's accepting the language L1 and L2 respectively. Design automaton to recognize the language. (12.5)

- (a) $L_1 \cup L_2$
- (b) $L_1 - L_2$
- (c) $L_1 \cap L_2$

Where $L_1 = \{\text{No. of } a's \text{ in the string defined over } a, b \text{ is even}\}$
And $L_2 = \{\text{no of } b's \text{ in the string defined over over } a, b \text{ is odd}\}$

- Q3 Define Nondeterministic automata. Explain the mechanism to convert NDFA into DFA. (12.5)

UNIT-II

- Q4 Define Pushdown automata. What is instantaneous descriptor. Design a pushdown automata to recognize the language $L=\{a^n b^{2n} | n > 1\}$ (12.5)

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UNIT-III

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UNIT-IV

- Q8 Write your views on the following "Every P-class problem is an NP-class problem". Also Prove that clique problem is NP complete. (12.5)
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END TERM EXAMINATION

FIFTH SEMESTER [B.TECH] DECEMBER 2017

Paper Code: IT-307

Subject: Digital Signal Processing

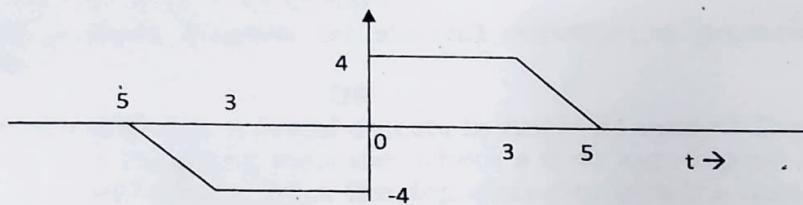
Time: 3 Hours

Maximum Marks: 75

Note: Attempt any five questions including Q.no. 1 which is compulsory.
Assume missing data if any.

Q1 Attempt any five: (5x5=25)

- Find the Fourier Coefficient of the signal $f(t) = \sin \omega_0 t$.
- Verify following system for Linearity and Time Invariance:
 - $y(t) = x^2(t)$,
 - $y(t) = \sin t \cdot x(t)$,
 - $y(t) = x(at)$, and
 - $y(t) = \log x(t)$.
- What is the difference between Causal System or Non-Causal System.
- Prove that discrete time harmonics are not always periodic in frequency.
- Find the Fourier Coefficient of the signal which is full wave rectifier signal.
- Write a short note filter bank.
- Compare IIR and FIR.
- Explain the need of low pass filter with a decimator and mathematically prove that $\omega_x = \omega_y D$.
- Short note on Frequency Sampling realization of FIR filters.

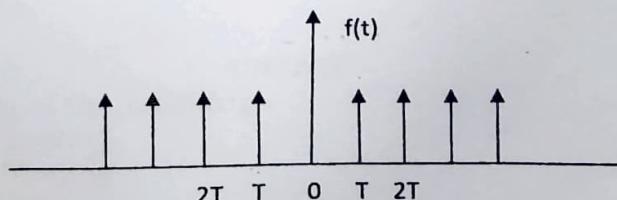
Q2 (a) Signal $f(t)$ is defined as below: (6.5)

A signal $g(t)$ is realized by multiplying $f(t)$ with $\delta(t + 4) + \delta(t - 4)$ is the integral of the signal or power signal. Hence find the Energy or Power.

- Find the response of discrete time LTI system having the input and impulse responses as given below $f[n] = a^n u[n]$, $h[n] = a^n u[n]$. (6)

Q3 (a) Derive the relationship between Trigonometric Fourier Series and Exponential Fourier Series. (6.5)

- Draw the Complex Spectrum of the given below and also find the Fourier series. (6)



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Q4 (a) Find the Fourier Transform of the signal.

$$(i) f(t) = \frac{1}{\pi t}, \quad (ii) f(t) = t \left(\frac{\sin t}{\pi t} \right)^2$$

(6.5)

(b) Find the number of complex additions and complex multiplications required to find DFT for 16 point signal. Compare them with number of computations required, if FFT algorithm is used.

(6)

Q5 (a) Compute DFT of a sequence, $x(n) = \{1,2,2,2,1,0,0,0\}$ using DIF-FFT algorithm. Sketch its magnitude spectrum.

(b) Find 8-point FFT of, $x(n) = \{1,2,2,2,1\}$ using signal flow graph of Radix-2 Decimation in frequency FFT.

(6.5)

(6)

Q6 Derive the Expression for impulse invariance technique for obtaining transfer function of digital filter from analog filter. Derive necessary equation for relationship between frequency of analog and digital filter.

(12.5)

Q7 Compare various windows used for designing FIR filters.

(12.5)

Q8 Compare various windows used for designing FIR filters.

(12.5)

Please write your Exam Roll No.)

Exam Roll No.

END TERM EXAMINATION

FIFTH SEMESTER [B.TECH.] DECEMBER 2017

Paper Code: IT-309
Time: 3 Hours

Subject: Object Oriented Software Engineering

Maximum Marks: 75

Note: Attempt all question as directed. Internal Choice is indicated.

- Q1 Answer the following questions: (5x5=25)
- (a) What are primary and secondary actors? Give examples.
 - (b) What is the use of stubs and Drivers in testing?
 - (c) Discuss the types of relationships and associations in class diagrams.
 - (d) What is the difference between Sequence diagrams and Collaboration diagrams?
 - (e) Discuss the benefits of OOSE over traditional SE.

UNIT-I

- Q2 (a) Discuss various software development life cycle models. Write merits and demerits of all. (10)
(b) What are standards involved in software development? Enlist. (2.5)

OR

- Q3 (a) What are the phases of Object Oriented Unified processing? Explain. (4)
(b) Differentiate between verification and validation. (3)
(c) What is the use of Requirement Elicitation? Explain at least two techniques used for requirement elicitation. (5.5)

UNIT-II

- Q4 (a) Is there any difference between USE CASE and SCENARIO? If yes/no, explain with the help of an example. (8)
(b) Construct a class diagram for student registration process in your university. (4.5)

OR

- Q5 (a) What are the different types of objects in Analysis model? Consider the case study of a Recycling machine, where a user can deposit recyclable bottles, cans and crates. Once the depositor deposits the items, he gets printed receipt. Create and analysis models showing the different types of objects and interaction between different objects. (12.5)

UNIT-III

- Q6 Consider the ARENA multimedia case study (Virtual Techspace, where virtual gaming tournaments can be held, played or watched). Write the problem statement and draw state chart diagram. (12.5)

OR

- Q7 Draw interaction diagrams (Both Sequence and Communication Diagrams) for ATM machine. (12.5)

UNIT-IV

- Q8 Explain any two of the following:- (6.25x2=12.5)
- (a) Integration Testing
 - (b) State Based Testing
 - (c) Testing Process

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END TERM EXAMINATION

FIFTH SEMESTER [B.TECH.] DECEMBER 2017

Paper Code: IT-309

Subject: Object Oriented Software Engineering

Time: 3 Hours

Maximum Marks: 60

Note: Attempt all question as directed. Internal Choice is indicated.

- Q1 Answer the following questions: (4x5=20)
- (a) What are primary and secondary actors? Give examples.
 - (b) What is the use of stubs and Drivers in testing?
 - (c) Discuss the types of relationships and associations in class diagrams.
 - (d) What is the difference between Sequence diagrams and Collaboration diagrams?
 - (e) Discuss the benefits of OOSE over traditional SE.

UNIT-I

- Q2 (a) Discuss various software development life cycle models. Write merits and demerits of all. (8)
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UNIT-II

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UNIT-III

- Q6 Consider the ARENA multimedia case study (Virtual Techspace, where virtual gaming tournaments can be held, played or watched). Write the problem statement and draw state chart diagram. (10)

OR

- Q7 Draw interaction diagrams (Both Sequence and Communication Diagrams) for ATM machine. (10)

UNIT-IV

- Q8 Explain any two of the following:- (5x2=10)
- (a) Integration Testing
 - (b) State Based Testing
 - (c) Testing Process

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END TERM EXAMINATION

FIFTH SEMESTER [B.TECH.] DECEMBER 2017

Paper Code: IT-311

Subject: Digital Design Using VHDL

Time: 3 Hours

Maximum Marks: 60

Note: Attempt five questions including Q.No1, which is compulsory. Assume missing data if any:-.

- Q1 (a) Discuss data types of VHDL. (5x4=20)
(b) Differentiate between signal and variable.
(c) Define RTL.
(d) Differentiate between delta, Inertial and Transport delay.
e) Explain the process statement with example.
- Q2 (a) Design 5:32 Decoder using a macro of 2:4 and 3:8 decoder. (7)
(b) What is operator overloading? Discuss. (3)
- Q3 (a) Explain Gajski 'Y' chart. (5)
(b) Design a 4-Bit adder using a component of full adder. (5)
- Q4 a) Design a 4-Bit up/down Binary Counter using VHDL. (5)
b) Write VHDL Code for D and T flip flops. (5)
- Q5 a) Design an universal shift Register using VDHL. (5)
b) Write VHDL Code for 3 to 8 decoder. (5)
- Q6 a) Design a FSM of 4-Bit Serial adder. (5)
b) Write VHDL code for 8x1 multiplexer. (5)
- Q7 Explain: - (10)
(i) State Table
(ii) State diagram
(iii) Mealy model
(iv) Moore model
- Q8 a) Design a FSM of shift-and-add multiplier (5)
b) What are various operators used in VHDL? Discuss. (5)
- Q9 a) Design a SRAM using VHDL. (5)
b) What are sequential and concurrent statement? Explain. (5)

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END TERM EXAMINATION

FIFTH SEMESTER [B.TECH.] DECEMBER 2017

Paper Code: IT-311

Subject: Digital Design Using VHDL

Time: 3 Hours

Maximum Marks: 75

Note: Attempt five questions including Q.No1, which is compulsory. Assume missing data if any:-.

- Q1 (a) Discuss data types of VHDL. (5x5=25)
(b) Differentiate between signal and variable.
(c) Define RTL.
(d) Differentiate between delta, Inertial and Transport delay.
e) Explain the process statement with example.
- Q2 (a) Design 5:32 Decoder using a macro of 2:4 and 3:8 decoder. (8)
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(ii) State diagram
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b) What are sequential and concurrent statement? Explain. (6.5)

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END TERM EXAMINATION

FIFTH SEMESTER [B.TECH/M.TECH] DECEMBER 2017

Paper Code: IT-303

Subject: Analog and Digital Communications

Time: 3 Hours

Maximum Marks: 75

Note: Attempt any five questions including Q.no. 1 which is compulsory.
Select one question from each Unit. Assume missing data if any.

- Q1 (a) Compare PCM and Delta Modulation in terms of their figure of merits.
 (b) A source emits one of four messages randomly every 1 microsecond. The probabilities of these messages are 0.5, 0.3, 0.1 and 0.1. Messages are independently generated (i) what is the source entropy?
 (ii) obtain a compact binary code and determine the average length of the codeword, the efficiency and the redundancy of this code rate.
 (c) Determine the Nyquist sampling rate and sampling interval for the signal (i) $\sin(100\pi t) + \sin(200\pi t)$ (ii) $\cos^2(2000\pi t)$.
 (d) Draw and explain circuit of envelope detector for AM.
 (e) Discuss Quadrature Amplitude Modulation (QAM) with the help of block diagram. (5x5=25)

Unit-I

- Q2 (a) The output power of 60% modulated AM generator is 2 A. To what value will this current rise if the generator is modulated additionally by another audio wave, whose modulation index is 0.6? What will be the percentage power saving if the carrier and one of the sideband are now suppressed. (6.5)
 (b) Explain trapezoidal method of monitoring A.M waveform directly on an oscilloscope. Sketch trapezoidal pattern for $0 \leq m \leq 1$. (6)
- Q3 (a) Explain balanced modulator. Why a ring modulator is known as a double balanced modulator. (6.5)
 (b) Explain Phasing method for generation SSBSC signal in detail. (6)

Unit-II

- Q4 (a) Explain Foster-Seelay discriminator in detail. (6.5)
 (b) Explain the importance of pre-emphasis and de-emphasis circuits. Why it is not useful in phase modulation but useful in frequency modulation? (6)
- Q5 (a) Explain the Armstrong method of FM generation with neat diagram. (6.5)
 (b) An FM wave is given by $e(t) = 20 \sin(6 * 10^8 t + 7 \sin 1250t)$. Determine (i) carrier frequency (ii) modulating frequency (iii) modulation index (iv) maximum deviation and (v) Transmitted power. (6)

Unit-III

- Q6 (a) Write the difference between coherent and non-coherent detection techniques? Describe non-coherent detection of FSK signal. (6.5)
 (b) What is advantage of Differential Phase-Shift Keying (DPSK) over BPSK? Explain DPSK modulation technique in detail. (6)

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IT-303

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- Q7 (a) What is Delta Modulation? Draw the block diagram of Delta modulator transmitter and explain its working with waveforms. (6)
- (b) A television signal with bandwidth of 4.2 MHz is transmitted using binary PCM. The number of quantization levels are 512. Calculate: (6)
- (i) Code word length
 - (ii) Transmission bandwidth
 - (iii) Final bit rate
 - (iv) Output signal to quantization noise ratio

Unit-IV

- Q8 (a) A source emits three equiprobable message randomly and independently. Find the source entropy. Find a compact binary code and the average length of the code word, the code efficiency and the redundancy. (6)
- (b) Construct a single-error correct (7, 4) linear block code and the corresponding decoding table. (6)
- Q9 (a) Define information and entropy of a source. What is mutual information? What is its significance? A memoryless source emits messages m_1 and m_2 with probabilities 0.8 and 0.2 respectively. Find the Huffman binary code for this source and determine its efficiency. (6)
- (b) Explain code tree, code trellis and state diagram for convolution encoders having generator polynomial $g_1 = [101]$ and $g_2 = [111]$. (6)

(Please write your Exam Roll No.)

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END TERM EXAMINATION

FIFTH SEMESTER [B.TECH/M.TECH] DECEMBER 2017

Paper Code: IT-303

Subject: Analog and Digital Communications

Time: 3 Hours

Maximum Marks: 60

Note: Attempt any five questions including Q.no. 1 which is compulsory.
Select one question from each Unit. Assume missing data if any.

- Q1 (a) Compare PCM and Delta Modulation in terms of their figure of merits.
(b) A source emits one of four messages randomly every 1 microsecond. The probabilities of these messages are 0.5, 0.3, 0.1 and 0.1. Messages are independently generated (i) what is the source entropy?
(ii) obtain a compact binary code and determine the average length of the codeword, the efficiency and the redundancy of this code rate.
(c) Determine the Nyquist sampling rate and sampling interval for the signal (i) $\sin(100\pi t) + \sin(200\pi t)$ (ii) $\cos^2(2000\pi t)$.
(d) Draw and explain circuit of envelope detector for AM.
(e) Discuss Quadrature Amplitude Modulation (QAM) with the help of block diagram.

(5x4=20)

Unit-I

- Q2 (a) The output power of 60% modulated AM generator is 2 A. To what value will this current rise if the generator is modulated additionally by another audio wave, whose modulation index is 0.6? What will be the percentage power saving if the carrier and one of the sideband are now suppressed. (5)
(b) Explain trapezoidal method of monitoring A.M waveform directly on an oscilloscope. Sketch trapezoidal pattern for $0 \leq m \leq 1$. (5)
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- Q7 (a) What is Delta Modulation? Draw the block diagram of Delta modulator transmitter and explain its working with waveforms. (5)
 (b) A television signal with bandwidth of 4.2 MHz is transmitted using binary PCM. The number of quantization levels are 512. Calculate: (5)
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 (ii) Transmission bandwidth
 (iii) Final bit rate
 (iv) Output signal to quantization noise ratio

Unit-IV

- Q8 (a) A source emits three equiprobable message randomly and independently. Find the source entropy. Find a compact binary code the average length of the code word, the code efficiency and the redundancy. (5)
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 (b) Explain code tree, code trellis and state diagram for convolution encoders having generator polynomial $g_1 = [101]$ and $g_2 = [111]$. (5)

(Please write your Exam Roll No.)

Exam Roll No.

END TERM EXAMINATION

FIFTH SEMESTER [B.TECH/M.TECH] DECEMBER-JANUARY 2018

Paper Code: IT 305

Subject: Computer Architecture

Time : 3 Hours

Maximum Marks : 75

Note: Attempt any five questions including Q.NO. 1 which is compulsory.
Select one question from each unit.

- Q1. Answer the following: (5x5=25)
- Perform the following decimal numbers to the bases indicated:
7652 to octal and binary
1938 to hexadecimal to binary
175 to binary
 - Explain BSA direct addressing, indirect addressing, Immediate addressing and Register addressing.
 - Write a program to add two 8 bit numbers using 8085 instruction set.
 - Write a short note on micro coded CPU.
 - An instruction is stored at location 300 with its address field at location 301. The address field has the value 400. A processor register R1 contains the number 200. Evaluate the effective address if the addressing mode of the instruction is:
 - Direct
 - Immediate
 - Relative

Unit-I

- Q2. a) Register A holds the 8 bit binary 11011001. Determine the b operation and the logic microoperation to be perform in order to change the value in A to (4)
i) 01101101
ii) 11111101
- b) Explain IEEE 754 floating point standard. (4)
- c) Perform the arithmetic operation $(+42)+(-13)$ and $(+42)-(-13)$ in binary using signed 2's complement representation for negative numbers. (4.5)

- Q3. a) Show the block diagram of the hardware that implement the following register transfer statement: (5)
 $y: R2 \leftarrow R1, R1 \rightarrow R2$
- b) Draw a diagram for 4 bit binary adder. (5)
- c) What is selective complement operation? (2.5)

Unit-II

- Q4. a) Draw a diagram showing basic computer registers connected to a common bus. (8.5)
- b) Consider a stack where SP=000000, calculate how many items are there in the stack of: (4)
i) FULL = 1 and EMTY = 0
ii) FULL = 0 and EMTY = 1
- Q5. a) Draw a flowchart for showing how an Interrupt is handled by the computer. (6)

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- b) What is the difference between a direct and an indirect address instruction? How many references to memory are needed for each type of instruction to bring an operand into a processor register? (6.5)

Unit-III

Q6. a) What is the difference between hardwired control and microprogrammed control? (3)

b) Explain in details the instruction cycle state diagram with interrupt. (6)

c) What is data bus, Control bus and address bus? (3.5)

Q7. a) A relative mode branch type of instruction is stored in memory at an address equivalent to decimal 750. The branch is made to an address equivalent to decimal 500.

i) What should be the value of the relative address field of the instruction (in decimal)?

ii) Determine the relative address value in the binary using 12 bits. (Why must the no. be in 2's complement?)

iii) Determine the binary value in PC after the fetch phase and calculate binary value of 500. (8)

b) Draw design of accumulator logic. (4.5)

Unit-IV

Q8. Write short notes of the following:

a) DMA (3)

b) A synchronous data transfer (3)

c) RS 422 standard (3)

d) UART (3.5)

END TERM EXAMINATION

FIFTH SEMESTER [B.TECH/M.TECH] DECEMBER-JANUARY 2018

Paper Code: IT 305

Time : 3 Hours

Subject: Computer Architecture

Maximum Marks : 60

Note: Attempt any five questions including Q.NO. 1 which is compulsory.
Select one question from each unit.

Q1. Answer the following:

(4x5=20)

- Perform the following decimal numbers to the bases indicated:
 - 7652 to octal and binary
 - 1938 to hexadecimal to binary
 - 175 to binary
- Explain BSA direct addressing, indirect addressing, Immediate addressing and Register addressing.
- Write a program to add two 8 bit numbers using 8085 instruction set.
- Write a short note on micro coded CPU.
- An instruction is stored at location 300 with its address field at location 301. The address field has the value 400. A processor register R1 contains the number 200. Evaluate the effective address if the addressing mode of the instruction is:
 - Direct
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Unit-I

Q2. a) Register A holds the 8 bit binary 11011001. Determine the b operation and the logic microoperation to be perform in order to change the value in A to

(3)

i) 01101101

ii) 11111101

(3)

b) Explain IEEE 754 floating point standard.
c) Perform the arithmetic operation $(+42)+(-13)$ and $(+42)-(-13)$ in binary using signed 2's complement representation for negative numbers.

(4)

Q3. a) Show the block diagram of the hardware that implement the following register transfer statement:

(4)

$y^t: R2 \leftarrow R1, R1 \rightarrow R2$

(4)

b) Draw a diagram for 4 bit binary adder.

(2)

c) What is selective complement operation?

Unit-II

Q4. a) Draw a diagram showing basic computer registers connected to a common bus.

(7)

b) Consider a stack where SP=000000, calculate how many items are there in the stack of:

(3)

i) FULL = 1 and EMTY = 0

ii) FULL = 0 and EMTY = 1

Q5. a) Draw a flowchart for showing how an Interrupt is handled by the computer.

(5)

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[2]

- b) What is the difference between a direct and an indirect address instruction? How many references to memory are needed for each type of instruction to bring an operand into a processor register? (5)

Unit-III

- Q6. a) What is the difference between hardwired control and microprogrammed control? (2)
- b) Explain in details the instruction cycle state diagram with interrupt. (5)
- c) What is data bus, Control bus and address bus? (3)
- Q7. a) A relative mode branch type of instruction is stored in memory at an address equivalent to decimal 750. The branch is made to an address equivalent to decimal 500.
- i) What should be the value of the relative address field of the instruction (in decimal)? (7)
- ii) Determine the relative address value in the binary using 12 bits. (Why must the no. be in 2's complement?) (3)
- iii) Determine the binary value in PC after the fetch phase and calculate binary value of 500. (3)
- b) Draw design of accumulator logic.

Unit-IV

- Q8. Write short notes of the following: (2.5)
- a) DMA (2.5)
- b) A synchronous data transfer (2)
- c) RS 422 standard (3)
- d) UART

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END TERM EXAMINATION

FIFTH SEMESTER [B.TECH./M.TECH.] DECEMBER 2019

Paper Code: IT-311

Subject: Digital Design Using VHDL

Time : 3 Hours

Maximum Marks : 75

Note: Attempt any five questions including Q.no. 1 which is compulsory.

- Q1**
- a) Differentiate between procedure & function. (3)
 - b) Define RTL. (3)
 - c) Write constant declaration for the number of bits in a 32- bit word and for the number π (3.14) (3)
 - d) Explain implicit and explicit sequencing. (3)
 - e) What is the difference between 16# 23DF# and X "23DF". (3)
 - f) Differentiate between signal and variable. (3)
 - g) Define attribute. (3)
 - h) Compare between PAL & PLA structure. Give their application. (4)
- Q2**
- a) Give VHDL code to design 4 bit binary up counter. (6.5)
 - b) Explain behavioral, Data flow and structural modeling in detail. (6)
- Q3**
- a) Design 3:8 decoder circuit with VHDL. (6.5)
 - b) Explain delta, transport & Inertial delay with example. (6)
- Q4**
- a) Explain Mealy and Moore Machine. (4)
 - b) Explain Block statement. (4)
 - c) Draw state graph for binary multiplier. (4.5)
- Q5**
- a) Write VHDL code for following circuit (6.5)
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- Q6**
- a) Design Half Adder using VHDL. (6.5)
 - b) Discuss design of data control sub system. (6)
- Q7**
- a) What is micro-programmed controller. Explain structure of micro-programmed controller in brief. (6.5)
 - b) Explain micro instruction sequencing in brief. (6)
- Q8**
- a) Design 4 bit multiplexer circuit using VHDL. (6.5)
 - b) Design and explain serial adder with accumulator. (6)
- Q9**
- Write short note:
 - a) EDA tools. (4)
 - b) Concept of operator overloading. (4)
 - c) VHDL data types. (4.5)

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