

END TERM EXAMINATION

FIFTH SEMESTER [B.TECH./M.TECH.] DECEMBER 2019

Paper Code: IT-311

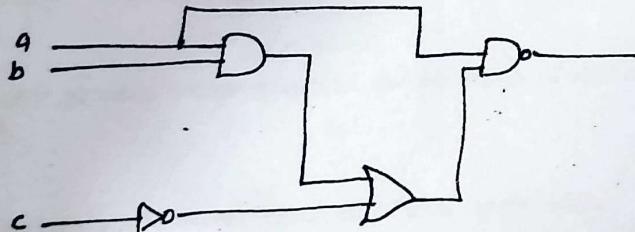
Subject: Digital Design Using VHDL

Time : 3 Hours

Maximum Marks :75

Note: Attempt any five questions including Q.no.1 which is compulsory.

- | | |
|----|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Q1 | a) Differentiate between procedure & function. (3)
b) Define RTL. (3)
c) Write constant declaration for the number of bits in a 32-bit word and for the number π (3.14) (3)
d) Explain implicit and explicit sequencing. (3)
e) What is the difference between 16# 23DF# and X "23DF". (3)
f) Differentiate between signal and variable. (3)
g) Define attribute. (3)
h) Compare between PAL & PLA structure. Give their application. (4) |
| Q2 | a) Give VHDL code to design 4 bit binary up counter. (6.5)
b) Explain behavioral, Data flow and structural modeling in detail. (6) |
| Q3 | a) Design 3:8 decoder circuit with VHDL. (6.5)
b) Explain delta, transport & Inertial delay with example. (6) |
| Q4 | a) Explain Mealy and Moore Machine. (4)
b) Explain Block statement. (4)
c) Draw state graph for binary multiplier. (4.5) |
| Q5 | a) Write VHDL code for following circuit (6.5) |



- | | |
|----|-------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Q6 | a) Design Half Adder using VHDL. (6.5)
b) Discuss design of data control sub system. (6) |
| Q7 | a) What is micro-programmed controller. Explain structure of micro-programmed controller in brief. (6.5)
b) Explain micro instruction sequencing in brief. (6) |
| Q8 | a) Design 4 bit multiplexer circuit using VHDL. (6.5)
b) Design and explain serial adder with accumulator. (6) |
| Q9 | Write short note:
a) EDA tools. (4)
b) Concept of operator overloading. (4)
c) VHDL data types. (4.5) |

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END TERM EXAMINATION

FIFTH SEMESTER [B.TECH.] DECEMBER 2017

Paper Code: IT-311

Subject: Digital Design Using VHDL

Time: 3 Hours

Maximum Marks: 60

Note: Attempt five questions including Q.No1, which is compulsory. Assume missing data if any:-.

- Q1 (a) Discuss data types of VHDL. (5x4=20)
(b) Differentiate between signal and variable.
(c) Define RTL.
(d) Differentiate between delta, Inertial and Transport delay.
e) Explain the process statement with example.
- Q2 (a) Design 5:32 Decoder using a macro of 2:4 and 3:8 decoder. (7)
(b) What is operator overloading? Discuss. (3)
- Q3 (a) Explain Gajski 'Y' chart. (5)
(b) Design a 4-Bit adder using a component of full adder. (5)
- Q4 a) Design a 4-Bit up/down Binary Counter using VHDL. (5)
b) Write VHDL Code for D and T flip flops. (5)
- Q5 a) Design an universal shift Register using VDHL. (5)
b) Write VHDL Code for 3 to 8 decoder. (5)
- Q6 a) Design a FSM of 4-Bit Serial adder. (5)
b) Write VHDL code for 8x1 multiplexer. (5)
- Q7 Explain: - (10)
(i) State Table
(ii) State diagram
(iii) Mealy model
(iv) Moore model
- Q8 a) Design a FSM of shift-and-add multiplier (5)
b) What are various operators used in VHDL? Discuss. (5)
- Q9 a) Design a SRAM using VHDL. (5)
b) What are sequential and concurrent statement? Explain. (5)

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END TERM EXAMINATION

FIFTH SEMESTER [B.TECH.] DECEMBER 2017

Paper Code: IT-311

Subject: Digital Design Using VHDL

Time: 3 Hours

Maximum Marks: 75

Note: Attempt five questions including Q.No1, which is compulsory. Assume missing data if any:-.

- Q1 (a) Discuss data types of VHDL. (5x5=25)
(b) Differentiate between signal and variable.
(c) Define RTL.
(d) Differentiate between delta, Inertial and Transport delay.
e) Explain the process statement with example.
- Q2 (a) Design 5:32 Decoder using a macro of 2:4 and 3:8 decoder. (8)
(b) What is operator overloading? Discuss. (4.5)
- Q3 (a) Explain Gajski 'Y' chart. (6)
(b) Design a 4-Bit adder using a component of full adder. (6.5)
- Q4 a) Design a 4-Bit up/down Binary Counter using VHDL. (6.5)
b) Write VHDL Code for D and T flip flops. (6)
- Q5 a) Design an universal shift Register using VDHL. (6.5)
b) Write VHDL Code for 3 to 8 decoder. (6)
- Q6 a) Design a FSM of 4-Bit Serial adder. (6)
b) Write VHDL code for 8x1 multiplexer. (6.5)
- Q7 Explain: - (12.5)
(i) State Table
(ii) State diagram
(iii)Mealy model
(iv)Moore model
- Q8 a) Design a FSM of shift-and-add multiplier (6)
b) What are various operators used in VHDL? Discuss. (6.5)
- Q9 a) Design a SRAM using VHDL. (6)
b) What are sequential and concurrent statement? Explain. (6.5)

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END TERM EXAMINATION

FIFTH SEMESTER [B.TECH./M.TECH.] DECEMBER 2014- January 2015

Paper Code: IT311

Subject: Digital Design Using VHDL

Time : 3 Hours

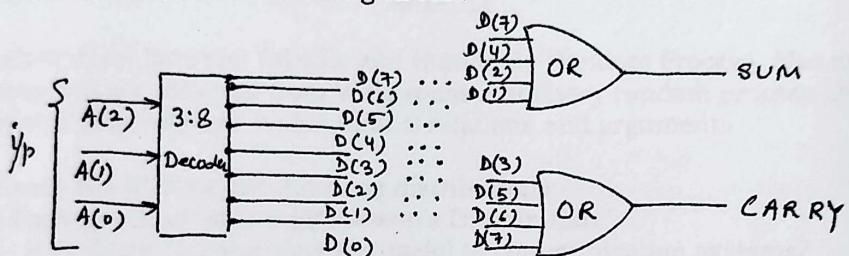
Maximum Marks :60

Note: Attempt any five questions including Q.no.1 which is compulsory.
Select one question from each unit.

- Q1** (a) Briefly outline the purpose of following VHDL modeling constructs:-
 (i) Entity Declaration (ii) Process statement
 (b) Write variable declaration for a counter, initialized to 0; a status flag used to indicate whether a module is busy and a standard-logic value used to store a temporary results.
 (c).Write a Wait Statement that suspends a process until a signal "ready" changes to '1' or until a maximum of 5ms has elapsed.
 (d) Define state machine. **(5x4=20)**

UNIT-I

- Q2** (a) Write a VHDL code for following circuit: **(5)**



- (b) Write an entity declaration and a behavioural architecture body for a two-input multiplexer with input parts 'a', 'b' and 'set' and an output port 'z'. If the set input is '0' the value of 'a' should be copied to 'z', otherwise the value of 'b' should be copied to 'z'. Write a VHDL code to implement the circuit. **(5)**

OR

- Q3** (a) Explain Generic and blocks construct. **(5)**
 (b) Design an 8:1 MUX using with-select statement. **(5)**

UNIT-II

- Q4** (a) Write an 'if' statement that sets a variable 'odd' to '1' if an integer 'n' is odd, or to '0' if it is even. **(5)**
 (b) Write a loop statement that samples a bit input 'd' when a clock input 'clk' changes to '1'. So long as 'd' is 'zero', the loop continues executing. When 'd' is '1' the loop exits. **(5)**

OR

- Q5** (a) Differentiate between signal and variable. **(5)**
 (b) Design a binary asynchronous counter. **(5)**

UNIT-III

- Q6** Design and explain serial Adder suing FSM. **(10)**

OR

- Q7** Explain RTL. **(10)**

UNIT-IV

- Q8** Design and explain Shift-And-Add Multiplier. **(10)**

OR

- Q9** Explain Delta, Inertial and transport delay with example. **(10)**

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END TERM EXAMINATION

FIFTH SEMESTER [B.TECH./M.TECH.] - DECEMBER 2010

Subject: Digital System Design Using VHDL

Paper Code: IT311

Paper ID: 15311

Time : 3 Hours

Maximum Marks : 60

Note: Attempt any five questions including Q.1 which is compulsory.

- Q1 (a) What is Behavioral and structural modeling? Give example using Full subtractor.
(b) Give the declaration and specification of user defined attributes. Give an example using enumerated encoding.
(c) Compare Moore and Melay state model. Give example using a serial adder.
(d) What is GENERIC? Design a generic parity detector.
(e) Give the VHDL code for designing signed comparator. (4x5=20)
- Q2 (a) Which standard gave standardization to VHDL language? Give the summary of VHDL design synthesis using a block diagram. (3)
(b) Give VHDL code for binary to grey code converter. (4)
(c) Compare Array, Port array and Records. Give VHDL code in support of your statements. (3)
- Q3 (a) Can addition between data type of BIT is possible? How do you allow addition between value of type BIT_VECTOR? Explain by giving example. Use the same technique to add an integer to a binary 1 bit number. Give VHDL code for the same. (4)
(b) Design and implement an Arithmetic logic unit using multiplexer. Write the VHDL code for it. (6)
- Q4 (a) What is PROCESS? Design a DFF using PROCESS. (2)
(b) Write VHDL code for 8-bit unsigned carry ripple adder. (6)
(c) Explain the role of GENERATE statement in VHDL. (2)
- Q5 (a) Compare Inertial Delay, delta delay and Transport delay. Give example. (3)
(b) Design a circuitry for a RAM with separate input output data buses. Give VHDL code for the implementation. (7)
- Q6 Write VHDL program for any two of the following;-(5+5)
(a) Signed Multiplier
(b) 8-bit register
(c) Floating point adder
(d) BCD counter
- Q7 Using the FSM approach design a traffic light controller. Assume that a 60Hz clock is available. (10)

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END TERM EXAMINATION

FIFTH SEMESTER [B.TECH] NOVEMBER-DECEMBER 2018

Paper Code: IT-311
Time: 3 Hours

Subject: Digital Design Using VHDL

Maximum Marks: 75

Note: Attempt any five questions including Q no. 1 which is compulsory.

- Q1 (a) Explain the behavioral and structural modeling in VHDL. (4)
(b) Define signal and variables. (4)
(c) Explain the use of generic statement in VHDL. (4)
(d) What is process statement in VHDL? Explain. (4)
(e) What are function and procedure in VHDL? Explain. (4)
(f) What is operator overloading in VHDL? Explain. (5)
- Q2 (a) What are the different data types used in VHDL? Discuss. (6)
(b) Explain about different operator used in VHDL. (6.5)
- Q3 Write a VHDL code for- (12.5)
(a) Full Adder
(b) 4x1 multiplexer
(c) BCD to 7segment decoder
- Q4 Write the VHDL program for- (12.5)
(a) D-flip flop
(b) Synchronous counter
(c) 4 bit-Shift Register with PIPO
- Q5 (a) Write VHDL for arithmetic logic unit. (6)
(b) What are concurrent and sequential statement in VHDL? Explain. (6.5)
- Q6 (a) Explain the Moore and Mealy state models and give examples. (6)
(b) Write VHDL description of 4-bit carry look Ahead adder. (6.5)
- Q7 (a) Explain the following terms:- (6)
(i) State Machine
(ii) State diagram
(iii) State table
(iv) State Assignment
(b) Write VHDL behavioral model for 32-bit adder. (6.5)
- Q8 (a) Explain the inertial and transport delay model in VHDL. (6)
(b) Write the behavioral model for 4x4 binary multiplier. (6.5)
- Q9 Explain the following:- (6)
(a) ASM chart
(b) SRAM design (6.5)

END TERM EXAMINATION

FIFTH SEMESTER [B.TECH/M.TECH] DECEMBER 2013

Paper Code: IT-311

Subject: Digital System Design
using VHDL

Time : 3 Hours

Maximum Marks :60

Note: Attempt any five questions, including Q.no.1 is compulsory. Select one question from each Unit.

- Q.No.1 (a) Discuss design flow and synthesis process in VHDL.
(b) What are the Moore and Mealy machines? Compare them. (5*4=20)
(c) What is process statement and how it is used in VHDL? Give example.
(d) What is a resolution function in VHDL? Discuss.
(e) What is port mapping? How port mapping is used in VHDL language?

UNIT-I

- Q. No. 2 (a) Discuss different data types used in VHDL? Explain with examples. (5)
(b) What is meant by operator overloading? Give an example. (5)
Q. No.3 Write VHDL codes for 2: 4 decoder and 4:1 multiplexer using behavioral modeling style. (10)

UNIT-II

- Q. No.4 Write down the truth table and VHDL code for the 4-bit up/down counter. Draw the circuit and output waveforms. (10)
Q. No.5 Write down the truth table and VHDL code for the 4-bit left to right shift register. Draw the circuit and output waveforms. (10)

UNIT-III

- Q. No.6. Write state table and draw the state diagram for D flip-flop, T flip flop, JK flip-flop. Also write the VHDL code for these flip-flops. (10)
Q. No.7 Design a clocked sequential circuit and that operates according to the given state table. Use D flip flops. Also write the VHDL code. (10)

Present state (AB)	Input (X)	Next state(AB)	Output (Y)
00	0	00	0
00	1	01	1
01	0	10	0
01	1	01	0
10	0	10	0
10	1	11	1
11	0	11	0
11	1	00	0

UNIT-IV

- Q. No. 8 (a) Explain the inertial and transport delay model in VHDL.. (5)
(b) How can a multiplier circuit be defined in synthesis? (5)
Q. No.9 Explain in detail the ASM technique of designing a sequential circuit. (10)

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END TERM EXAMINATION

FIFTH SEMESTER [B.TECH/M.TECH] DECEMBER 2016 – JANUARY 2017

Paper Code: IT-311

Subject: Digital Design using VHDL

Time: 3 Hours

Maximum Marks: 60

Note: Attempt any five questions including Q.no. 1 which is compulsory.
Select one question from each Unit.

- Q1 (a) What is the difference between the literals $16 \# 23\text{DF} \#$ and $X "23\text{DF}"$. (2)
(b) Define attribute. (2)
(c) Define RTL. (2)
(d) Differentiate between procedure and function. (2)
(e) Explain following:
 (i) S' delayed (5 ns) (2)
 (ii) S' Last active (2)
 (iii) S' event (2)
 (iv) S' transduction (2)
(f) Compare signals and variables. (2)
(g) Draw circuit for carry ripple adder. (2)
(h) Explain implicit and explicit sequencing. (2)
(j) Write VHDL code for signed multiplier. (4)

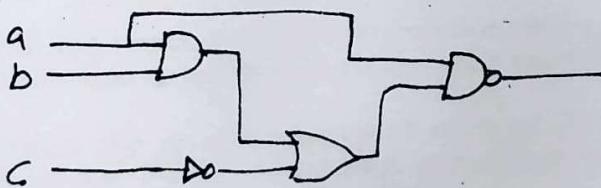
Unit-I

- Q2 (a) Explain Behanard, Data flow and structural modeling in detail. (5)
(b) Give VHDL code to design 4-bit binary up counter. (5)

Unit-II

- Q4 (a) Draw block diagram of 4-bit binary multiplier. Explain it. (5)
(b) Design 2:4 and 3:8 decoder circuit using VHDL. (5)

- Q5 (a) Write VHDL code for following circuit: (6)



- (b) Write a short note on field programming gate array logic. (FPGAs). (4)

Unit-III

- Q6 Design FSM of BCD counter. (10)

- Q7 (a) Explain Delta, Transport and initial delay with example. (5)
(b) Write short note on design of SRAM. (5)

Unit-IV

- Q8 (a) Explain micro instruction sequencing in brief. (5)
(b) Design half adder using VHDL code. How do you implement floating point adder circuit in VHDL. (5)

- Q9 (a) Explain Mealy-type FSH for serial adder. (5)
(b) Explain design of Arbiter. (5)

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Exam Roll No.

END TERM EXAMINATION

FIFTH SEMESTER [B.TECH/M.TECH] DECEMBER 2015-JANUARY 2016

Paper Code: IT-311

Subject: Digital Design Using VHDL

Time: 3 Hours

Maximum Marks: 60

Note: Attempt any five questions including Q.no.1 which is compulsory.

Select one question from each Unit.

Q1 Explain following in brief. Use block diagram when necessary.

- (a) Explain Gajski's 'Y' chart. (5)
- (b) Discuss delay in VHDL. (5)
- (c) Explain RTC. (5)
- (d) Define signal attribute to VHDL. (5)

Unit-I

Q2 (a) Design a 3:8 Decoder using VHDL. (4)

- (b) Design a 5:32 Decoder using a macro of 2:4 and 3:8 decoder with VHDL. (6)

Q3 (a) Design a full adder using VHDL. (4)

- (b) Design a 4-Bit Adder using a macro of full adder with Generate Statement. (6)

Unit-II

Q4 (a) Design a behavioral model of 3-Bit asynchronous counter. (5)

- (b) Differentiate between signal and variable. (5)

Q5 (a) Design a 4-Bit serial-in-serial-out shift Register. (5)

- (b) Design a S-R flip flop using VHDL. (5)

Unit-III

Q6 Design a 4-Bit serial Adder using VHDL. (10)

Q7 Explain state diagram of 4 x 4 Bit multiplier circuit. (10)

Unit-IV

Q8 Explain design of Bus architecture using MUX. (10)

Q7 Design a RAM using VHDL. (10)

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END TERM EXAMINATION

FIFTH SEMESTER [B.TECH/M.TECH] DECEMBER 2016 – JANUARY 2017

Paper Code: IT-311

Subject: Digital Design using VHDL

Time: 3 Hours

Maximum Marks: 60

Note: Attempt any five questions including Q.no. 1 which is compulsory.
Select one question from each Unit.

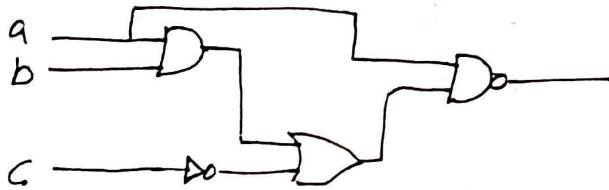
- Q1 (a) What is the difference between the literals $16 \# 23 DF \#$ and $X " 23 DF "$. (2)
(b) Define attribute. (2)
(c) Define RTL. (2)
(d) Differentiate between procedure and function. (2)
(e) Explain following: (2)
(i) S' delayed (5 ns)
(ii) S' Last active
(iii) S' event
(iv) S' transduction
(f) Compare signals and variables. (2)
(g) Draw circuit for carry ripple adder. (2)
(h) Explain implicit and explicit sequencing. (2)
(j) Write VHDL code for signed multiplier. (4)

Unit-I

- Q2 (a) Explain Behanard, Data flow and structural modeling in detail. (5)
(b) Give VHDL code to design 4-bit binary up counter. (5)
- Q3 (a) Design 4-bit multiplexer circuit using VHDL. (5)
(b) Explain Microprogrammed controller. (5)

Unit-II

- Q4 (a) Draw block diagram of 4-bit binary multiplier. Explain it. (5)
(b) Design 2:4 and 3:8 decoder circuit using VHDL. (5)
- Q5 (a) Write VHDL code for following circuit: (6)



- (b) Write a short note on field programming gate array logic. (FPGAs). (4)

Unit-III

- Q6 Design FSM of BCD counter. (10)
- Q7 (a) Explain Delta, Transport and initial delay with example. (5)
(b) Write short note on design of SRAM. (5)

Unit-IV

- Q8 (a) Explain micro instruction sequencing in brief. (5)
(b) Design half adder using VHDL code. How do you implement floating point adder circuit in VHDL. (5)
- Q9 (a) Explain Mealy-type FSH for serial adder. (5)
(b) Explain design of Arbiter. (5)

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END TERM EXAMINATION

FIFTH SEMESTER [B.TECH/M.TECH] DECEMBER 2016 – JANUARY 2017

Paper Code: IT-311
Time: 3 Hours

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Maximum Marks: 60

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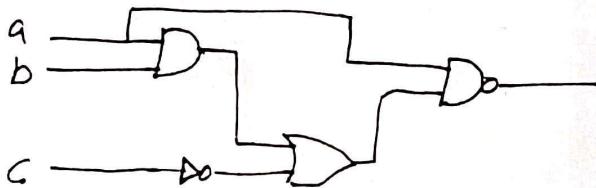
- Q1 (a) What is the difference between the literals $16 \# 23 DF \#$ and $X " 23 DF "$. (2)
(b) Define attribute. (2)
(c) Define RTL. (2)
(d) Differentiate between procedure and function. (2)
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 (i) S' delayed (5 ns)
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(f) Compare signals and variables. (2)
(g) Draw circuit for carry ripple adder. (2)
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(j) Write VHDL code for signed multiplier. (4)

Unit-I

- Q2 (a) Explain Behanard, Data flow and structural modeling in detail. (5)
(b) Give VHDL code to design 4-bit binary up counter. (5)
- Q3 (a) Design 4-bit multiplexer circuit using VHDL. (5)
(b) Explain Microprogrammed controller. (5)

Unit-II

- Q4 (a) Draw block diagram of 4-bit binary multiplier. Explain it. (5)
(b) Design 2:4 and 3:8 decoder circuit using VHDL. (5)
- Q5 (a) Write VHDL code for following circuit: (6)



- (b) Write a short note on field programming gate array logic. (FPGAs). (4)

Unit-III

- Q6 Design FSM of BCD counter. (10)
- Q7 (a) Explain Delta, Transport and initial delay with example. (5)
(b) Write short note on design of SRAM. (5)

Unit-IV

- Q8 (a) Explain micro instruction sequencing in brief. (5)
(b) Design half adder using VHDL code. How do you implement floating point adder circuit in VHDL. (5)
- Q9 (a) Explain Mealy-type FSH for serial adder. (5)
(b) Explain design of Arbiter. (5)

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U-15
Exam Roll No.

END TERM EXAMINATION

FIFTH SEMESTER [B.TECH/M.TECH] DECEMBER 2015-JANUARY 2016

Paper Code: IT-311

Subject: Digital Design Using VHDL

Time: 3 Hours

Maximum Marks: 60

Note: Attempt any five questions including Q.no. 1 which is compulsory.
Select one question from each Unit.

Q1 Explain following in brief. Use block diagram when necessary.

- (a) Explain Gajski's 'Y' chart. (5)
- (b) Discuss delay in VHDL. (5)
- (c) Explain RTC. (5)
- (d) Define signal attribute to VHDL. (5)

Unit-I

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(b) Design a 5:32 Decoder using a macro of 2:4 and 3:8 decoder with VHDL. (6)

Q3 (a) Design a full adder using VHDL. (4)

(b) Design a 4-Bit Adder using a macro of full adder with Generate Statement. (6)

Unit-II

Q4 (a) Design a behavioral model of 3-Bit asynchronous counter. (5)

(b) Differentiate between signal and variable. (5)

Q5 (a) Design a 4-Bit serial-in-serial-out shift Register. (5)

(b) Design a S-R flip flop using VHDL. (5)

Unit-III

Q6 Design a 4-Bit serial Adder using VHDL. (10)

Q7 Explain state diagram of 4×4 Bit multiplier circuit. (10)

Unit-IV

Q8 Explain design of Bus architecture using MUX. (10)

Q7 Design a RAM using VHDL. (10)

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END TERM EXAMINATION

FIFTH SEMESTER [B.TECH] NOVEMBER-DECEMBER 2018

Paper Code: IT-311

Subject: Digital Design Using VHDL

Time: 3 Hours

Maximum Marks: 75

Note: Attempt any five questions including Q no. 1 which is compulsory.

- Q1 (a) Explain the behavioral and structural modeling in VHDL. (4)
(b) Define signal and variables. (4)
(c) Explain the use of generic statement in VHDL. (4)
(d) What is process statement in VHDL? Explain. (4)
(e) What are function and procedure in VHDL? Explain. (4)
(f) What is operator overloading in VHDL? Explain. (5)
- Q2 (a) What are the different data types used in VHDL? Discuss. (6)
(b) Explain about different operator used in VHDL. (6.5)
- Q3 Write a VHDL code for- (12.5)
(a) Full Adder
(b) 4x1 multiplexer
(c) BCD to 7segment decoder
- Q4 Write the VHDL program for- (12.5)
(a) D-flip flop
(b) Synchronous counter
(c) 4 bit-Shift Register with PIPO
- Q5 (a) Write VHDL for arithmetic logic unit. (6)
(b) What are concurrent and sequential statement in VHDL? Explain. (6.5)
- Q6 (a) Explain the Moore and Mealy state models and give examples. (6)
(b) Write VHDL description of 4-bit carry look Ahead adder. (6.5)
- Q7 (a) Explain the following terms:- (6.5)
(i) State Machine
(ii) State diagram
(iii) State table
(iv) State Assignment
(b) Write VHDL behavioral model for 32-bit adder.
- Q8 (a) Explain the inertial and transport delay model in VHDL. (6)
(b) Write the behavioral model for 4x4 binary multiplier. (6.5)
- Q9 Explain the following:- (6.5)
(a) ASM chart
(b) SRAM design

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B/328

END TERM EXAMINATION

SIXTH SEMESTER [B.TECH./M.TECH.] MAY- JUNE 2016

Paper Code: IT-314

Subject: Digital System Design

Time: 3 Hours

Maximum Marks: 60

Note: Attempt any five questions including Q.no1 which is compulsory.

Q1 Attempt all:

- (a) Mention various types of functional modules used in RTL system. (3)
- (b) Differentiate between procedure and function. (3)
- (c) Explain implicit and explicit sequencing. (3)
- (d) Draw the stage graph for binary multiplier. (3)
- (e) Explain Block statement. (3)
- (f) Explain various signal attributes. (2)
- (g) Compare PAL and PLAs in short. (3)

Q2 (a) Explain the difference between combinational and sequential circuits in detail. (5)

(b) Explain Behavioral, Data Flow and structure modeling in detail. (5)

Q3 (a) Differentiate between sequential statement and concurrent statements. (5)

(b) Explain 4-bit multiplexer circuit using VHDL. (5)

Q4 (a) Design 4-bit up/down synchronous counter. (5)

(b) Explain Micro programmed controller. (5)

Q5 (a) Explain various components of RTL system. (5)

(b) Design and explain serial adder with accumulator. (5)

Q6 (a) Write a short note on field programming Gate Arrays. (FPGAs) Logic. (5)

(b) Explain Mealy and Moore Machine. (5)

Q7 (a) Explain micro-instruction sequencing. (5)

(b) Explain Mealy type FSM for serial adder. (5)

Q8 (a) Explain concept of overloading in detail. (5)

(b) Discuss manufacturing and functional Testing. (5)

Q9 (a) Differentiate between register array and RAM. Explain their generic architecture. (5)

(b) Explain Delta, Transport and inertial delay with example. (5)

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END TERM EXAMINATION

SIXTH SEMESTER [B.TECH] MAY-JUNE 2017

Paper Code: IT-314

Subject: Digital System Design

Time: 3 Hours

Maximum Marks: 60

Note: Attempt any five questions including Q. no. 1 which is compulsory.

- Q1 (a) What is the difference between sequential and combinational circuits?
Discuss. (3.5)
(b) Discuss the difference between array and records types. (3.5)
(c) What is the role of VHDL in circuit design? Discuss. (2)
(d) What is place and route tool? Discuss. (2)
(e) What are multiple signal drivers? Explain. (3.5)
(f) Write a VHDL code of 4 to 1 multiplexer using the case statement. (3.5)
(g) What is test bench? Explain. (2)
- Q2 (a) For a 2 to 4 decoder write down VHDL code using structural, data flow and behavioral modeling. (5)
(b) Discuss package and configuration used in VHDL. (5)
- Q3 (a) Explain resolution functions. Discuss with any example. (5)
(b) What is operator overloading in VHDL? Discuss. (5)
- Q4 For a D flip flop and T flip flop write down the VHDL code in behavioral modeling and structural modeling. (10)
- Q5 (a) For a 3 bit up/down counter write the VHDL code in data flow and structural modeling. (5)
(b) For a 4 bit serial in serial out register write down VHDL code in behavioral modeling. (5)
- Q6 (a) Write down the VHDL program for BCD to seven segment decoder in data flow modeling. (5)
(b) Discuss and explain the inertial and transport delay in VHDL. (5)
- Q7 (a) Discuss and explain the block statement with any example. (5)
(b) What are concurrent and sequential statements? Give examples. (5)
- Q8 (a) What are function and procedures? Discuss with examples. (5)
(b) What is generic? Show an example how a component can be made general with the use of generic. (5)
- Q9 Write short note on:-
(a) FPGA and CPLD (5)
(b) PLA and PAL (5)

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END TERM EXAMINATION

SIXTH SEMESTER [B.TECH] MAY- JUNE 2018

Paper Code: IT-314

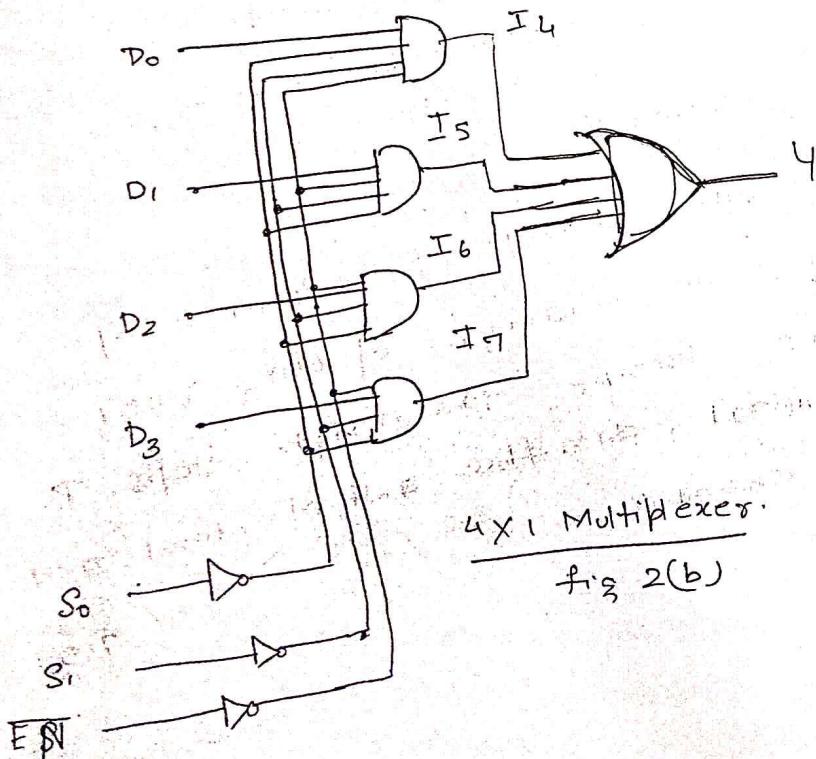
Subject: Digital System Design

Time: 3 Hours

Maximum Marks: 75

Note: Attempt any five questions including Q.no1 which is compulsory.

- Q1 (a) Explain the structure of VHDL module and basics.
(b) Write VHDL code for the serial adder circuit
(c) What is a test bench in VHDL.
(d) What is a vector? Give an example for VHDL
(e) Explain data flow and behavioural description in VHDL. (5x5=25)
- Q2 (a) Write VHDL model for a 4 to 1 multiplexer. (6)
(b) What are the advantages of using VHDL in digital design? Describe the design steps. Briefly explain behavioral, data flow and structural architecture bodies giving examples. (6.5)
- Q3 (a) Write VHDL code for a D Latch using variable assignment and signal assignment statements. With simulation waveforms clearly distinguish between the statements. (6)
(b) How do you assign delay to a signal assignment statement? Explain with an example in VHDL. (6.5)
- Q4 (a) For the multiplexer circuit of fig. write signal declaration and assignment statements in VHDL. Assume 10 n sec as propagation delay. Write your comments wherever it is applicable. (6.5)



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IT-314

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- (b) Explain how an object that has a width of more than 1 bit is declared in VHDL using vector data types. (6)
- Q5 (a) Write the block diagram and function table of a SRAM. Using these, write a VHDL description for 16x8 SRAM. (6.5)
 (b) Write a VHDL code for finding largest element of an array. (6)
- Q6 (a) Explain about inertial delay and Transport delay models in VHDL. (6.5)
 (b) Explain simulation? Explain about Gate level simulation, behavioural, simulation & functional. (6)
- Q7 (a) What is operator overloading? Explain. (6.5)
 (b) Describe functions in VHDL. (6)
- Q8 Write short notes on:-
 (a) Synthesis steps with flow chart. (4)
 (b) Discuss VHDL Package with example. (4)
 (c) Programmable logic Arrays (PLAs). (4.5)
- Q9 (a) Explain CPLD (6)
 (b) Discuss architecture of FPGA. (6.5)

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END TERM EXAMINATION

FIFTH SEMESTER [B.TECH/M.TECH] DECEMBER 2015-JANUARY 2016

Paper Code: IT-311

Subject: Digital Design Using VHDL

Time: 3 Hours

Maximum Marks: 60

Note: Attempt any five questions including Q.no.1 which is compulsory.

Select one question from each Unit.

Q1 Explain following in brief. Use block diagram when necessary.

- (a) Explain Gajski's 'Y' chart. (5)
- (b) Discuss delay in VHDL. (5)
- (c) Explain RTC. (5)
- (d) Define signal attribute to VHDL. (5)

Unit-I

Q2 (a) Design a 3:8 Decoder using VHDL. (4)

- (b) Design a 5:32 Decoder using a macro of 2:4 and 3:8 decoder with VHDL. (6)

Q3 (a) Design a full adder using VHDL. (4)

- (b) Design a 4-Bit Adder using a macro of full adder with Generate Statement. (6)

Unit-II

Q4 (a) Design a behavioral model of 3-Bit asynchronous counter. (5)

- (b) Differentiate between signal and variable. (5)

Q5 (a) Design a 4-Bit serial-in-serial-out shift Register. (5)

- (b) Design a S-R flip flop using VHDL. (5)

Unit-III

Q6 Design a 4-Bit serial Adder using VHDL. (10)

Q7 Explain state diagram of 4 x 4 Bit multiplier circuit. (10)

Unit-IV

Q8 Explain design of Bus architecture using MUX. (10)

Q7 Design a RAM using VHDL. (10)

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END TERM EXAMINATION

FIFTH SEMESTER [B.TECH/M.TECH] DECEMBER 2016 – JANUARY 2017

Paper Code: IT-311

Subject: Digital Design using VHDL

Time: 3 Hours

Maximum Marks: 60

Note: Attempt any five questions including Q.no. 1 which is compulsory.
Select one question from each Unit.

- Q1 (a) What is the difference between the literals $16 \# 23\text{ DF} \#$ and $X " 23\text{ DF}$. (2)
(b) Define attribute. (2)
(c) Define RTL. (2)
(d) Differentiate between procedure and function. (2)
(e) Explain following:
 (i) S' delayed (5 ns) (2)
 (ii) S' Last active (2)
 (iii) S' event (2)
 (iv) S' transduction (2)
(f) Compare signals and variables. (2)
(g) Draw circuit for carry ripple adder. (2)
(h) Explain implicit and explicit sequencing. (2)
(j) Write VHDL code for signed multiplier. (4)

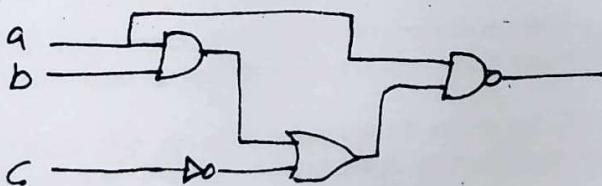
Unit-I

- Q2 (a) Explain Behanard, Data flow and structural modeling in detail. (5)
(b) Give VHDL code to design 4-bit binary up counter. (5)

Unit-II

- Q4 (a) Draw block diagram of 4-bit binary multiplier. Explain it. (5)
(b) Design 2:4 and 3:8 decoder circuit using VHDL. (5)

- Q5 (a) Write VHDL code for following circuit: (6)



- (b) Write a short note on field programming gate array logic. (FPGAs). (4)

Unit-III

- Q6 Design FSM of BCD counter. (10)

- Q7 (a) Explain Delta, Transport and initial delay with example. (5)
(b) Write short note on design of SRAM. (5)

Unit-IV

- Q8 (a) Explain micro instruction sequencing in brief. (5)
(b) Design half adder using VHDL code. How do you implement floating point adder circuit in VHDL. (5)

- Q9 (a) Explain Mealy-type FSH for serial adder. (5)
(b) Explain design of Arbiter. (5)

END TERM EXAMINATION

FIFTH SEMESTER [B.TECH/M.TECH] DECEMBER 2013

Paper Code: IT-311

Subject: Digital System Design
using VHDL

Time : 3 Hours

Maximum Marks :60

Note: Attempt any five questions, including Q.no.1 is compulsory. Select one question from each Unit.

- Q.No.1 (a) Discuss design flow and synthesis process in VHDL.
(b) What are the Moore and Mealy machines? Compare them. (5*4=20)
(c) What is process statement and how it is used in VHDL? Give example.
(d) What is a resolution function in VHDL? Discuss.
(e) What is port mapping? How port mapping is used in VHDL language?

UNIT-I

- Q. No. 2 (a) Discuss different data types used in VHDL? Explain with examples. (5)
(b) What is meant by operator overloading? Give an example. (5)
Q. No.3 Write VHDL codes for 2: 4 decoder and 4:1 multiplexer using behavioral modeling style. (10)

UNIT-II

- Q. No.4 Write down the truth table and VHDL code for the 4-bit up/down counter. Draw the circuit and output waveforms. (10)
Q. No.5 Write down the truth table and VHDL code for the 4-bit left to right shift register. Draw the circuit and output waveforms. (10)

UNIT-III

- Q. No.6. Write state table and draw the state diagram for D flip-flop, T flip flop, JK flip-flop. Also write the VHDL code for these flip-flops. (10)
Q. No.7 Design a clocked sequential circuit and that operates according to the given state table. Use D flip flops. Also write the VHDL code. (10)

Present state (AB)	Input (X)	Next state(AB)	Output (Y)
00	0	00	0
00	1	01	1
01	0	10	0
01	1	01	0
10	0	10	0
10	1	11	1
11	0	11	0
11	1	00	0

UNIT-IV

- Q. No. 8 (a) Explain the inertial and transport delay model in VHDL.. (5)
(b) How can a multiplier circuit be defined in synthesis? (5)
Q. No.9 Explain in detail the ASM technique of designing a sequential circuit. (10)

END TERM EXAMINATION

FIFTH SEMESTER [B.TECH] NOVEMBER-DECEMBER 2018

Paper Code: IT-311
Time: 3 Hours

Subject: Digital Design Using VHDL

Maximum Marks: 75

Note: Attempt any five questions including Q no. 1 which is compulsory.

- Q1 (a) Explain the behavioral and structural modeling in VHDL. (4)
(b) Define signal and variables. (4)
(c) Explain the use of generic statement in VHDL. (4)
(d) What is process statement in VHDL? Explain. (4)
(e) What are function and procedure in VHDL? Explain. (4)
(f) What is operator overloading in VHDL? Explain. (5)
- Q2 (a) What are the different data types used in VHDL? Discuss. (6)
(b) Explain about different operator used in VHDL. (6.5)
- Q3 Write a VHDL code for- (12.5)
(a) Full Adder
(b) 4x1 multiplexer
(c) BCD to 7segment decoder
- Q4 Write the VHDL program for- (12.5)
(a) D-flip flop
(b) Synchronous counter
(c) 4 bit-Shift Register with PIPO
- Q5 (a) Write VHDL for arithmetic logic unit. (6)
(b) What are concurrent and sequential statement in VHDL? Explain. (6.5)
- Q6 (a) Explain the Moore and Mealy state models and give examples. (6)
(b) Write VHDL description of 4-bit carry look Ahead adder. (6.5)
- Q7 (a) Explain the following terms:- (6)
(i) State Machine
(ii) State diagram
(iii) State table
(iv) State Assignment
(b) Write VHDL behavioral model for 32-bit adder. (6.5)
- Q8 (a) Explain the inertial and transport delay model in VHDL. (6)
(b) Write the behavioral model for 4x4 binary multiplier. (6.5)
- Q9 Explain the following:- (6)
(a) ASM chart
(b) SRAM design (6.5)

END TERM EXAMINATION

FIFTH SEMESTER [B.TECH./M.TECH.] - DECEMBER 2010

Subject: Digital System Design Using VHDL

Paper Code: IT311

Paper ID: 15311

Time : 3 Hours

Maximum Marks : 60

Note: Attempt any five questions including Q.1 which is compulsory.

- Q1 (a) What is Behavioral and structural modeling? Give example using Full subtractor.
(b) Give the declaration and specification of user defined attributes. Give an example using enumerated encoding.
(c) Compare Moore and Melay state model. Give example using a serial adder.
(d) What is GENERIC? Design a generic parity detector.
(e) Give the VHDL code for designing signed comparator. (4x5=20)
- Q2 (a) Which standard gave standardization to VHDL language? Give the summary of VHDL design synthesis using a block diagram. (3)
(b) Give VHDL code for binary to grey code converter. (4)
(c) Compare Array, Port array and Records. Give VHDL code in support of your statements. (3)
- Q3 (a) Can addition between data type of BIT is possible? How do you allow addition between value of type BIT_VECTOR? Explain by giving example. Use the same technique to add an integer to a binary 1 bit number. Give VHDL code for the same. (4)
(b) Design and implement an Arithmetic logic unit using multiplexer. Write the VHDL code for it. (6)
- Q4 (a) What is PROCESS? Design a DFF using PROCESS. (2)
(b) Write VHDL code for 8-bit unsigned carry ripple adder. (6)
(c) Explain the role of GENERATE statement in VHDL. (2)
- Q5 (a) Compare Inertial Delay, delta delay and Transport delay. Give example. (3)
(b) Design a circuitry for a RAM with separate input output data buses. Give VHDL code for the implementation. (7)
- Q6 Write VHDL program for any two of the following;-(5+5)
(a) Signed Multiplier
(b) 8-bit register
(c) Floating point adder
(d) BCD counter
- Q7 Using the FSM approach design a traffic light controller. Assume that a 60Hz clock is available. (10)

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END TERM EXAMINATION

FIFTH SEMESTER [B.TECH./M.TECH.] DECEMBER 2014- January 2015

Paper Code: IT311

Subject: Digital Design Using VHDL

Time : 3 Hours

Maximum Marks :60

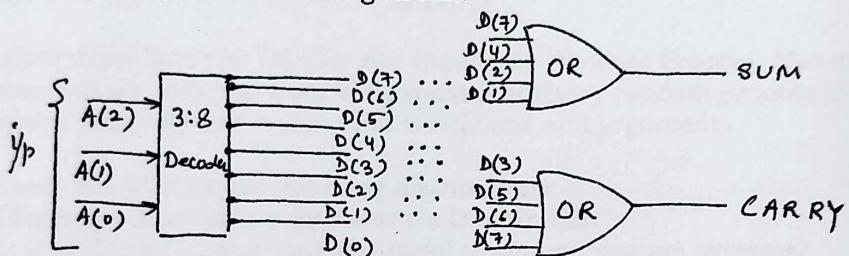
**Note: Attempt any five questions including Q.no. 1 which is compulsory.
Select one question from each unit.**

- Q1 (a) Briefly outline the purpose of following VHDL modeling constructs:-
(i) Entity Declaration (ii) Process statement
(b) Write variable declaration for a counter, initialized to 0; a status flag used to indicate whether a module is busy and a standard-logic value used to store a temporary results.
(c).Write a Wait Statement that suspends a process until a signal "ready" changes to '1' or until a maximum of 5ms has elapsed.
(d) Define state machine. (5x4=20)

UNIT-I

- Q2** (a) Write a VHDL code for following circuit:-

(5)



- (b) Write an entity declaration and a behavioural architecture body for a two-input multiplexer with input parts 'a', 'b' and 'set' and an output port 'z'. If the set input is '0' the value of 'a' should be copied to 'z', otherwise the value of 'b' should be copied to 'z'. Write a VHDL code to implement the circuit. (5)

OR

- Q3** (a) Explain Generic and blocks construct.
 (b) Design an 8:1 MUX using with-select statement.

UNIT-II

- Q4 (a) Write an 'if' statement that sets a variable 'odd' to '1' if an integer 'n' is odd, or to '0' if it is even. (5)
(b) Write a loop statement that samples a bit input 'd' when a clock input 'clk' changes to '1'. So long as 'd' is 'zero', the loop continues executing. When 'd' is '1' the loop exits. (5)

OR

- Q5 (a) Differentiate between signal and variable. (5)
 (b) Design a binary asynchronous counter. (5)

UNIT-III

- Q6** Design and explain serial Adder using FSM. **(10)**

OR

- Q7 Explain RTL.** (10)

UNIT-IV

- Q8** Design and explain Shift-And-Add Multiplier. **(10)**

OR

- Q9** Explain Delta, Inertial and transport delay with example. (10)

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END TERM EXAMINATION

FIFTH SEMESTER [B.TECH./M.TECH.] DECEMBER 2019

Paper Code: IT-311

Subject: Digital Design Using VHDL

Time : 3 Hours

Maximum Marks :75

Note: Attempt any five questions including Q.no.1 which is compulsory.

- | | | |
|----|-------------------------------------------------------------------------------------------------------|-------|
| Q1 | a) Differentiate between procedure & function. | (3) |
| | b) Define RTL. | (3) |
| | c) Write constant declaration for the number of bits in a 32-bit word and for the number π (3.14) | (3) |
| | d) Explain implicit and explicit sequencing. | (3) |
| | e) What is the difference between 16# 23DF# and X "23DF". | (3) |
| | f) Differentiate between signal and variable. | (3) |
| | g) Define attribute. | (3) |
| | h) Compare between PAL & PLA structure. Give their application. | (4) |
| Q2 | a) Give VHDL code to design 4 bit binary up counter. | (6.5) |
| | b) Explain behavioral, Data flow and structural modeling in detail. | (6) |
| Q3 | a) Design 3:8 decoder circuit with VHDL. | (6.5) |
| | b) Explain delta, transport & Inertial delay with example. | (6) |
| Q4 | a) Explain Mealy and Moore Machine. | (4) |
| | b) Explain Block statement. | (4) |
| | c) Draw state graph for binary multiplier. | (4.5) |
| Q5 | a) Write VHDL code for following circuit | (6.5) |
| | | |
| Q6 | a) Design Half Adder using VHDL. | (6.5) |
| | b) Discuss design of data control sub system. | (6) |
| Q7 | a) What is micro-programmed controller. Explain structure of micro-programmed controller in brief. | (6.5) |
| | b) Explain micro instruction sequencing in brief. | (6) |
| Q8 | a) Design 4 bit multiplexer circuit using VHDL. | (6.5) |
| | b) Design and explain serial adder with accumulator. | (6) |
| Q9 | Write short note: | (4) |
| | a) EDA tools. | (4) |
| | b) Concept of operator overloading. | (4.5) |
| | c) VHDL data types. | (4.5) |

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END TERM EXAMINATION

FIFTH SEMESTER [B.TECH.] DECEMBER 2017

Paper Code: IT-311

Subject: Digital Design Using VHDL

Time: 3 Hours

Maximum Marks: 60

Note: Attempt five questions including Q.No1, which is compulsory. Assume missing data if any:-.

- Q1 (a) Discuss data types of VHDL. (5x4=20)
(b) Differentiate between signal and variable.
 (i) Define RTL.
(d) Differentiate between delta, Inertial and Transport delay.
e) Explain the process statement with example.
- Q2 (a) Design 5:32 Decoder using a macro of 2:4 and 3:8 decoder. (7)
(b) What is operator overloading? Discuss. (3)
- Q3 (a) Explain Gajski 'Y' chart. (5)
(b) Design a 4-Bit adder using a component of full adder. (5)
- Q4 a) Design a 4-Bit up/down Binary Counter using VHDL. (5)
b) Write VHDL Code for D and T flip flops. (5)
- Q5 a) Design an universal shift Register using VDHL. (5)
b) Write VHDL Code for 3 to 8 decoder. (5)
- Q6 a) Design a FSM of 4-Bit Serial adder. (5)
b) Write VHDL code for 8x1 multiplexer. (5)
- Q7 Explain: - (10)
(i) State Table
(ii) State diagram
(iii) Mealy model
(iv) Moore model
- Q8 a) Design a FSM of shift-and-add multiplier (5)
b) What are various operators used in VHDL? Discuss. (5)
- Q9 a) Design a SRAM using VHDL. (5)
b) What are sequential and concurrent statement? Explain. (5)

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END TERM EXAMINATION

FIFTH SEMESTER [B.TECH.] DECEMBER 2017

Paper Code: IT-311

Subject: Digital Design Using VHDL

Time: 3 Hours

Maximum Marks: 75

Note: Attempt five questions including Q.No1, which is compulsory. Assume missing data if any:-.

- Q1 (a) Discuss data types of VHDL. (5x5=25)
(b) Differentiate between signal and variable.
(c) Define RTL.
(d) Differentiate between delta, Inertial and Transport delay.
e) Explain the process statement with example.
- Q2 (a) Design 5:32 Decoder using a macro of 2:4 and 3:8 decoder. (8)
(b) What is operator overloading? Discuss. (4.5)
- Q3 (a) Explain Gajski 'Y' chart. (6)
(b) Design a 4-Bit adder using a component of full adder. (6.5)
- Q4 a) Design a 4-Bit up/down Binary Counter using VHDL. (6.5)
b) Write VHDL Code for D and T flip flops. (6)
- Q5 a) Design an universal shift Register using VDHL. (6.5)
b) Write VHDL Code for 3 to 8 decoder. (6)
- Q6 a) Design a FSM of 4-Bit Serial adder. (6)
b) Write VHDL code for 8x1 multiplexer. (6.5)
- Q7 Explain: - (12.5)
(i) State Table
(ii) State diagram
(iii)Mealy model
(iv)Moore model
- Q8 a) Design a FSM of shift-and-add multiplier (6)
b) What are various operators used in VHDL? Discuss. (6.5)
- Q9 a) Design a SRAM using VHDL. (6)
b) What are sequential and concurrent statement? Explain. (6.5)

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