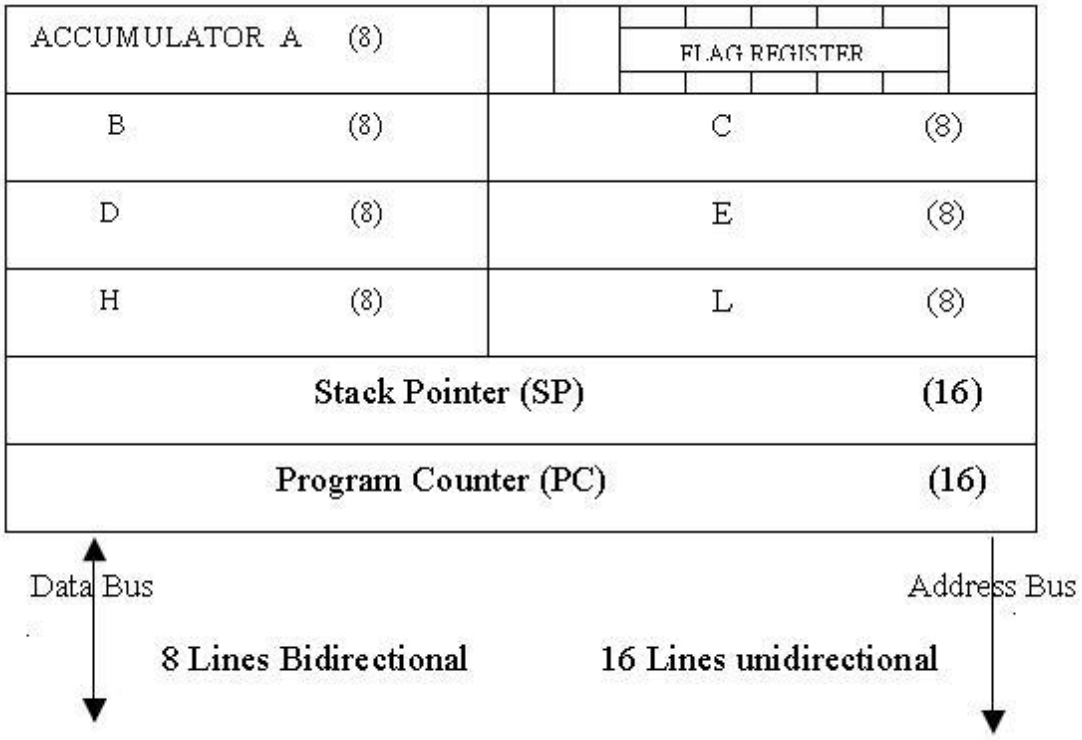
Draw the programming model of 8085

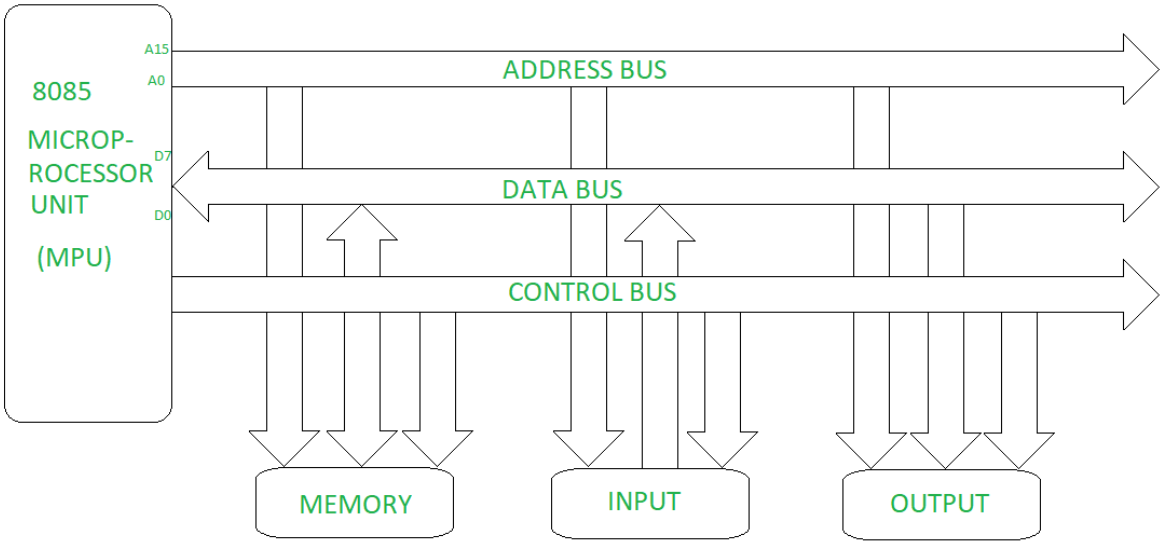


Mention the size of address bus and data bus in a) 4004 b) Pentium 4

Microprocessor	Address Bus Size	Data Bus Size
Intel 4004	12 bits	4 bits
Pentium 4	36 bits	64 bits

Explain the 8085 Bus structure

- **Address bus:** The address bus is a 16-bit bus that is used to specify the memory location or I/O device with which the microprocessor wants to communicate. It is unidirectional, which means that data can only flow from the microprocessor to the memory or I/O device.
- **Data bus:** The data bus is an 8-bit bus that is used to transfer data between the microprocessor and the memory or I/O device. It is bidirectional, which means that data can flow in both directions between the microprocessor and the memory or I/O device.
- **Control bus:** The control bus is used to manage the data transfer between the microprocessor and the memory or I/O device. These signals indicate the type of data transfer that is being performed, such as read, write, or interrupt.

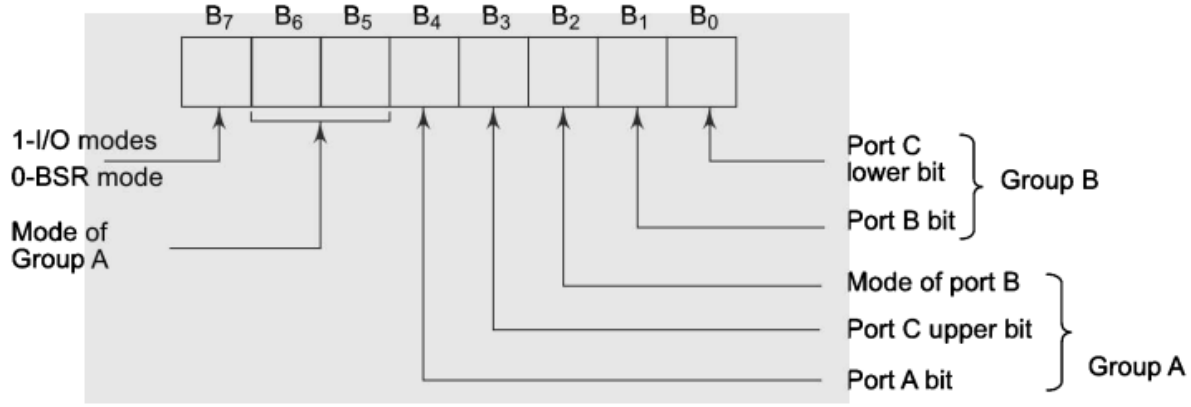


Bus organization system of 8085 Microprocessor

How does 8086 differentiate between and opcode and instruction data

The 8086 microprocessor differentiates between an opcode and instruction data by the number of bytes that are fetched from memory. The opcode is always 1 byte long, while the instruction data can be 1, 2, or 3 bytes long. The number of bytes that are fetched is determined by the opcode itself.

Explain the control word format of 8255 in I/O and BSR mode



Group A modes

B_6	B_5	Mode
0	0	mode 0
0	1	mode 1
1	0	mode 2
1	1	x

(i) Port B mode is either 0 or 1 depending upon B2 bit.

(ii) A port is an output port if the port bit is 0 else it is input port

Fig. 5.18(b) *I/O Mode Control Word Register Format*

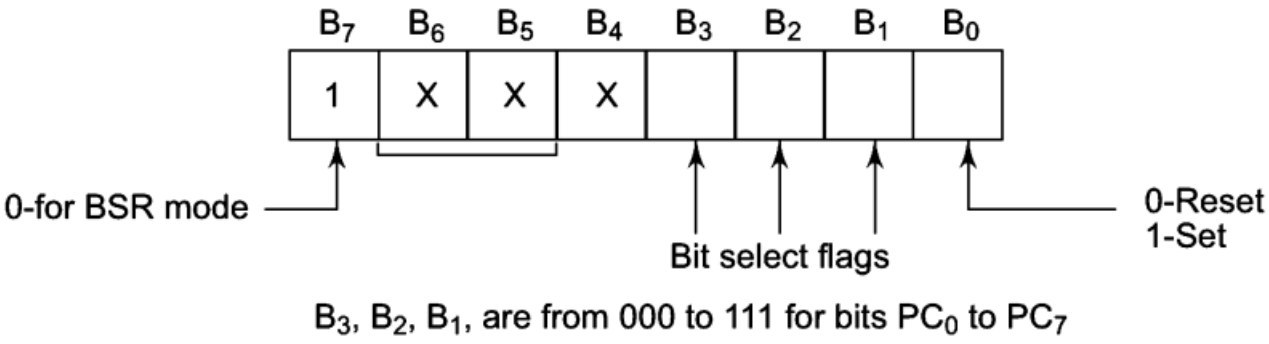


Fig. 5.18(a) *BSR Mode Control Word Register Format*

Elaborate the dedicated need of Keyboard/Display controller with 8086

The 8086 microprocessor does not have any built-in support for keyboard or display devices. This means that in order to use these devices, the microprocessor needs to be interfaced with a dedicated keyboard/display controller. There are three main reasons:

1. The keyboard and display devices are very different from each other.
2. The keyboard and display devices are very fast.
3. The keyboard and display devices are often used simultaneously.

Describe any two Flag manipulations and machine control instructions of 8086

- **LAHF** − Used to load AH with the low byte of the flag register.
- **SAHF** − Used to store AH register to low byte of the flag register.

- **STC** − Used to set carry flag CF to 1
- **CLC** − Used to reset carry flag CF to 0

What is the significance of DAA instruction? Explain with the help of an example

The DAA (Decimal Adjust After Addition) instruction is used to adjust the result of an addition operation that involves BCD numbers. The DAA instruction is significant because it ensures that the result of the addition operation is always a valid BCD number.

Example:

MOV AL, 01H

ADD AL, 02H

DAA

Explain the function of following signals a) TEST b) NMI c) HLDA d) INTR

TEST: The 8086 enters into a wait state after execution of the WAIT instruction until a LOW signal on the TEST pin.

NMI: It is a positive edge triggered nonmaskable interrupt request.

HLDA: On receiving HOLD signal processor outputs HLDA signal HIGH as an acknowledgement.

INTR: It is a level triggered maskable interrupt request.

Explain physical address formation in 8086

The contents of the CS register are multiplied by 16 and then the offset is added to generate physical address.

Example:

If code segment is 1234H and offset address is 0002H then find physical address.

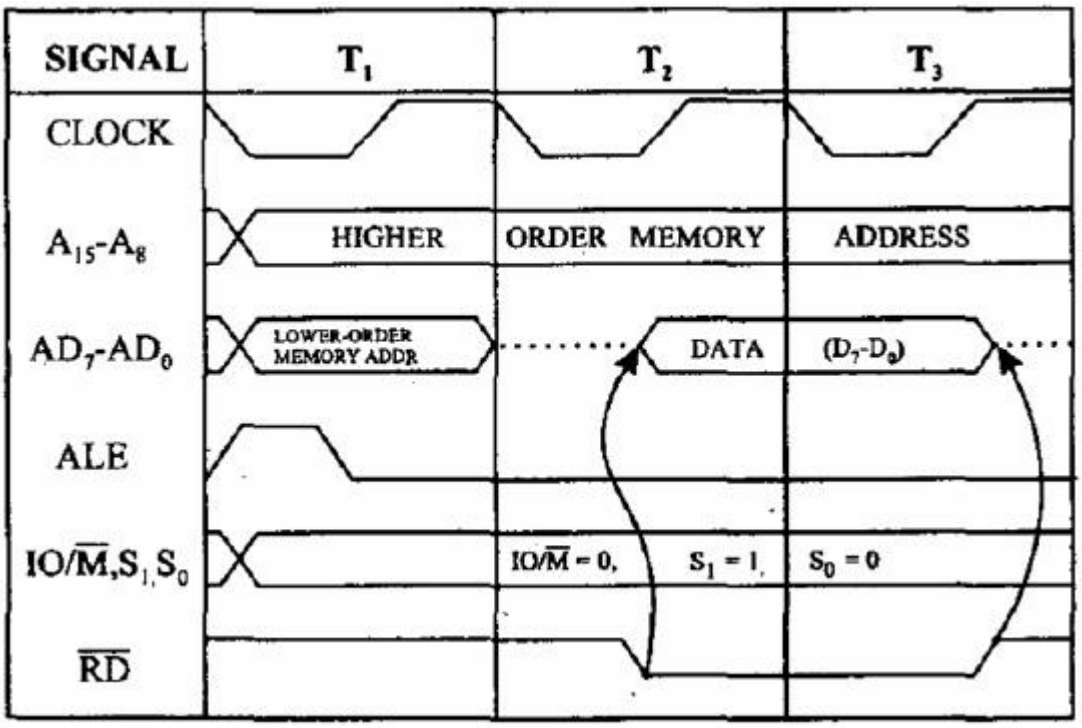
Physical Address = CS×10H+OA

=1234H×10H+ 0002H

= 12340H + 0002H

= 12342H

Draw and explain Memory Read timing diagram of 8085



Explain any six processor control instructions of 8086

- **STC** − Used to set carry flag CF to 1
- **CLC** − Used to clear carry flag CF to 0
- **STD** − Used to set the direction flag DF to 1
- **CLD** − Used to clear the direction flag DF to 0
- **STI** − Used to set the interrupt enable flag to 1
- **CLI** − Used to clear the interrupt enable flag to 0

Write a program to find out the number of positives and negatives numbers from a given series of signed numbers

```
ASSUME CS:CODE, DS:DATA
DATA SEGMENT
LIST DW 2579H, 0A500H, 0C009H, 0159H, 0B900H
COUNT EQU 05H
DATA ENDS
CODE SEGMENT
START:      XOR BX, BX
            XOR DX, DX
            MOV AX, DATA
            MOV DS, AX
            MOV CL, COUNT
            MOV SI, OFFSET LIST
AGAIN:      MOV AX, [SI]
            SHL AX, 01
            JC NEG
            INC BX
            JMP NEXT
NEG:        INC DX
NEXT:       ADD SI, 02
            DEC CL
            JNZ AGAIN
            MOV AH, 4CH
            INT 21H
            CODE ENDS
            END START
```

Write a program to perform one byte BCD addition

```
ASSUME CS:CODE, DS:DATA
DATA SEGMENT
            OPR1 EQU 92H
            OPR2 EQU 52H
RESULT DB 02 DUP(00)
DATA ENDS

CODE SEGMENT
START:      MOV AX, DATA
            MOV DS, AX
            MOV BL, OPR1
            XOR AL, AL
            MOV AL, OPR2
            ADD AL, BL
            DAA
            MOV RESULT, AL
            JNC MSBO
            INC [RESULT+1]
MSBO:       MOV AH, 4CH
            INT 21H
CODE ENDS
END START
```

Explain the architecture of Numeric processor 8087

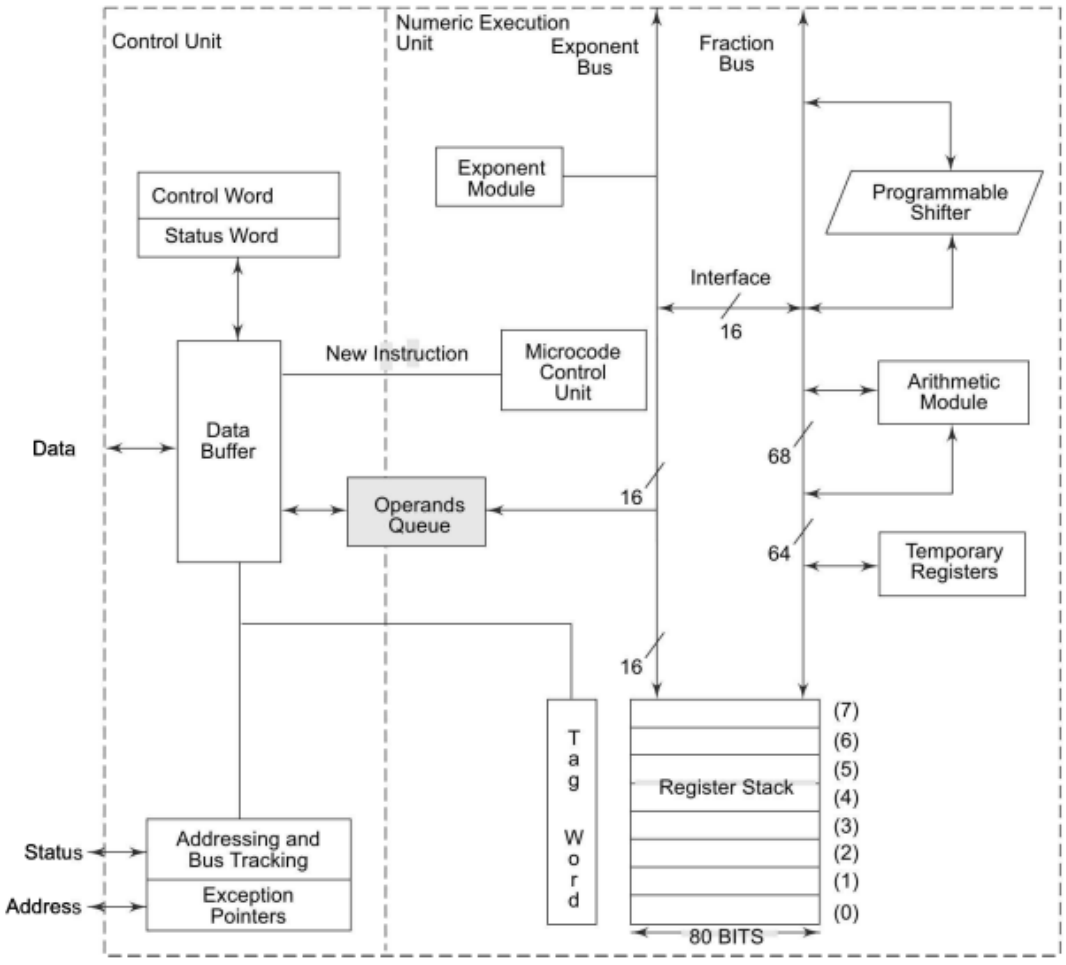


Fig. 8.12(a) *8087 Architecture*

Write short note on Paging in 80386

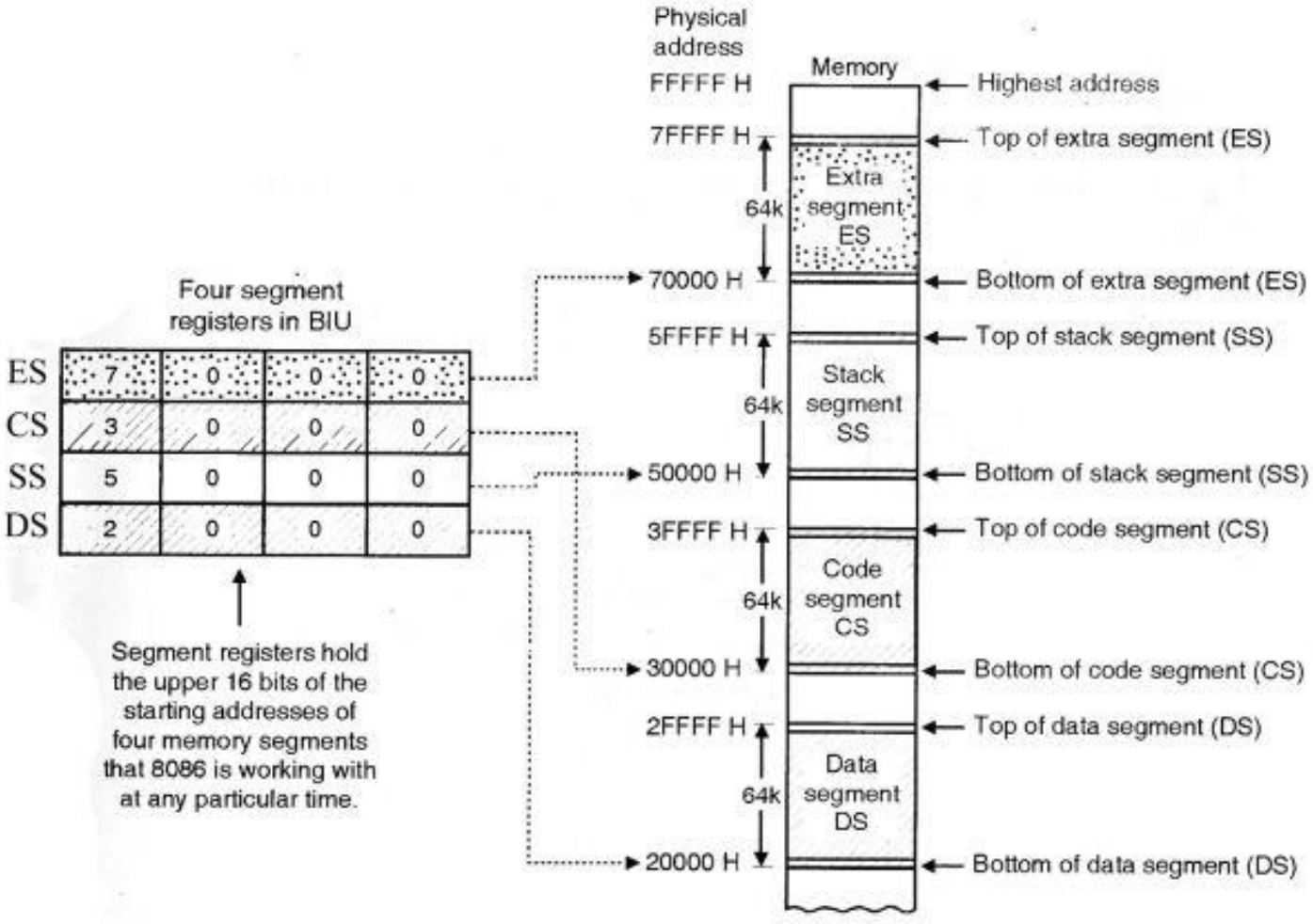
Paging divides the memory into fixed-size pages. The main advantage of the paging system is that it is not required in the complete segment of a task in the physical memory at any time. But only some required pages of the segments should he available in the physical memory for the execution. Subsequently, the memory requirement for the specified task has been reduced, and the CPU can use the available memory for other tasks. The paging technique can be used to manage the physical memory for multitasking operating systems.

Explain the stack structure of 8086 in detail

1. The CS register holds the upper 16-bits of the starting address of the segment from which the BIU is currently fetching the instruction code byte.

2. The SS register is used for the upper 16-bits of the starting address for the program stack

3. ES register and DS register are used to hold the upper 16-bits of the starting address of the two memory segments which are used for data.



Write short note on Protected Virtual addressing mode in 80286

The 80286 executes a fully upward-compatible superset of the 8086 instruction set in protected virtual address mode. The PVAM operation of the 80286 processor provides memory management and protection mechanisms and associated instructions. This operating mode also provides extended physical and virtual memory address space, memory protection mechanisms and new operations to support operating systems and virtual memory.

What is the interrupt vector table of 8086? Explain its structure

In an Interrupt Structure of 8086, the first 1 KB of memory from 00000H to 003FFH is reserved for storing the starting addresses of interrupt service routines. This block of memory is called the **Interrupt Vector Table.**

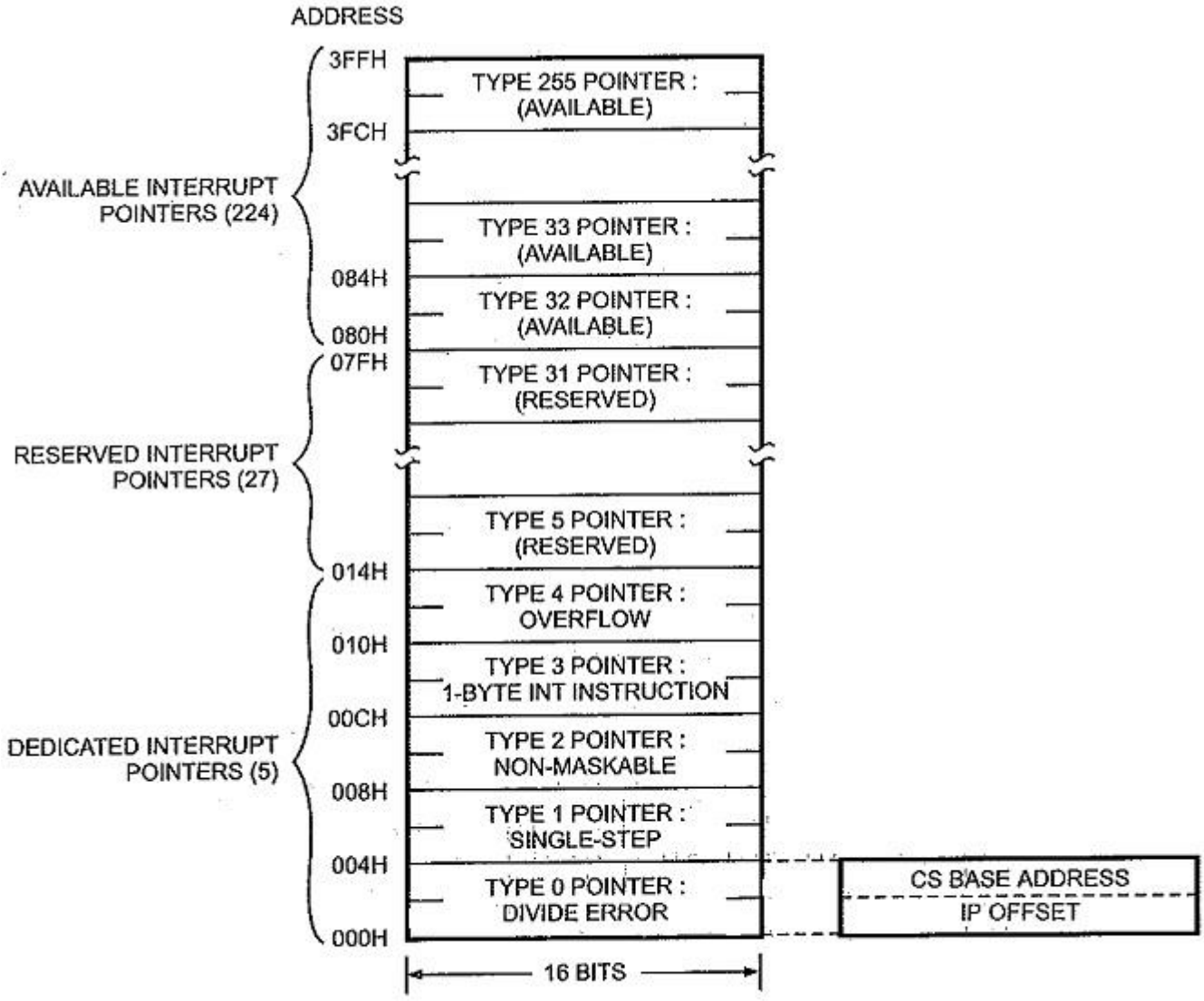


Fig. 9.2 8086 interrupt vector table

Define MACRO. State difference between MACRO and Subroutine

A macro is a set of instructions that are stored as a single instruction. Macros are used to simplify programming by allowing programmers to define frequently used code snippets.

Macro	Subroutine
A set of instructions that are stored as a single instruction.	A named section of code that can be called from other parts of the program.
The macro's code is expanded inline when it is invoked.	The subroutine's code is called by name
Does not return control to the calling program.	Returns control to the calling program

Draw the block diagram for the internal architecture of 8257