Give an example of one address Microprocessor.

8085 is a one address microprocessor.

Which stack is used in 8085?

The 8085 microprocessor uses a LIFO (Last In First Out) stack to store data during program execution.

After power on at what absolute address 8086 starts execution.

After power on, the 8086 microprocessor starts execution at physical address FFFF0h.

What is called "Scratch pad of Pentium microprocessor".

MMX(Multi-Media Extensions) registers is called the "scratch pad of the Pentium microprocessor".

Which mode of 8255 is suitable for interfacing parallel printer and keyboard?

Mode 2 of the 8255 is suitable for interfacing parallel printer and keyboard.

Which mode of 8254 is suitable for generating square wave ?

Mode 3 of the 8254 is suitable for generating square wave.

How many keys and characters displays is possible in 8279.

Mode	Keys	Characters
Display Scan	64	16
Display Entry	64	8

8086 microprocessor is interfaced to 8254. What is the maximum number which the clock frequency on one of the times is divided?

The 8254 programmable interval timer (PIT) can divide the clock frequency on one of the timers by a maximum of 65,535.

How many bit combinations are there in a word?

Word Size	Number of Bit Combinations

8 bits	2^8
16 bits	2^16
32 bits	2^32
64 bits	2^64

What is the function of "NOP"

NOP (No Operation) is used:

- to insert a delay into a program
- to ensure that a piece of code is aligned on a memory boundary.
- to prevent pipeline hazards.
- to debug a program

Why crystal is preferred clock source?

Crystal is preferred as a clock source due to:

- **High stability:** Crystal oscillators are very stable
- **Low phase noise:** Crystal oscillators also have low phase noise
- **Small size:** Crystal oscillators are relatively small and lightweight
- **Low cost:** Crystal oscillators are relatively inexpensive

What is the purpose for which the signal "Ready" is available in 8085 and 8086?

The READY signal in 8085 and 8086 is used to indicate that the device is ready to send or receive data. If READY is low, then the CPU has to wait for READY to go high. It allows the CPU to interface with slow devices and prevent data corruption.

What is the operation performed by instruction "CBW of 8086. Give an example for its use.

The CBW instruction in 8086 is a **byte to word** conversion instruction. The CBW instruction is a useful instruction for converting between byte and word values. It is also a necessary instruction for using the IDIV instruction with negative values.

What is the use of 8251?

The 8251 is a Universal Synchronous/Asynchronous Receiver/Transmitter (USART).

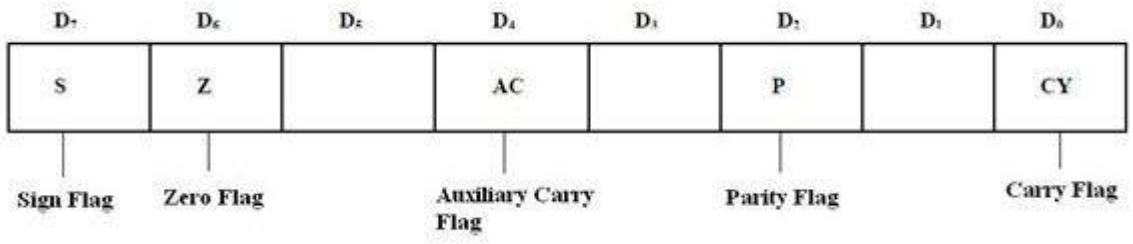
The 8251 can be used in a variety of applications, including:

- **Serial communication:** The 8251 can be used to communicate with other devices over a serial link. This can be used for a variety of purposes, such as transferring data between devices, controlling peripherals, and debugging software.
- **Modem control:** The 8251 can be used to control modems. This can be used for a variety of purposes, such as dialing phone numbers, sending and receiving data, and controlling modem features.
- **UART emulation:** The 8251 can be used to emulate a Universal Asynchronous Receiver/Transmitter (UART). This can be used to interface with devices that expect to communicate with a UART, such as serial terminals and microcontrollers.

What is PSW in 8085? Explain the contents of PSW

The Program Status Word (PSW) in 8085 is a 16-bit register that contains the status of the CPU. It is divided into two parts: Accumulator (A) and Flag register.

The Accumulator is an 8-bit register that stores the current value of the accumulator. The Flag register is an 8-bit register that contains the status flags of the CPU.



1) **Carry flag(CF):** This flag is set whenever there has been a carry out of, or a borrow into, the higher order bit of the result.

2) **Parity flag(PF):** This flag is set whenever the result has even parity, an even number of 1 bits. If parity is odd, PF is cleared.

3) **Auxiliary Carry flag(AF):** This flag is set whenever there has been a carry out of the lower nibble into the higher nibble or a borrow from higher nibble into the lower nibble of an 8-bit quantity, else AF is reset.

4) **Zero flag(ZF):** This flag is set, when the result of operation is zero, else it is reset.

5) **Sign flag(SF):** This flag is set, when MSB (Most Significant Bit) of the result is 1.

How "BIU" of 8086 generate 20-bit address to access external memory

Generation of 20-bit Address: The contents of the CS register are multiplied by 16 i.e., shifted by 4 position to the left by inserting 4 zero bits and then the offset i.e. the contents of IP register are added to the shifted contents of CS to generate physical address.

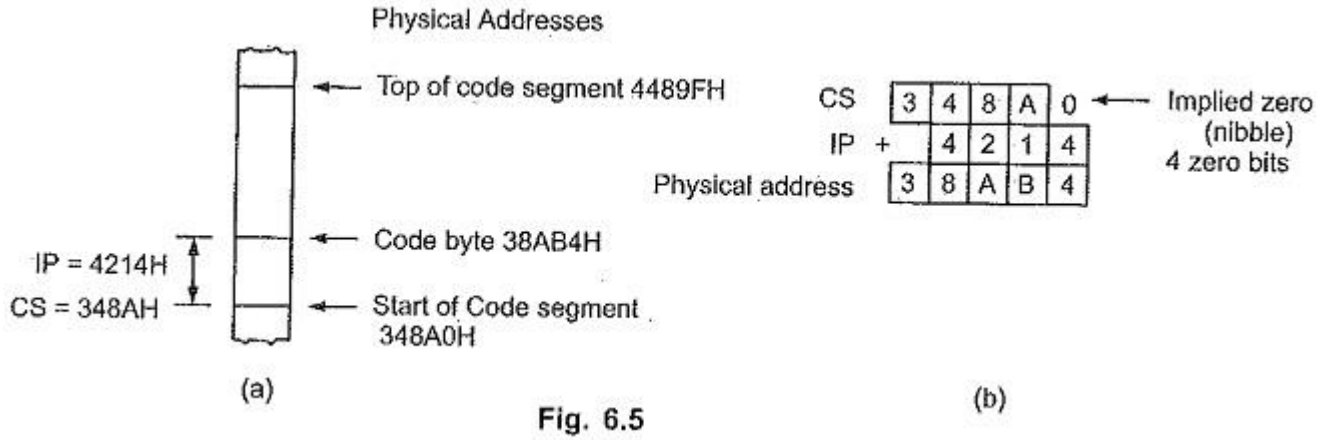


Fig. 6.5

Describe the pipelined architecture of 8086.

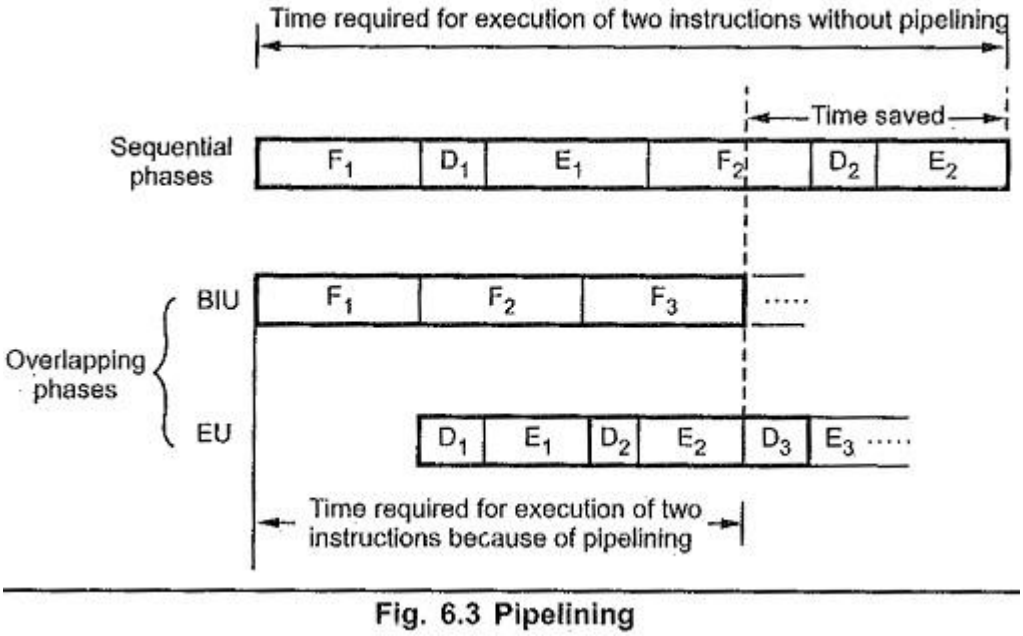


Fig. 6.3 Pipelining

To speed up program execution, the BIU fetches **six instruction bytes** ahead of time from the memory. These prefetched instruction bytes are held for the execution unit in a group of registers called **Queue**. The BIU continues this process as long as the queue is not full. Due to this, execution unit gets the ready instruction in the queue and instruction fetch time is eliminated. Feature of fetching the next instruction while the current instruction is executing is called **pipelining**.

Discuss the segment memory concept used in 8086

The physical address of the Internal Architecture of 8086 is 20-bits wide to access 1 Mbyte memory locations. However, its registers and memory locations which contain logical addresses are just 16-bits wide. Hence 8086 uses memory segmentation. It treats the 1 Mbyte of memory as divided into segments, with a maximum size of a segment as 64 Kbytes. Thus any location within the segment can be accessed using 16 bits.

For the selection of the four active segments the 16-bit segment registers are provided within the BIU of the 8086. These four registers are:

Code segment (CS) register, the data segment (DS) register, the stack segment (SS) register, and the extra segment (ES) register.

1. The **CS register** holds the upper 16-bits of the starting address of the segment from which the BIU is currently fetching the instruction code byte.
2. The **SS register** is used for the upper 16-bits of the starting address for the program stack (all stack related instructions will operate on stack)
3. **ES register and DS register** are used to hold the upper 16-bits of the starting address of the two memory segments Which are used for data.

What is the purpose of "ALE" BHE, DT/R and DEN pins of 8086? Show their timing in the system bus cycle of 8086?

ALE (Address Latch Enable): This signal is provided by 8086 to demultiplex the AD_0-AD_{15} into A_0-A_{15} and D_0-D_{15} using external latches.

BHE/S_7: BHE (Bus High Enable): Low on this pin during first part of the machine cycle, indicates that at least one byte of the current transfer is to be made on higher order byte AD_{15}-AD_8; otherwise the transfer is made on lower order byte AD_7-AD_0.

DT/R (Data Transmit/Receive): This signal is used to control data flow direction. High on this pin indicates that the 8086 is transmitting the data and low indicates that the 8086 is receiving the data.

DEN (Data Enable): This signal informs the transceivers that the CPU is ready to send or receive data

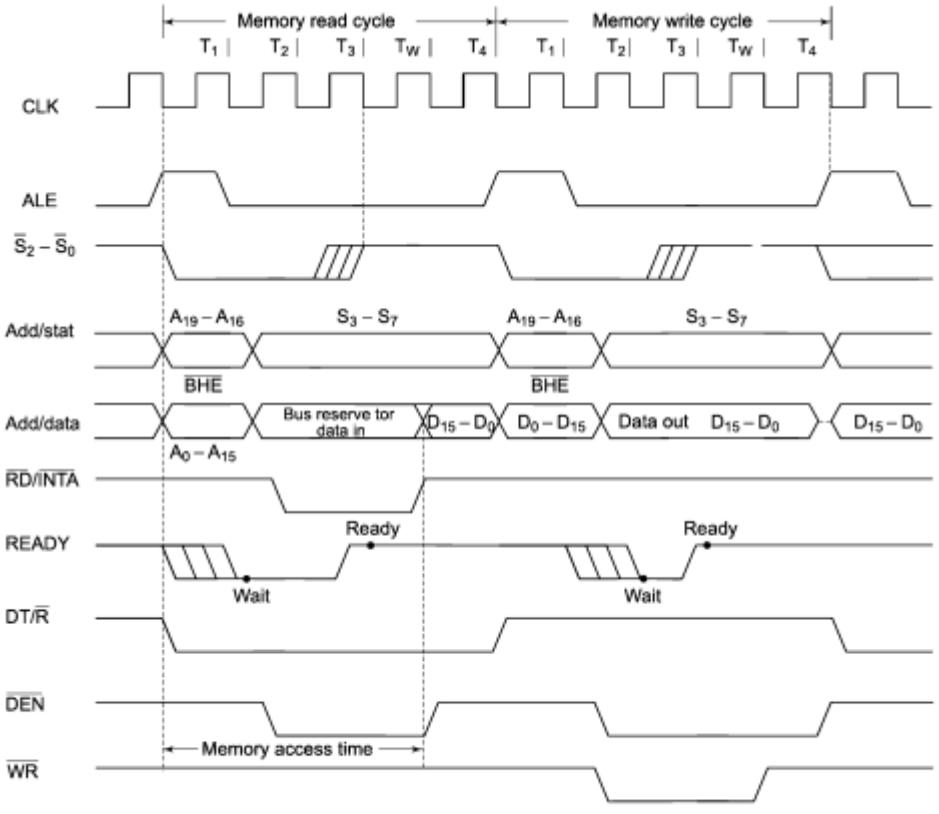


Fig. 1.8 *General Bus Operation Cycle of 8086*

Give the instruction sequence that compares the first 10 bytes beginning at STRG1 with the first ten bytes beginning at STRG2 and branches to MATCH if they are equal, otherwise continues in sequence?

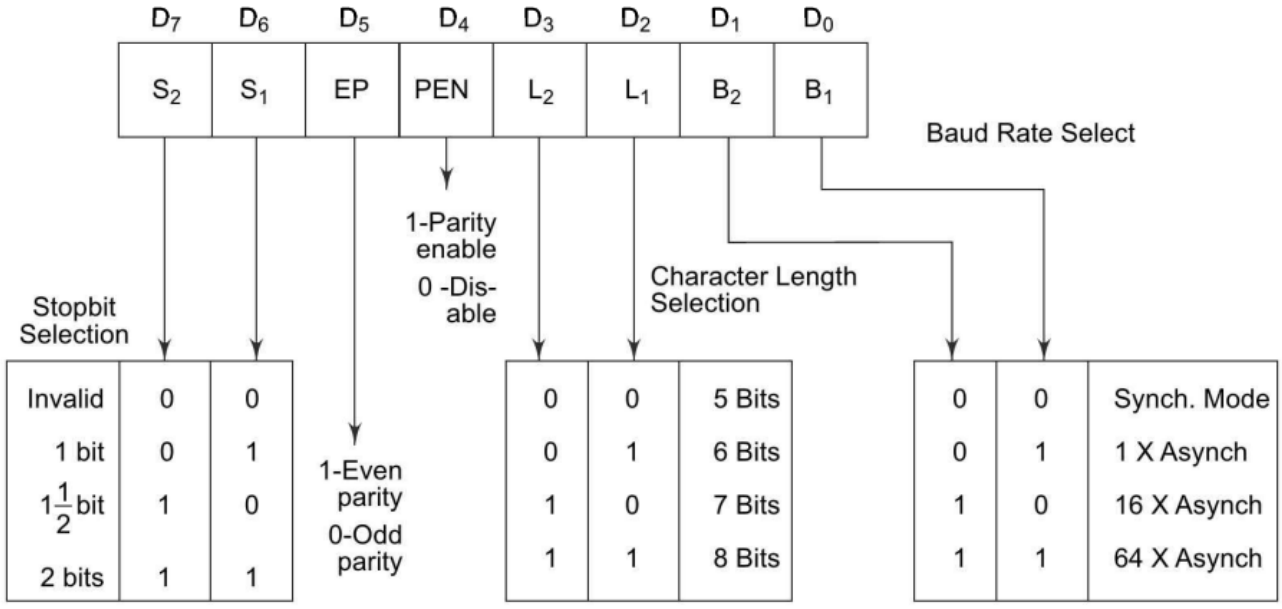
```
MOV AX, OFFSET STRG1
MOV BX, OFFSET STRG2
MOV CX, 10

LOOP:
MOV AL, [AX]
CMP AL, [BX]
JE MATCH
INC AX
INC BX
LOOP LOOP
```

Describe tightly coupled and loosely coupled systems with examples

Loosely Coupled	Tightly Coupled
There is distributed memory in loosely coupled multiprocessor system.	There is shared memory, in tightly coupled multiprocessor system.
Loosely Coupled Multiprocessor System has low data rate.	Tightly coupled multiprocessor system has high data rate.
The cost of loosely coupled multiprocessor system is less.	Tightly coupled multiprocessor system is more costly.
In loosely coupled multiprocessor system, modules are connected through **Message transfer system** network.	While there is PMIN, IOPIN and ISIN networks.
In loosely coupled multiprocessor, Memory conflicts don’t take place.	While tightly coupled multiprocessor system have memory conflicts.
Loosely Coupled Multiprocessor system has low degree of interaction between tasks.	Tightly Coupled multiprocessor system has high degree of interaction between tasks.

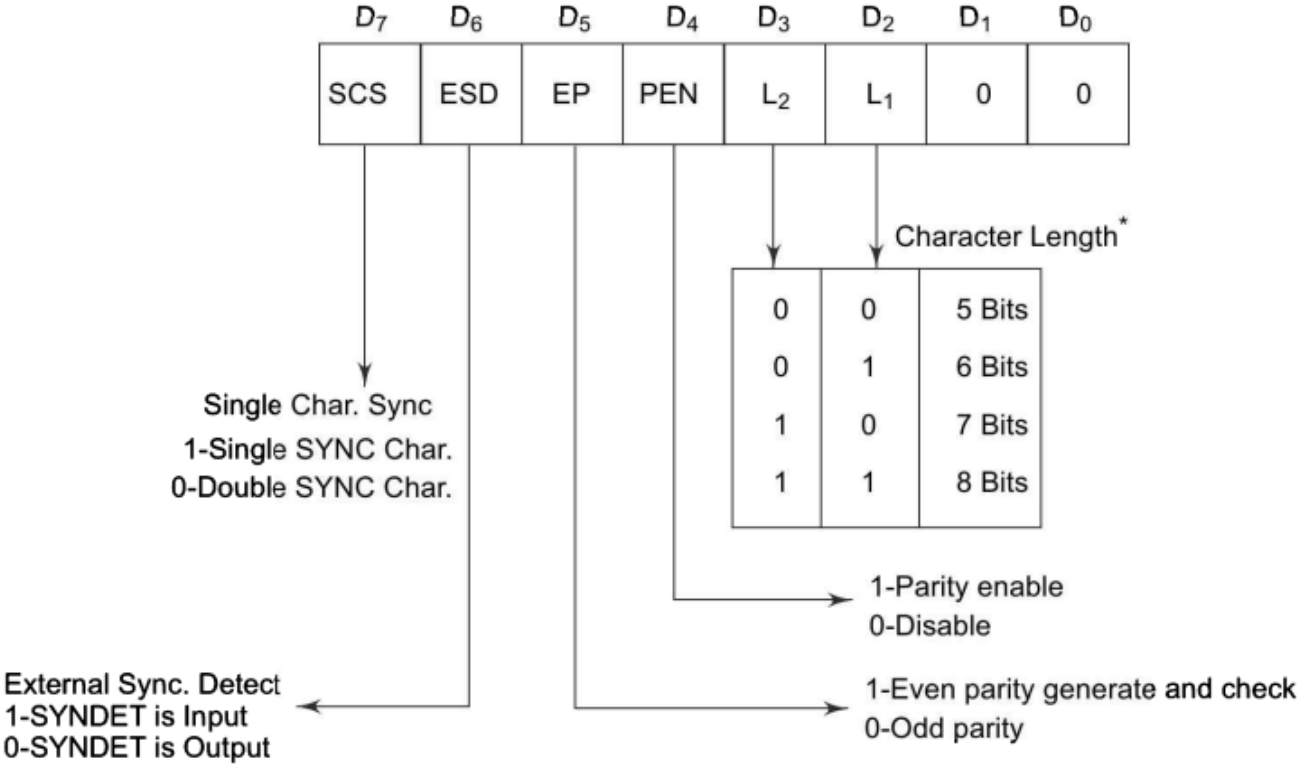
In loosely coupled multiprocessor, there is direct connection between processor and I/O devices.	While in tightly coupled multiprocessor, IOPIN helps connection between processor and I/O devices.
Applications of loosely coupled multiprocessor are in distributed computing systems.	Applications of tightly coupled multiprocessor are in parallel processing systems.

Discuss the mode instruction format of 8251 for synchronous and asynchronous mode of operation.



N.B.—Stop bit selection as above is only for transmitter. Receiver never requires more than one stop bit

Fig. 6.28 *Mode Instruction Format Asynchronous Mode*



* If the character size less than 8-bits, the remaining bits are set to 'O'.

Fig. 6.30 *Synchronous Mode Instruction Format*