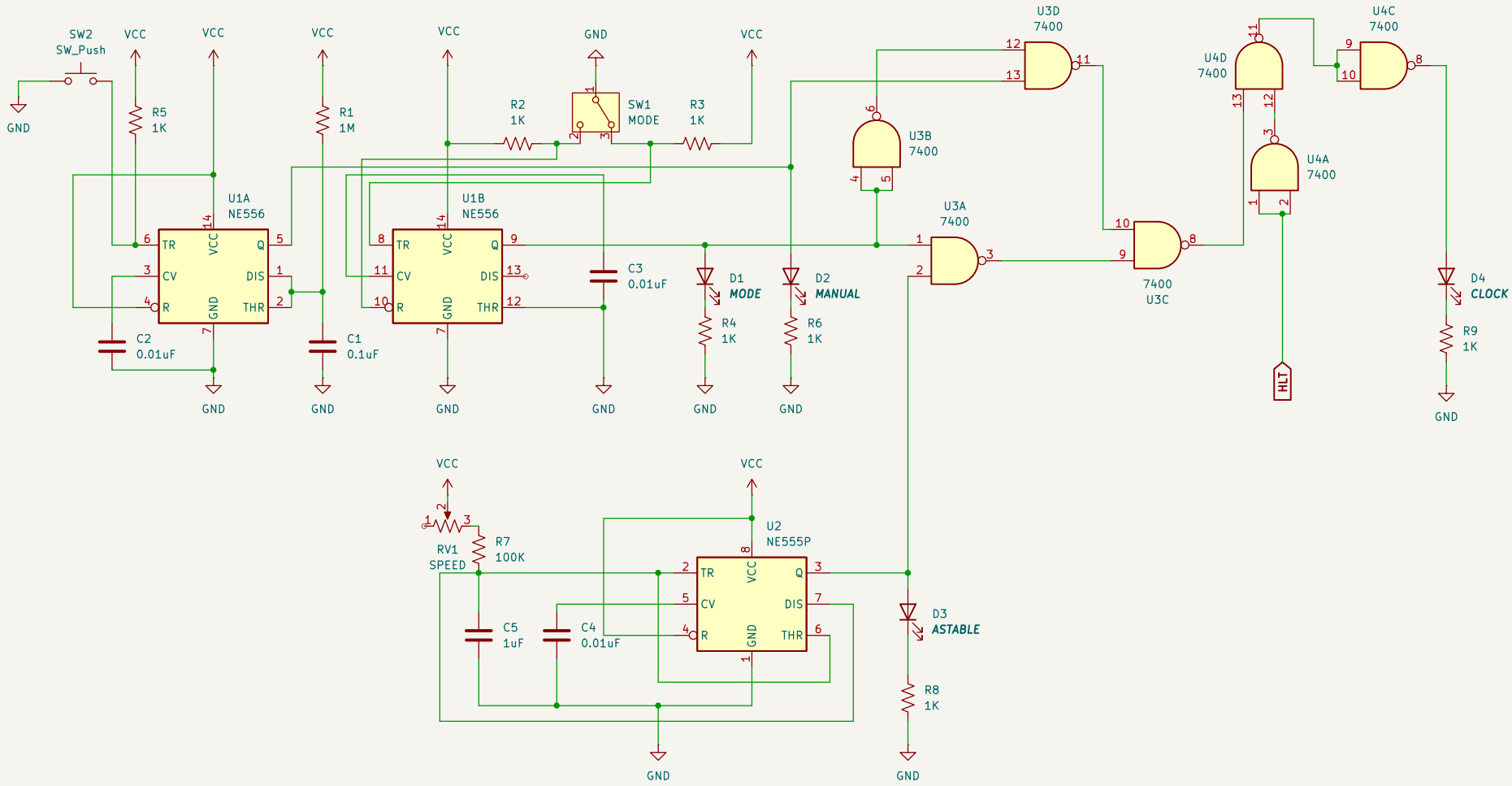
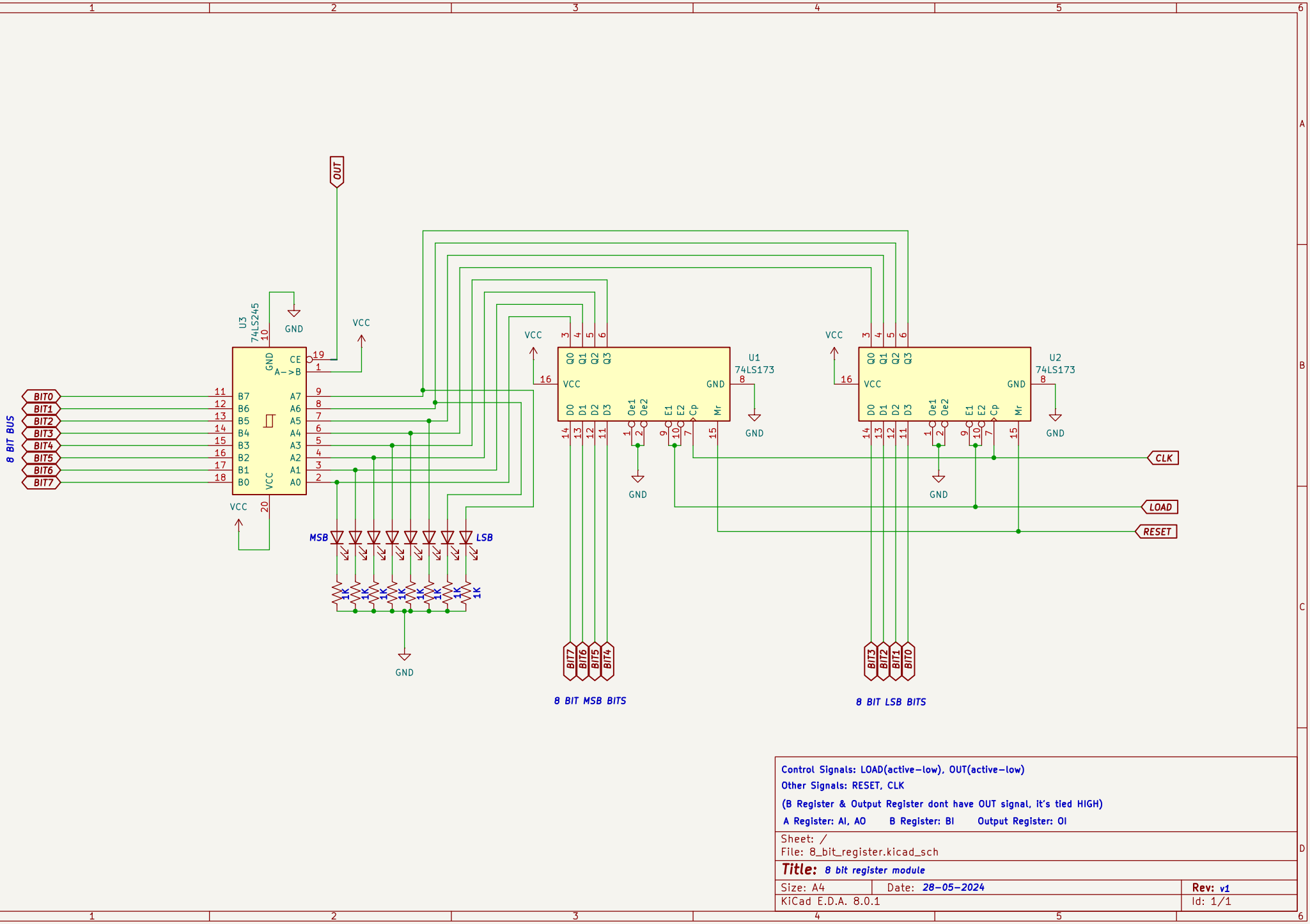


HLT is the Halt control signal
This module has two modes – Manual clock and Auto clock

Sheet: /		
File: 8_bit_cpu_clock_module.kicad_sch		
Title: CLOCK MODULE		
Size: A4	Date: 23-05-2024	**Rev:** v1
KiCad E.D.A. 8.0.1		Id: 1/1



Control Signals: LOAD(active-low), OUT(active-low)

Other Signals: RESET, CLK

(B Register & Output Register dont have OUT signal, it's tied HIGH)

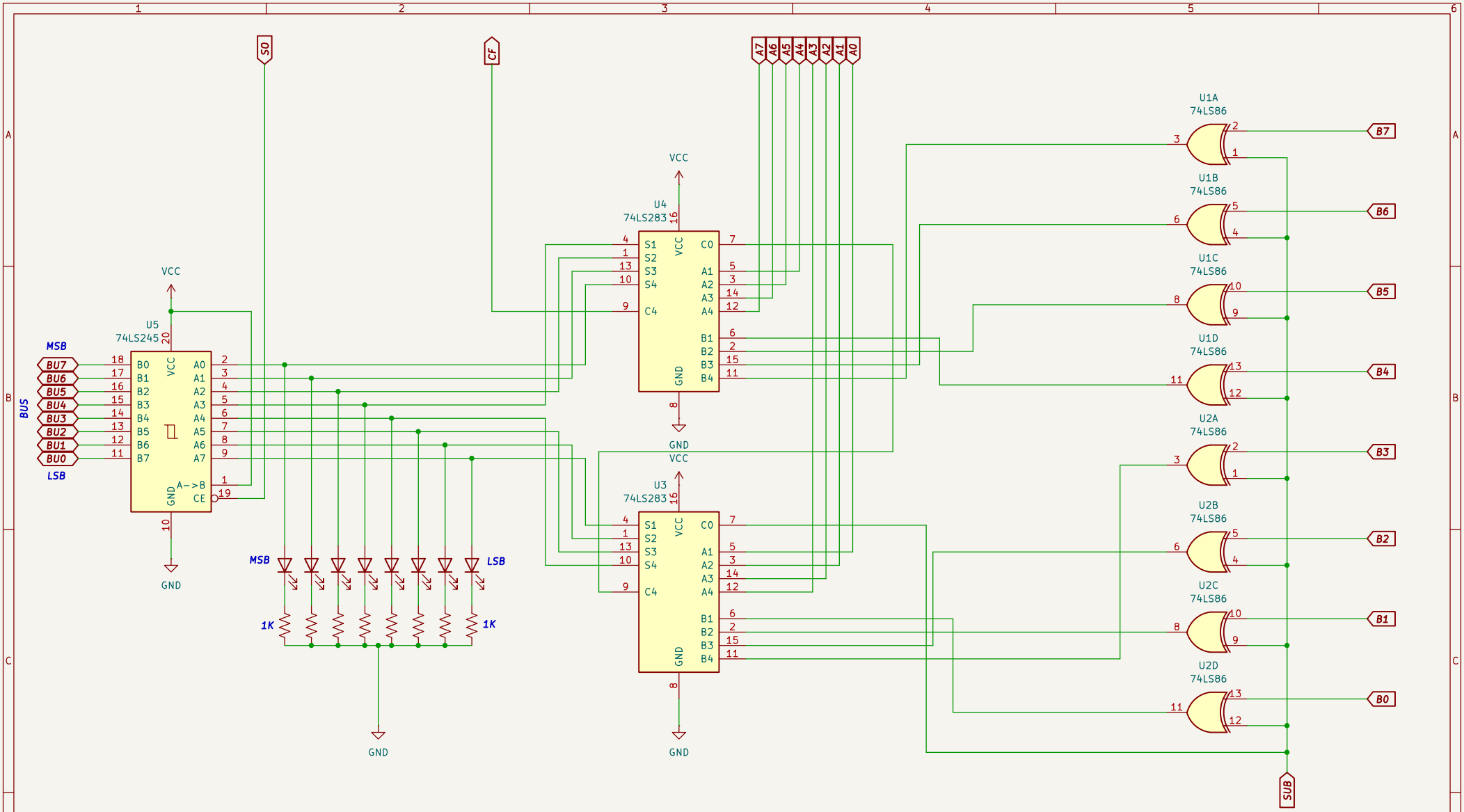
A Register: AI, AO B Register: BI Output Register: OI

Sheet: /

File: 8_bit_register.kicad_sch

Title: *8 bit register module*

Size: A4	Date: *28-05-2024*	**Rev:** *v1*
KiCad E.D.A. 8.0.1		Id: 1/1

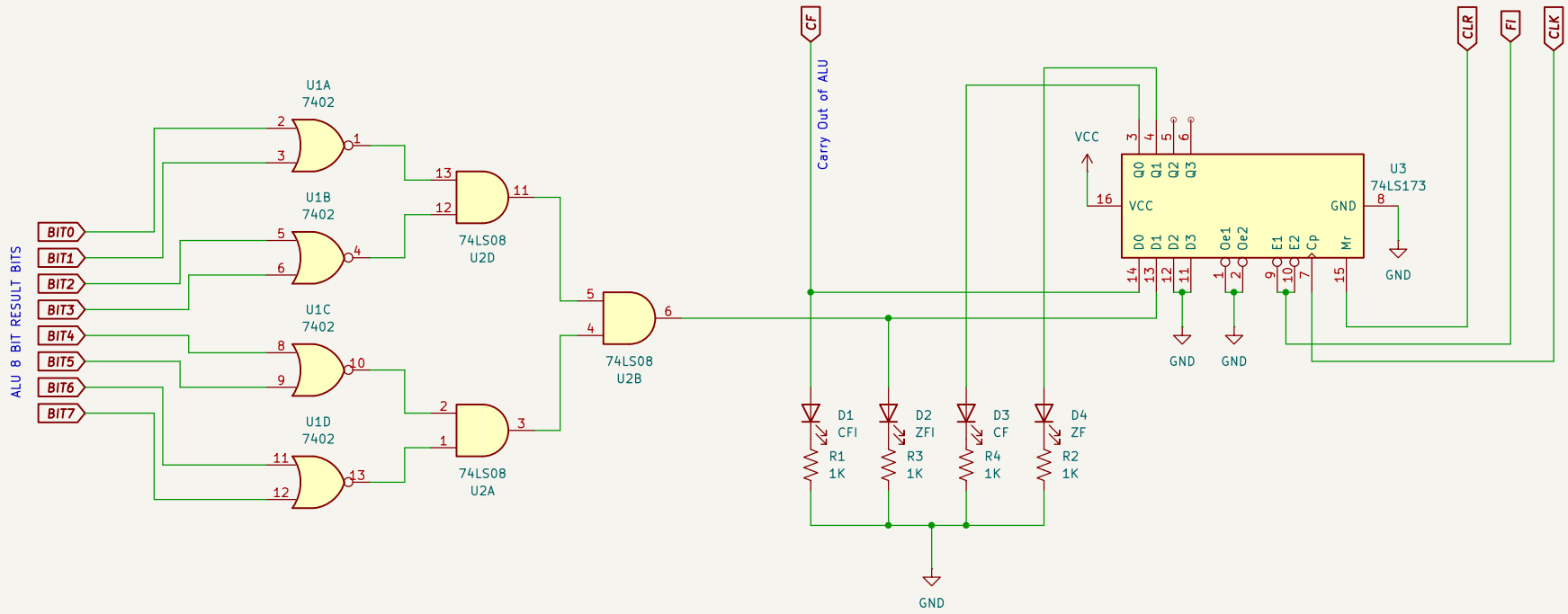


Control Signals: SO(active-low) & SUB
CF is the Carry Out that goes to Flag register input
A0-A7 is output of Accumalator & B0-B7 is the output of B register

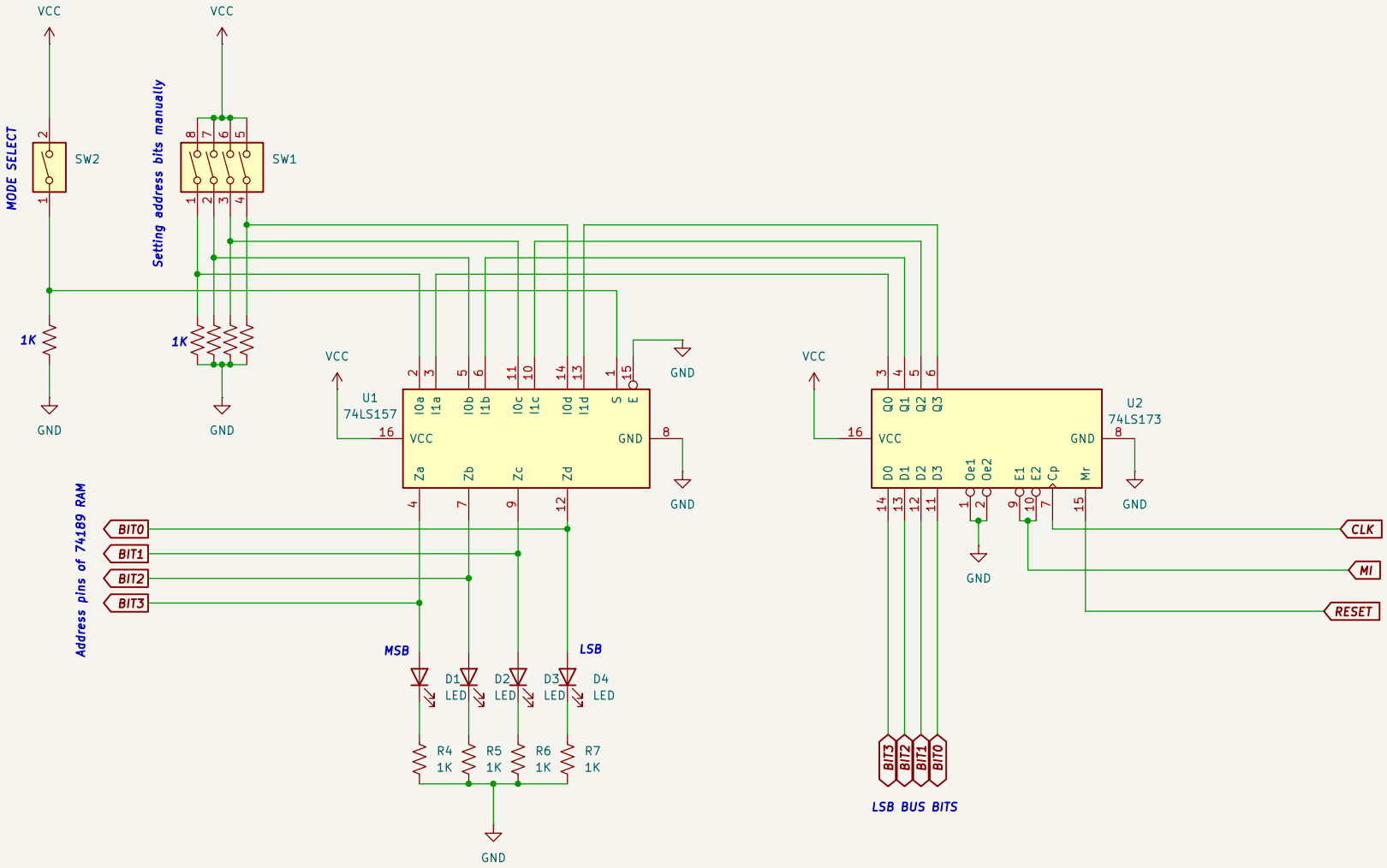
Sheet: /
File: ALU.kicad_sch

Title: *ALU*

Size: A4	Date: *03-06-2024*	**Rev:** *v1*
KiCad E.D.A. 8.0.1		Id: 1/1



Sheet: /		
File: flags_register.kicad_sch		
Title: FLAGS REGISTER		
Size: A4	Date: 24-05-2024	Rev: v1
KiCad E.D.A. 8.0.1		Id: 1/1



Control Signals: MI(active-low)

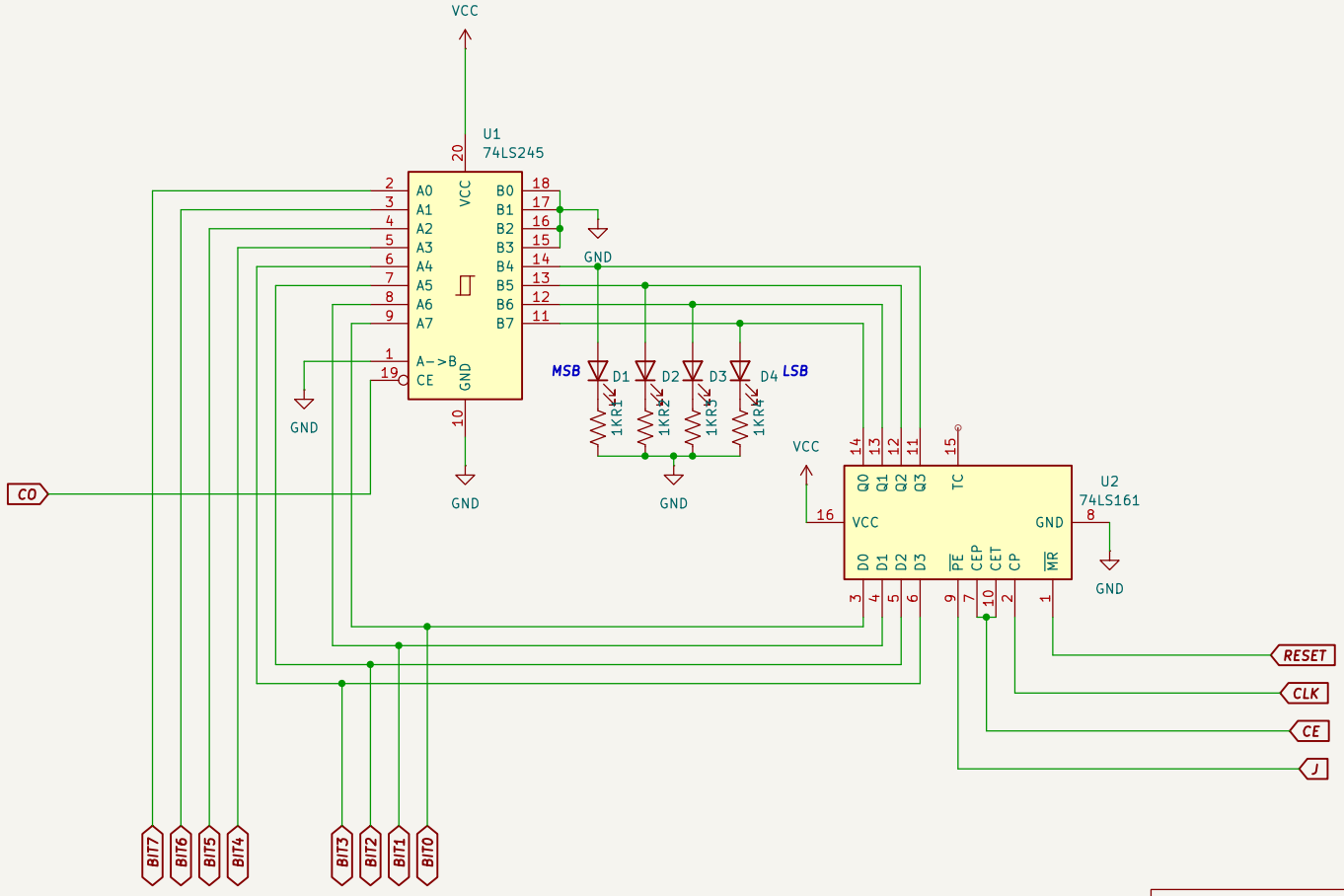
MODE SELECT switches between RUN mode and PROGRAM mode

Sheet: /
File: Memory_address_register.kicad_sch

Title: *Memory Address Register*

Size: A4 | Date: *30-05-2024* | **Rev:** *v1*

KiCad E.D.A. 8.0.1 | Id: 1/1

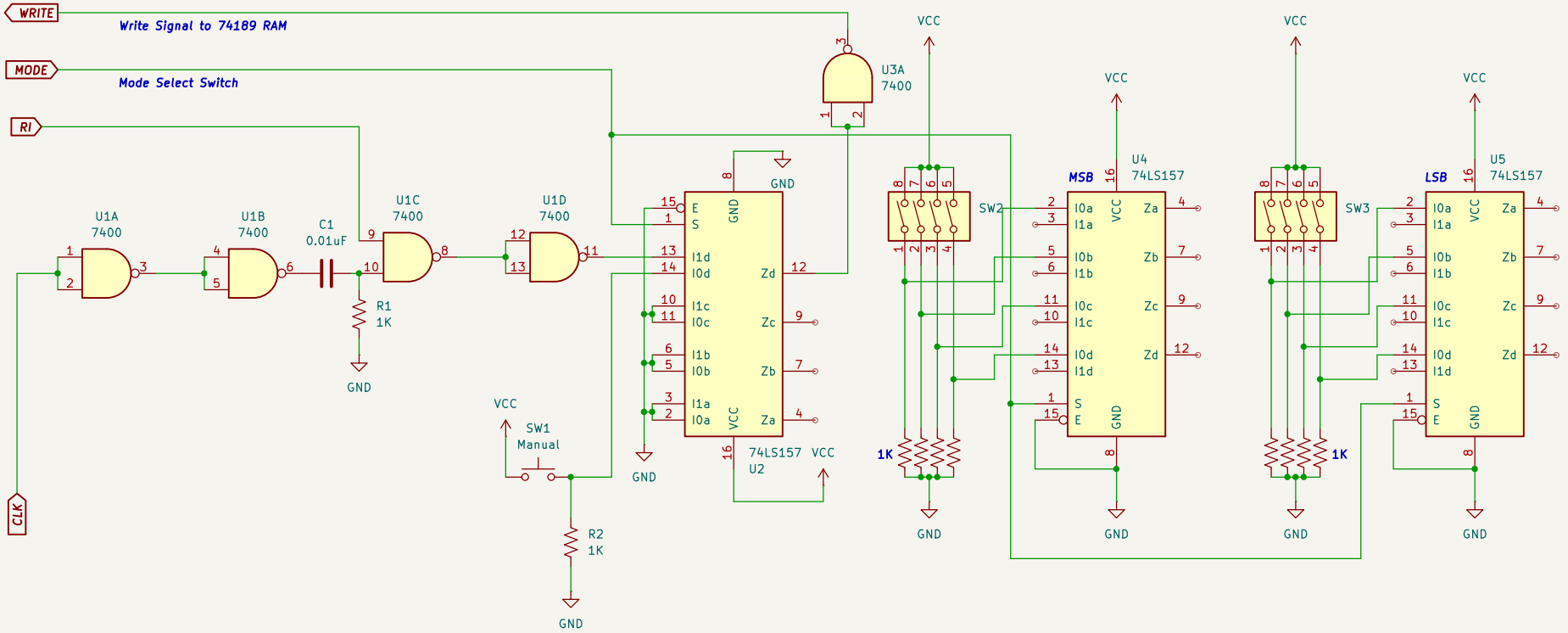


Control Signals: CO(active-low), J(active low), CE

Sheet: /
File: program_counter.kicad_sch

Title: *Program Counter*

Size: A4	Date: *25-05-2024*	**Rev:** *v1*
KiCad E.D.A. 8.0.1		Id: 1/1



Control Signals: RI — *U4(MSB) U5(LSB)*

The input pins 3,6,10,13 on U4 & U5 are connected to 74245 on RAM module

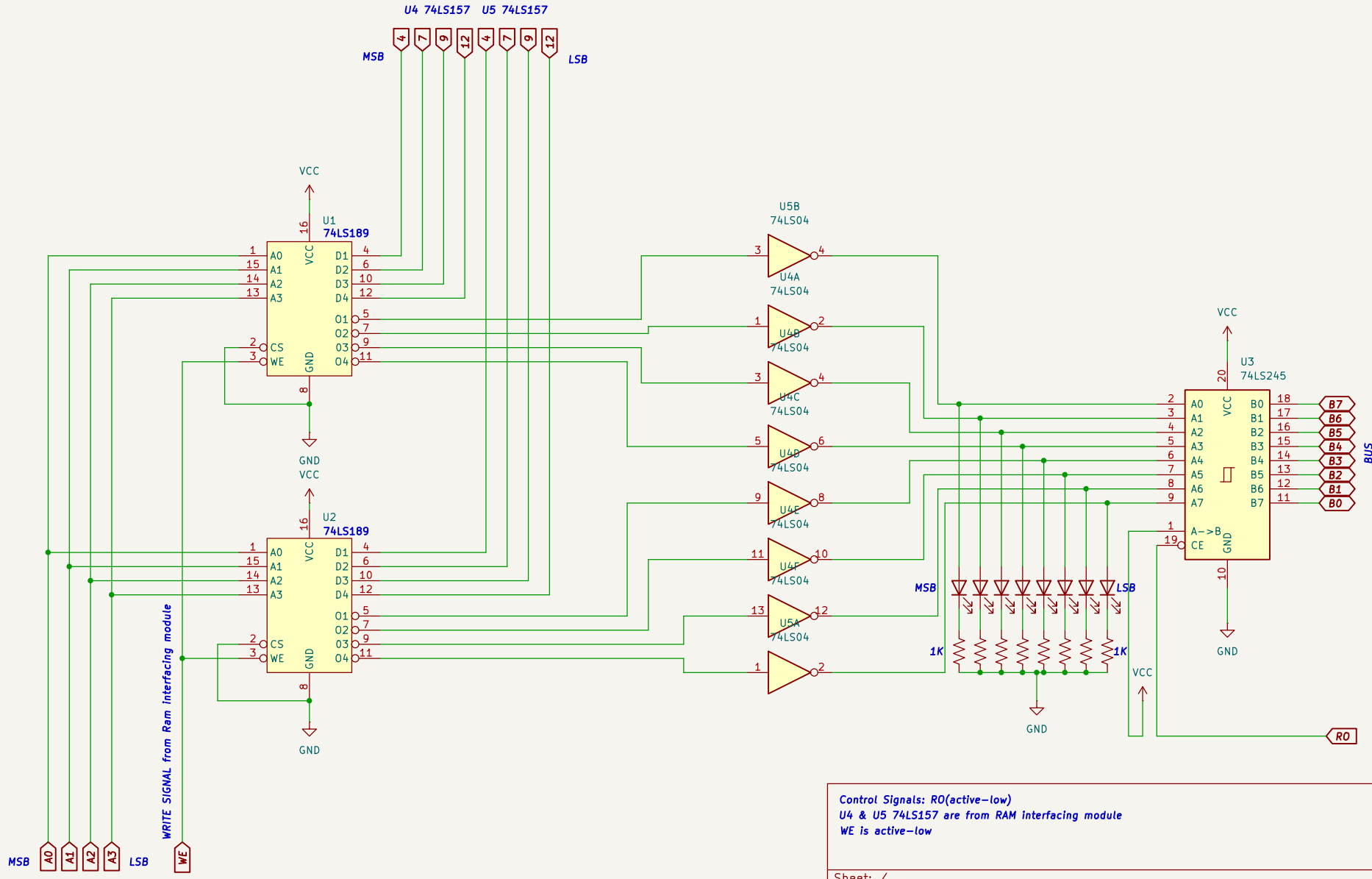
The output pins 4,7,9,12 on U4 and U5 are connected to data inputs on 74189 RAM

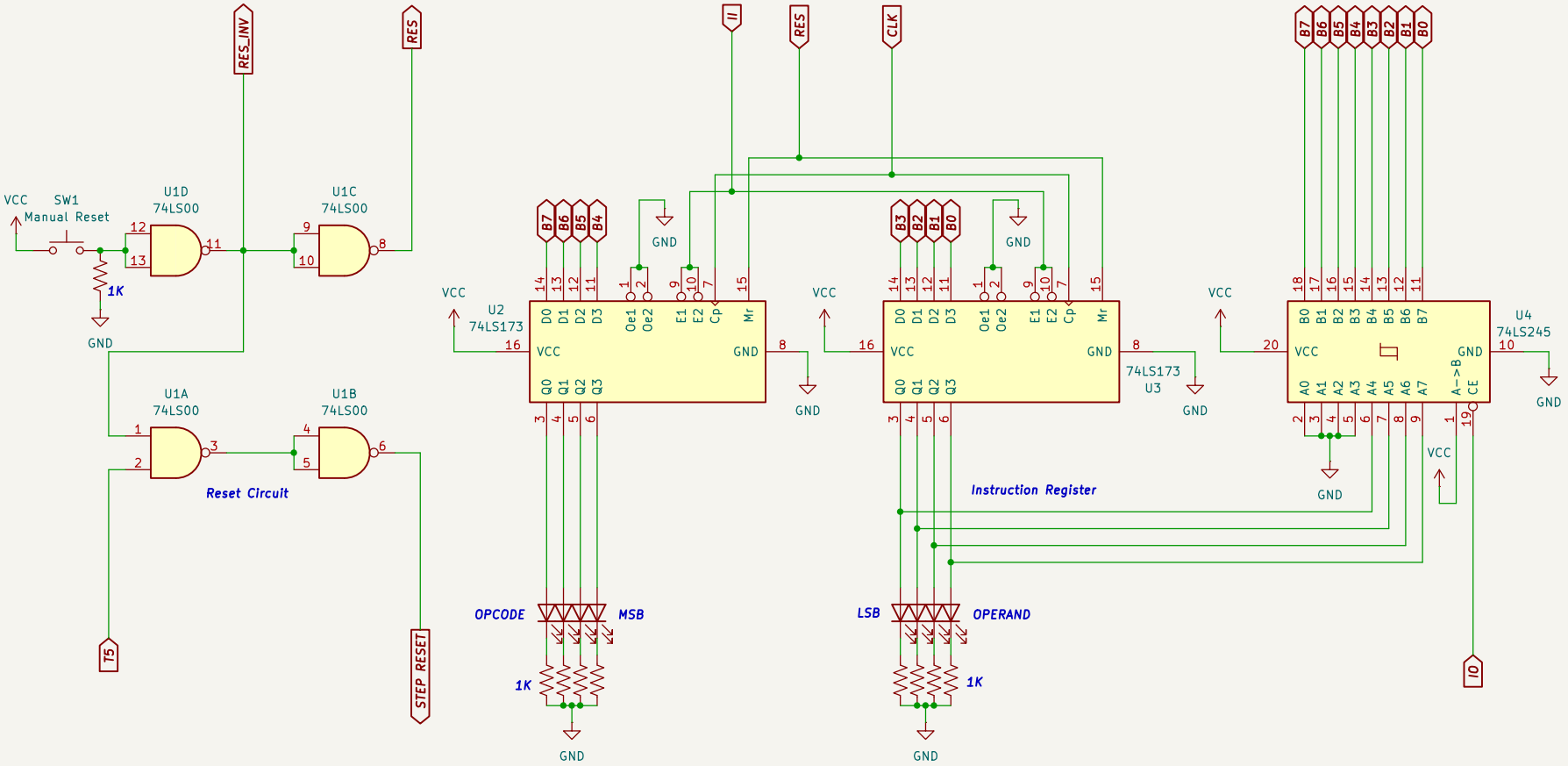
U4 & U5 select 8 bit input data to 74189 between DIP switches (Manual Mode) & 8 Bit BUS

Sheet: /
File: ram_interfacing.kicad_sch

Title: *Ram Interfacing*

Size: A4	Date: *01-06-2024*	**Rev:** *v1*
KiCad E.D.A. 8.0.1		Id: 1/1


U4 74LS157 U5 74LS157
MSB
LSB
4 7 9 12 4 7 9 12
VCC
U1
74LS189
A0 A1 A2 A3
D1 D2 D3 D4
O1 O2 O3 O4
CS WE GND
GND
U2
74LS189
WRITE SIGNAL from Ram interfacing module
U5B
74LS04
U4A
U4B
U4C
U4D
U4E
U4F
U5A
U3
74LS245
A0 A1 A2 A3 A4 A5 A6 A7
B0 B1 B2 B3 B4 B5 B6 B7
A->B
CE
BUS
B7 B6 B5 B4 B3 B2 B1 B0
1K
RO
MSB
LSB
A0 A1 A2 A3
WE
Address from MAR
Control Signals: RO(active-low)
U4 & U5 74LS157 are from RAM interfacing module
WE is active-low
Sheet: /
File: RAM_module.kicad_sch
Title: RAM Module
Size: A4
Date: 06-06-2024
Rev: v1
KiCad E.D.A. 8.0.1
Id: 1/1



Control Signals: II(active-low), IO(active-low)
T5 is the 5th state output of 74138, it resets itself on the 6th micro-step
RES_INV is the active-low reset signal & RES is the active-high reset signal

Sheet: /		
File: reset_and_instruction_register.kicad_sch		
Title: *Reset Circuit & Instruction Register*		
Size: A4	Date: *04-06-2024*	**Rev:** *v1*
KiCad E.D.A. 8.0.1		Id: 1/1