CLASS : S.E. COMP **SUBJECT : DEL**

EXPT. NO. : 11 **DATE :**

TITLE : COMBINATIONAL LOGIC DESIGN USING VHDL

OBJECTIVE :

1. Design and simulation of 4:1 Multiplexer circuit using all modeling style
2. Design and simulation of Full adder circuit using all modeling style

SOFTWARE : Modelsim version 6.5

THEORY :

VHDL is very high speed integrated circuit hardware description language. It is a widely used language that describes the behavior of a digital system. The language has constructs that enable to express the concurrent or the sequential behavior of digital systems with or without timing.

Features of VHDL:

1. VHDL can be used at different complexity levels from single logic gate to complete system in the same simulation environment.
2. VHDL supports flexible design methodologies like top-down, bottom-up or mixed.
3. It supports both synchronous and asynchronous timing models.

VHDL code is composed of at least 3 fundamental sections:

1. Library declarations
2. Entity
3. Architecture

Library Declaration: It is a collection of commonly used codes which can be shared by other designs as well. The code is usually written in the form of functions, procedures or components which are placed inside the packages and then compiled into the destination library.

Syntax: Library library_name;

Use library_name. package_name.package ports;

Three following libraries are used:

IEEE, Standard and work.

As standard and work libraries are included by default, library IEEE should be declared in a program.

The library, package and ports used and declared in the program are:

```
Librart IEEE;
Use IEEE.std_logic_1164.all;
```

Entity Declaration: It is an interface between a design and the external environment. An entity gives the list and specifications of all the inputs and outputs in the design. A design may contain multiple entities and each entity has architecture.

Syntax: entity entity_name is

```
Port( port_name1: mode signal_type;
      Port_name2: mode signal_type);
 End entity_name;
```

Architecture Declaration: The architecture describes the underlying functionality or internal organization or operation of the entity. A single entity can have multiple architectures.

Every architecture has two parts- Declaration (optional) and code.

Syntax: architecture architecture_name of entity_name is

Declarations if any

Begin

End architecture_name;

Object types:

- Signal: It represents the circuit interconnections. It is used to pass the values in and out of the component or a circuit.
  Syntax: signal signal_name:signal_type;
- Variable: It is used to represent the local information.
  Syntax: variable variable_name:variable_type;
- Constant: It is used to assign default values.
  Syntax: constant constant_name:constant_type:=value;

Data types:

- Bit: It is a two level logic assigned to a constant or variable.
- Bit_vector(x downto 0): It represents 8-bit vector with leftmost bit as MSB.
- Bit_vector(0 to x): It represents 8-bit vector with rightmost bit as MSB.

Types of modeling:

- Dataflow modeling
- Structural modeling
- Behavioral modeling
- Mixed modeling

Data Flow Modeling:

It uses set of concurrent assignment statements.

The data is viewed as flowing through the design from input to output.

Each of the statements can be activated when any of its input changes its value.

4:1 multiplexer:

4 inputs: I0, I1, I2, I3
1 output: Y
2 select lines: S1, S0

The circuit can be described by the following equation:

Y= not (S1) . not (S0). I0 + not (S1). S0.I1 + S1.not(S0). I2 + S1. S0. I3

Structural Modeling:

A digital circuit can be described with the help of small modules where outputs are functions of the inputs.
In this modeling, set of interconnected components are used which can be used to create a very low level description of a circuit.
Components that build the circuit are declared and used in the architecture of the design.

Component declaration:

It is a virtual design entity which needs to be declared in the architecture. The component is the basic circuit which builds the complete design.
Syntax: Component component_name
Port(port_name1:mode port_type;
Port_name2:mode port_type);
End component_name;

Syntax for port map: Port map is used for mapping the intermediate signals.

Signal: entity_name port map(variables to port map with)

PROCEDURE :

- Create a project in modelsim.
- Create a VHDL Source file.
- Library Declaration
- Entity Declaration
- Architecture Declaration
- Code writing using different modeling style
- End

CONCLUSION:

REFFRENCE:

1. **R.P.Jain "Modern Digital Electronics" TMH 4th Edition**
2. **J.Bhaskar " VHDL Primer S"Prentice Hall 3rd Edition**
3. **Douglas Perry" VHDL Programming by Example"TMH 4th Edition**

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