Department of Computer Engineering

CLASS :   S.E. COMP   **SUBJECT : DEL**

EXPT. NO. : 10   **DATE :**

TITLE   :   ALGORITHMIC STATE MACHINE

OBJECTIVE   :

1. Design and Implement waveform generator circuit using ASM based Multiplexer controller method

APPARATUS   :

Digital-Board, GP-4Patch-Cords, IC-74LS74, IC74153,IC-74LS32, IC-74LS08 ,IC-74LS04 and Required Logic gates if any.
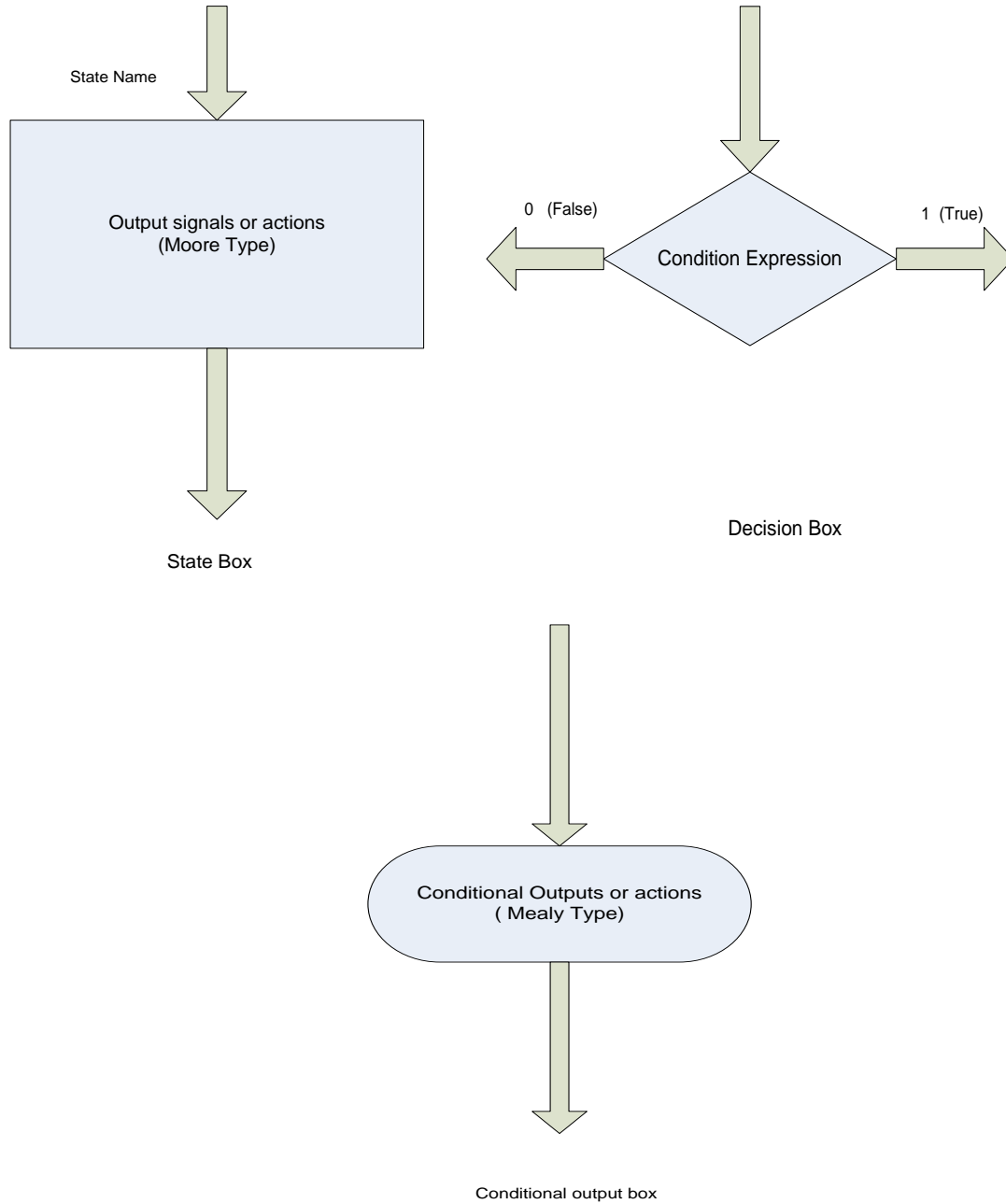
THEORY   :

1. ASM means algorithmic state machine.
2. It is a type of flowchart that can be used to represent the state transitions and generated outputs for finite state machine(FSM)
3. ASM charts are similar to traditional flowcharts.
4. Unlike a traditional flowchart, this includes timing information. This chart specifies that the FSM flows from one state to another only after each active clock edge.

   Basic elements used in ASM Chart:
1. State Box
2. Decision Box
3. Conditional output Box

These are shown in the figure given below:

State Name

Output signals or actions
(Moore Type)

State Box

0 (False)   Condition Expression   1 (True)

Decision Box

Conditional Outputs or actions
(Mealy Type)

Conditional output box

State Box:

A rectangle represents a state of the FSM.It is equivalent to node in the state diagram or row in the state table. The name of the state should be indicated outside the box in left top corner. Moore types of outputs are listed inside the box.

Decision Box:

A diamond indicates that the stated condition expression has to be tested and an exit path has to be chosen accordingly. The condition expression Consists of one or many inputs.

Conditional output Box:

The oval denotes the output signals that are of Mealy type. These output depend on the values of state variables and the Inputs of FSM.The condition that determines whether such outputs are generated is specified in a decision box

Significance:

It is an aid to design the complex circuits.ASM charts are used to describe complex circuits that include one or more FSM's and another circuitry such as registers, counters, adders, multipliers etc.

ASM Blocks:

1. It is a structure which consists of single state box and any decision and conditional output boxes that the state box may be connected to.
2. It has one entry path and any number of exit paths.
3. Each block describes the state of the system during the interval of one clock pulse.

PROCEDURE   :

1. Make the connections as per the Logic circuit of waveform generator circuit using and Verify its functionality.

Design of Waveform generator using multiplexer controller method

Timing Diagram:

1. Waveform generator has 4 states i.e. 00,01,10,11.
2. In the waveform generator, circuit always goes to next state irrespective of values of X1 and X2.
3. Output of each state is observed according to the input combinations X1X2.

ASM Chart:

State Transition Table:

Dec. Equ.	PRESENT STATE		Ext. I/Ps		NEXT STATE		MUX. OUTPUT		Final O/P
	X1	X2	(S_1) Q_A	(S_0) Q_B	(D_A) Q_A^+	(D_B) Q_B^+	M1	M2	Z
0	0	0	0	0					
1	0	0	0	1					
2	0	0	1	0					
3	0	0	1	1					
4	0	1	0	0					
5	0	1	0	1					
6	0	1	1	0					
7	0	1	1	1					
8	1	0	0	0					
9	1	0	0	1					
10	1	0	1	0					
11	1	0	1	1					
12	1	1	0	0					
13	1	1	0	1					
14	1	1	1	0					
15	1	1	1	1					

K- Map Simplification for Z:

Logic Diagram:
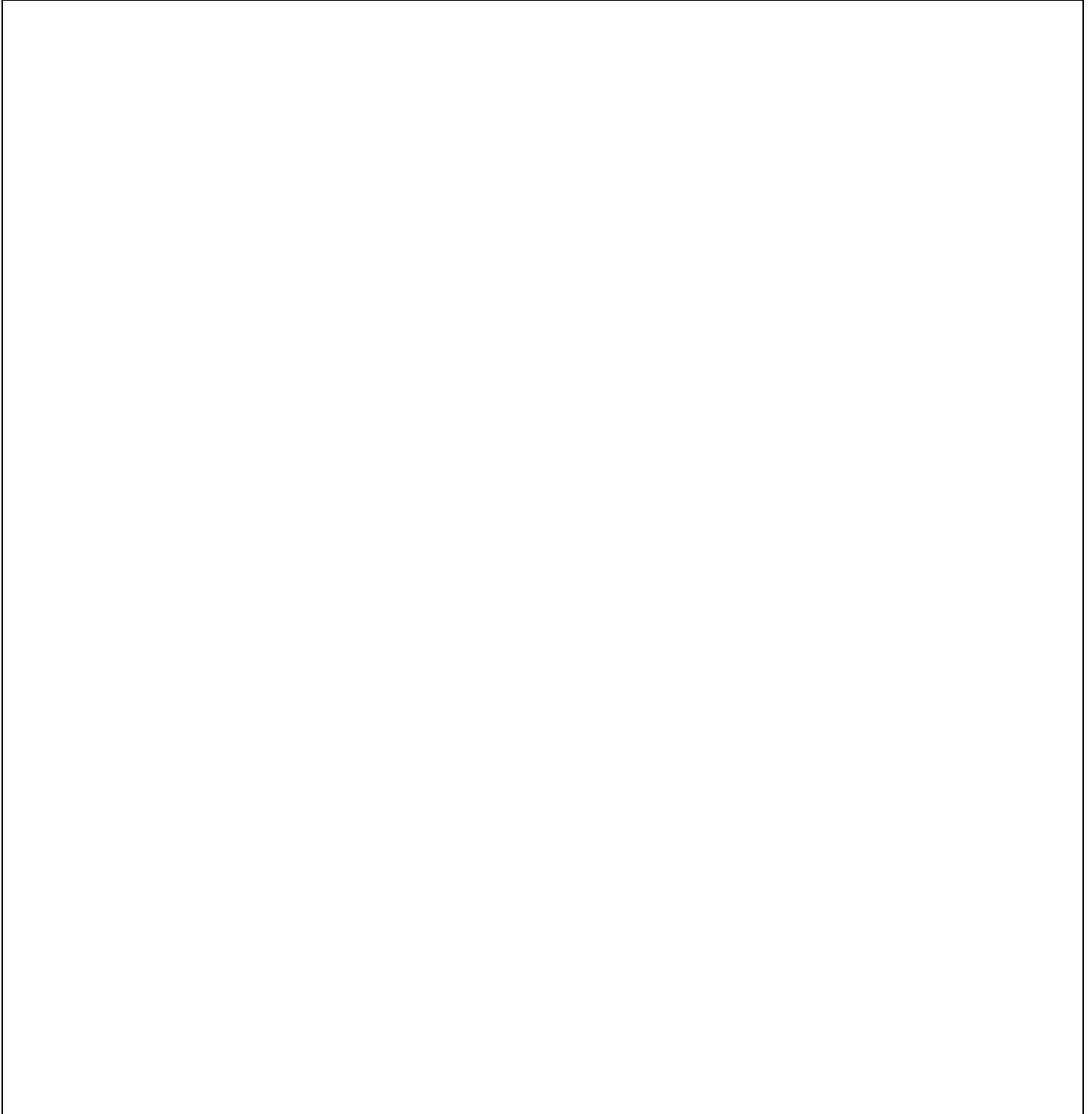
Logic gates/MSI Device required for Implementation

Sr.No.	Title	Name of the IC	Number of Gates required	IC Required
01	Waveform Generator Circuit using Mux.controller method			

CONCLUSION:

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REFFRENCE:

1. **R.P.Jain "Modern Digital Electronics" TMH 4th Edition**

2. **D.Leach,Malvino,Saha,"Digital Principles and Applications",TMH**

Subject teacher Sign with Date   Remark