CLASS : S.E. COMP **SUBJECT : DEL**

EXPT. NO. : 7 **DATE :**

TITLE : UP/DOWN COUNTER CIRCUIT

OBJECTIVE :

1. Design and Implement 3-bit Asynchronous (Ripple) UP/DOWN –Counter using Mode control switch (Use-IC-74LS76) and verify its truth-table.

   Draw Timing diagram

   When M=0: Circuit perform UP –Counting operation

   When M=1: Circuit perform DOWN –Counting operation

2. Design and Implement 3-bit Synchronous UP/DOWN –Counter using Mode control switch (Use-IC-74LS76) and verify its truth-table.

   Draw Timing diagram

   When M=0: Circuit performs UP –Counting operation

   When M=1: Circuit performs DOWN –Counting operation

3. Design and Implement MOD-N Counter circuit using IC-74LS90 and IC-74LS191

   Draw Timing Diagram.

APPARATUS :

Digital-Board, GP-4 Patch-Cords, IC-74LS76, IC-74LS90, IC-74LS191, IC-74LS32, IC-74LS04/IC-74LS08 and Required Logic gates if any

THEORY :

Counter is a Sequential Logic device which can be use to count the number of pulses given to the circuit. Counter can be classified into two category one is Synchronous and other is Asynchronous (Ripple) In case of Asynchronous counter output of first flip-flop goes to the clock of next and so on, and input of all flip-flop is connected to VCC for IC-74LS76.

All set and reset pin is connected to VCC.Asynchronous counter is easy to design as compared to Synchronous Counter. Synchronous Counter is faster than Asynchronous Counter.IC-74LS76 is Dual M/S-JK filp-flop, which means in one IC there are two M/S-JK filp-flop are contained.

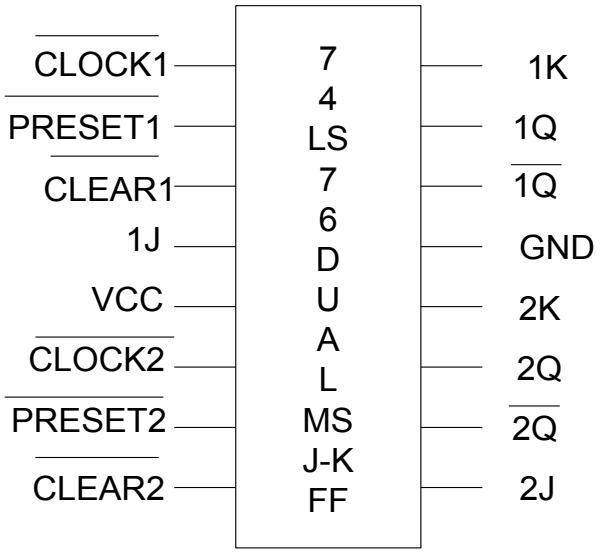
IC -7490 is called as a 4-bit MS-JK Flip-flop decade (BCD) Ripple counter. It contains 4 -master slave flip flops internally connected to provide MOD-2 i.e. divide by 2 and MOD-5 i.e. divide by 5 counter.MOD-2 and Mod-5 counters can be used independently or in cascading. Each Counter has a separate clock input to initiate state changes of the counter on the high to low clock transition. Since the o/p from the divide by 2 section is not internally connected to the succeeding stages. The device may be operated in various counting modes. In a BCD counter the CP1 input must be externally connected to Q0 output. The CP0 input receives the incoming count producing a BCD count sequence.

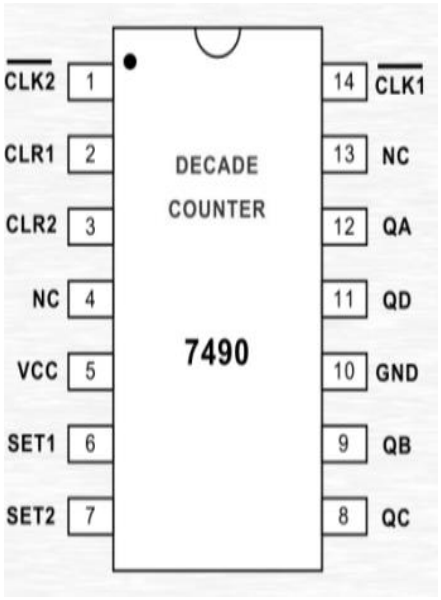
It is also provided with additional gating to provide a divide by 2 counter and binary counter for which the count cycle length is divide by 5. The device may be operated in various counting modes.

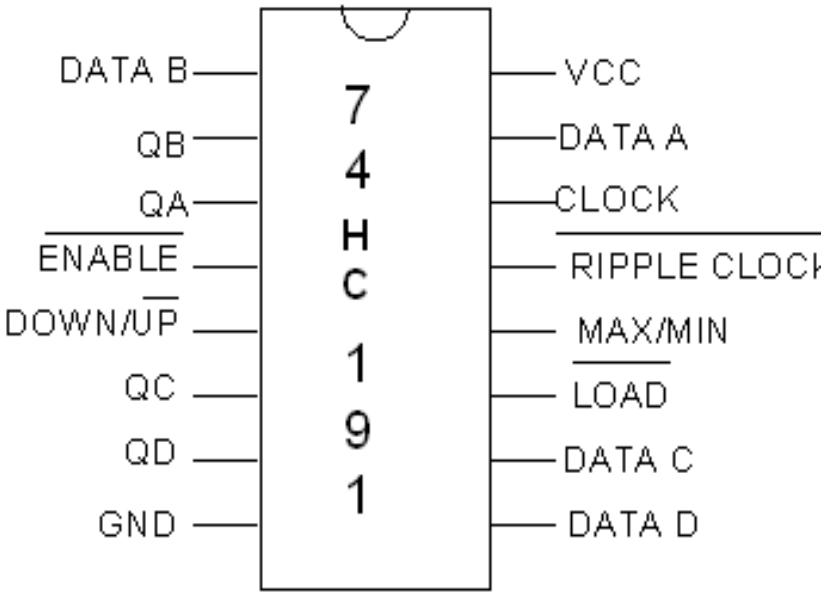
There are 2 reset inputs R0 (1) and R0 (2) both of which need to be connected to the ‘logic 1’ for clearing all flip flops. Two set inputs Rg(1) and Rg(2) when

connected to logic are used for setting counter to 1001 (BCD 9).IC74191 is 4-bit binary parallel presettable Programmable UP/DOWN synchronous counter. It contains 4 master slave J-K flip flops with internal gating and steering logic to provide asynchronous reset and synchronous count up/down operations; its asynchronous parallel capability permits the counter to be preset to any desire number. D0 to D3 are the parallel data inputs. Information present on the parallel data inputs D0 to D3 is loaded into the counter and appears on the output when the load **PL** input is low this operation is overrides the counting function .counting is inhabited by the high level on the enable CE input, when CE input is low internal state changes are initiated synchronously by the low to high transitions of the clock inputs the up/down input signal determines the direction of input.

PIN Diagram :







PROCEDURE :

1. Make the connections as per the Logic circuit of 3-bit Asynchronous UP/ DOWN Counter circuit using IC-74LS76 and Verify its Truth Table.
2. Make the connections as per the Logic circuit of 3-bit Synchronous UP/ DOWN Counter circuit using IC-74LS76 and Verify its Truth Table.
3. Make the connections as per the Logic circuit of MOD-N Counter circuit using IC-74LS90 /IC-74LS191 and Verify its Truth Table.

Design of 3-bit (Ripple) UP/DOWN-Counter Using Mode control S/W

Dec. Equ.	M	Q	Qbar	Derived Logic (Y)
	0	0	1	
	0	1	0	
	1	0	1	
	1	1	0	

K-MAP for Derived Logic

Logic diagram:

Observation Table:

CLOCK PULSE	Mode control (M)	Output		
		Q_A	Q_B	Q_C
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
CLOCK PULSE	Mode control (M)	Output		
		Q_A	Q_B	Q_C
0	1	1	1	1
1	1	1	1	0
2	1	1	0	1
3	1	1	0	0
4	1	0	1	1
5	1	0	1	0
6	1	0	0	1
7	1	0	0	0

Design of 3-bit Synchronous UP/DOWN-Counter Using Mode control Input (Switch)

M	PRESENTSTATE			NEXT STATE			INPUT					
	Q_A	Q_B	Q_C	Q_A^+	Q_B^+	Q_C^+	J_A	K_A	J_B	K_B	J_C	K_C
0	0	0	0									
0	0	0	1									
0	0	1	0									
0	0	1	1									
0	1	0	0									
0	1	0	1									
0	1	1	0									
0	1	1	1									
1	1	1	1									
1	1	1	0									
1	1	0	1									
1	1	0	0									
1	0	1	1									
1	0	1	0									
1	0	0	1									
1	0	0	0									

K-Map Simplification for J_A , K_A , J_B , K_B , J_C , K_C

Logic Diagram:

Design of MOD-2 / MOD-5 /MOD-10/MOD-20 Counter using IC-7490
Logic Diagram: (MOD-2 / MOD-5 Counter)

Logic Diagram: (MOD-10 / MOD-20 Counter)

Observation Table: Decade Counter

CLOCK PULSE	Output			
	Q_3	Q_2	Q_1	Q_0
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1

Design of MOD-7 Counter using IC-7490

Dec.Equ.	OUTPUT				RESET LOGIC
	Q_3	Q_2	Q_1	Q_0	Y
0	0	0	0	0	
1	0	0	0	1	
2	0	0	1	0	
3	0	0	1	1	
4	0	1	0	0	
5	0	1	0	1	
6	0	1	1	0	
7	0	1	1	1	
8	1	0	0	0	
9	1	0	0	1	

K-Map for Reset Logic

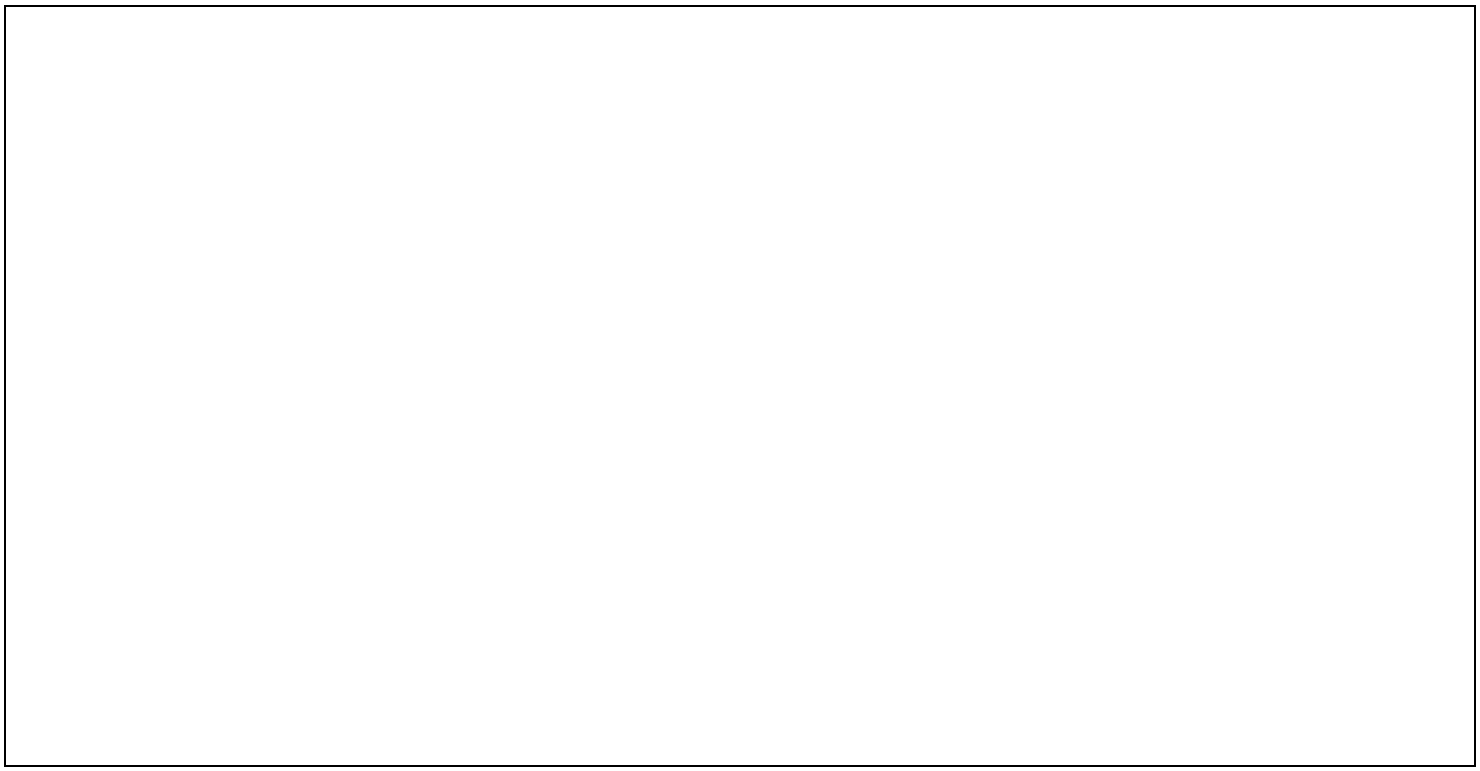
Logic Diagram: (MOD-7 Counter)

Design of 4-bit UP and DOWN /Programmable MOD-N Counter using IC-74191

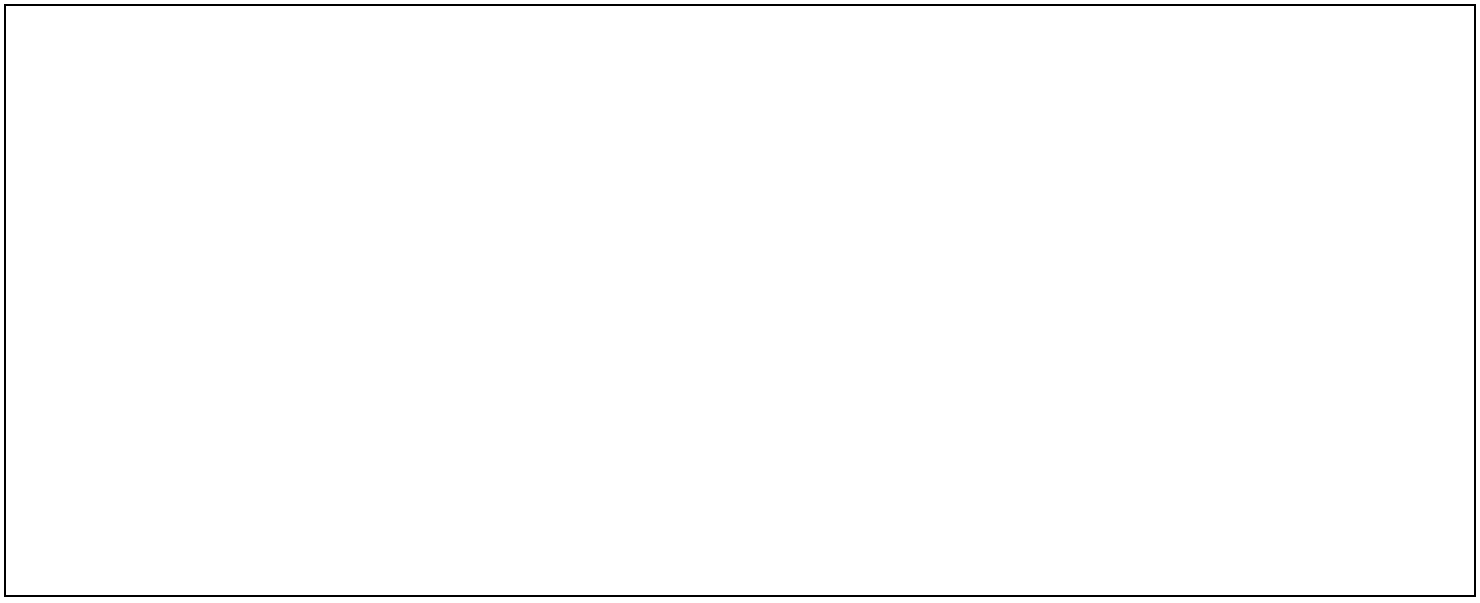
Function Table: IC-74191

PL	CE	CLK	Up/DOWN	Data Input				Output				Mode of Operation
				D_3	D_2	D_1	D_0	Q_3	Q_2	Q_1	Q_0	
0	×	×	×	1	0	0	0	1	0	0	0	Parallel Load
1	0	1	0	-	-	-	-	0	0	0	0	Up Counting
								To				
								1	1	1	1	
1	0	1	1	-	-	-	-	1	1	1	1	Down Counting
								To				
								0	0	0	0	

Logic Diagram: (4-bit UP Counter)



Logic Diagram: (4-bit Down Counter)



Logic Diagram :(4-bit Presettable Programmable MOD-N UP/Down Counter)

Logic Gates / MSI Device required for Implementation:

Sr.No.	Title	Name of the IC	Number of Gates required	IC Required
01	3-bit Ripple UP/DOWN Counter			
02	3-bit Synchronous UP/DOWN Counter			

03	MOD-02/05/10 Counter			
04	MOD-20 Counter			
05	MOD-07 Counter			
06	4-Bit UP/DOWN Counter			
07	MOD-N Presettable Programmable Counter			

CONCLUSION:

REFFRENCE:

1. **R.P.Jain "Modern Digital Electronics" TMH 4th Edition**
2. **D.Leach,Malvino,Saha,"Digital Principles and Applications",TMH**

Subject teacher Sign with Date Remark