CLASS: S.E.COMP **SUBJECT :DEL**

EXPT. NO.:4 **DATE:**

TITLE : MULTIPLEXER / DEMULTIPLEXER

OBJECTIVE :

1. Verification of Function table of IC-74LS153
2. Design and Implement 8:1 MUX using IC-74LS153 and verify its truth Table
3. Realization of the following Boolean expression using IC-74153 and verify its truth-Table
   F(A,B,C,D)=∑m( )
4. Verification of Function table of IC-74LS138
5. Realization of the following Boolean expression using IC-74138 and verify its truth-Table
   F(A,B,C)=∑m( )

APPARATUS :

Digital-Board, GP-4Patch-Cords, IC-74LS32, IC-74LS08 / IC-74LS04 / IC-74LS153/IC-741LS38 and Required Logic gates if any.

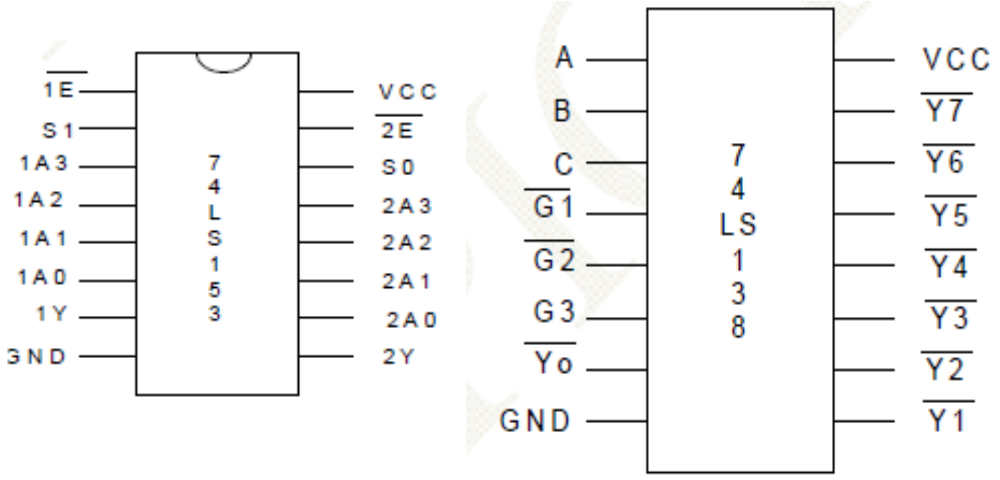
THEORY :

Multiplexer is a combinational logic device, which has many input & one output, this output can be selected according to select input. IC-74LS153 is Dual 4:1 MUX. It is a 16-pin dual in-line packaged IC, which has two enable pins (STROBE Active Low). We can design 8:1 MUX using cascading of Two 4:1 MUX. This is achieved with the help of enable / strobe inputs and multiplexer tree is designed. To implement 8:1 MUX we need

3 select lines and one output. Use dual 4:1 MUX for select lines 2 are common, use enable pin for 3rd select line. Connect the first strobe of first 4:1 MUX and the second strobe of second 4:1 MUX through one Inverter. This is 3rd select line only one 4:1 MUX will become active at one time. Connect outputs of 2 -MUX to OR get so that we get one output .

De-Multiplexer/Decoder is a combinational logic device, which has one input & many output, one output can be selected according to select input. IC-74LS138 is 3 to 8 Line Decoder/Demultiplexer. It is a 16-pin dual packaged IC, which has three enable pins (2-STROBE Active Low and one Active High). IC-74LS138 produces complementary output. i.e. the output of 74LS138 is Active Low. We can design any combinational circuits using IC-74LS138. DEMUX/Decoder performs reverse operation to that of Multiplexer

PIN DIAGRAM:



PROCEDURE :

1. Make the connections as per the Pin diagram of IC-74LS153 and Verify its Truth Table.
2. Make the connections as per the Logic circuit of 8:1 MUX and Verify its Truth Table
3. Make the connections as per Logic circuit of the given function and Verify its Truth Table
4. Make the connections as per the pin diagram of IC-74LS138 and Verify its Truth Table
5. Make the connections as per the Logic circuit of given function and Verify its Truth Table

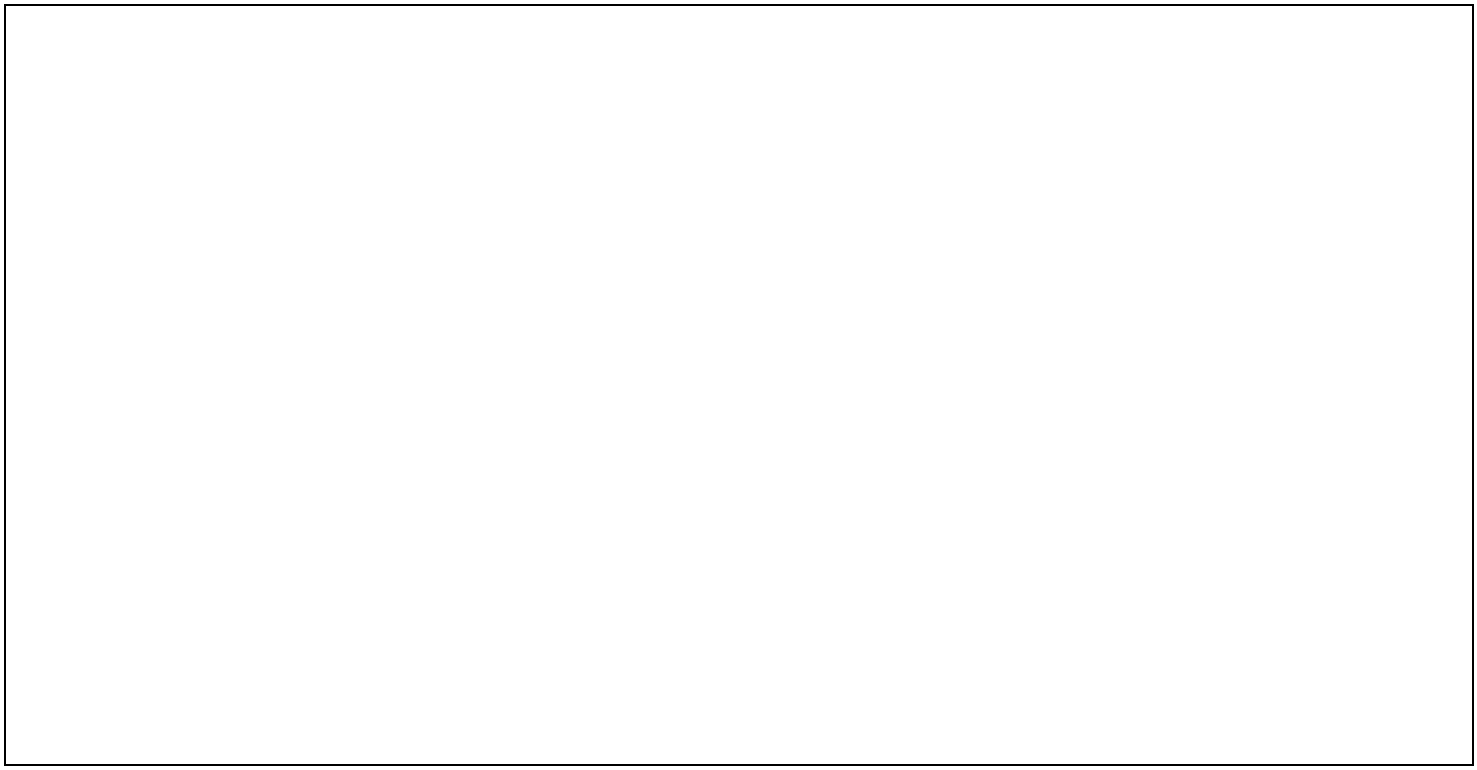
Design of Multiplexer

Function Table: IC-74LS153

Chip Enable I/P		Select Input		OUTPUT	
1E	2E	S_1(MSB)	S_0(LSB)	MUX-I (1Y)	MUX-2 (2Y)
0	0	0	0		
0	0	0	1		
0	0	1	0		
0	0	1	1		

Logical Expression:

Logic Diagram:



Design of 8:1 MUX.using IC-74LS153

Design Table:

S2 (MSB)	S1	S0 (LSB)	OUTPUT (Y)
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

Logical Expression:

Logic Diagram:

Design of Realization of Boolean expression using IC-74LS153

F(A,B,C,D)=Σ( )

(LSB Variable Reduction Method)

Decimal Equ.	A (MSB) (s2)	B (s1)	C (so)	D (LSB)	OUTPUT Y	Derived Logic
0	0	0	0	0		
1	0	0	0	1		
2	0	0	1	0		
3	0	0	1	1		
4	0	1	0	0		
5	0	1	0	1		
6	0	1	1	0		
7	0	1	1	1		
8	1	0	0	0		
9	1	0	0	1		
10	1	0	1	0		
11	1	0	1	1		
12	1	1	0	0		
13	1	1	0	1		
14	1	1	1	0		
15	1	1	1	1		

Logic Diagram:

Design of Realization of Boolean expression using IC-74LS153

F(A,B,C,D)=Σ( )

(MSB Variable Reduction Method)

Decimal Equ.	A (MSB) (s2)	B (s1)	C (so)	D (LSB)	OUTPUT Y	Derived Logic
0	0	0	0	0		
1	0	0	0	1		
2	0	0	1	0		
3	0	0	1	1		
4	0	1	0	0		
5	0	1	0	1		
6	0	1	1	0		
7	0	1	1	1		
8	1	0	0	0		
9	1	0	0	1		
10	1	0	1	0		
11	1	0	1	1		
12	1	1	0	0		
13	1	1	0	1		
14	1	1	1	0		
15	1	1	1	1		

Implementation Table:

Logic Diagram:

Design of Decoder

Function Table : IC-74LS138

Chip Enable Input			Active Low Output							
G_3	G_2	G_1	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
1	0	0								
1	0	0								
1	0	0								
1	0	0								
1	0	0								
1	0	0								
1	0	0								
1	0	0								

Logical Expression:

Logic Diagram:

Design of Realization of Boolean expression using IC-74LS138

F(A,B,C,D)=Σ( )

Decimal Equ.	A	B	C	OUTPUT F(A,B,C)
0	0	0	0	
1	0	0	1	
2	0	1	0	
3	0	1	1	
4	1	0	0	
5	1	0	1	
6	1	1	0	
7	1	1	1	

Logical Expression:

Logic Diagram:

Logic Gates / MSI Device required for Implementation:

Sr.No.	Title	Name of the IC	Number of Gates required	IC Required
01	Design of 8:1 MUX.			
02	Realization of Boolean expression using LSB reduction method			

03	Realization of Boolean expression using MSB reduction method			
04	Realization of Boolean expression using Decoder IC			

CONCLUSION:

REFFRENCE:

1. **R.P.Jain "Modern Digital Electronics" TMH 4th Edition**
2. **D.Leach,Malvino,Saha,"Digital Principles and Applications",TMH**

Subject teacher Sign with Date Remark