CLASS : S.E. COMP **SUBJECT : DEL**

EXPT. NO. : 11 **DATE :**

TITLE : SEQUENTIAL LOGIC DESIGN USING VHDL

OBJECTIVE :

1. Design and simulation of 4-bit Asynchronous UP/DOWN Counter using mode control Input (M) (Use Behavioral Modeling style)
   When M=0;Circuit perform UP-Counting operation
   When M=1;Circuit perform DOWN-Counting operation

2. Design and simulation of 4-bit Asynchronous UP/DOWN Counter using mode control Input (M) using T-Flip-flop as a Component
3. Design and simulation of 4-bit synchronous UP/DOWN Counter using mode control input(M) using T-Flip-flop as a Component

SOFTWARE : Modelsim version 6.5

THEORY : Counter is a sequential logic design which can be used to count the number of clock pulses given to the circuit. Counter can be classified into two categories: Asynchronous and Synchronous. Asynchronous counter output of the first flip-flop goes to the clock input of next flip-flop and so on. Inputs of all flipflop are connected to Logic 1 (VCC) because counter is a frequency divider application and being a suitable flip-flop is a T-flip-flop.

Asynchronous counter is is easy to design as compared to Synchronous counter circuit

but Synchronous counter is faster than the Asynchronous counter.

PROCEDURE :

- Create a project in modelsim.
- Create a file.
- Library Declaration
- Entity Declaration
- Architecture Declaration
- Code writing using Behavioral / Structural modeling style
- End

CONCLUSION:

REFFRENCE:

1. **R.P.Jain "Modern Digital Electronics" TMH 4th Edition**
2. **J.Bhaskar " VHDL Primer S"Prentice Hall 3rd Edition**
3. **Douglas Perry" VHDL Programming by Example"TMH 4th Edition**

Subject teacher Sign with Date Remark