```
1   `timescale 1ns / 1ps
2
3   ////////////////////////////////////////////////////////////////////////////////
4   // Company:
5   // Engineer:
6   //
7   // Create Date:   12:48:37 06/25/2021
8   // Design Name:   I2C_Master
9   // Module Name:   E:/Documents/Books & Notes/SEMESTER 4/DIGITAL SYSTEM DESIGN USING
    VERILOG/Open Ended/Code/I2C_Verilog/I2C_Master.v
10  // Project Name:  I2C_Verilog
11  // Target Device:
12  // Tool versions:
13  // Description:
14  //
15  // Verilog Test Fixture created by ISE for module: I2C_Master
16  //
17  // Dependencies:
18  //
19  // Revision:
20  // Revision 0.01 - File Created
21  // Additional Comments:
22  //
23  ////////////////////////////////////////////////////////////////////////////////
24
25  module I2C_TestBench;
26
27     // Inputs
28     reg clk;
29     reg rst;
30     reg [6:0] addr;
31     reg [7:0] data_in;
32     reg enable;
33     reg rw;
34
35     // Outputs
36     wire [7:0] data_out;
37     wire ready;
38
39     // Bidirs
40     wire i2c_sda;
41     wire i2c_scl;
42
43     // Instantiate the Unit Under Test (UUT)
44     I2C_Master master (
45        .clk(clk),
46        .rst(rst),
47        .addr(addr),
48        .data_in(data_in),
49        .enable(enable),
50        .rw(rw),
51        //.data_out(data_out),
52        .ready(ready),
53        .i2c_sda(i2c_sda),
54        .i2c_scl(i2c_scl)
55     );
56
```

```
57
58      I2C_Slave slave (
59       .sda(i2c_sda),
60       .scl(i2c_scl)
61       );
62
63      initial begin
64         clk = 0;
65         forever begin
66            clk = #1 ~clk;
67         end
68      end
69
70      initial begin
71         // Initialize Inputs
72         clk = 0;
73         rst = 1;
74
75         // Wait 100 ns for global reset to finish
76         #100;
77
78         // Add stimulus here
79         rst = 0;
80         addr = 7'b1000100;
81         data_in = 8'b11110110;
82         rw = 0;
83         enable = 1;
84         #10;
85         enable = 0;
86
87         #500
88         $finish;
89
90      end
91   endmodule
```