



Centre of Excellence in VLSI

# CERTIFICATE OF COMPLETION

*This is to certify that*

**YASH ANAND SHINGAVI**

*has successfully completed*

**RISC-V RV32I RTL Design using Verilog HDL**

*Online Course on 23rd day of June 2023*

*Celebrating*  
**10 YEARS**  
*Of Excellence*



**SIVAKUMAR P R**  
CEO, MAVEN SILICON

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