Application Reference Slip

Application No	: **3310205523**	Name	: **YASH DADASAHEB SHELAR**
Application Date	: **27-08-2023**	Date of Birth	: **16-11-2004**
Blood Group	: **Unknown**	Father	: **DADASAHEB SARJERAO SHELAR**
Applicant Gender	: **Male**		

Services Requested	Documentary Proof Required
1. ISSUE OF NEW DL (MCWG)	**• Learner Licence/LLs together** **• Address Proof (Present)**

Your application is accepted for processing and quote this Application Number 3310205523 for all future reference .

An SMS has been sent to your registered mobile Number : ******6008 .

Note 1: Applicant should take print out of the **Application Form (pre filled)** and duly signed with all required Documents to the concerned RTO / RLA office.

2: The online facility of application submission, upload documents, payment of fees, slot booking etc., does not complete the process of issue of Driving Licence or any other Service requested. The applicant has to compulsorily visit the concerned Road Transport Office to finish the process of issue of Driving Licence and/or any other associated services.

3: Applicants are requested to note that after completion of all stages mentioned under `Applicant Stages', the applicant has to visit the concerned Road Transport Office on the scheduled date of appointment, along with the necessary documents to complete the remaining process **(or)** In cases where online slot booking facility is not available for any particular RTO, the applicant has to go to the concerned Road Transport Office at the earliest along with the necessary documents, to complete the remaining process.

For any reference visit: https://sarathi.parivahan.gov.in/sarathiservice

Applicant Address :

PANCHARATNA MHADA SANKUL 3-C/401 ANANDI SADAN
MANKHURD
MAHARASHTRA NAGAR
Pincode : 400088

RTO Location :

RTO,MUMBAI (EAST)
B-2, 3RD FLOOR, WADALA
WADALATRUCK TERMINAL,
MUMBAI(E),MUMBAI
PinCode: 400037
Phone: 02224036479
View RTO Location

- **Application Form (pre filled)**
- **Print Acknowledgement**

NAME: YASH SHELAR
SE COMPS C31
ROLL NO: 2203153

THADOMAL SHAHANI TSEC ENGINEERING COLLEGE

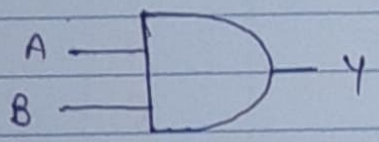
Experiment 2

AIM: To verify the truth table of various logic gates using ICs.

1) AND gate

The output of AND gate is 1 if & only if both inputs are high

Symbol:



Equation

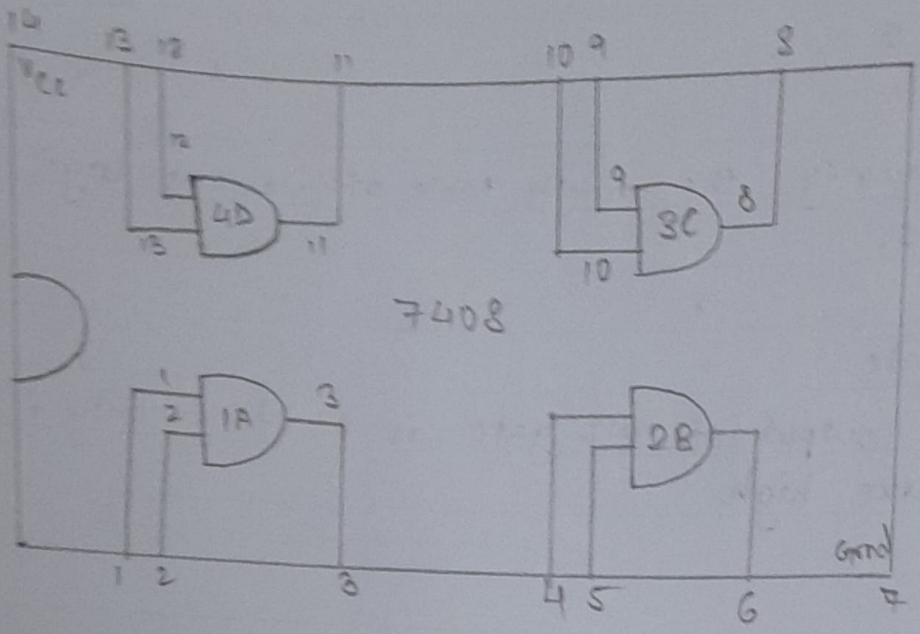
$Y = A \cdot B$

Truth table:

INPUT		OUTPUT
A	B	Y
1	1	1
1	0	0
0	1	0
0	0	0

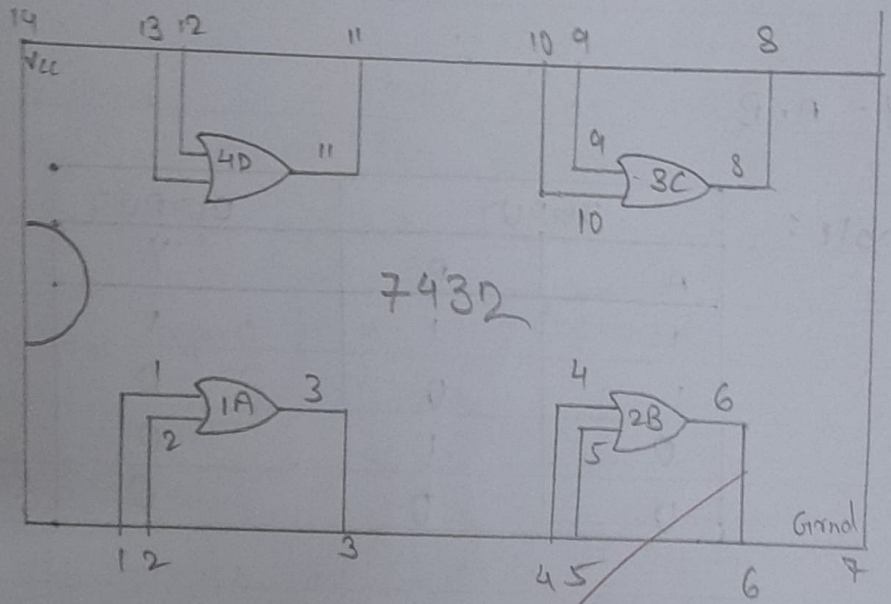
2) OR gate

The output of an OR gate is 1 if & only if one or more inputs are 1

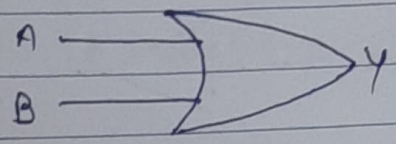


2 I/P AND GATE

2 I/P OR GATE



Symbol :



Equation :

$$Y = A + B$$

Truth table :

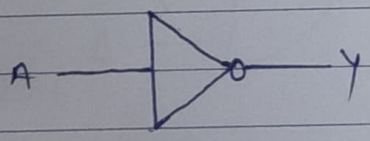
Input		Output
A	B	Y
1	1	1
1	0	1
0	1	1
0	0	0

3) NOT Gate

The NOT operation is also referred as ~~impar~~ inversion or complementation. As it inverts the value.

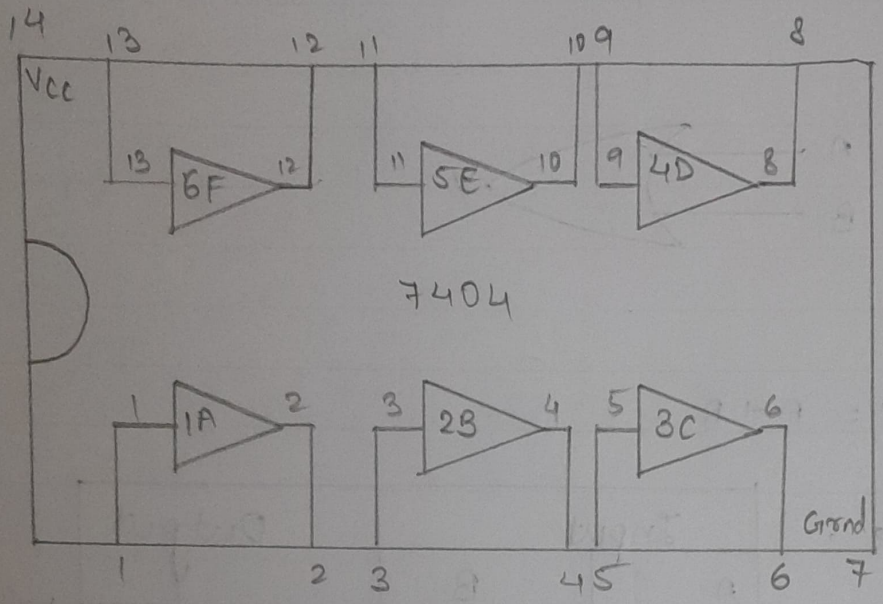
Equation : $Y = \bar{A}$

Symbol :



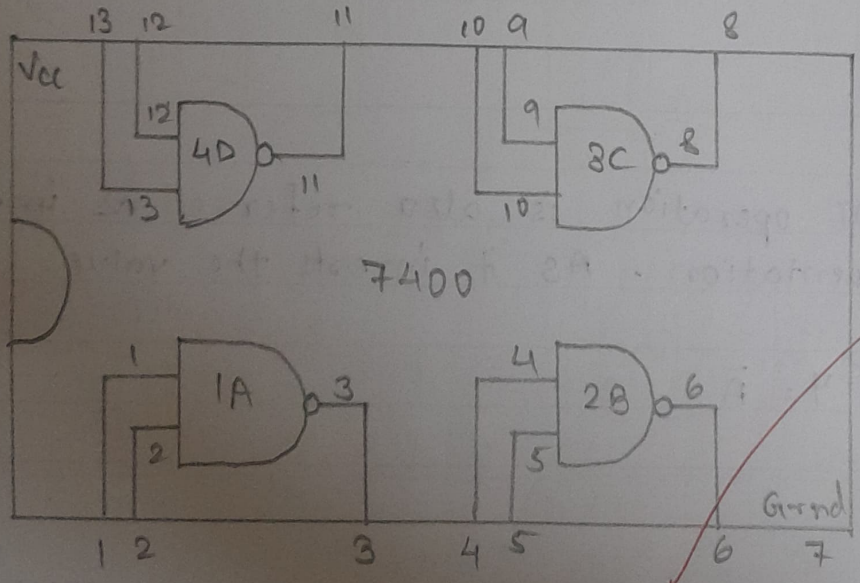
Truth table :

Input	Output
A	Y
1	0
0	1



NOT GATE

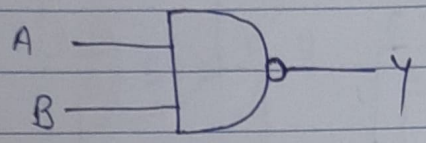
2I/P NAND GATE



4) NAND gate

NAND is a combination of AND gate & NOT gate

Symbol:



Equation:

$$Y = \overline{A \cdot B}$$

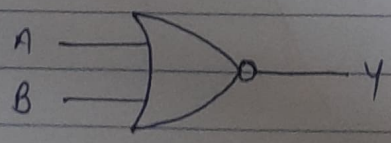
Truth table:

Input		Output
A	B	Y
1	1	0
1	0	1
0	1	1
0	0	1

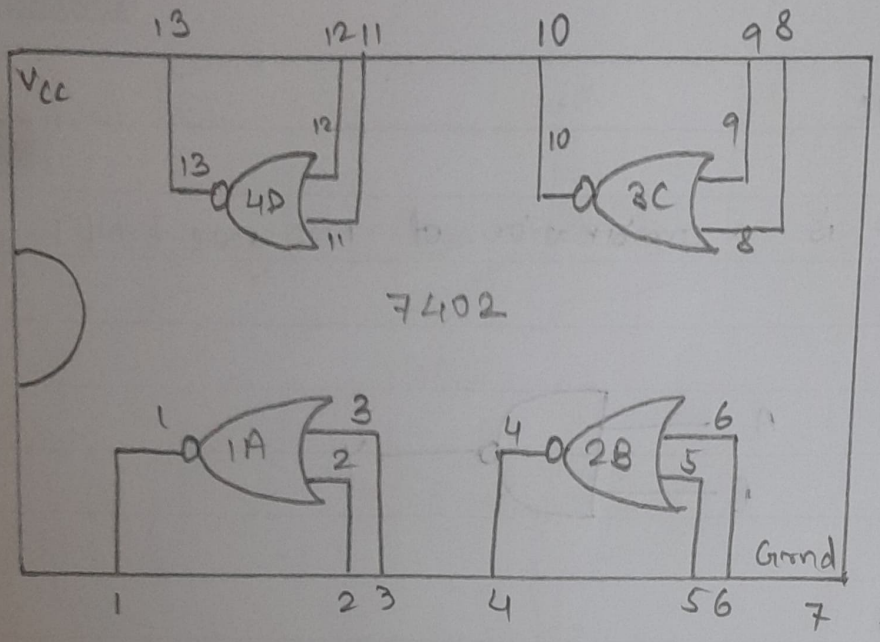
5) NOR gate

NOR is a combination of OR gate & NOT gate

Symbol:

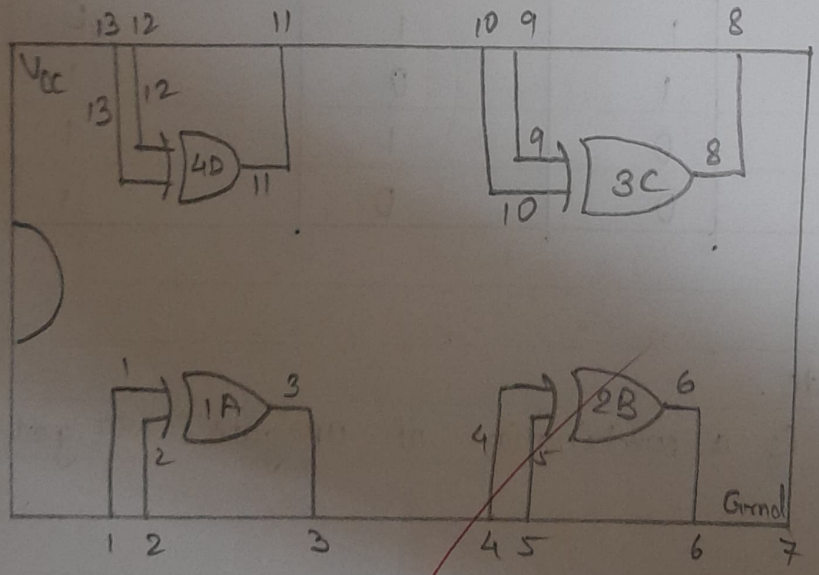


Equation: $Y = \overline{A+B}$



2 I/P NOR GATE

2 I/P EX-OR GATE



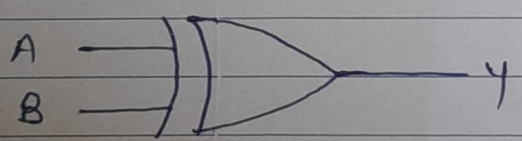
Truth table :

INPUT		OUTPUT
A	B	Y
1	1	0
1	0	0
0	1	0
0	0	1

6) EX-OR gate

It is widely used in digital circuits. It is not a basic operation.

Symbol :



Equation : A EX-OR B = $A \oplus B = \bar{A} \cdot B + A \cdot \bar{B}$

Truth table :

Input		Output
A	B	Y
1	1	0
1	0	1
0	1	1
0	0	0

Conclusion : Thus we have verified basic logic GATES

29.08.2023