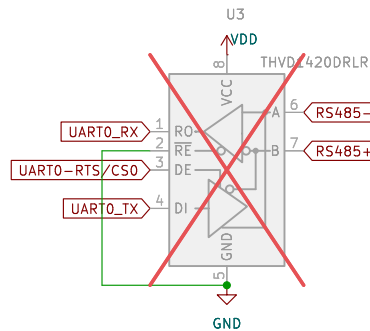
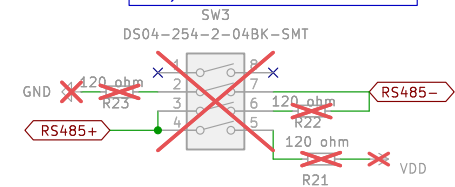


Have pullups on all the Chip select lines to the shift reg, because I have tied the two clocks together and if the outputs are disabled they will be floating, there is no buffer



Can't populate due to parts not being available from China. Will have to manually populate



I really wanted to have Bias and termination resistors optional per device, but space constraints are real, and extra switches on board really does not make sense

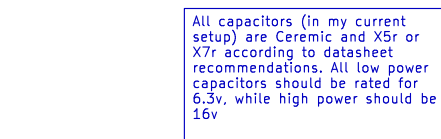
Author: Asher Edwards
Licensed under CERN-OHL-S v2

Sheet: /Periphery/
File: Periphery.kicad_sch

Title: CACKLE – Hub/Periphery

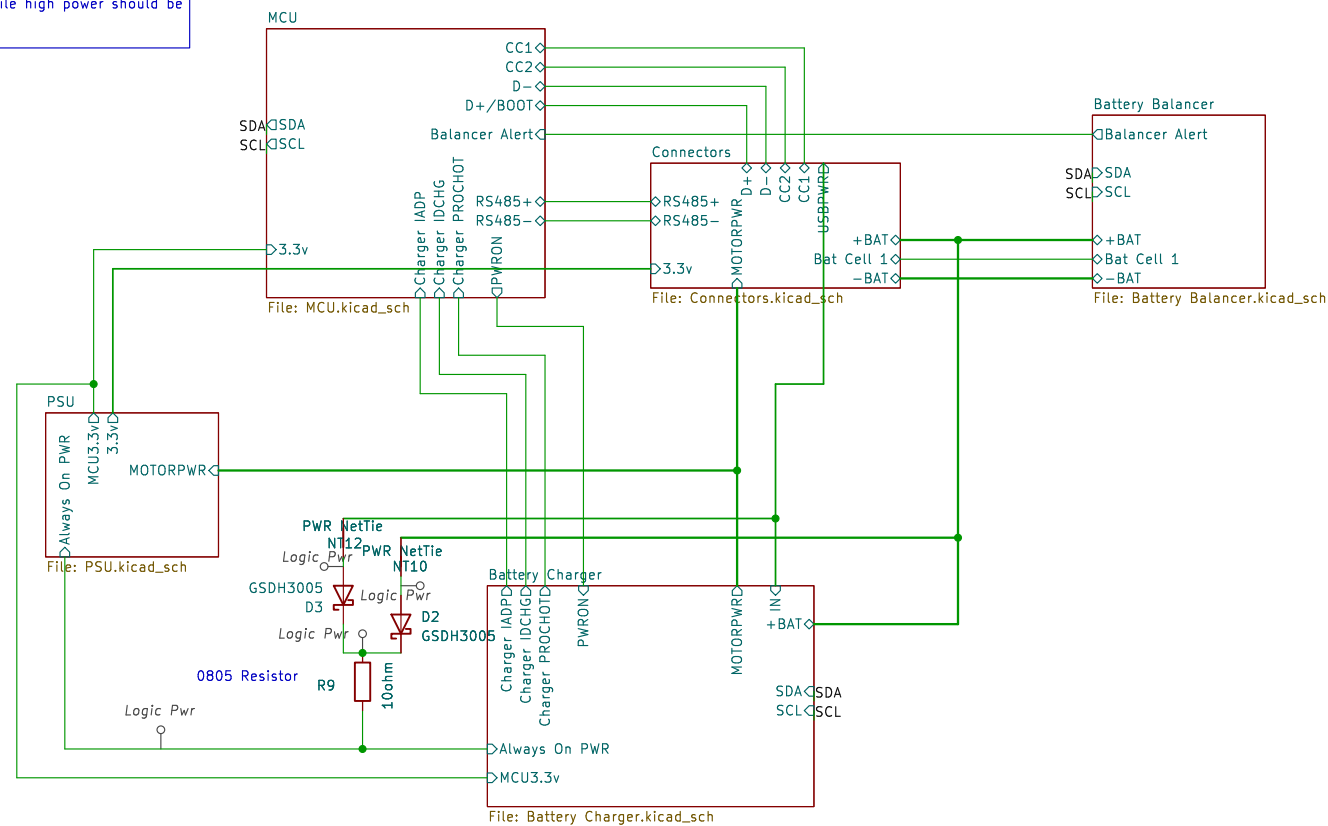
Size: A4 Date: 2024-10-08
KiCad E.D.A. 8.0.7

Rev: V1
Id: 3/3



Several components are not orderable from JLCPCB, or cannot be assembled by them (the power edge connectors). So I have added DNP indicators on those

all
mosfets I
currently
have are
not on
jlcpb



I might want to find a better diode for blocking current, but 0.01ma leakage doesn't seem bad

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Author: Asher Edwards

Sheet: /

File: 2s 40A PSU and charger.kicad_sch

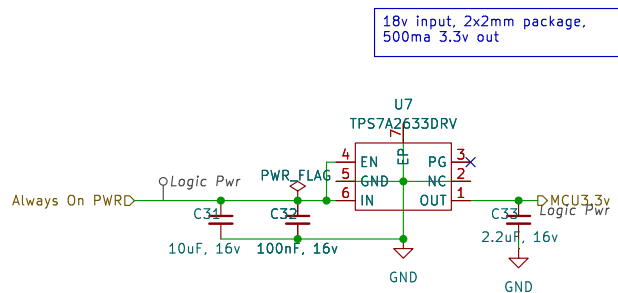
Title: CACKLE 2s 40A PSU & Charger

Size: A4 Date: 2024-12-23

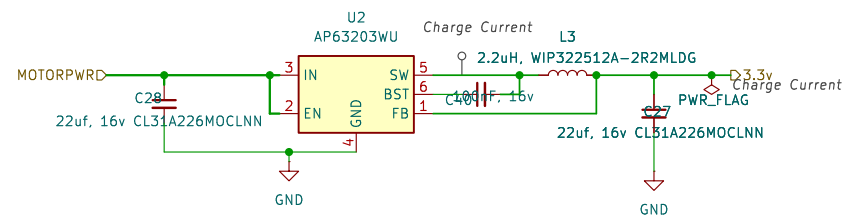
KiCad E.D.A. 8.0.7

Rev: V1

Id: 1/6



Onboard MCU 3.3v Supply, 100mA



Main 3.3v Supply, 2A

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Author: Asher Edwards

Sheet: /PSU/

File: PSU.kicad_sch

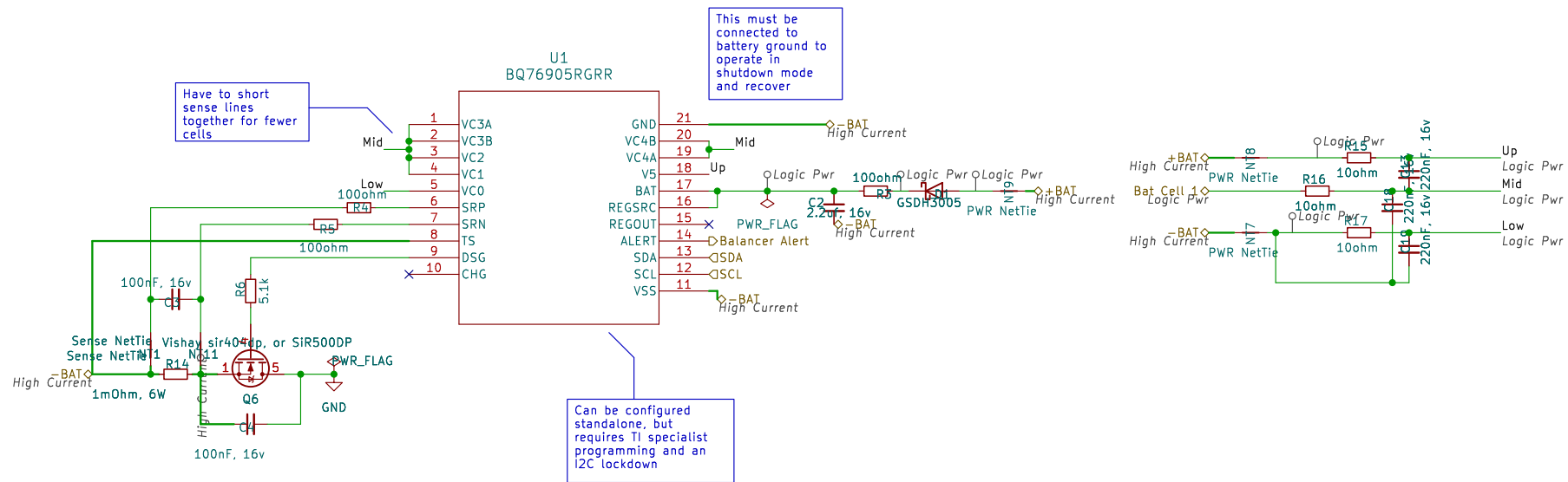
Title: CACKLE 2s 40A PSU & Charger

Size: A4 Date: 2024-12-23

KiCad E.D.A. 8.0.7

Rev: V1

Id: 2/6



Licensed under CERN-OHL-S

Author: Asher Edwards

Sheet: /Battery Balancer/

File: Battery Balancer.kicad_sch

Title: CACKLE 2s 40A PSU & Charger

Size: A4

Date: 2024-12-23

Rev: V1

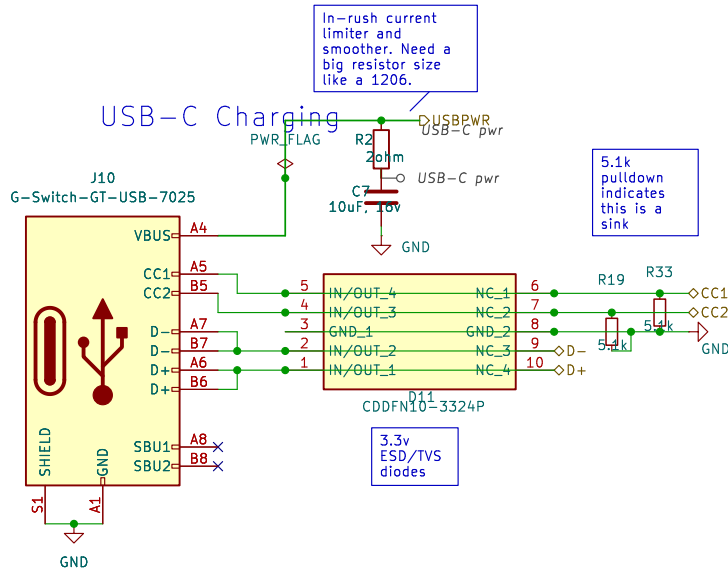
KiCad E.D.A. 8.0.7

Id: 4/6

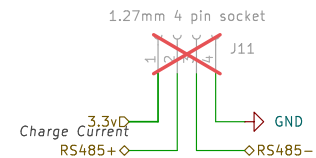
Inputs Outputs

USB-C Charging

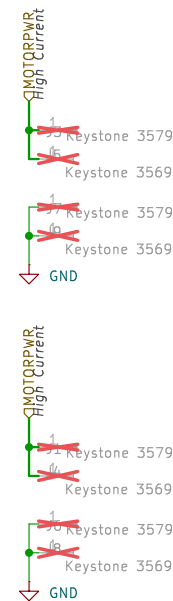
Possible USB-C connectors:
G-Switch 7025 (shorter). G-switch 7010asv



Hubs Connector

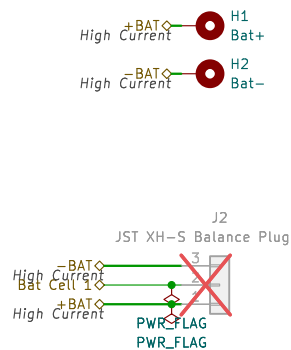


Driver Power



Not populated due to custom handling required, and the parts aren't available from China.

Battery Plugs



Licensed under CERN-OHL-S

Author: Asher Edwards

Sheet: /Connectors/

File: Connectors.kicad_sch

Title: CACKLE 2s 40A PSU & Charger

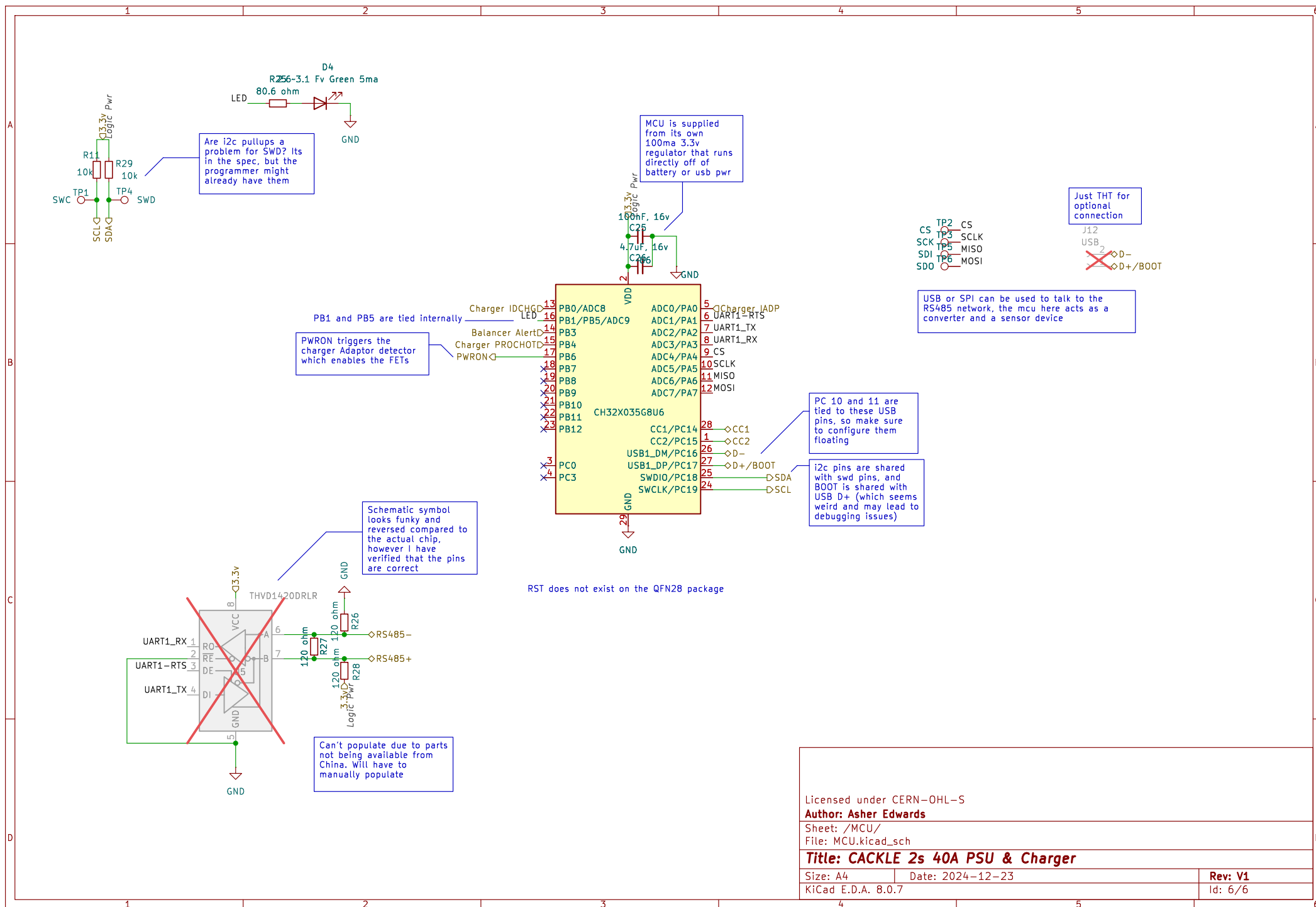
Size: A4

Date: 2024-12-23

Rev: V1

KiCad E.D.A. 8.0.7

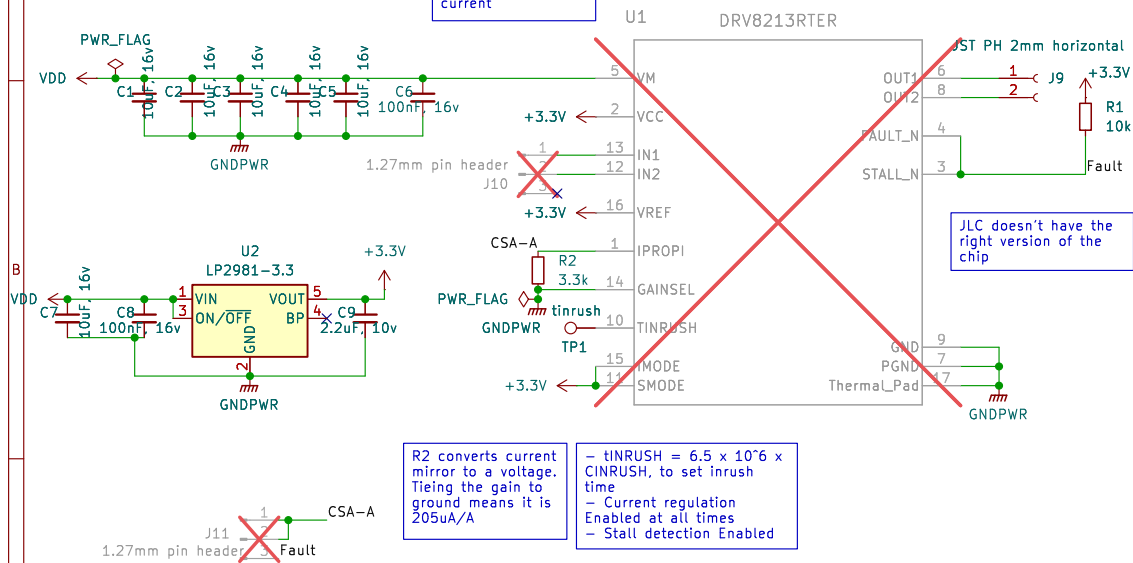
Id: 5/6



Any capacitors on the power supply line should be rated above my intended voltage range of 3.7–7.4v
The bulk capacitance on VM should also be really high

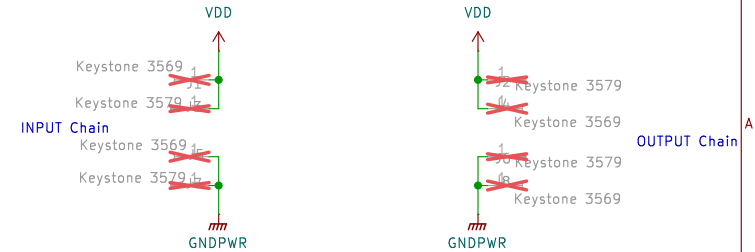
$VIPROPI(V) = IPROPI(A) \times RIPROPI(\Omega)$
Max of 2.05v on output w/3.3v VM. Needs 1.25v headroom to maintain accuracy.
 $OCP\ is\ =\ (VVREF(V) / RIPROPI(\Omega)) / AIPROPI(\mu A/A)$
In my case, that is 4.7 A

GAIN sel to ground has 205uA/A gain, allowing the max current



R2 converts current mirror to a voltage. Tying the gain to ground means it is 205uA/A

– $tINRUSH = 6.5 \times 10^{-6} \times CINRUSH$, to set inrush time
– Current regulation Enabled at all times
– Stall detection Enabled



JLC doesn't have these parts, and I need to add some custom processing to cut the 3569 parts in half, so not populated

Sheet: /
File: DRV8213 brushed Motor Driver.kicad_sch

Title:

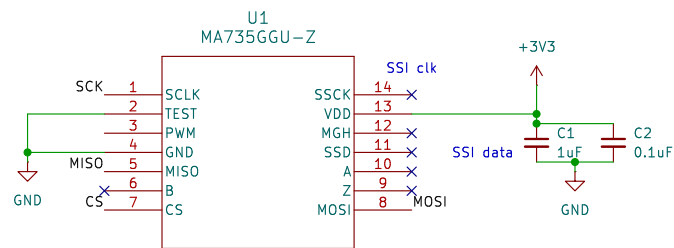
Size: A4

Date: 2024-08-17

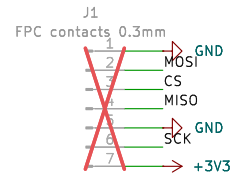
Rev: V1

KiCad E.D.A. 8.0.7

Id: 1/1



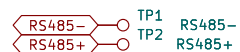
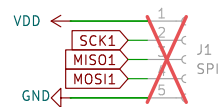
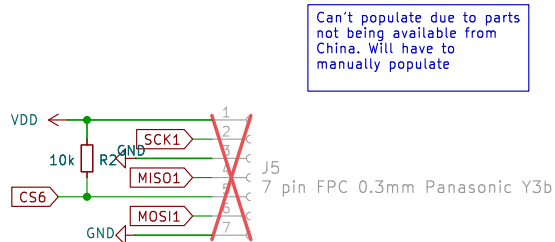
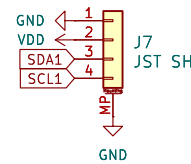
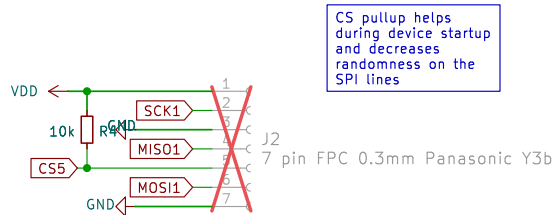
Internal pulldowns
on all SPI lines



Ideally each signal line is
next to a ground line.
However, this is an
extremely space limited
part so the most natural
wiring from the chip out
takes priority. CS kinda
acts like ground when it
is selected

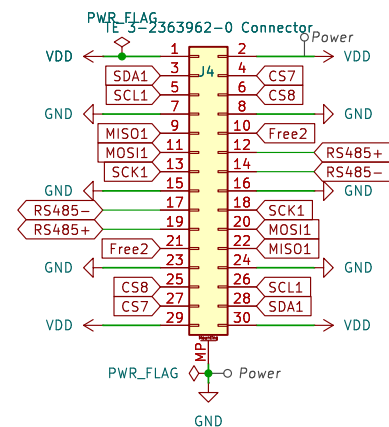
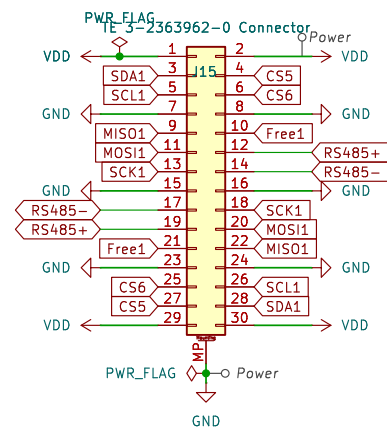
Supports SPI mode 0 or 3,
automatically

Sheet: /		
File: MA735 encoder board.kicad_sch		
Title:		
Size: A4	Date:	Rev:
KiCad E.D.A. 8.0.7	Id: 1/1	



The CS pins can be used as a generic output, but they are only expected to be digital outputs (some hubs use a shift register on these). Free1 can be anything

Bottom Side Plugs



Author: Asher Edwards

Sheet: /
File: 2 connector Sensor Board.kicad_sch

Title: Two connector sensor board

Size: A4 Date: 2024-12-27

KiCad E.D.A. 8.0.7

Rev: V1

Id: 1/1