

Switching Characteristics and Datasheet Realisation of MOSFET

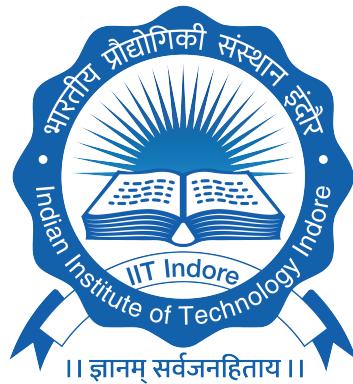
B .Tech. Project

*Submitted in partial fulfillment of the requirements
of the degree of*
Bachelor of Technology
in
Electrical Engineering

By

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Under the guidance of
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Dec. 2025

Declaration

I hereby declare that the project entitled “Switching Characteristics and Datasheet Realisation of MOSFET ” submitted in partial fulfillment for the award of the degree of Bachelor of Technology in ‘Electrical Engineering ’ completed under the supervision of Dr. B . Prathap Reddy, Assistant Professor, Electrical Department, IIT Indore is an authentic work.

Further, I declare that I have not submitted this work for the award of any other degree elsewhere.

I declare that this written submission represents my ideas in my own words and where other's ideas or words have been included, I have adequately cited and referenced the original sources. I also declare that I have adhered to all principles of academic honesty and integrity and have not misinterpreted or fabricated or falsified any idea/data/fact/source in my submission. I understand that any violation of the above will be cause for disciplinary action by the institute and can also evoke penal action from the sources which have thus not been properly cited or from whom proper permission has not been taken when needed.

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Date: 03-12-2025

Place: IIT Indore

Preface

This report on “**Switching Characteristics and Datasheet Realisation of MOSFET** ” is prepared under the guidance of Dr.B.Prathap Reddy.

This report presents the study and analysis of MOSFET switching behaviour, gate-driver design, and converter performance as part of my project work. The objective of this work was to understand how practical switching characteristics differ from datasheet values and to evaluate the influence of gate drivers, switching conditions, and test methods such as the Double Pulse Test. The study also includes implementation of non-isolated and isolated gate-driver circuits, hardware evaluation, simulation analysis in LTspice, and verification of MOSFET performance in asynchronous and synchronous buck converters.

This project has helped me gain deeper insight into device-level behaviour, driver requirements, and efficiency considerations in real power-electronics systems. I sincerely thank my guide, faculty members, and laboratory staff for their support and assistance throughout the completion of this work. I also acknowledge all resources and references that contributed to the successful development of this report.

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B. Tech. Project Approval Certificate

This is to certify that the dissertation titled "**Switching Characteristics and Datasheet Realisation of MOSFET**" submitted by , (Roll No. 220002032) is approved for the award of degree of **Bachelor of Technology** in **Electrical Engineering**.



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A special gratitude and love goes to my family for their unfailing support.

Abstract

This project studies how the IRF840 MOSFET behaves during switching by testing different types of gate drivers—including a basic non-isolated driver, the TLP250 isolated driver, and the more advanced TLP5214 smart driver. Their effect on gate current, dv/dt , and switching times is examined through design calculations, LTspice simulations, and hardware testing. The study also uses a Double Pulse Test (DPT) to accurately measure turn-on and turn-off delays, rise and fall times, diode reverse-recovery, and switching energy. Pulses are generated using the TMS320F28379D Launchpad with DSP programming in Code Composer Studio. The measured switching parameters such as Q_{gs} , Q_{gd} , Q_g , $td(on)$, $td(off)$, tr , tf , and diode recovery traits are compared with datasheet values to confirm the reliability of the results.

The project also applies the MOSFET analysis to practical power-electronics circuits by building both an asynchronous buck converter and a synchronous buck converter. These setups help examine how gate resistance, switching frequency, and the type of gate driver affect conduction loss, switching loss, and overall efficiency. This practical work connects datasheet theory with real operating behavior, giving a clearer understanding of how a MOSFET actually performs in a converter. The efficiency results from both converters highlight the balance between switching speed, losses, and performance in real designs.

The experimental results closely matched the datasheet values, showing that the measurement methods and test setup were accurate and reliable. The study offers useful understanding of how MOSFETs behave, how to choose the right gate driver, and how to reduce switching and conduction losses—important factors for designing efficient power converters.

The combined findings from the driver testing, Double Pulse Test, and converter experiments give a complete picture of the MOSFET’s switching performance. These results are also used to support an algorithm developed for future work, which can automatically estimate datasheet parameters from real switching data. This approach moves toward smarter, data-driven MOSFET characterization for advanced power-electronics applications.

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List of Abbreviations

MOSFET → Metal-Oxide-Semiconductor Field-Effect Transistor

IGBT → Insulated Gate Bipolar

PWM → Pulse-Width Modulation

UVLO → Under Voltage Lockout

DESAT → Desaturation

DPT → Double Pulse Test

EMI → Electromagnetic Interference

BJT → Bipolar Junction Transistor

DSP → Digital Signal Processing

DC → Direct Current

IC → Integrated circuit

Nomenclature

Symbols

V_{in}	Input voltage (V)
V_o	Output voltage (V)
V_{gs}	Gate-source voltage (V)
V_{ds}	Drain-source voltage (V)
R_g	Gate resistance (Ω)
Q_{gs}	Gate-source capacitance (C)
Q_{gd}	Gate-drain capacitance (C)
Q_g	Total gate charge (C)
I_g	Gate current(A)
$t_d(on)$	Turn-on delay time (s)
t_r	Rise time (s)
$t_d(off)$	Turn-off delay time (s)
t_f	Fall time (s)
t_{off}	Turn-off time (s)
I_L	Inductor Current (A)
E_{on}	Turn-on energy (J)
E_{off}	Turn-off energy (J)
P_{sw}	Switching loss (W)
P_{con}	Conduction loss (W)

Chapter 1

Introduction

1.1 Introduction

MOSFET as a switch is most commonly used in power-electronic circuits due to their fast switching capability and ease of gate control, making their dynamic behaviour an essential area of study. The switching transition of a MOSFET is influenced by gate charge, parasitic capacitances, driver strength and gate resistance, which determine its overall performance and efficiency. This creates the need for practical evaluation of switching characteristics to understand how the device responds during turn-on and turn-off transitions. Gate driver circuits play a crucial role in shaping these transitions by controlling the charging and discharging of the gate. Analysing switching waveforms allows accurate measurement of delays, rise and fall times, and switching losses. Such understanding is essential for validating datasheet parameters and optimising MOSFET operation. This project focuses on these aspects to establish a clear link between theoretical specifications and practical device behaviour.

1.2 Motivation for BTP and Problem statement

The motivation for this project comes from the growing demand for better switching control, higher efficiency and reliable performance in modern power-electronic systems such as inverters, EV drives , SMPS, converters. The Fig. 1.1 and Fig. 1.2 shows us the necessity of MOSFET as a switch in everyday power electronic applications like design of solar inverters and electric vehicles.

Efficient switching control of power MOSFETs is vital to reducing losses and improving performance. Studying parameters such as delays, losses, and gate-charge behaviour helps improve driver design and overall circuit reliability. Furthermore, the need to simplify and speed up device characterisation motivates the development of an algorithm that can generate datasheet-level parameters from experimental switching results. This enables smarter, faster, and more accurate decision-making in power-electronics design.

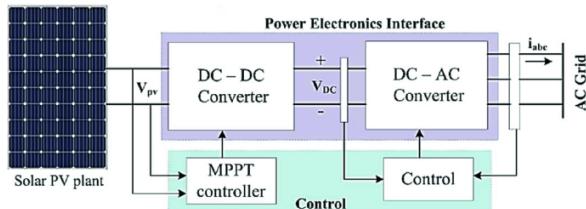


Figure 1.1: Block diagram of solar inverter with converters

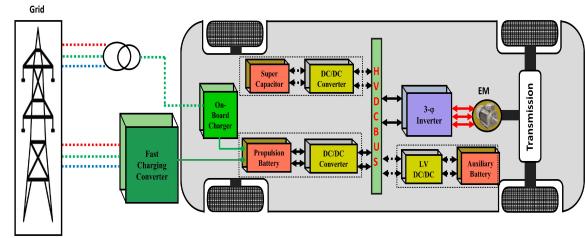


Figure 1.2: Block diagram of electric vehicle with converters

In light of these requirements, this project explores the switching characteristics of the IRF840 MOSFET using multiple gate-driver circuits and standard evaluation techniques like double pulse test, and investigates its behaviour in practical converter configurations. The introduction of an algorithm-based approach for datasheet parameter realisation further extends this work toward automated device characterization, addressing the growing need for intelligent analysis tools in modern power electronics design.

The problem statement aligns with the motivation which aims to

- Analyze MOSFET switching behavior (delays, losses)
- Optimize gate driver design
- Validate datasheet parameters through testing
- Apply to real-world power electronics applications

Chapter 2

Literature Review

2.1 Introduction

MOSFETs are frequently selected as the main switching components due to their rapid performance and simple gate control. It is a three-terminal device consisting of a gate, drain, and source. The gate voltage controls the current between the drain and source, making it a voltage-controlled device. Its dynamic behavior is significantly affected by parasitic capacitances like C_{gs} , C_{gd} , and C_{ds} , which impact gate-charge and the duration required for the device to switch ON or OFF. These capacitances (C_{gs} , C_{gd}) also lead to the Miller effect, influencing dv/dt and switching transitions [1]. Working primarily in switch mode, a MOSFET continuously charges and discharges its gate capacitances with each cycle, making factors such as delay time, rise time, and fall time crucial for performance evaluation. Grasping these traits lays the groundwork for assessing switching losses, driver efficiency, and the general performance of devices in real-world applications.

2.1.1 Gate current

A MOSFET turns ON when a positive peak gate current provided by the driver circuit flows into the gate, rapidly charging the gate capacitances and pushing V_{gs} above the threshold [1], causing the channel between the drain and source to form. It turns OFF when a negative peak gate current pulls charge out of the gate, discharging the capacitances and collapsing the channel.

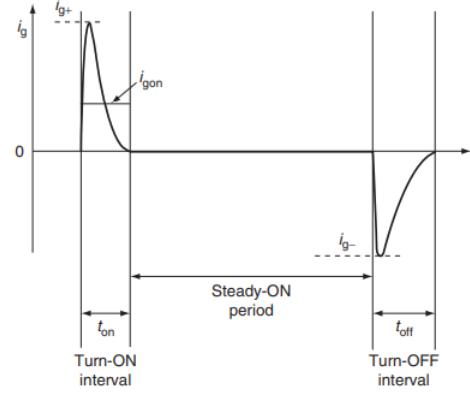


Figure 2.1: Gate current

The gate current appears as an impulse as shown in Fig. 2.1 because the gate behaves like a capacitor. It draws a large current only at the moment of charging or discharging, and once the voltage settles, the current naturally drops to nearly zero. Thus, only short, sharp current peaks are required to switch the MOSFET between its ON and OFF states. This can be understood by observing Fig. 2.1, which shows us the positive and negative peak impulsive currents only during turning on and turning off of the MOSFET. The gate current is zero during steady on and steady off periods [1].

2.1.2 MOSFET Turn-on mechanism

When the gate driver sends a voltage pulse that increases, a brief surge of current at the gate occurs due to the MOSFET gate being have as a capacitive point. This present powers the internal capacitances C_{gs} and C_{gd} depicted in Fig.2.2, resulting in V_{gs} should rise until it surpasses the threshold voltage, creating a conduction pathway to develop and the drain current to ascend. The C_{gd} charging in the Miller region additionally determines the drain-voltage transition [1].

2.1.3 MOSFET Turn-off mechanism

When the gate driver lowers the gate voltage, the accumulated the charge in the capacitances of the MOSFET gate discharges as illustrated in Fig. 2.3, generating a reverse gate current. C_{gs} and C_{gd} discharge their charge, causing V_{gs} to drop below the threshold. previous value, the channel breaks down, and the drain current defolds. The release of C_{gd} in the Miller area regulates the increase in drain voltage and finishes the turn-off [1].

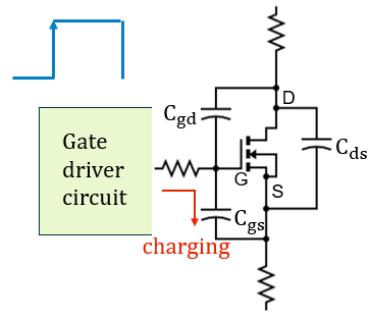


Figure 2.2: Gate charging

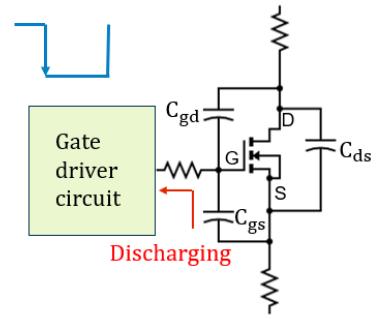


Figure 2.3: Gate discharging

2.2 Summary

The major factors influencing the MOSFET turn-on and turn-off are

- Gate-source voltage
- Gate resistance
- Gate Driver Strength (Drive Current)
- Gate capacitance
- Gate charge

Among these factors, gate resistance and gate driver greatly influence switching. These parameters are varied in the further parts of the report for better design and efficiency.

Chapter 3

MOSFET Gate Drivers

MOSFET gate drivers are tailored circuits that effectively manage the charging and discharging of the MOSFET gate capacitances, ensuring swift and dependable switching. Because the MOSFET gate functions as a capacitive load, the driver needs to provide brief pulses of high current to enable quick changes between ON and OFF states. Gate drivers assist in ensuring stable switching by supplying appropriate voltage levels, minimizing switching losses, and averting triggers caused by unwanted noise.

Features

- Provide the required gate voltage and current to switch the MOSFET quickly.
- Acts as power amplifiers and convert low-power control signals to high-current signals for the requirements of the MOSFET gate [3].
- Offer level shifting when the control signal voltage differs from the required gate voltage [3].
- Provide immunity from noise to prevent false triggering in high dv/dt conditions [3].
- Include protective functions such as UVLO (Under-Voltage Lockout), Miller clamping, dead-time control, and fault signaling [3].

These features are provided by various types of gate driver circuits such as Non-isolated gate driver with Push-pull circuit, Bootstrap circuit, charge pump and Non-isolated gate driver with Optocouplers, pulse transformer [3].

Out of all these types of gate driver circuits, we mainly analyse the design of non-isolated gate drivers with push-pull circuit and isolated gate driver with optocouplers like TLP250 , TLP5214.

3.1 Non-isolated gate driver

A non-isolated gate driver circuit for a MOSFET is an uncomplicated driver setup in which the control electronics and the power stage utilize the same ground. It amplifies

the low-level control signal from a microcontroller or PWM source, allowing the MOSFET gate to be turned on and off rapidly. Due to the absence of an isolation barrier, these drivers are small, affordable, and exhibit minimal delay. They typically incorporate a driver IC or buffer transistors together with gate resistors to control switching speed. Non-isolated drivers function effectively for low-side switching and various applications where the MOSFET's source is connected to the same ground as the controller.

3.1.1 Design and Simulation

The non-isolated gate driver uses a push-pull arrangement built from two NPN and one PNP transistor pair as shown in Fig.3.1, to provide both sourcing and sinking current to the MOSFET gate. When the input pulse from microcontroller turns on Q3 and Q3 turns ON Q1, the NPN transistor pulls the gate high through gate resistor, allowing the MOSFET to turn ON quickly by charging its gate capacitances.

When the input pulse goes low, Q2 conducts, rapidly pulling the gate to ground and discharging the gate capacitances, ensuring fast turn-OFF. Resistors set the base currents of the transistors, ensuring proper switching and protecting them from excessive drive. Load resistance at drain acts as the MOSFET load path, while body diode provides reverse-voltage protection for switching transients. Since the driver and power stage share a common ground, the circuit is non-isolated but delivers strong gate drive for fast switching.

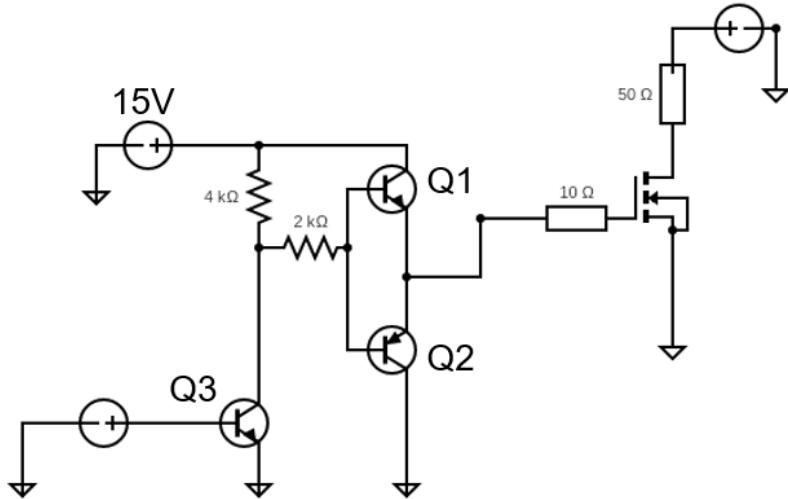


Figure 3.1: Design of non-isolated gate driver circuit

Calculations

Given the MOSFET parameters from the datasheet of IRF840:

$$V_{DS(max)} = 500 \text{ V}, \quad Q_{g(max)} = 63 \text{ nC}, \quad V_{GS(max)} = 20 \text{ V}$$

The total gate charge is related to the average gate current by: $Q_g = I_g \times t_{on}$

Assuming the switching transition time, $t_{on} = 0.5 \mu\text{s}$

The required gate current becomes:

$$I_g = \frac{Q_g}{t_{on}} = \frac{63 \text{ nC}}{0.5 \mu\text{s}} = 126 \text{ mA}$$

To ensure fast charging and to account for peak behaviour, the peak gate current is taken as:

$$I_{g(peak)} = 2 \times I_g = 2 \times 126 \text{ mA} = 252 \text{ mA}$$

The gate resistance is therefore calculated using: $R_g = \frac{V_{CC}}{I_{g(peak)}}$

Given the driver supply voltage: $V_{CC} = 15 \text{ V}$

$$R_g = \frac{15}{0.252} = 59.5 \Omega$$

Thus, the required gate/limiting resistance for the non-isolated gate driver is:

$$R_g \approx 60 \Omega$$

3.1.2 Simulation Results

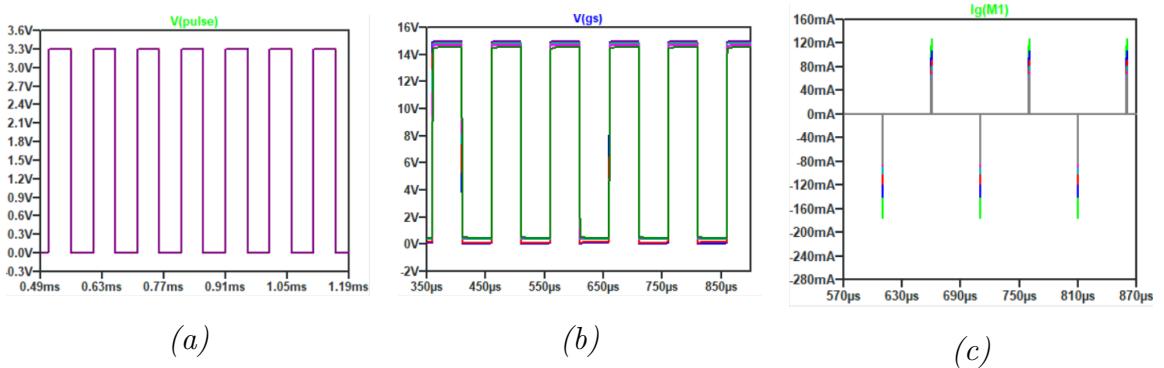


Figure 3.2: (a) Pulse of 3.3V at input of gate driver from microcontroller (X-axis:time ; Y-axis:Volatage) (b) V_{gs} of 15V at gate terminal provided by the gate driver(X-axis:time ; Y-axis:Volatage) (c)Positive and negative impulse currents at the MOSFET gate(X-axis:time ; Y-axis:Current)

The simulated waveforms in Figure 3.2 clearly demonstrate the correct operation of the gate-driver stage. The microcontroller provides a 3.3 V pulse, as shown in Fig. 3.2(a), which is successfully amplified by the gate driver to a 15 V V_{gs} signal at the MOSFET gate in Fig. 3.2(b). The corresponding gate-charge behaviour is observed in Fig. 3.2(c), where the positive and negative impulse currents during turn-on and turn-off transitions indicate rapid charging and discharging of the MOSFET's parasitic capacitances.

Figure 3.3 further illustrates the dynamic switching performance of the MOSFET. During the turn-on transient in Fig. 3.3(a), the drain current increases while V_{ds} decreases, whereas the opposite trend is observed during the turn-off transient in Fig. 3.3(b). Additionally, the presence of the Miller plateau in the V_{gs} waveform shown in Fig. 3.3(c) confirms correct modelling of the MOSFET's switching behaviour.

These results collectively verify the proper functioning of the MOSFET gate driver and confirm that the simulated switching dynamics align with expected device characteristics.

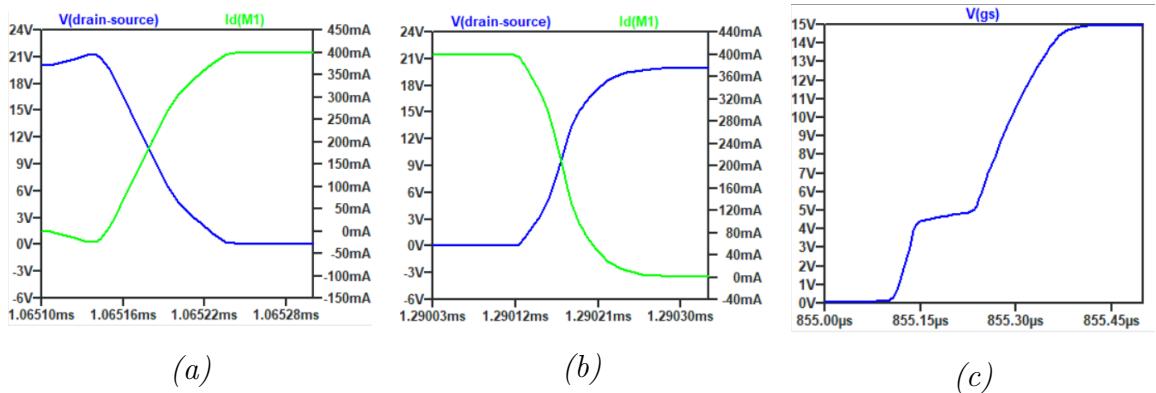


Figure 3.3: (a) Turn-on transient of MOSFET(X-axis:time ; Y-axis: Volatage) (b) Turn-off transient of MOSFET(X-axis:time ; Y-axis: Volatage) (c) Waveform of V_{gs} with miller plateau (X-axis:time ; Y-axis: Voltage)

3.1.3 Variation of Gate Resistance

By varying the gate resistance from 10 ohm to 100 ohm , the non-isolated gate driver circuit is simulated in LTspice to obtain the following results.

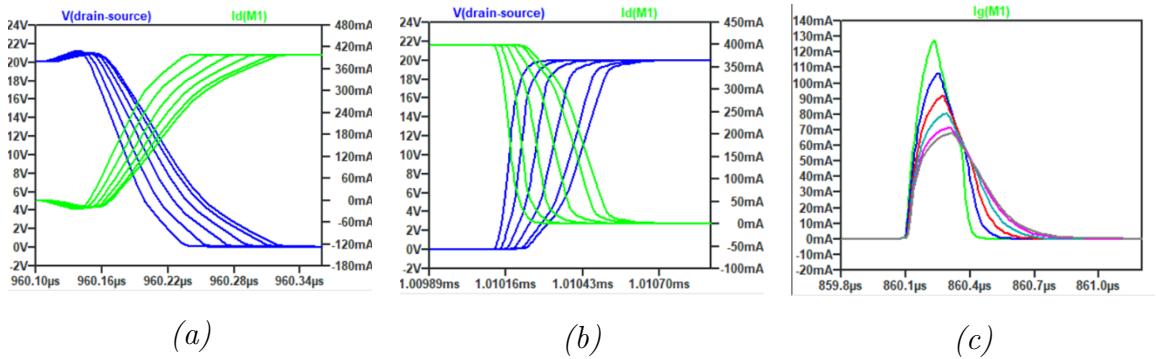


Figure 3.4: (a) Turn-on transient when gate resistance is varied (b) Turn-on transient when gate resistance is varied (c) Waveforms of gate current for different values of gate resistance

Table 3.1: Variation of parameters with gate resistance

Gate resistance (Ω)	Peak current (mA)	Turn-on time (ns)	Turn-off time (ns)
10	127.6	118	151.4
30	106.57	140	189
50	91.6	162	247
70	80.68	182.2	306.5
90	71.92	195.7	374
100	68.19	203.5	390.4

The simulated waveforms in Figure 3.4 show that increasing the gate resistance significantly affects the MOSFET's switching behaviour. As the resistance increases, the turn-on and turn-off slopes become slower, resulting in longer transition durations (Fig. 3.4(a),(b)). The gate current peaks reduce noticeably with higher resistance values, as seen in Fig. 3.4(c), indicating slower charging and discharging of the gate capacitances.

These trends are quantitatively confirmed in Table 3.1, where the peak current drops from 127.6 mA to 68.19 mA as gate resistance increases from 10ohm to 100ohm. Correspondingly, both turn-on and turn-off times increase, demonstrating the direct impact of gate resistance on switching speed and driver performance.

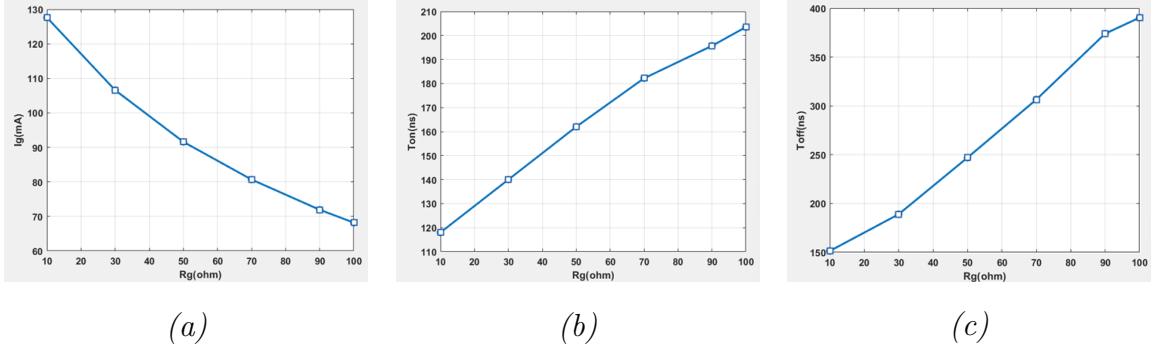


Figure 3.5: (a) Variation of peak gate current with gate resistance (b) Variation of turn-on time with gate resistance (c) Variation of turn-off time with gate resistance

Calculation of gate charge:

$$Q_{gs} = I_{avg} \cdot \Delta t$$

$$Q_{gs} = 80 \text{ mA} \times 0.12 \mu\text{s} = 9.6 \text{ nC}$$

$$Q_{gd} = 85 \text{ mA} \times 0.24 \mu\text{s} = 20.4 \text{ nC}$$

$$Q_g = Q_{gs} + Q_{gd} = 9.6 + 20.4 = 30 \text{ nC}$$

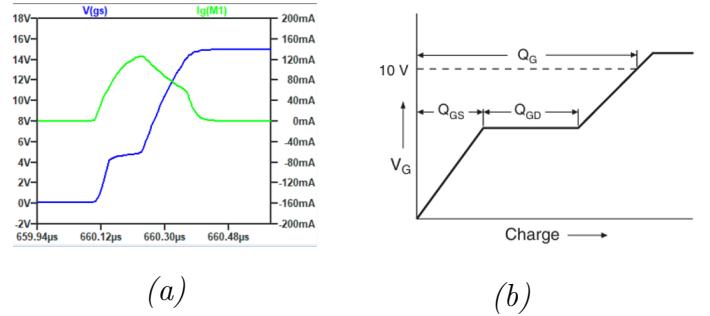


Figure 3.6: (a) Waveform of V_{gs} and I_g (b) Gate charge waveform

The gate-charge plot in Fig.3.6 illustrates the variation of gate voltage and gate current during the MOSFET turn-on process. The total gate charge is computed by multiplying the average gate current with the time interval of each charging region, namely Q_{gs} and Q_{gd} . The quantity Q_{gs} is obtained from the initial rise of V_{gs} , while Q_{gd} corresponds to the Miller plateau where V_{gs} remains nearly constant [3]. Adding these components yields the total gate charge Q_g , which represents the energy required by the driver to fully turn on the MOSFET.

3.1.4 Hardware Setup and Results

The non-isolated gate driver is implemented on a prototype board as shown in Fig. 3.7, using discrete transistors, resistors, and a gate resistor to shape the MOSFET's switching behaviour. A PWM pulse generated from the LaunchPad microcontroller drives the gate driver circuit, ensuring controlled turn-on and turn-off transitions. A regulated DC power supply provides the required operating voltages for both the driver stage and the MOSFET load. The oscilloscope monitors the output waveform, confirming proper switching and stable operation of the non-isolated driver setup.

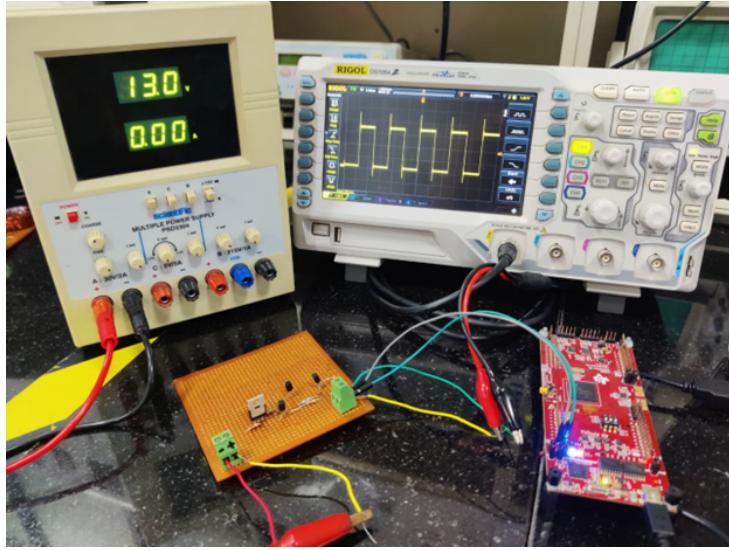


Figure 3.7: Hardware of non-isolated gate driver

Results

The following results are obtained upon hardware implementation of Non-isolated gate driver circuit. The results in Fig. 3.8(a) and Fig. 3.8(b) shows us the gate-source voltage waveform with the effect of miller clamp and a 12.5V drain-source voltage waveform respectively .

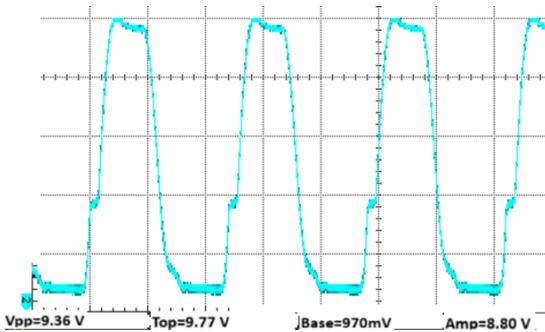


Fig. 3.8(a) Waveform of gate-source voltage

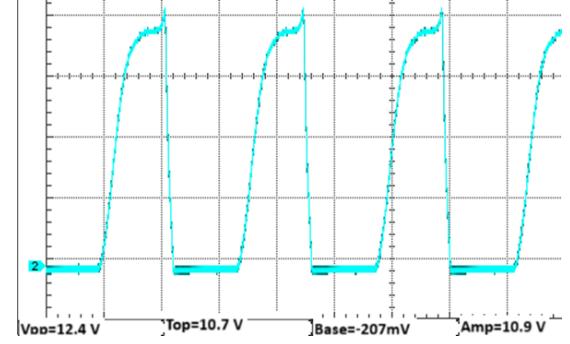


Fig. 3.8(b) Waveform of drain-source voltage

3.2 Isolated gate driver

Isolated gate-driver circuits provide electrical separation between the control circuitry and the high-voltage power stage, ensuring safe and stable switching. They use devices like optocouplers or transformer based drivers to block noise and prevent ground-loop issues. This isolation allows the driver to control MOSFETs whose source terminals may float at high voltage. As a result, these drivers enhance noise immunity, protect sensitive control electronics, and enable reliable high-side or high-voltage switching [10].

Optocouplers

Optocouplers are isolation components that convert light into electrical signals through an LED and a phototransistor, enabling total electrical isolation [10]. They safeguard low-voltage control circuits from high-voltage surges while also guaranteeing clear and noise-resistant signal transmission. The input is a phototransistor and the output is an LED, thereby ensuring galvanic isolation as illustrated in Fig. 3.8

Optocouplers such as TLP250 and TLP5214 are used in design of gate driver circuits and further analysis.

3.2.1 Gate driver using TLP250

The TLP250 is an optically isolated MOSFET gate driver that uses an internal LED and photodetector to provide safe signal isolation. Its pinout as shown in Fig. 3.9, includes input-side pins for the LED drive, output-side pins for gate drive, and supply pins so that the power is isolated at the output stage [8].

The device typically operates with a 10–30 V supply and can deliver peak output currents around 1.5 A [8], suitable for charging and discharging MOSFET gate capacitances. It offers high common-mode noise immunity, ensuring stable switching in electrically noisy environments. With propagation delays in the range of hundreds of nanoseconds [8], the TLP250 is widely used for isolated low-to-medium switching frequency applications.

Design and Simulation

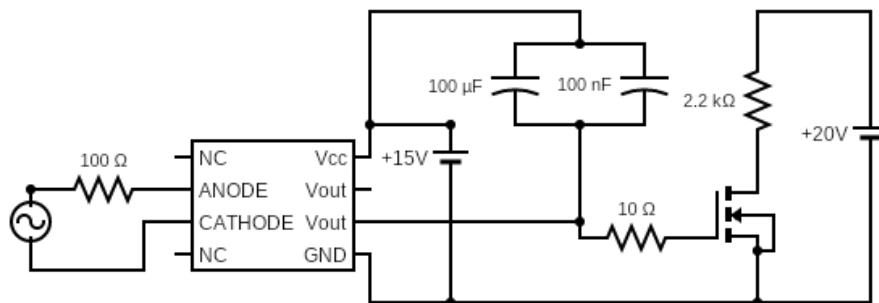


Figure 3.10: Circuit diagram of the TLP250-based isolated gate driver

The LTspice circuit designed according to the Fig. 3.10, uses a TLP250 optocoupler which is modeled with behavioural .subckt code , to provide isolated gate drive for the

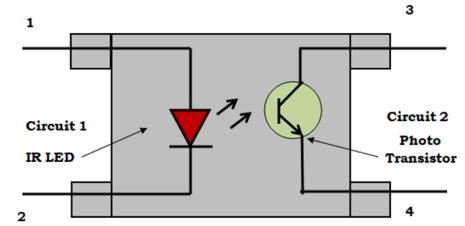


Figure 3.8: Gate charging

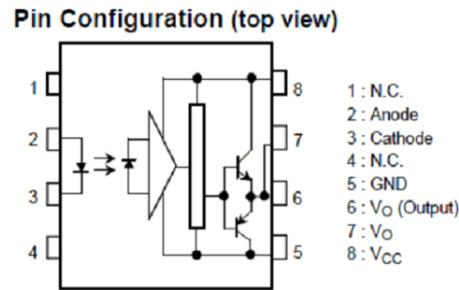


Figure 3.9: pinout of TLP250

IRF530 MOSFET. The input pulse source of 3.3V from the TMS320F28379D LaunchPad drives the TLP250 LED through a resistor, which limits LED current and sets the input switching level. The output side of the TLP250 is powered by a 15V isolated supply, ensuring safe separation from the high-voltage 20V MOSFET stage. The driver output is fed to the MOSFET gate through gate resistance, which controls gate charging current and reduces switching noise. Load resistance of the MOSFET drain, allowing V_{gs} and V_{ds} waveforms to be observed. This setup enables analysis of isolated gate-drive behavior and switching transitions in LTspice.

3.2.2 Smart Gate driver using TLP5214

The TLP5214 is a smart isolated gate driver with a 16-pins as shown in Fig.3.11. It typically operates from a 15 V output-side supply and can deliver peak gate currents up to ± 4 A [9], enabling fast charging and discharging of MOSFET gate.

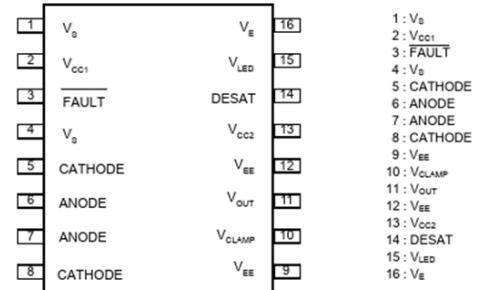


Figure 3.11: Pin configuration of TLP5214

It is called smart gate driver as it has many unique features such as

- Optical isolation between control and power stages for safety and noise immunity [11].
- Built-in Desaturation (DESAT) protection to detect overcurrent and protect the switch [11].
- Integrated Miller clamp to prevent false turn-on [11].
- Under-Voltage Lockout (UVLO) on the output-side supply to avoid weak gate drive [11].
- Fault output pin for reporting abnormal conditions to the controller [11].

Design and Simulation

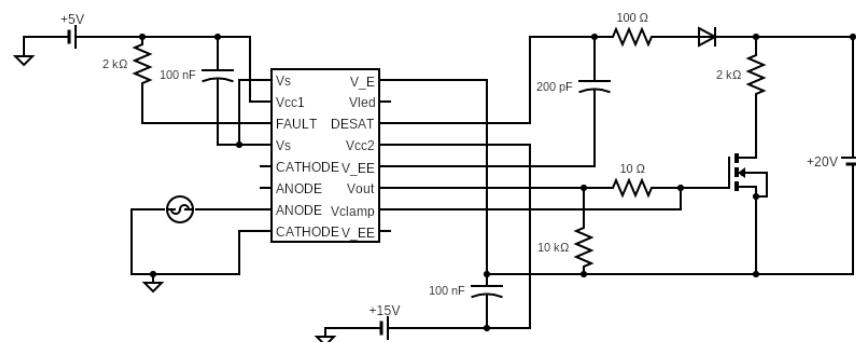


Figure 3.12: Circuit diagram of the TLP5214-based isolated gate driver

The circuit in Fig. 3.12, uses the TLP5214 smart gate driver to control a MOSFET with improved switching safety and noise immunity. The input control signal drives the internal LED of the TLP5214, while a 5V supply and filtering capacitor ensure clean input-side operation. The output stage is powered by a 15V supply, which provides the required gate drive voltage and is stabilized using a decoupling capacitor. A series gate resistor limits peak gate current, while additional resistors and capacitors at the output shape dv/dt and suppress oscillations. The DESAT pin and diode network offer over-current protection, allowing the driver to pull the FAULT signal low during abnormal switching. Overall, this circuit provides isolated, protected, and well-shaped gate drive for reliable MOSFET switching.

Simulation Results

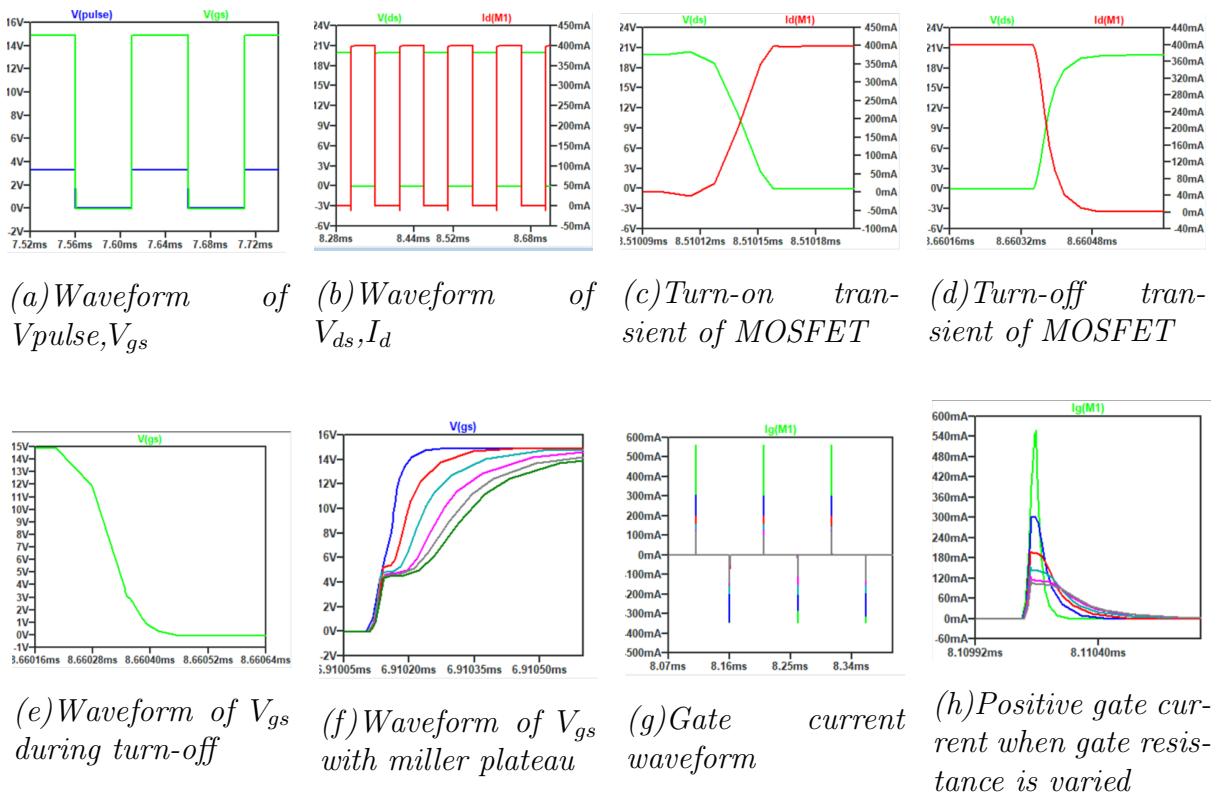


Figure 3.13: Simulation results of TLP250, TLP5214

The simulation results in Figure 3.13 confirm the correct operation of the gate-driver–MOSFET system across different switching conditions. The input pulse and corresponding gate voltage (Fig. 3.13(a)) as well as the drain–source and current waveforms (Fig. 3.13(b)) validate proper signal amplification. The MOSFET’s dynamic behaviour is captured through the turn-on and turn-off transients (Fig. 3.13(c)–(e)), including the distinct Miller plateau region visible in Fig. 3.13(f). Additionally, the gate-current characteristics (Fig. 3.13(g)–(h)) show how variations in gate resistance influence peak gate current and switching speed.

3.2.3 Variation of Gate Driver Characteristics

To study how different gate drivers influence MOSFET switching behaviour, the gate current and gate-source voltage (V_{gs}) waveforms were examined for three driver types: a non-isolated driver, the TLP250, and the more advanced TLP5214. The comparison focused on important factors such as peak gate current, turn-off characteristics, and the rate at which the gate voltage changes (dV_{gs}/dt).

1. Comparison of Peak Gate Current

The peak gate current is an important factor because it determines how quickly the MOSFET's input capacitances can be charged, which in turn influences the device's turn-on speed. The simulation results clearly highlight the differences among the three drivers:

- **Non-isolated driver:** Supplies around 130 mA of peak gate current as shown in Fig. 3.14(a), leading to slower gate charging and a moderate switching speed.
- **TLP250:** Provides a higher peak current of about 350 mA as depicted in Fig. 3.14(b), resulting in quicker turn-on transitions and reduced switching delay.
- **TLP5214:** Delivers the highest peak gate current, close to 590 mA Fig. 3.14(c), enabling very fast gate charging and noticeably quicker switching during turn-on.

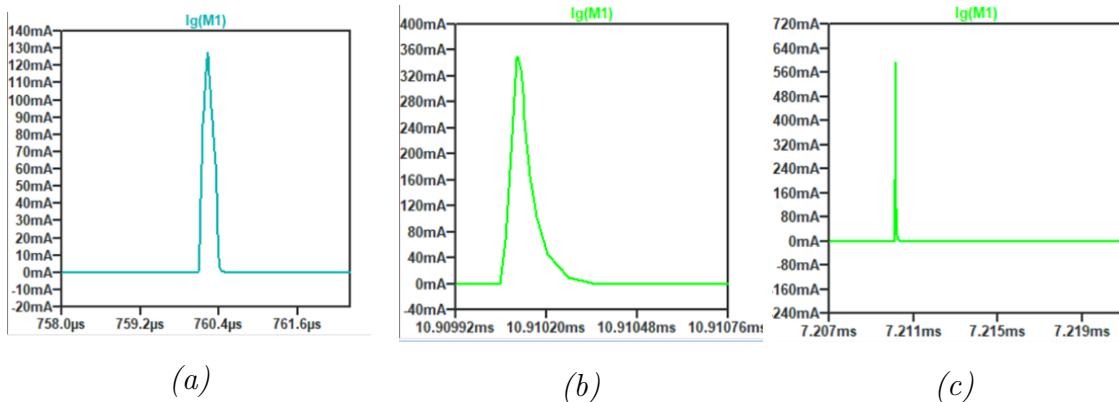


Figure 3.14: Peak gate currents of (a) non-isolated gate driver (b) Gate driver using TLP250 (C) Gate driver using TLP5214

These variations are clearly reflected in the peak-current bar graph (Fig. 3.16 (a)), which highlights the contrast among the three driver types.

2. Turn-off Characteristics

The turn-off behaviour is just as important as turn-on, since a rapid discharge of the gate can create high di/dt and lead to voltage overshoot. The turn-off waveforms of the TLP250 and TLP5214 show clear distinctions:

- **TLP250:** Fig. 3.15 (a) shows a steep drop in V_{gs} , indicating a very fast turn-off. This can be advantageous at lower switching frequencies, but at higher speeds it may place additional stress on the MOSFET.

- **TLP5214:** Produces a more gradual and controlled decrease in V_{gs} as depicted in Fig.3.15 (b). This helps limit voltage overshoot, reduces switching noise and EMI, and lowers stress on the device. The slightly slower turn-off improves overall reliability.

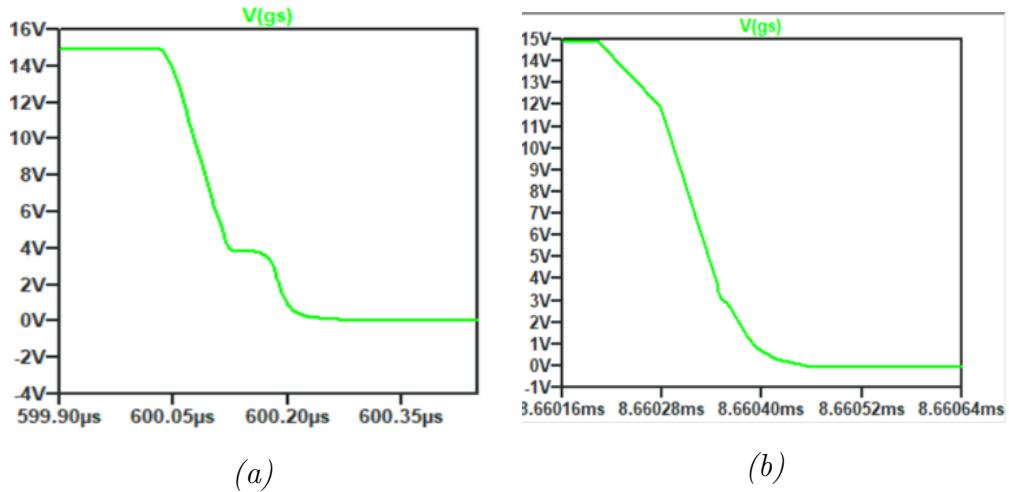


Figure 3.15: (a) Fall in V_{gs} during turn-off in TLP250 , (b) Fall in V_{gs} during turn-off in TLP5214

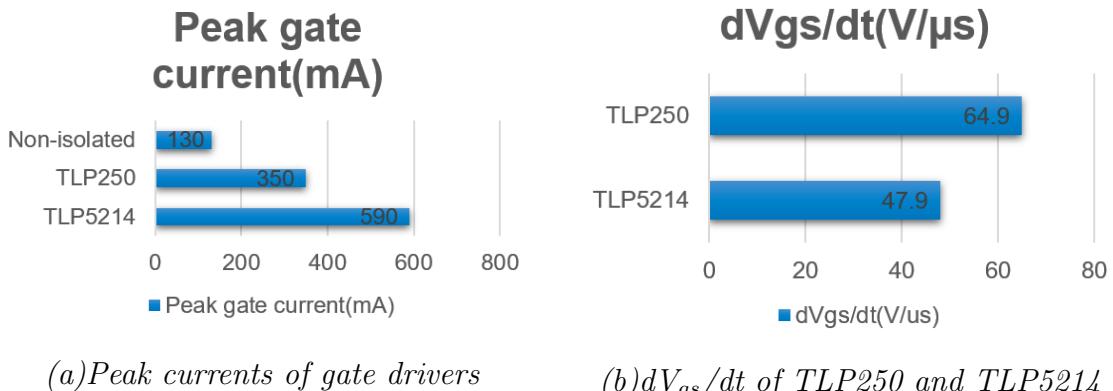


Figure 3.16: Comparison of gate-driver current and dV/dt characteristics

3.3 Summary

Both non-isolated and isolated gate drivers are useful in power-electronics, but they serve different purposes depending on the application. Non-isolated drivers are simple, low-cost, and suitable for low-side MOSFET switching in low-voltage converters; however, because they do not provide galvanic isolation, they are more vulnerable to noise and cannot be used safely for high-side switching. In contrast, isolated gate drivers like the TLP250 and TLP5214 offer much better noise immunity, stronger gate-drive strength, and built-in protection features such as DESAT detection, UVLO, and fault signalling [11]. These capabilities allow the MOSFET to switch more efficiently and safely, especially

in high-power or high-voltage circuits. Overall, both driver types have their own place, but isolated gate drivers are generally the preferred option when reliability, safety, and high-performance switching are required.

Table 3.2: *Summary of Non-Isolated and Isolated Gate Drivers*

Parameter	Non-Isolated Driver	TL ^P 250	TL ^P 5214 (Smart Driver)
Isolation	No	Yes	Yes
Peak Gate Current	Low	Moderate	High (± 4 A)
Protection Features	None	Limited	Multiple (DESAT, UVLO, Miller clamp)
Switching Speed	High	Moderate	Very High
Turn-off Strength	Weak	Moderate	Strong
Use Cases	Low-side low-voltage	General converters	High-performance converters

Chapter 4

Double Pulse Test

4.1 Introduction

The Double Pulse Test (DPT) is a common method used to study how a power MOSFET behaves while switching. It helps measure important factors like switching losses, how fast the current and voltage change (di/dt and dv/dt) [2], and how the device responds during rapid transitions—conditions similar to real operation. Engineers also use DPT results to check whether their MOSFET simulation models are accurate and to spot any switching problems before using the device in high-frequency power converters.

4.2 Design and Simulation

In LTspice, this Double Pulse Test circuit is designed as shown in Fig. 4.1 . It uses a non-isolated gate driver to apply two controlled pulses through a 10ohm gate resistor, allowing precise switching of the MOSFET. The output capacitor stabilizes the supply, enabling accurate observation of turn-on, turn-off transitions, and switching losses

The Double Pulse Test uses two carefully timed gate pulses to evaluate the MOSFET's switching behavior.

- **Pulse1** used to build up the inductor current and create the required load condition [2].
- **Pulse2** allows the actual switching event to be observed, capturing how the MOSFET behaves as the current transfers between the device and the freewheeling diode [2].
- **Turn-off Delay Time ($t_{d(off)}$)**: The time from the removal of the gate signal to the point where the drain current begins to decrease or the drain voltage starts to rise [1].

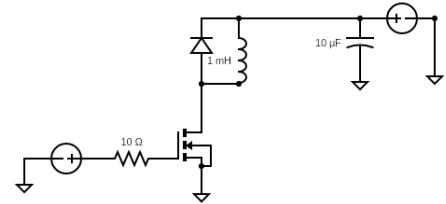


Figure 4.1: Gate charging

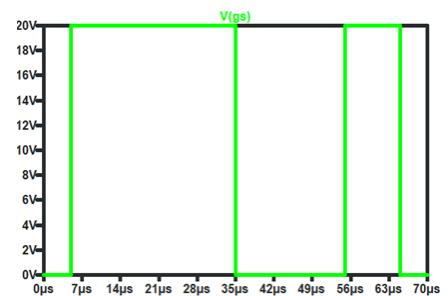


Figure 4.2: Circuit diagram of double pulse test

This technique enables the measurement of:

- **Turn-on Delay Time ($t_{d(on)}$):** The time between the application of the gate-drive signal and the moment when the drain current begins to rise or the drain voltage starts to fall [1].
- **Rise Time (t_r):** The time required for the drain current to increase from 10% to 90% of its final value, or for the drain voltage to drop from 90% to 10% during turn-on [1].

$$t_{ON} = t_{d(on)} + t_r$$

- **Fall Time (t_f):** The time required for the drain current to fall from 90% to 10% of its value, or for the drain voltage to increase from 10% to 90% during turn-off [1].

$$t_{OFF} = t_{d(off)} + t_f$$

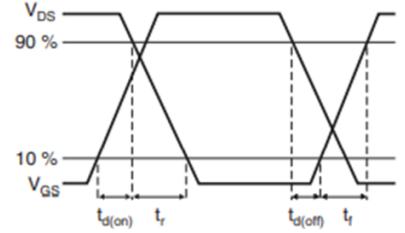


Figure 4.3: Switching characteristics

4.3 Simulation Results

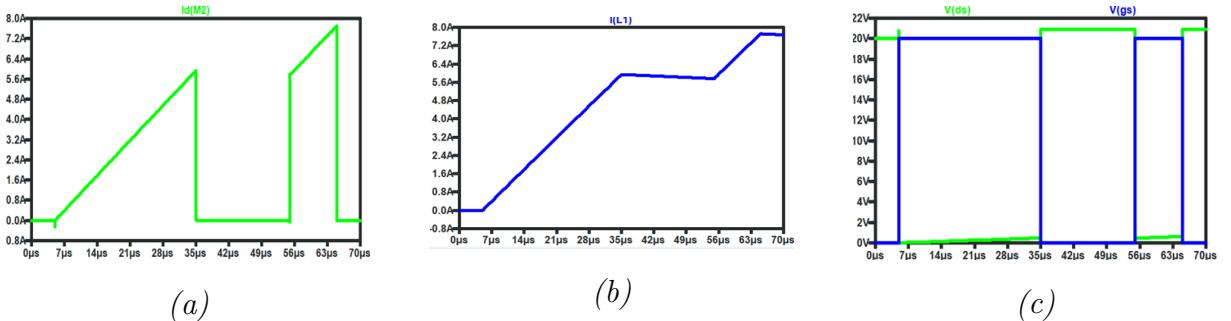


Figure 4.4: Simulation results of double pulse (a) Waveform of drain current (b) Waveform of inductor current (c) Turning on and off transient

Measured Switching Parameters:

- Turn-on delay time ($t_{d(on)}$) = 6.0109 ns
- Rise time (t_r) = 7.1035 ns
- Turn-on time (t_{on}) = 13.1144 ns
- Turn-off delay time ($t_{d(off)}$) = 7.122 ns
- Fall time (t_f) = 9.406 ns
- Turn-off time (t_{off}) = 16.528 ns

4.4 Hardware Setup

The hardware DPT setup uses the TMS320F28379D LaunchPad to generate the required double pulses, taking advantage of its high-resolution ePWM modules. With a 200 MHz operating frequency, the controller provides highly accurate and stable switching signals. In this setup, the MOSFET is driven using a non-isolated gate driver.

Hardware Features

- High-precision pulse generation using the ePWM modules.
- Dual-core 200 MHz processor ensures reliable and deterministic control.
- Supports both isolated and non-isolated gate driver interfaces.
- Provides accurate switching control essential for DPT measurements.

TMS320F28379D Specifications

- Input Voltage : 3.3 V
- Supply Voltage Range : 10–15 V
- Maximum GPIO drive strength: 8 mA
- Number of ePWM modules : 24
- Operating Frequency : 200 MHz

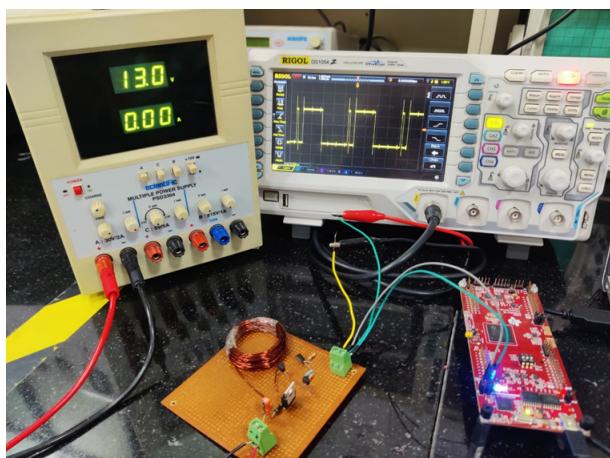


Figure 4.5: Fig : Hardware setup for Double Pulse Test

Air-core Inductor Calculation
(Wheeler's Formula):

$$L = \frac{r^2 N^2}{9r + 10l}$$

Where:

- Radius of coil (r) = 1 inch
- Length of coil (l) = 0.8 inch
- Number of turns (N) = 40

$$L \approx 94 \mu H$$

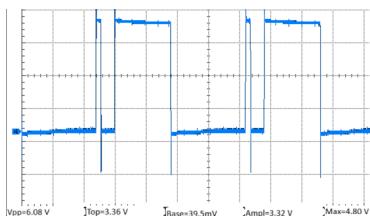


Figure 4.6: Fig : Waveform of pulse input

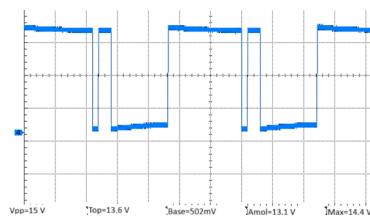


Figure 4.7: Fig : Waveform of gate-source voltage

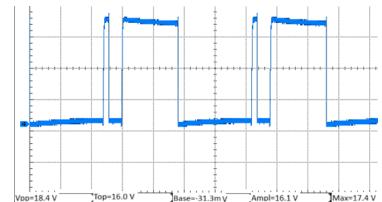


Figure 4.8: Fig : Waveform of drain-source voltage

4.5 Hardware Results

These waveforms show that the MOSFET's switching behaviour in the hardware test is closely aligned with the simulation results. This agreement confirms that the DPT setup, the gate driver, and ePWM pulse generation are functioning correctly and producing reliable switching performance.

4.6 Summary

The Double Pulse Test was performed successfully on both both LTspice and the hardware prototype. The test clearly captured the MOSFET's switching behaviour, including rise and fall times as well as dv/dt and di/dt characteristics. The close relation between the hardware measurements and the simulated waveforms shows that the gate driver design and the pulse generation approach are reliable and effective.

Chapter 5

Practical applications of MOSFET switching

MOSFET switching is widely used in power-electronics hardware where fast, efficient voltage and current control is required. In practical DC–DC converters, especially buck converters, the MOSFET operates as a high-speed switch that directly influences efficiency, ripple performance, and overall power quality. Because of this, understanding real switching behaviour is essential for achieving reliable and optimized buck-converter operation discussed later in the report.

5.1 Asynchronous Buck Converter

An asynchronous buck converter uses a single MOSFET as the main switch and a diode as the free-wheel path to step down a higher DC voltage to a lower level. The MOSFET controls energy delivery to the inductor during the ON state, while the diode conducts during the OFF state to maintain current flow [4] [5] [12]. This simple structure makes the asynchronous buck easy to implement.

Design and simulation

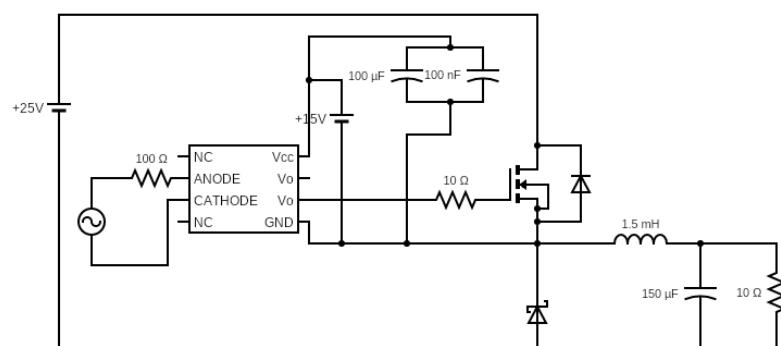


Figure 5.1: Circuit diagram of asynchronous buck converter

The LTspice schematic as shown in Fig.5.1 implements an isolated gate driver feeding a low-side MOSFET through a 10ohm gate resistor; input pulses are sent via a series 100ohm resistor to the driver LED. The MOSFET switches a buck-stage consisting of a 1.5 mH inductor, a 150 μ F output capacitor and a resistive load, with freewheeling diodes handling current commutation. Decoupling capacitors on the driver supply stabilize the isolated 15 V gate rail and reduce switching noise. This setup allows measurement of V_{gs} , V_{ds} , inductor current and switching losses to evaluate driver performance and converter behaviour.

Calculations

- $V_{in} = 25 \text{ V}$, Output Power = 10 W
- Duty cycle $D = 0.4$, Switching frequency $f_s = 20 \text{ kHz}$

$$V_{out} = V_{in} \times D = 10 \text{ V}$$

$$\Delta I_L = 0.2 \times I_{out} = 0.2 \text{ A}$$

Inductance Calculation (CCM)

$$L = \frac{(V_{in} - V_{out}) \times D}{\Delta I_L \times f_s}$$

$$L = 1.5 \text{ mH}$$

Capacitance Calculation (5% Ripple)

$$C = \frac{\Delta I_L}{8f_s \Delta V_{out}} \approx 150 \mu\text{F}$$

Diode

- Schottky diode
- $I_{avg} = 1 \text{ A}$

5.1.1 Simulation Results

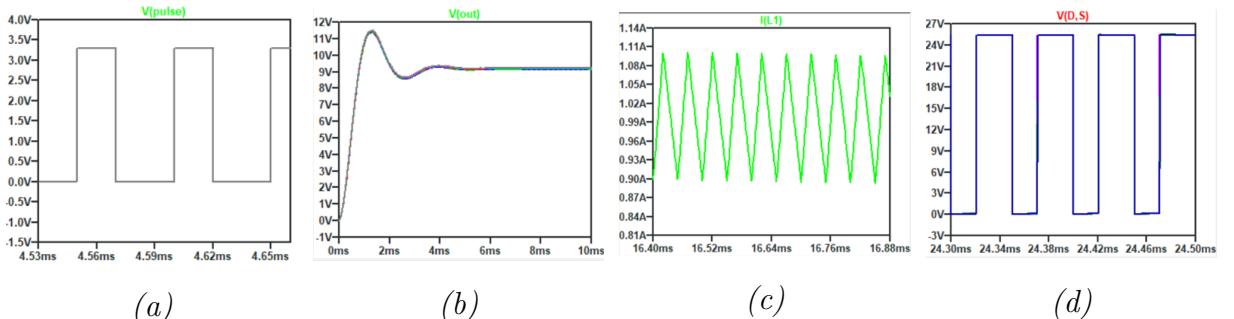


Figure 5.2: Simulation results of asynchronous buck converter (a)Input pulse = 3.3V (b) V_{out} of converter = 10V (c) $\Delta I_L = 0.2\text{A}$ (d) waveform of $V_{ds} = 25\text{V}$

5.1.2 Analysis of Losses and Efficiency

The losses in the asynchronous buck converter are majorly because of the losses in MOSFET and diode [12]. The losses in MOSFET are of two types

- Switching Losses - when the MOSFET is turning on and off

$$P_{sw} = (E_{on} + E_{off})f_s$$

- Turn-On Energy - Energy dissipated during transition from OFF to ON state

$$E_{on} = \frac{V_{ds}I_dt_{on}}{2}$$

- Turn-Off Energy - Energy dissipated during the transition from the ON to OFF state

$$E_{off} = \frac{V_{ds}I_dt_{off}}{2}$$

- Conduction Losses - When the MOSFET is conducting current through drain and source terminal [1].

$$P_{con} = I_{d,rms}^2 R_{ds(on)}$$

- Losses in diode - $P_{diode} = (1 - D)I_{diode}V_f$

From the above formulas the losses are calculated from the simulation results obtained by varying the gate resistance from 10ohm - 100ohm , and the following table is derived

Table 5.1: Variation of different parameters with gate resistance

R_g (Ω)	t_{on} (ns)	t_{off} (ns)	E_{on} (μJ)	E_{off} (μJ)	P_{sw} (W)	Efficiency (%)
10	62	111	0.697	1.248	0.039	94.43
30	75	131	0.843	1.437	0.0463	94.37
50	83	154	0.933	1.732	0.0533	94.31
70	110	187	1.237	2.103	0.0668	94.18
90	135	259	1.518	2.913	0.0886	93.99
100	148	296	1.665	3.33	0.10	93.89

The data in Table 5.1 shows that increasing the gate resistance leads to a noticeable rise in both the turn-on and turn-off times, indicating slower MOSFET switching. As a result, the switching energies E_{on} and E_{off} also increase with higher R_g , contributing to greater overall switching losses. This trend is reflected in the switching power P_{sw} , which rises from 0.039 W at 10 Ω to 0.10 W at 100 Ω . Consequently, the converter efficiency decreases slightly as the gate resistance increases, confirming the performance trade-off illustrated in Fig.5.3. The conduction losses are independent of these parameters; thus it is constant

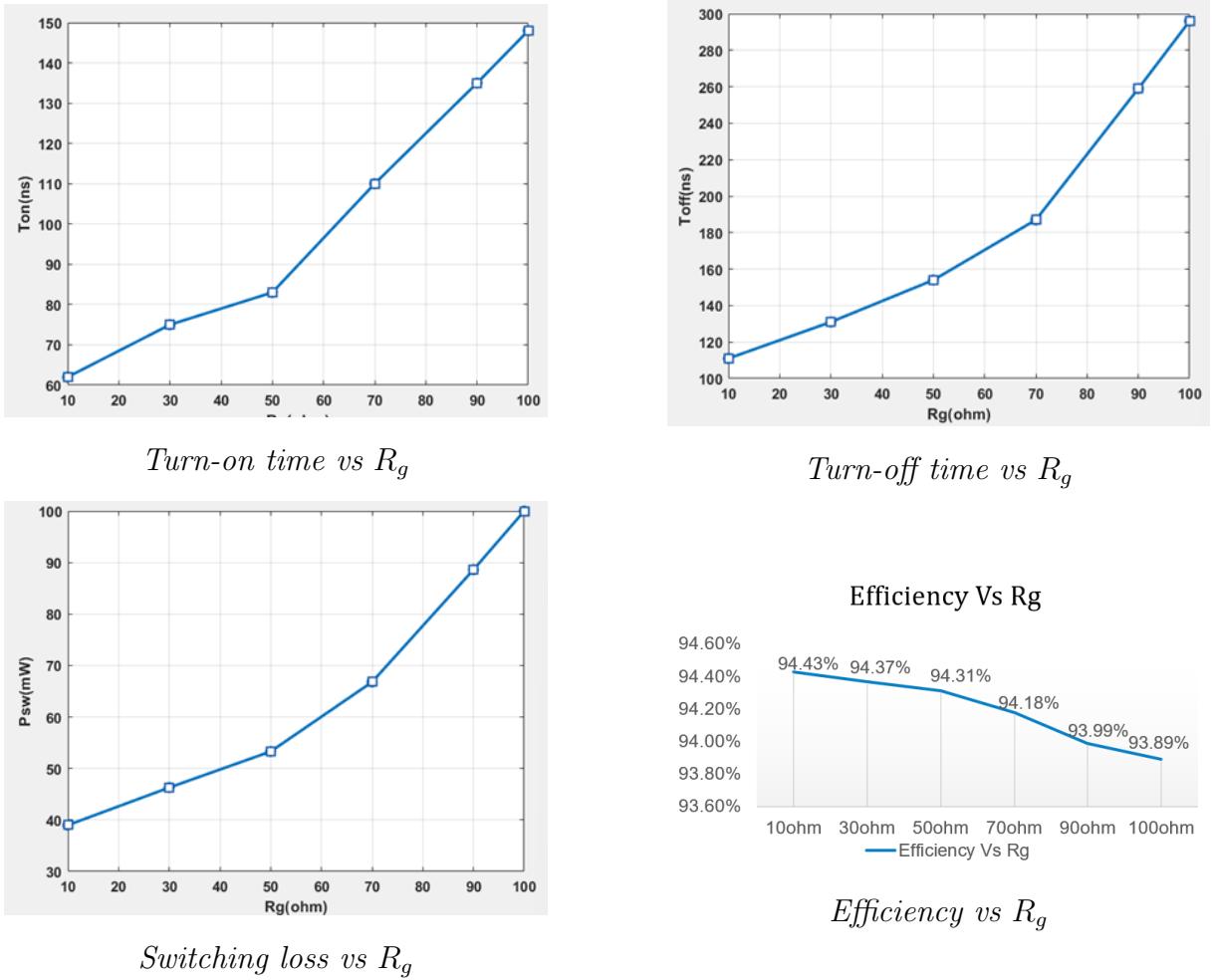


Figure 5.3: Variation of t_{on}, t_{off}, P_{sw} and efficiency with gate resistance

5.1.3 Variation of Switching Frequency

Switching frequency plays a major role in determining both the switching losses and the overall efficiency of a converter. In this analysis, the switching frequency f_s is varied while keeping the gate resistance fixed at ($R_g = 10\Omega$) as depicted in the table 5.2. As the switching frequency increases, the MOSFET is forced to turn ON and OFF more times per second. This causes the switching losses to rise almost proportionally with f_s . At higher frequencies, especially in the range of 500 kHz to 1 MHz, these losses become significant, leading to a noticeable drop in converter efficiency. The table 5.2 and graphs Fig. 5.4 provided clearly shows how increasing the switching frequency affects loss distribution and overall performance.

Table 5.2: Variation of efficiency with switching frequency

Switching frequency f_s	P_{sw} (mW)	Efficiency (%)
10 kHz	19.45	95.67
20 kHz	39	94.43
50 kHz	97.25	93.92
100 kHz	194.5	93.07

- The switching frequency is varied while maintaining a constant gate resistance of ($R_g = 10\Omega$).

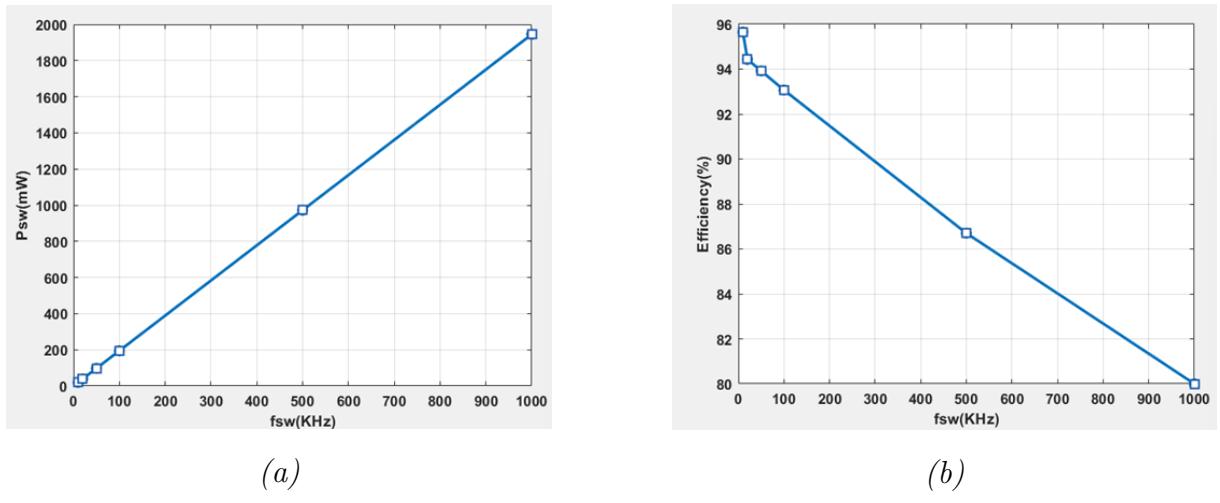


Figure 5.4: (a) P_{sw} vs f_{sw} (b)Efficiency vs f_{sw}

- As the frequency increases, the MOSFET is required to switch more frequently, which leads to a nearly linear rise in switching losses as shown in Fig.5.4.
- These additional losses directly impact the converter's performance by lowering its overall efficiency.

5.2 Synchronous Buck Converter

A synchronous buck converter is a step-down DC-DC converter that uses two MOSFETs instead of a diode to improve performance [4] [12]. The lower MOSFET replaces the diode, which reduces conduction losses and boosts efficiency, especially at low output voltages. This design also helps the converter run cooler and handle higher currents more effectively. Because the switches can be controlled precisely, the converter achieves faster and cleaner switching. Due to these benefits, synchronous buck converters are commonly used in high-efficiency power supplies and modern electronic systems. [4] [12]

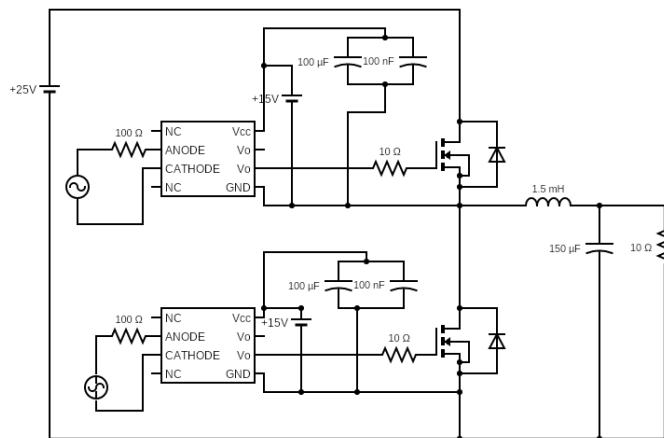


Figure 5.5: Synchronous buck converter circuit

5.2.1 Design and simulation

The circuit designed as shown in Fig. 5.5, uses two gate-driver stages to control the upper and lower MOSFETs using separate pulse signals. Each driver boosts the low-level input pulse to a 15 V gate signal, ensuring proper switching of the MOSFETs. The MOSFET pair supplies power to an LC output filter, which smooths the waveform and delivers a stable output to the load. By applying two timed pulses, the circuit allows controlled switching operation suitable for buck-converter or switching-stage analysis in LTspice. The converter was operated using the following pulse and timing settings: a high-side duty cycle $D_{HS} = 0.4$, a low-side duty cycle $D_{LS}=0.596$ and a dead time of $0.2\mu s$. Using these parameters, the output voltage can be estimated from the high-side duty ratio as:

$$V_{out} \approx D_{HS} \cdot V_{in} = 10 V$$

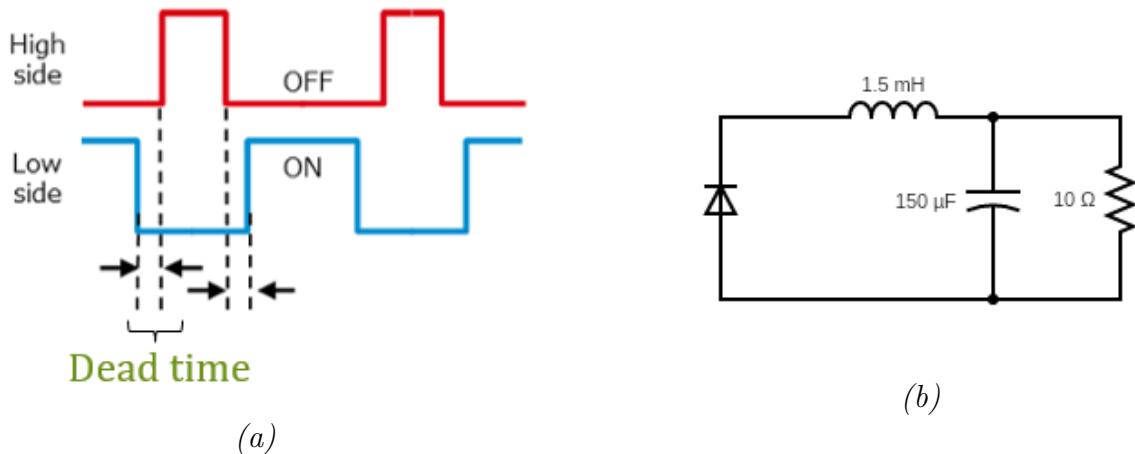
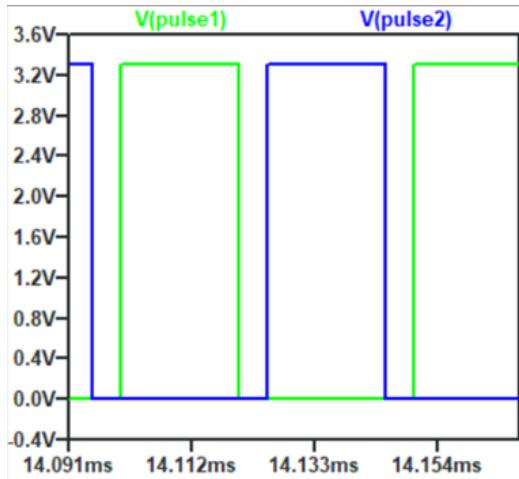


Figure 5.6: (a)Dead time between high-side and low-side MOSFETs (b)Equivalent circuit during dead time

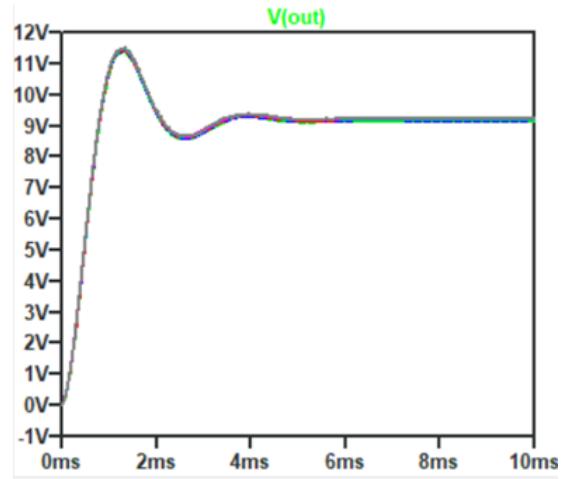
Figure 5.6 illustrates the concept of dead time, showing the brief interval when both the high-side and low-side MOSFETs are kept OFF to prevent shoot-through [5]. The equivalent circuit during this interval shows that the inductor current freewheels through the diode, maintaining continuity of current flow [5].

5.2.2 Simulation Results

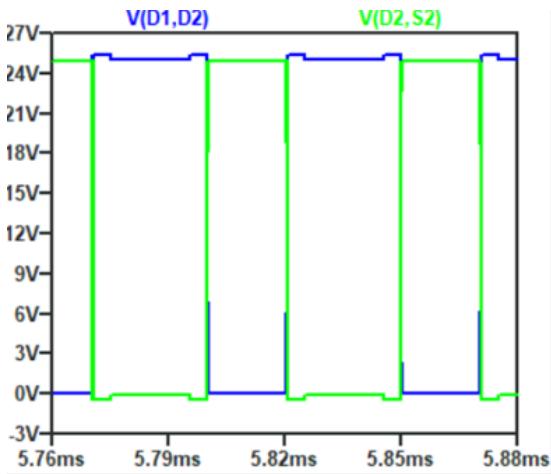
Figure 5.7 demonstrates how introducing dead time between the PWM pulses allows the converter to switch safely without overlap between the high-side and low-side MOSFETs. As seen in Fig. 5.7(b), the output voltage gradually stabilizes at 10 V, showing that the LC filter effectively smooths the switching pulses. The drain-source waveforms in Fig. 5.7(c) reveal proper alternation between the switches, indicating that the dead-time control prevents shoot-through. Meanwhile, the inductor current in Fig. 5.7(d) follows a smooth triangular pattern, confirming correct energy transfer during the charging and discharging phases of each switching cycle. [5]



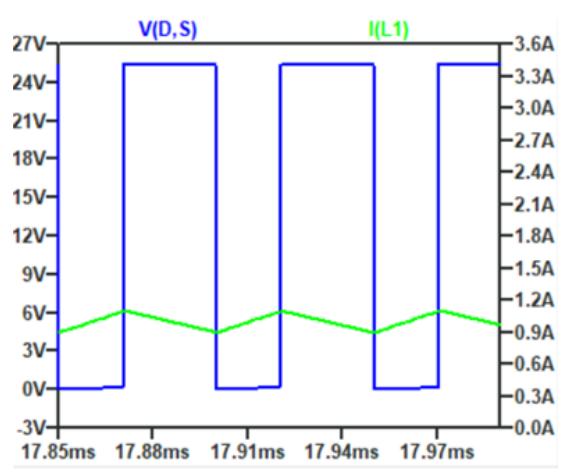
(a)



(b)



(c)



(d)

Figure 5.7: (a) PWM pulse with dead time (b) Output Voltage of (10 V) of converter (c) Drain-source voltages of both MOSFETs (d) Charging and discharging of inductor current with V_{ds} of the low-side MOSFET

5.2.3 Losses and Efficiency Calculation

The main losses in a synchronous buck converter include:

- Conduction losses in the high-side and low-side MOSFETs
 - Switching losses during turn-on and turn-off
 - Body diode losses, ignored because of very less dead time

In a synchronous buck converter, the total power loss comes from both MOSFETs and can be expressed as:

$$P_{\text{losses}} = P_1 + P_2 = 2(P_{sw} + P_{con}).$$

The efficiency is then determined using:

$$\eta = \frac{P_{out}}{P_{out} + P_{losses}},$$

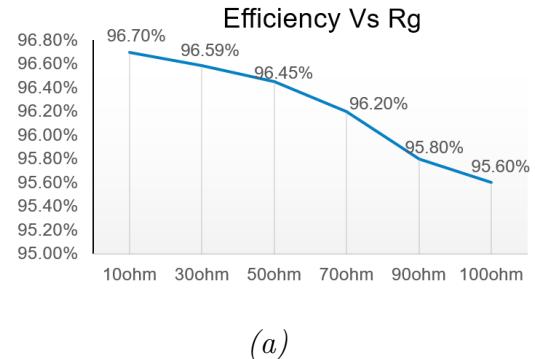
where the output power is:

$$P_{out} = 10 W$$

As the gate resistance increases, the MOSFET takes longer to switch ON and OFF. This slower switching action increases the switching losses, which in turn causes a noticeable drop in overall efficiency. Thus, higher gate resistance leads to reduced converter performance.

Table 5.3: Variation of efficiency with gate resistance

R_g (Ω)	Efficiency (%)
10	96.7
30	96.59
50	96.45
70	96.20
90	95.8
100	95.6



(a)

Figure 5.8: (a)Efficiency vs. gate resistance

The efficiency gradually decreases with increasing gate resistance as shown in the graph Fig.5.8(a), showing that higher R_g slows down the MOSFET switching transitions and results in greater switching losses.

5.3 Summary

The table below highlights the key differences between asynchronous and synchronous buck converters in terms of components, efficiency, losses, and application suitability.

Table 5.4: Comparison of Asynchronous and Synchronous Buck Converters

Features	Asynchronous Buck	Synchronous Buck
Low-side element	Diode	MOSFET
Efficiency	Moderate	High
Dead-time requirement	None	Required
Conduction losses	High (diode drop)	Low (MOSFET $R_{DS(on)}$)
Control complexity	Simple	More complex
Suitable for	Low-cost systems	High-efficiency converters

In summary, Synchronous buck converters switch faster and efficient when compared to asynchronous buck converters. Thus, we analysed the switching of MOSFET for single switch and double switch power electronic applications.

Chapter 6

Conclusions and Future Work

6.1 Conclusions

Table 6.1: Datasheet Realisation for IRF840 MOSFET

Specification	Method	Conditions	Obtained Value	Datasheet Value	Remark
Gate-Source charge (Q_{gs})	MOSFET gate driver	$V_{gs} = 10V$, $V_{ds} = 400V$, $I_d = 8A$	9.6 nC	9.3 nC	✓ Valid
Gate-Drain charge (Q_{gd})	MOSFET gate driver	$V_{gs} = 10V$, $V_{ds} = 400V$, $I_d = 8A$	20.4 nC	32 nC	✓ Valid
Gate charge (Q_g)	MOSFET gate driver	$V_{gs} = 10V$, $V_{ds} = 400V$, $I_d = 8A$	30 nC	63 nC (max)	✓ Valid
Turn-on delay time ($t_{d(on)}$)	Double pulse test	$V_{DD} = 250V$, $I_d = 8A$, $R_g = 9.1\Omega$, $R_d = 31\Omega$	6.0109 ns	14 ns	✓ Valid
Rise time (t_r)	Double pulse test	$V_{DD} = 250V$, $I_d = 8A$, $R_g = 9.1\Omega$, $R_d = 31\Omega$	7.1035 ns	23 ns	✓ Valid
Turn-off delay time ($t_{d(off)}$)	Double pulse test	$V_{DD} = 250V$, $I_d = 8A$, $R_g = 9.1\Omega$, $R_d = 31\Omega$	7.122 ns	49 ns	✓ Valid
Fall time (t_f)	Double pulse test	$V_{DD} = 250V$, $I_d = 8A$, $R_g = 9.1\Omega$, $R_d = 31\Omega$	16.528 ns	20 ns	✓ Valid
Body diode reverse recovery time (t_{rr})	Double pulse test	$I_f = 8A$, $di/dt = 100A/\mu s$	800 ns	970 ns (max)	✓ Valid
Diode reverse recovery charge (Q_{rr})	Double pulse test	$I_f = 8A$, $di/dt = 100A/\mu s$	1.2 μC	4.2 μC	✓ Valid

The Table 6.1 clearly shows the validation of IRF840 MOSFET parameters with experimental results obtained from gate driver measurements, simulations and calculations and the Double Pulse Test. Key dynamic characteristics, such as gate charge, switching delays, transition times, and diode reverse recovery parameters, were measured and compared against the datasheet values. The results closely matched the manufacturer's specifications, with all deviations remaining within acceptable limits. This confirms that

the implemented gate-driver circuits are functioning correctly and supports the reliability of the switching performance analysis conducted throughout the project. So we come to a conclusion that the method followed to obtain datasheet parameters are valid and can be further useful to give inputs to an algorithm for accurate prediction of datasheet of any given MOSFET.

6.2 Future scope of work

- Developing an intelligent algorithm to estimate a MOSFET's datasheet parameters using experimental inputs from gate driver evaluations and Double Pulse Testing.
- This method automates the characterization process, allowing faster and more accurate extraction of device parameters while reducing manual effort.
- The algorithm can be further extended to support predictive modelling and optimization of power semiconductor devices in real-time applications.

Appendix A

A.1

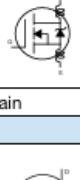
SPECIFICATIONS ($T_J = 25^\circ\text{C}$, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT	
Static							
Drain-source breakdown voltage	V_{DSS}	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$	500	-	-	V	
V_{DS} temperature coefficient	$\Delta V_{DS}/T_J$	Reference to 25°C , $I_D = 1 \text{ mA}$	-	0.78	-	$\text{V}/^\circ\text{C}$	
Gate-source threshold voltage	V_{GTH}	$V_{DS} = V_{GS}, I_D = 250 \mu\text{A}$	2.0	-	4.0	V	
Gate-source leakage	I_{GSS}	$V_{GS} = \pm 20 \text{ V}$	-	-	± 100	nA	
Zero gate voltage drain current	I_{DSS}	$V_{DS} = 500 \text{ V}, V_{GS} = 0 \text{ V}$	-	-	25	μA	
		$V_{DS} = 400 \text{ V}, V_{GS} = 0 \text{ V}, T_J = 125^\circ\text{C}$	-	-	250		
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS} = 10 \text{ V}$	$I_D = 4.8 \text{ A}^b$	-	-	0.85	Ω
Forward transconductance	g_{fs}	$V_{DS} = 50 \text{ V}, I_D = 4.8 \text{ A}^b$	4.9	-	-	S	
Dynamic							
Input capacitance	C_{iss}	$V_{GS} = 0 \text{ V}, V_{DS} = 25 \text{ V}, f = 1.0 \text{ MHz}$, see fig. 5	-	1300	-	pF	
Output capacitance	C_{oss}		-	310	-		
Reverse transfer capacitance	C_{rys}		-	120	-		
Total gate charge	Q_g	$V_{GS} = 10 \text{ V}$	$I_D = 8 \text{ A}, V_{DS} = 400 \text{ V}$, see fig. 6 and 13 ^b	-	-	63	
Gate-source charge	Q_{gs}			-	-	9.3	
Gate-drain charge	Q_{gd}			-	-	32	
Turn-on delay time	$t_{d(on)}$			-	14	-	
Rise time	t_r	$V_{DD} = 250 \text{ V}, I_D = 8 \text{ A}$ $R_g = 9.1 \Omega, R_D = 31 \Omega$, see fig. 10 ^b		-	23	-	
Turn-off delay time	$t_{d(off)}$			-	49	-	
Fall time	t_f			-	20	-	
Internal drain inductance	L_D			-	4.5	-	
Internal source inductance	L_S	Between lead, 6 mm (0.25") from package and center of die contact 		-	7.5	-	
Gate input resistance	R_g			$f = 1 \text{ MHz}$, open drain	0.6	-	
Drain-Source Body Diode Characteristics							
Continuous source-drain diode current	I_S	MOSFET symbol showing the integral reverse p-n junction diode		-	-	8.0	
Pulsed diode forward current ^a	I_{SM}			-	-	32	
Body diode voltage	V_{SD}	$T_J = 25^\circ\text{C}, I_S = 8 \text{ A}, V_{GS} = 0 \text{ V}^b$		-	-	2.0	
Body diode reverse recovery time	t_{rr}			-	460	970	
Body diode reverse recovery charge	Q_{rr}			-	4.2	8.9	
Forward turn-on time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D)					

Figure A.1: Datasheet of IRF840

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