

# **Switching Characteristics and Data Sheet Realization of MOSFET**

## **B .Tech Project**

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# Chapter 1

## Introduction

### 1.1 Introduction

A metal oxide semiconductor field effect transistor (MOSFET) is one of the most widely used components in modern electronics [1]. It has three main terminals gate, source, and drain and is used primarily to switch signals or control power[1]. Unlike some devices that rely on current, the MOSFET is controlled by the voltage applied at the gate, which regulates how much current flows from the source to the drain. The device can work in different modes depending on the voltage applied, such as when it is completely off (cutoff), partly on (linear/triode), or fully on (saturation). Its performance during switching, especially the speed of turning on and off, is very important when designing circuits like gate drivers.

Due to their high input impedance and efficient performance, MOSFETs are well suited for use in both low-power and high-power systems. Key characteristics such as the gate threshold voltage and the resistance between the drain and the source directly affect how much power is lost during operation. To help engineers use them correctly, manufacturers provide a datasheet that lists these values and other details. This allows designers to choose the right MOSFET and design circuits for the best performance.

### 1.2 Motivation for BTP

The motivation for this project comes from the critical role MOSFETs play in modern power electronics and digital circuits. Understanding practical switching characteristics such as the turn on delay, rise time, turn off delay, and fall time is vital to enhance device performance and to reduce energy losses during switching events.

### 1.3 Theme of Work

- Simulate both isolated and non-isolated MOSFET gate driver circuits to examine and control their switching dynamics.
- Use the double pulse test technique to derive MOSFET switching metrics: turn-on delay, rise time, turn-off delay, and fall time[2].
- Design and simulate a buck converter in a single switch topology, and compare its behavior with a bridge (or half-bridge) configuration.
- Build and test the double pulse test circuit in hardware using the TMS320F28379D LaunchPad, under control of Code Composer Studio, to validate the simulated switching behavior.

# Chapter 2

## Literature Review

### 2.1 Gate Driver Circuits

A gate driver circuit controls the voltage and current applied to the gate of a MOSFET, allowing fast and efficient switching. It ensures that the transistor turns on and off cleanly, improving overall performance. MOSFET gate driver circuits play a crucial role in power electronics by ensuring that proper voltage and current levels are supplied to control switches efficiently and reliably [3]. These circuits can be classified as non-isolated or isolated. Non-isolated drivers are simpler but lack safety from high-voltage transients, while isolated drivers (e.g., using optocouplers like TLP250 and TLP5214) provide better protection and noise immunity by electrically separating control and power sections.

#### 2.1.1 Key characteristics of advanced drivers

The key characteristics of advanced drivers like TLP250 include high-speed switching, low output impedance, and the ability to drive high-power devices efficiently. The TLP5214 improves on this by offering dual-channel operation, built-in under-voltage lockout, and fault detection features for enhanced device protection and control. -

### 2.2 Double Pulse Test

The double pulse test method is widely used to evaluate switching behavior [2]. Measures parameters such as switching losses, diode reverse recovery, energy loss, and timing characteristics critical for improving device performance.

### 2.3 Bridge Circuits

A bridge circuit using two MOSFETs includes one high-side transistor and one low-side transistor that work together to manage current through a load. The high-side MOSFET connects the load to the positive voltage, while the low-side MOSFET connects it to the ground. In bridge circuits, managing the dead time during alternate switching of MOSFETs is essential to avoid short circuits [4]. However, rapid voltage changes can cause gate voltage spikes due to parasitic capacitance, which may lead to unwanted turn on or damage.

To address this, surge suppression techniques [5] are implemented:

- Miller clamp transistors prevent false turning on from voltage spikes.
- Schottky diodes quickly clamp voltage surges and work with bypass capacitors to reduce noise.
- Prevention capacitors stabilize gate voltage but may slightly reduce switching speed.

### 2.4 Summary

This chapter reviews the essential role of MOSFET gate driver circuits, highlighting their impact on switching speed, efficiency, and reliability through various driver types, including non-isolated and isolated configurations with optocouplers such as TLP250 and TLP5214. It also explains the double-pulse test method for assessing switching performance and discusses bridge circuit analysis with techniques for suppressing harmful voltage surges to ensure device protection and stable operation.

# Chapter 3

## Switching Realization of MOSFETs

### 3.1 Non-Isolated Gate Drivers

Non-isolated gate driver circuit is designed as depicted in Fig.3.1, using 2 NPN and 1 PNP transistors arranged in a totem-pole configuration and connected to the gate of the MOSFET with a gate resistance, also called limiting resistance, as it limits the gate current, protecting the device from current spikes. The totem-pole configuration helps to convert low input signals to high gate signals for proper switching.

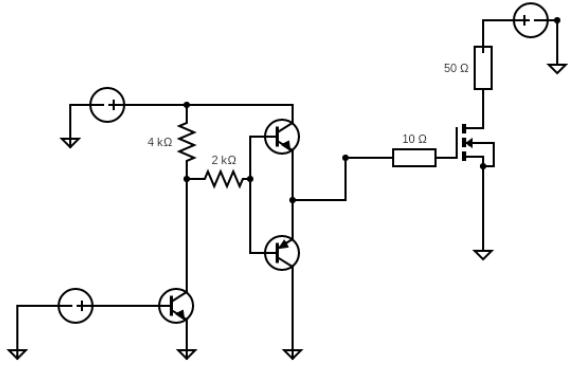


Figure 3.1: Circuit diagram of non-isolated gate driver

#### 3.1.1 Simulation Results

The IRF530 MOSFET, with a gate threshold voltage between 2 and 4V, a maximum drain-source voltage of 100V, and a maximum drain current of 14A [6], was simulated in a nonisolated gate driver circuit with variable gate resistance from  $10\Omega$  to  $100\Omega$ . The MOSFET was driven at a gate source voltage of 10V and a drain source voltage of 80V to ensure safe operation within its specifications while analyzing its switching behavior. The initiation of switching in the MOSFET is controlled by the applied gate voltage, while the rapid rise and fall of the gate current as shown in Fig.3.1.1.(c) marked by its positive and negative peaks facilitates fast turn on and turn off transitions of the device[3].

Table 3.1: Variation of gate current with gate resistance.

Gate resistance( $\Omega$ )	$I_{pk}$ (mA)
10	89.289
30	70.63
50	56.9
70	48.76
90	41.33
100	39.3

The transient behavior as shown in Fig.3.1.1.(b) of the MOSFET is largely governed by the charging and discharging of its intrinsic gate capacitance[3]. Changing the gate resistance revealed its impact on charging of capacitor, switching speed and current flow, with a lower resistance enabling faster switching but higher current peaks, as illustrated in Table 3.1.

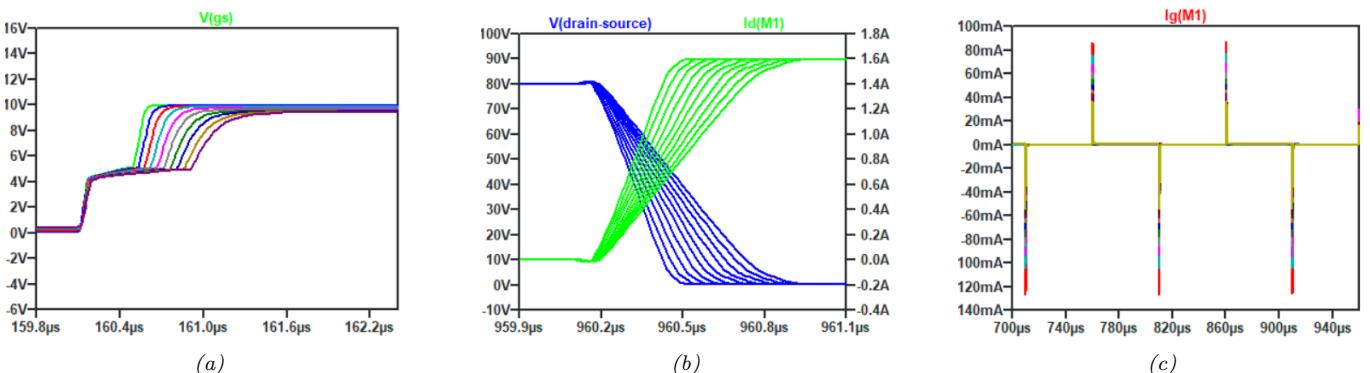


Figure 3.1.1: (a) Waveform of gate pulse depicting the miller clamp effect caused by the miller capacitance (b) Variation of drain voltage with drain current (c) Waveform of gate current

## 3.2 Double Pulse Test

The double pulse test circuit employs a MOSFET switching an inductive load, with a  $10\ \Omega$  gate resistor controlling speed and ringing. A  $1\text{ mH}$  inductor stores and releases energy, a  $10\ \mu\text{F}$  capacitor smooths the voltage, and a diode allows free-flowing current. Powered by DC and gate drive sources, it measures MOSFET switching times, losses, and diode behavior.

### 3.2.1 Simulation Results

The double pulse test simulation applies a  $30\ \mu\text{s}$  pulse, a  $20\ \mu\text{s}$  off interval, and a  $10\ \mu\text{s}$  pulse to the IRF530 MOSFET [6] to study its switching behavior. Transient waveforms of gate voltage, drain current, and inductor current were captured, showing a turn-on time of  $11.2\text{ns}$  and a turn-off time of  $73.2\text{ns}$ , consistent with the datasheet limits. The simulation validates the test setup and allows for analysis of switching losses and timing performance.

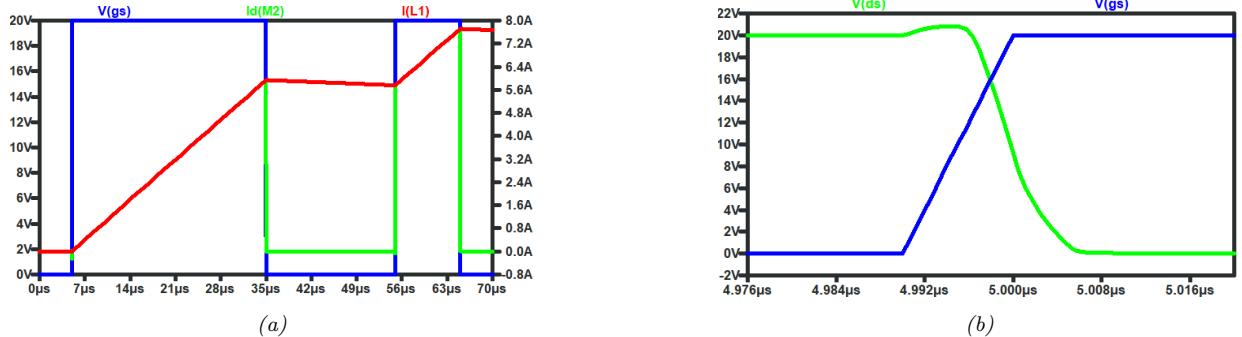


Figure 3.2.1: (a) Waveforms showing gate pulses, drain current and inductor current (b) Variation of  $V_{gs}$  and  $V_{ds}$

## 3.3 Single Switch Buck Converter

The single-switch buck converter efficiently steps down DC voltage, using a MOSFET with a  $10\ \Omega$  gate resistor, a  $3\text{ mH}$  inductor, a schottky diode, and a  $6.2\ \mu\text{F}$  capacitor to provide smooth, continuous output to a  $20\ \Omega$  load. Schottky diode has very less reverse recovery time and thus, helps in rapid switching.

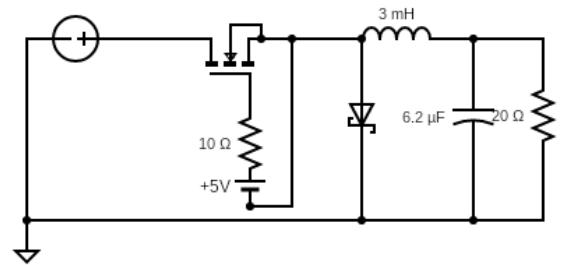


Figure 3.3: Circuit diagram of single switch buck converter

### 3.3.1 Simulation Results

In the simulation of a single-switch buck converter using the IRF530, the device is modeled under a  $50\text{ V}$  input, a series resistance of  $0.16\ \Omega$ . The converter operates at a switching frequency of  $20\text{ kHz}$  with a duty cycle of  $0.4$ . Transient waveforms for both turn-on and turn-off events are shown in Fig.3.3.1, illustrating the dynamic switching behavior. Using the device specifications and the simulation results, the contents of Table 3.3 are calculated.

Table 3.3: Variation of different parameters with gate resistance

Gate resistance ( $\Omega$ )	$T_{on}$ (ns)	$T_{off}$ (ns)	$E_{on}$ ( $\mu\text{J}$ )	$E_{off}$ ( $\mu\text{J}$ )	$P_{switching}$ (W)	$P_{conduction}$ (W)
10	28.6	80.2	0.65	2.2	0.057	0.1024
30	74.7	156	1.7	4.25	0.119	0.1024
50	119.2	240	2.7	6.53	0.184	0.1024
70	165	298	3.75	8.11	0.24	0.1024
90	218	359	4.95	9.77	0.295	0.1024

- Conduction losses:  $P_{cond} = I_{D,\text{rms}}^2 R_{DS(\text{on})}$
- ON-time energy ( $E_{on}$ ):  $E_{on} = \frac{V_{DS} I_D t_{on}}{2}$
- OFF-time energy ( $E_{off}$ ):  $E_{off} = \frac{V_{DS} I_D t_{off}}{2}$
- Switching losses:  $P_{switching} = (E_{on} + E_{off}) f_{sw}$

The plots in Figure 3.3.1 are obtained from the calculated data presented in Table 3.3. They illustrate that increasing the gate resistance causes both the turn-on and turn-off intervals to extend in an approximately linear fashion. As switching events take longer, the energy consumed during each transition increases, resulting in greater switching losses. Since conduction losses are not affected by gate resistance, their curve in Figure 3.3.1 remains constant. Consequently, the overall efficiency of the device is strongly influenced by switching losses, which are directly dependent on the selected gate resistance.

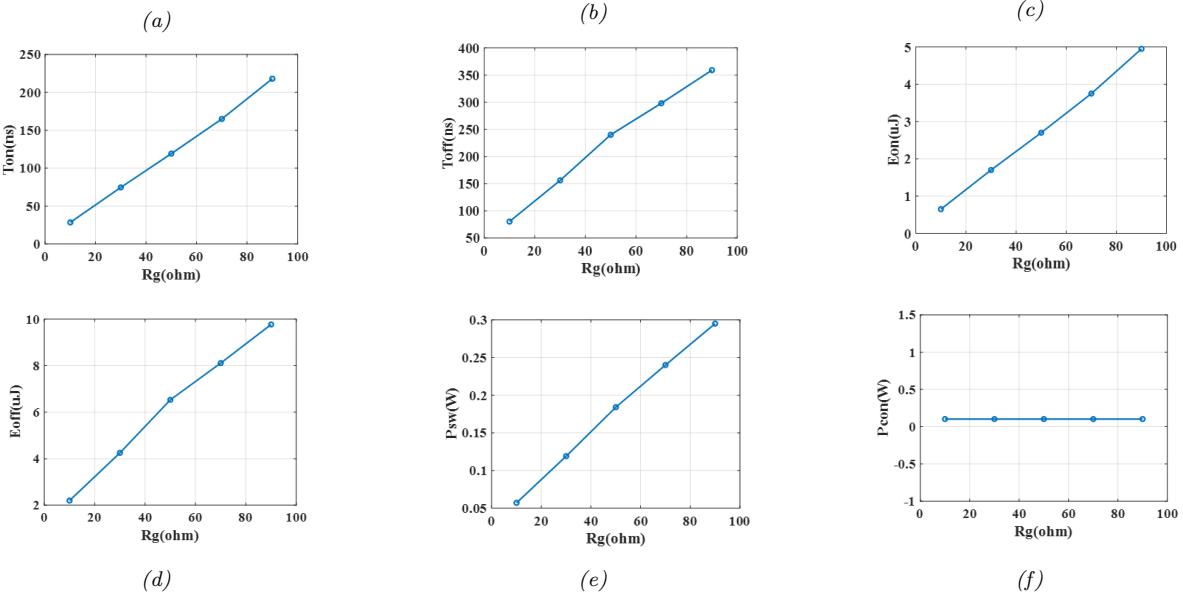


Figure 3.3.1: (a) Variation of on-time with gate resistance (b) Variation of off-time with gate resistance (c) Variation of on-time energy with gate resistance (d) Variation of off-time energy with gate resistance (e) Variation of switching losses with gate resistance (f) Variation of conduction losses with gate resistance

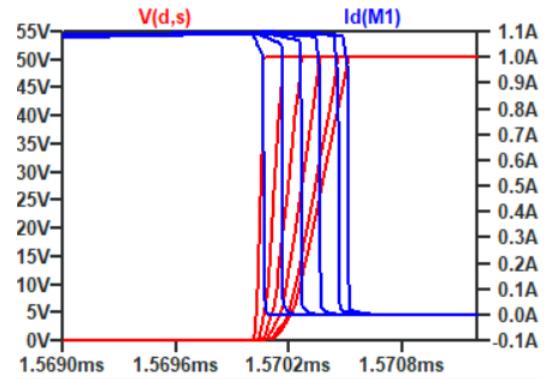


Figure 3.3.1: (g) Turn-off transient

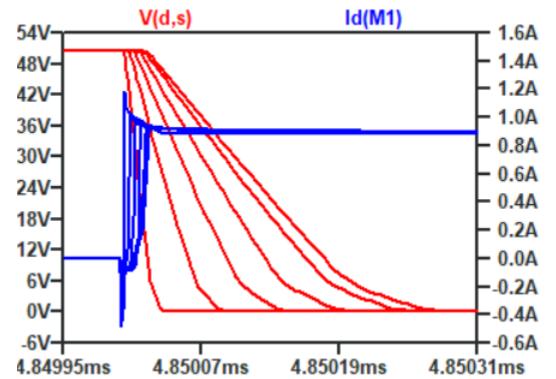


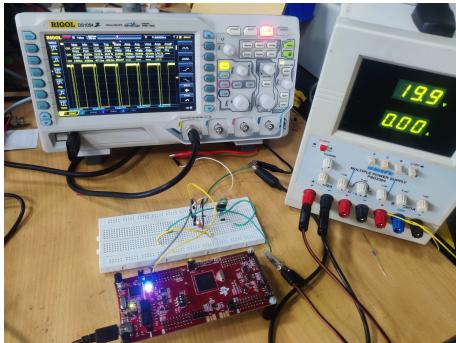
Figure 3.3.1: (h) Turn-on transient

# Chapter 4

## Hardware Setup and Experimental Results

### 4.1 Double Pulse Test

The double pulse test used a TMS320F28379D LaunchPad to generate gate pulses via its EPWM module with precise timing. The MOSFET and gate driver were built on a stable breadboard setup. In testing, a clean double-pulse waveform appeared on the oscilloscope, showing the correct switching of the MOSFET, thus confirming the accurate timing in the firmware. Although only output voltage and pulses could be measured in hardware (inductor current was visible only in simulation), the consistent double-pulse results validated both the code logic and the physical circuit.



(a)



(b)

Figure 4.1.0: (a) Hardware setup of double pulse test using launchpad F28379D (b) Double pulse waveform shown in oscilloscope

### 4.2 PCB Design of Isolated Gate Driver

The isolated gate driver PCB ensures safe and reliable MOSFET switching by maintaining galvanic isolation between the control and power stages. This prevents damage from transients and ground shifts while enabling high-speed operation. The design integrates driver circuitry with isolators, optimized power and signal paths, short low-inductance traces, and well-placed decoupling capacitors to reduce EMI and crosstalk. Its compact layout improves heat dissipation and power density, making it well-suited for high-frequency, high-reliability power conversion systems.

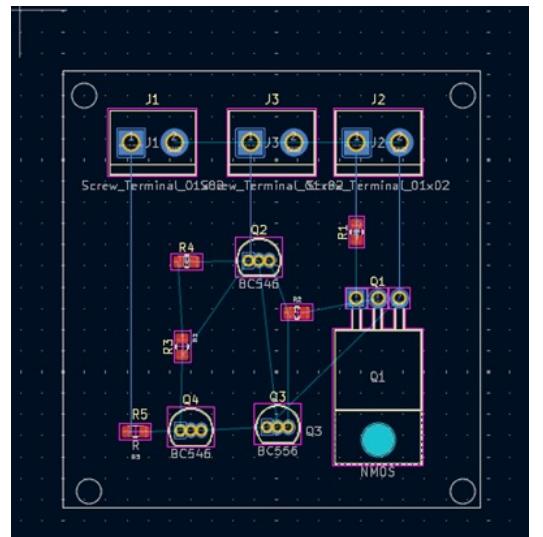


Figure 4.2.0: PCB design of isolated gate driver and its key features

# Chapter 5

## Conclusions and Future Work

### 5.1 Conclusions

The first phase of this project examined the switching behavior of MOSFETs using different types of gate drivers in LTspice simulations. Both isolated and non-isolated drivers were analyzed to understand their impact on noise immunity and switching speed. The double-pulse test highlighted switching losses and transient effects, while the half-bridge study stressed the importance of dead-time and surge control to avoid voltage spikes. These findings improve practical design insight and set the foundation for further work on datasheet development and driver comparisons.

### 5.2 Future Scope of Work

The following shall be implemented until the end of the B.Tech project:

- Simulation and analysis of the switching characteristics of the buck converter with half-bridge switch configuration.
- Simulation and hardware modeling of an isolated gate driver circuit.
- Comparison of practical switching characteristics with the datasheet specifications.

## References

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