

MPCA Lab

Week 1

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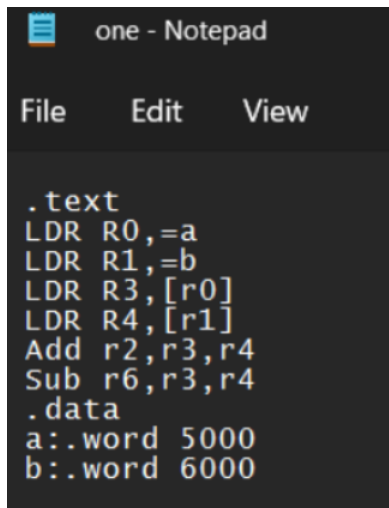
SRN : PES1UG21CS732

Section : L

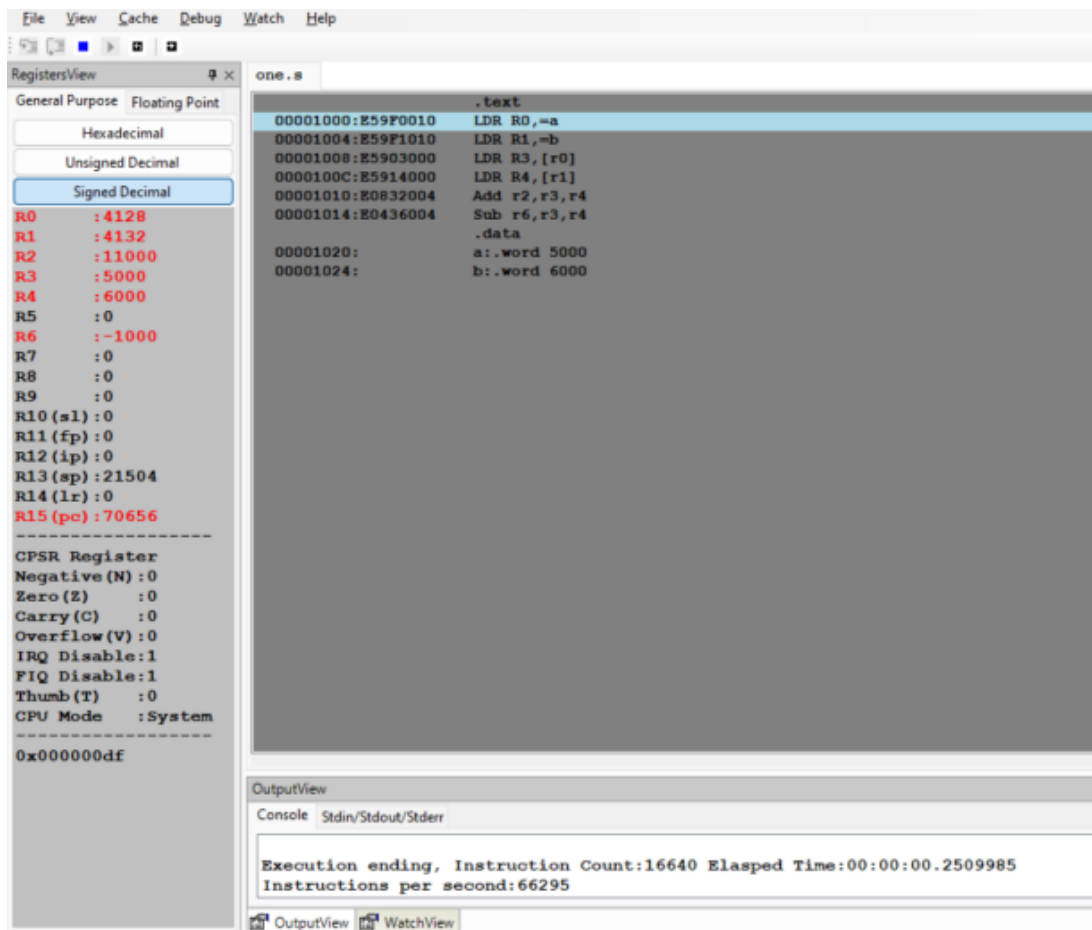
Sem : 4

Roll : 42

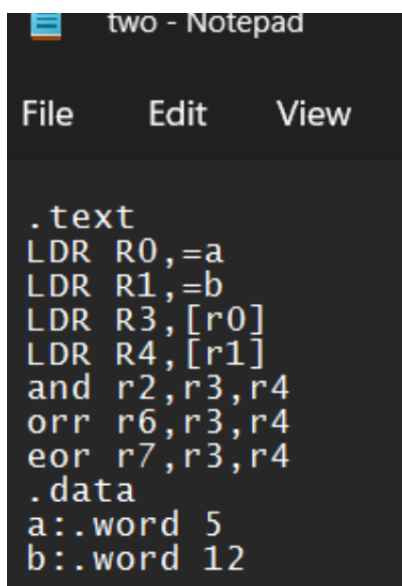
1)

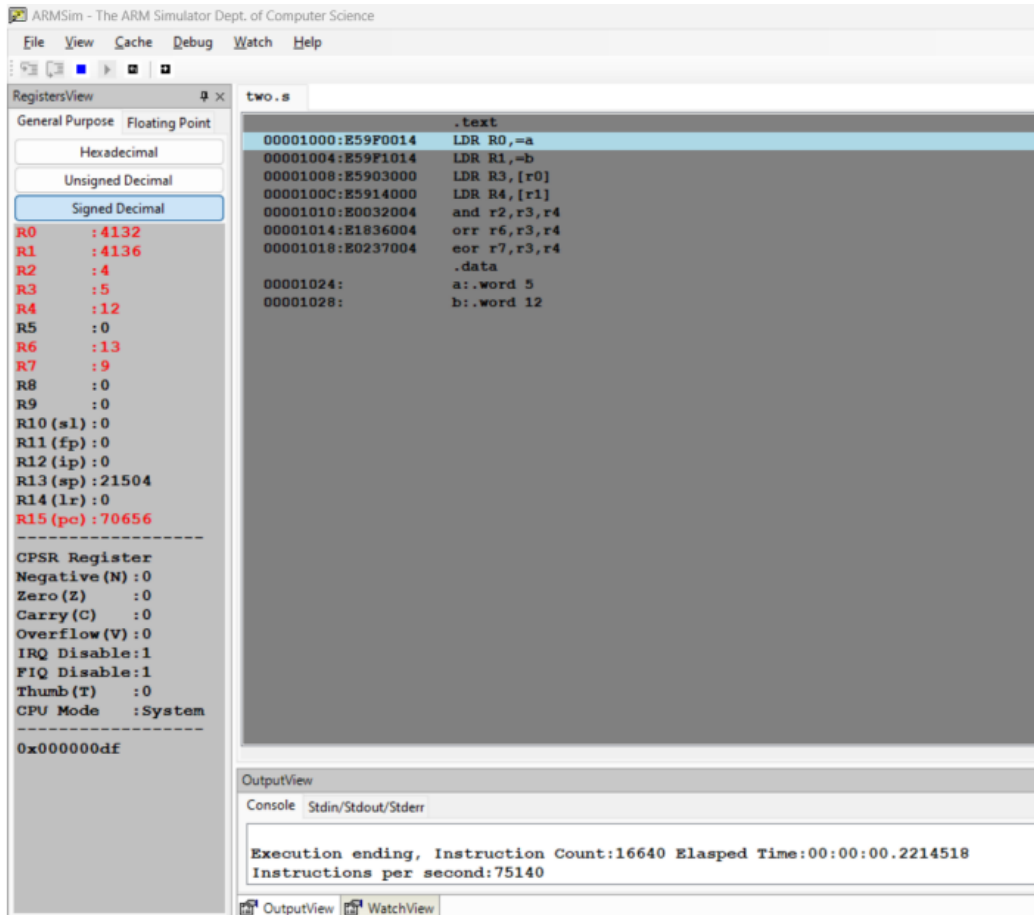


```
one - Notepad
File Edit View
.text
LDR R0,=a
LDR R1,=b
LDR R3,[r0]
LDR R4,[r1]
Add r2,r3,r4
Sub r6,r3,r4
.data
a:.word 5000
b:.word 6000
```



2)





3)

```
three - Notepad
File Edit View

.text
LDR R0,=a
LDR R1,=b
LDR R2,=c
LDR R3,=d
LDR R4,=e
LDR R5,[r0]
LDR R6,[r1]
LDR R7,[r2]
LDR R8,[r3]
LDR R9,[r4]
add r10,r5,r6
add r10,r10,r7
add r10,r10,r8
add r10,r10,r9
.data
a:.word 5
b:.word 12
c:.word 12
d:.word 12
e:.word 12
```

ARMSim - The ARM Simulator Dept. of Computer Science

File View Cache Debug Watch Help

RegistersView

General Purpose Floating Point

Hexadecimal

Unsigned Decimal

Signed Decimal

R0 : 4172

R1 : 4176

R2 : 4180

R3 : 4184

R4 : 4188

R5 : 5

R6 : 12

R7 : 12

R8 : 12

R9 : 12

R10 (s1) : 53

R11 (fp) : 0

R12 (ip) : 0

R13 (sp) : 21504

R14 (lr) : 0

R15 (pc) : 70656

CPSR Register

Negative (N) : 0

Zero (Z) : 0

Carry (C) : 0

Overflow (V) : 0

IRQ Disable : 1

FIQ Disable : 1

Thumb (T) : 0

CPU Mode : System

0x000000df

three.s

```
.text
00001000:E59F0030 LDR R0,=a
00001004:E59F1030 LDR R1,=b
00001008:E59F2030 LDR R2,=c
0000100C:E59F3030 LDR R3,=d
00001010:E59F4030 LDR R4,=e
00001014:E5905000 LDR R5,[r0]
00001018:E5916000 LDR R6,[r1]
0000101C:E5927000 LDR R7,[r2]
00001020:E5938000 LDR R8,[r3]
00001024:E5949000 LDR R9,[r4]
00001028:E085A006 add r10,r5,r6
0000102C:E08AA007 add r10,r10,r7
00001030:E08AA008 add r10,r10,r8
00001034:E08AA009 add r10,r10,r9
.data
0000104C: a:.word 5
00001050: b:.word 12
00001054: c:.word 12
00001058: d:.word 12
0000105C: e:.word 12
```

OutputView

Console Stdin/Stdout/Stderr

Execution ending, Instruction Count:16640 Elapsed Time:00:00:00.2523298

Instructions per second:65945

OutputView WatchView

4)

```
*four - Notepad

File Edit View

.text
LDR R0,=a
LDR R1,=b
LDR R2,[r0]
LDR R3,[r1]
and r4,r3,r2
.data
a:.word 6
b:.word 1
```

ARMSim - The ARM Simulator Dept. of Computer Science

File View Cache Debug Watch Help

RegistersView

General Purpose Floating Point

Hexadecimal

Unsigned Decimal

Signed Decimal

R0 : 4124

R1 : 4128

R2 : 6

R3 : 1

R4 : 0

R5 : 0

R6 : 0

R7 : 0

R8 : 0

R9 : 0

R10 (s1) : 0

R11 (fp) : 0

R12 (ip) : 0

R13 (sp) : 21504

R14 (lr) : 0

R15 (pc) : 70656

CPSR Register

Negative (N) : 0

Zero (Z) : 0

Carry (C) : 0

Overflow (V) : 0

IRQ Disable : 1

FIQ Disable : 1

Thumb (T) : 0

CPU Mode : System

0x000000df

four.s

```
.text
00001000:E59F000C LDR R0,=a
00001004:E59F100C LDR R1,=b
00001008:E5902000 LDR R2,[r0]
0000100C:E5913000 LDR R3,[r1]
00001010:E0034002 and r4,r3,r2
.data
0000101C: a:.word 6
00001020: b:.word 1
```

OutputView

Console Stdin/Stdout/Stderr

Execution ending, Instruction Count:16640 Elapsed Time:00:00:00.2380660

Instructions per second:69896

OutputView WatchView

5)

```
five - Notepad

File Edit View

.text
LDR R0,=a
LDR R1,=b
LDR R2,[r0]
LDR R3,[r1]
andeq r4,r3,r2
subne r5,r2,r3
.data
a:.word 1
b:.word 1
```

ARMSim - The ARM Simulator Dept. of Computer Science

File View Cache Debug Watch Help

RegistersView

General Purpose Floating Point

Hexadecimal

Unsigned Decimal

Signed Decimal

R0 : 4128

R1 : 4132

R2 : 1

R3 : 1

R4 : 0

R5 : 0

R6 : 0

R7 : 0

R8 : 0

R9 : 0

R10 (s1) : 0

R11 (fp) : 0

R12 (ip) : 0

R13 (sp) : 21504

R14 (lr) : 0

R15 (pc) : 70656

CPSR Register

Negative (N) : 0

Zero (Z) : 0

Carry (C) : 0

Overflow (V) : 0

IRQ Disable: 1

FIQ Disable: 1

Thumb (T) : 0

CPU Mode : System

0x000000df

five.s

.text

00001000:E59F0010 LDR R0,=a

00001004:E59F1010 LDR R1,=b

00001008:E5902000 LDR R2,[r0]

0000100C:E5913000 LDR R3,[r1]

00001010:00034002 andeq r4,r3,r2

00001014:10425003 subne r5,r2,r3

.data

00001020: a:.word 1

00001024: b:.word 1

OutputView

Console Stdin/Stdout/Stderr

Execution ending, Instruction Count:16640 Elapsed Time:00:00:00.2125254

Instructions per second:78296

OutputView WatchView