

MPCA Lab

Week 9

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Section : L

Sem : 4

Roll : 42

1. Consider a 4-way set associative mapping with 16 cache blocks and offset bit to 0. The memory block requests are in the order-0, 255, 1, 4, 3, 8, 133, 159, 216, 129, 63, 8, 48, 32, 73, 92, 155. If LRU and FIFO replacement policy is used, which cache block will not be present in the cache? Also, calculate the hit ratio and miss ratio.

Output :

Using FIFO :

ParaCache

Direct Mapped Cache Fully Associative Cache 2-Way SA 4-Way SA Cache Type Analysis Virtual Memory Knowledge Base

Replacement Policies
☒ FIFO ☐ LRU ☐ Random

Write Policies
☒ Write Back ☐ Write Through
☒ Write On Allocate ☐ Write Around

Cache Size (power of 2): 16
 Memory Size (power of 2): 2048
 Offset Bits: 0

Reset Submit

Instruction Load Submit

List of next 10 instructions:

Information
 The cycle has been completed.
 Please submit another instructions

Next Fast Forward

Statistics
 Hit Rate: 6%
 Miss Rate: 94%

List of Previous Instructions:

- Load 0 (Miss)
- Load 255 (Miss)
- Load 1 (Miss)
- Load 4 (Miss)
- Load 3 (Miss)
- Load 8 (Miss)
- Load 133 (Miss)
- Load 159 (Miss)
- Load 216 (Miss)
- Load 129 (Miss)
- Load 63 (Miss)
- Load 8 (Hit)
- Load 48 (Miss)
- Load 32 (Miss)
- Load 73 (Miss)
- Load 92 (Miss)
- Load 155 (Miss)

4-WAY SET ASSOCIATIVE CACHE

Instruction Breakdown

001010101	01	0
9 bit	2 bit	0 bit

Memory Block

0	135 W 0
1	155 W 0
2	187 W 0
3	160 W 0
4	199 W 0
5	194 W 0

Cache Table

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	0	B: 0 W: 0-0	0
1	1	55	B: 155 W: 0-0	0
2	1	65	B: 216 W: 0-0	0
3	1	0	B: 3 W: 0-0	0

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	1	B: 4 W: 0-0	0
1	1	0	B: 1 W: 0-0	0
2	1	c	B: 32 W: 0-0	0
3	1	4c	B: 133 W: 0-0	0

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	2	B: 8 W: 0-0	0
1	1	56	B: 159 W: 0-0	0
2	1	24	B: 92 W: 0-0	0
3	1	18	B: 63 W: 0-0	0

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	12	B: 48 W: 0-0	0
1	1	4a	B: 129 W: 0-0	0
2	0	-	0	0
3	1	1c	B: 73 W: 0-0	0

Missing Cache Block : 255

Hit Rate - 6%

Miss Rate - 94%

Using LRU :

ParaCache

Direct Mapped Cache Fully Associative Cache 2-Way SA 4-Way SA Cache Type Analysis Virtual Memory Knowledge Base

Replacement Policies
☐ FIFO ☒ LRU ☐ Random

Write Policies
☒ Write Back ☐ Write Through
☒ Write On Allocate ☐ Write Around

Cache Size (power of 2) 16
Memory Size (power of 2) 2048
Offset Bits 0

Reset Submit

Instruction
Load

Information
The cycle has been completed.
Please submit another instructions

Next Fast Forward

Statistics
Hit Rate 6%
Miss Rate 94%
List of Previous Instructions :
• Load 2 (Miss)
• Load 203 (Miss)
• Load 1 (Miss)
• Load 4 (Miss)
• Load 3 (Miss)
• Load 3 (Miss)
• Load 133 (Miss)
• Load 189 (Miss)
• Load 216 (Miss)
• Load 129 (Miss)
• Load 63 (Miss)
• Load 8 (Miss)
• Load 48 (Miss)
• Load 22 (Miss)
• Load 72 (Miss)
• Load 92 (Miss)
• Load 105 (Miss)

4-WAY SET ASSOCIATIVE CACHE

Instruction Breakdown

001010101	01	0
0 bit	2 bit	0 bit

Memory Block

0	1	2	3
B: 155 W: 0	B: 156 W: 0	B: 157 W: 0	B: 158 W: 0
B: 159 W: 0	B: 160 W: 0	B: 161 W: 0	B: 162 W: 0

Cache Table

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	0	B: 0 W: 0-0	0
1	1	55	B: 155 W: 0-0	0
2	1	85	B: 216 W: 0-0	0
3	1	0	B: 3 W: 0-0	0

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	1	B: 4 W: 0-0	0
1	1	0	B: 1 W: 0-0	0
2	1	c	B: 32 W: 0-0	0
3	1	4c	B: 153 W: 0-0	0

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	2	B: 6 W: 0-0	0
1	1	56	B: 159 W: 0-0	0
2	1	24	B: 52 W: 0-0	0
3	1	18	B: 63 W: 0-0	0

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	12	B: 48 W: 0-0	0
1	1	4a	B: 129 W: 0-0	0
2	0	-	0	0
3	1	1c	B: 73 W: 0-0	0

Missing Cache Block : 255

Hit Rate - 6%

Miss Rate - 94%