

MPCA Lab

Week 8

Name : Yashaswini Ippili

SRN : PES1UG21CS732

Section : L

Sem : 4

Roll : 42

- Consider a fully associative cache with 8 cache blocks (0-7). The memory block requests are in the order-
4, 3, 25, 8, 19, 6, 25, 8, 16, 35, 45, 22, 8, 3, 16, 25, 7
If LRU replacement policy is used, which cache block will have memory block 16?
Also, calculate the hit ratio and miss ratio.

Output :

ParaCache

Direct Mapped Cache Fully Associative Cache 2-Way SA 4-Way SA Cache Type Analysis Virtual Memory Knowledge Base

Replacement Policies
☐ FIFO ☒ LRU ☐ Random

Write Policies
☒ Write Back ☐ Write Through
☒ Write On Allocate ☐ Write Around

Cache Size (power of 2) 8
 Memory Size (power of 2) 2048
 Offset Bits 0

Reset Submit

Instruction
 Load 0
 List of next 10 instructions
 Submit

Information
 The cycle has been completed.
 Please submit another instructions

Next Fast Forward

Statistics
 Hit Rate 29%
 Miss Rate 71%

List of Previous Instructions :

- Load 4 (Miss)
- Load 3 (Miss)
- Load 25 (Miss)
- Load 8 (Miss)
- Load 19 (Miss)
- Load 6 (Miss)
- Load 25 (Miss)
- Load 8 (Miss)
- Load 16 (Miss)
- Load 35 (Miss)
- Load 45 (Miss)
- Load 22 (Miss)
- Load 8 (Miss)
- Load 3 (Miss)
- Load 16 (Miss)
- Load 25 (Miss)
- Load 7 (Miss)

FULLY ASSOCIATIVE CACHE

Instruction Breakdown
 0000000111 0
 11 bit 0 bit

Memory Block
 0: 7 W 0
 1: 8 W 0
 2: 8 W 0
 3: 8 W 0
 4: 8 W 0
 5: 8 W 0
 6: 8 W 0
 7: 8 W 0

Cache Table

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	0001000101	BLOCK 45 WORD 0 - 0	0
1	1	0000100010	BLOCK 22 WORD 0 - 0	0
2	1	0000100101	BLOCK 25 WORD 0 - 0	0
3	1	0000010000	BLOCK 8 WORD 0 - 0	0
4	1	0000000011	BLOCK 3 WORD 0 - 0	0
5	1	0000000111	BLOCK 7 WORD 0 - 0	0
6	1	0000010110	BLOCK 16 WORD 0 - 0	0
7	1	0000110101	BLOCK 35 WORD 0 - 0	0

Hit ratio : 29%

Miss ratio : 71%

Memory Block 16 is placed in cache block 6.

2. Consider the cache has 4 blocks. For the memory references-

5,12, 13, 17, 4, 12, 13, 17, 2, 13, 19, 13, 43, 61, 19

Which of the memory blocks will be present in the cache at the end of the sequence and What is the hit ratio and miss ratio for the following cache replacement algorithms -

a. Fully Associative FIFO

b. Fully Associative LRU

c. 2-way set associative mapping using LRU

a. Output :

The screenshot shows the ParaCache simulation interface. The configuration is set to a Fully Associative Cache with 4 blocks, 2048 memory size, and 0 offset bits. The replacement policy is FIFO. The instruction sequence is 5, 12, 13, 17, 4, 12, 13, 17, 2, 13, 19, 13, 43, 61, 19. The simulation results show a hit rate of 33% and a miss rate of 67%. The list of previous instructions is: Load 5 (Miss), Load 12 (Miss), Load 17 (Miss), Load 4 (Miss), Load 13 (Hit), Load 17 (Hit), Load 2 (Miss), Load 13 (Hit), Load 19 (Miss), Load 13 (Hit), Load 43 (Miss), Load 61 (Miss), Load 19 (Hit). The next index is 2 and the last index is 1.

Cache Table

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	00001000011	BLOCK 43 WORD 0 - 0	0
1	1	00001000011	BLOCK 61 WORD 0 - 0	0
2	1	00000011001	BLOCK 19 WORD 0 - 0	0
3	1	00000010011	BLOCK 13 WORD 0 - 0	0

The memory blocks that are not present in the cache are 5, 12, 17, 4 and 2.

Hit rate : 33%

Miss rate : 67%

b. Output:

ParaCache

Direct Mapped Cache Fully Associative Cache 2-Way SA 4-Way SA Cache Type Analysis Virtual Memory Knowledge Base

Replacement Policies

☐ FIFO ☒ LRU ☐ Random

Write Policies

☒ Write Back ☐ Write Through
☒ Write On Allocate ☐ Write Around

Cache Size (power of 2)

4

Memory Size (power of 2)

2048

Offset Bits

0

Reset Submit

Instruction

Load ▾ [pc.hex#] 0

List of next 10 instructions:

Load Instruction Submit

Information

The cycle has been completed.
Please submit another instructions

Next Fast Forward

Statistics

Hits Rate	40%
Miss Rate	60%

List of Previous Instructions :

- Load 5 [Miss]
- Load 12 [Miss]
- Load 12 [Miss]
- Load 12 [Miss]
- Load 17 [Miss]
- Load 4 [Miss]
- Load 12 [Hit]
- Load 12 [Hit]
- Load 17 [Hit]
- Load 2 [Miss]
- Load 13 [Hit]
- Load 19 [Miss]
- Load 19 [Hit]
- Load 43 [Miss]
- Load 61 [Miss]
- Load 19 [Hit]

Next Index: 2
Last Index: 1

FULLY ASSOCIATIVE CACHE

➡ Instruction Breakdown

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	0000110001	BLOCK 61 WORD 0 - 0	0
1	1	0000011001	BLOCK 19 WORD 0 - 0	0
2	1	0000011001	BLOCK 13 WORD 0 - 0	0
3	1	0000100011	BLOCK 43 WORD 0 - 0	0

⚑ Memory Block

0: 19 16 0
8: 14 16 0
8: 18 16 0
8: 12 16 0
8: 10 16 0
A: 18 16 0

⚑ Cache Table

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	0000110001	BLOCK 61 WORD 0 - 0	0
1	1	0000011001	BLOCK 19 WORD 0 - 0	0
2	1	0000011001	BLOCK 13 WORD 0 - 0	0
3	1	0000100011	BLOCK 43 WORD 0 - 0	0

The memory blocks that are not present in the cache are 5, 12, 17, 4 and 2.

Hit rate : 40%

Miss rate : 60%

c. Output :

ParaCache

Direct Mapped Cache Fully Associative Cache 2-Way SA 4-Way SA Cache Type Analysis Virtual Memory Knowledge Base

Replacement Policies
☐ FIFO ☒ LRU ☐ Random

Write Policies
☒ Write Back ☐ Write Through
☒ Write On Allocate ☐ Write Around

Cache Size (power of 2) 4
 Memory Size (power of 2) 2048
 Offset Bits 0

Reset Submit

Instruction
 Load
 List of next 10 instructions

Information
 The cycle has been completed.
 Please submit another instructions

Next Fast Forward

Statistics
 Hit Rate 33%
 Miss Rate 67%

List of Previous Instructions
 + Load 5 (Miss)
 + Load 12 (Miss)
 + Load 13 (Miss)
 + Load 17 (Miss)
 + Load 4 (Miss)
 + Load 13 (Hit)
 + Load 13 (Hit)
 + Load 2 (Miss)
 + Load 13 (Hit)
 + Load 19 (Miss)
 + Load 13 (Hit)
 + Load 43 (Miss)
 + Load 51 (Miss)
 + Load 19 (Miss)

2-WAY SET ASSOCIATIVE CACHE

Instruction Breakdown

	1	0
000001100		
10 bit	1 bit	0 bit

Memory Block

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	9	B 12 W 0 - 0	0
1	1	c	BLOCK 19 WORD 0 - 0	0

Cache Table

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	1	BLOCK 2 WORD 0 - 0	0
1	1	30	BLOCK 61 WORD 0 - 0	0

The memory blocks that are not present in the cache are 5, 17, 13, 4 and 43.

Hit ratio : 33%

Miss ratio : 67%