

# **MPCA Lab**

## **Week 7**

**Name :** Yashaswini Ippili

**SRN :** PES1UG21CS732

**Section :** L

**Sem :** 4

**Roll :** 42

1. Consider a direct mapped cache with 8 cache blocks (0-7). If the memory block requests are in the order 4, 3, 25, 8, 19, 6, 25, 8, 16, 35, 45, 22, 8, 3, 16, 25, 7, which of the memory blocks will be present in the cache at the end of the sequence? Also, calculate the hit ratio and miss ratio.

Output :

ParaCache

Direct Mapped Cache Fully Associative Cache 2-Way SA 4-Way SA Cache Type Analysis Virtual Memory Knowledge Base

Write Policies  
☒ Write Back ☐ Write Through  
☒ Write On Allocate ☐ Write Around

Cache Size (power of 2) 32  
Memory Size (power of 2) 2048  
Offset Bits 2

Reset Submit

Instruction Breakdown  
000000 001 11  
0 bit 3 bit 2 bit

Memory Block

Block	Word 0	Word 1	Word 2	Word 3
0	0	0	0	0
1	0	0	0	0
2	0	0	0	0
3	0	0	0	0
4	0	0	0	0
5	0	0	0	0
6	0	0	0	0
7	0	0	0	0

Cache Table

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	000000	BLOCK 0 WORD 0 - 3	0
1	1	000000	BLOCK 1 WORD 0 - 3	0
2	1	000000	BLOCK 2 WORD 0 - 3	0
3	0	-	0	0
4	0	-	0	0
5	1	000000	BLOCK 5 WORD 0 - 3	0
6	1	000000	BLOCK 6 WORD 0 - 3	0
7	0	-	0	0

Information  
The cycle has been completed.  
Please submit another instructions

Next Fast Forward

Statistics  
Hit Rate 12%  
Miss Rate 88%

List of Previous Instructions

- Load 4 (Miss)
- Load 3 (Miss)
- Load 25 (Miss)
- Load 8 (Miss)
- Load 19 (Miss)
- Load 6 (Miss)
- Load 25 (Miss)
- Load 8 (Miss)
- Load 16 (Miss)
- Load 35 (Miss)
- Load 45 (Miss)
- Load 22 (Miss)
- Load 8 (Miss)
- Load 3 (Miss)
- Load 16 (Miss)
- Load 25 (Miss)
- Load 7 (Miss)

2. Consider the cache has 4 blocks. For the memory references- 5,12, 13, 17, 4, 12, 13, 17, 2, 13, 19, 13, 43, 61, 19. What is the hit and miss ratio direct mapping. Which of the memory blocks will be present in the cache at the end of the sequence?

Output :

ParaCache

Direct Mapped Cache Fully Associative Cache 2-Way SA 4-Way SA Cache Type Analysis Virtual Memory Knowledge Base

Write Policies  
☒ Write Back ☐ Write Through  
☒ Write On Allocate ☐ Write Around

Cache Size (power of 2) 16  
Memory Size (power of 2) 2048  
Offset Bits 2  
Reset Submit

Instruction  
Load  on next#  
List of next 10 instructions  
Submit

Information  
The cycle has been completed.  
Please submit another instructions  
Next Fast Forward

Statistics  
Hit Rate 33%  
Miss Rate 67%  
List of Previous Instructions  
+ Load 5 [Miss]  
+ Load 12 [Miss]  
+ Load 13 [Hit]  
+ Load 17 [Miss]  
+ Load 4 [Miss]  
+ Load 12 [Hit]  
+ Load 13 [Hit]  
+ Load 17 [Miss]  
+ Load 2 [Miss]  
+ Load 12 [Miss]  
+ Load 19 [Miss]  
+ Load 13 [Hit]  
+ Load 43 [Miss]  
+ Load 61 [Miss]  
+ Load 19 [Hit]

**DIRECT MAPPED CACHE**

Instruction Breakdown

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	0000110	BLOCK 18 WORD 0-3	0
1	1	0000001	BLOCK 5 WORD 0-3	0
2	1	0000001	BLOCK 6 WORD 0-3	0
3	0	-	0	0

Memory Block

Block	Word	Value
0	0	B 0 W 0
0	1	B 0 W 1
0	2	B 0 W 2
0	3	B 0 W 3
1	0	B 1 W 0
1	1	B 1 W 1
1	2	B 1 W 2
1	3	B 1 W 3
2	0	B 2 W 0
2	1	B 2 W 1
2	2	B 2 W 2
2	3	B 2 W 3
3	0	B 3 W 0
3	1	B 3 W 1
3	2	B 3 W 2
3	3	B 3 W 3

3. Consider a main memory with 64-byte capacity and a cache memory of 8 bytes, initially empty. Consider the following addresses generated by CPU  
0,3,4,1,2,5,7,6,0,3,11,1,5,15,9,4,0,4,3. List the data that is replaced in cache lines.

Output :

ParaCache

Direct Mapped Cache Fully Associative Cache 2-Way SA 4-Way SA Cache Type Analysis Virtual Memory Knowledge Base

Write Policies  
☒ Write Back  
☐ Write Through  
☒ Write On Allocate  
☐ Write Around

Cache Size (power of 2) 8  
 Memory Size (power of 2) 64  
 Offset Bits 2

Reset Submit

Instruction  
 Load 0x00000000  
 List of next 10 instructions  
 Submit

Information  
 The cycle has been completed.  
 Please submit another instructions

Next Fast Forward

Statistics  
 Hit Rate 90%  
 Miss Rate 42%

List of Previous Instructions  
 + Load 0 (Miss)  
 + Load 3 (Hit)  
 + Load 4 (Miss)  
 + Load 1 (Hit)  
 + Load 2 (Hit)  
 + Load 5 (Hit)  
 + Load 7 (Hit)  
 + Load 6 (Hit)  
 + Load 0 (Hit)  
 + Load 3 (Hit)  
 + Load 11 (Miss)  
 + Load 1 (Miss)  
 + Load 2 (Hit)  
 + Load 15 (Miss)  
 + Load 9 (Miss)  
 + Load 4 (Miss)  
 + Load 0 (Miss)  
 + Load 4 (Hit)  
 + Load 3 (Hit)

DIRECT MAPPED CACHE

Instruction Breakdown  
 000 0 11  
 3 bit 1 bit 2 bit

Memory Block  
 B 0 W 0 B 0 W 1 B 0 W 2 B 0 W 3  
 B 1 W 0 B 1 W 1 B 1 W 2 B 1 W 3  
 B 2 W 0 B 2 W 1 B 2 W 2 B 2 W 3  
 B 3 W 0 B 3 W 1 B 3 W 2 B 3 W 3  
 B 4 W 0 B 4 W 1 B 4 W 2 B 4 W 3  
 B 5 W 0 B 5 W 1 B 5 W 2 B 5 W 3

Cache Table  

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	000	BLOCK 0 WORD 0 - 3	0
1	1	000	BLOCK 1 WORD 0 - 3	0