The Bombay Salesisan Society's

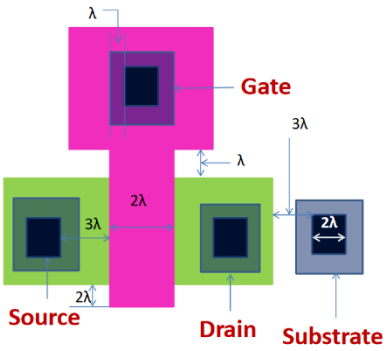
Don Bosco Institute of Technology,Kurla(W), Mumbai

INTERNAL ASSESSMENT I Solution

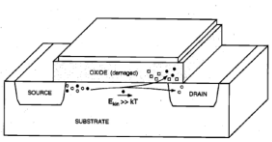
ECC503: Digital VLSI **Max. Marks: 20**

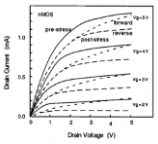
21/08/2024 **Time: 10.00 – 11.00am**

1. Attempt any five from 1a to 1f.
2. Attempt one sub-question from each of the remaining two questions.

Q. No.	Question
1a	**Explain Drain Induced barrier Lowering effect.** **Answer:** In short channel device, when positive voltage is applied to Drain of n channel MOSFET, drain channel junction becomes reverse bias and width of the drain depletion region penetrates towards source. Due to this drain depletion region electric field barrier at the source junction reduces which enables electrons from source region to entre in the channel and constitute drain current. This current leads to leakage current. This effect is called as Drain Induced Barrier Lowering. Full correctness of answer as per this will get **2** Marks. Partial correctness will get partial marks and no relevance with this answer will get zero mark. If students draw only relevant sketch, then he/she will get partial marks
1b	**Draw layout of NMOS using lambda rules.**  • Layout as per model answer gets Full (2) marks. • Only layout and no rules partial marking.
1c	**In N-Channel MOSFET unCox=150uA/V^2, W=20um, L=1um, V_{TO}=1V Find I_{DS} if (i)V_{GS}=5V and V_{DS}=5V (ii) V_{DS}=2V and V_{GS}=5V** **Answer:** (i) When V_{GS} and V_{DS} is 5V MOSFET is in Saturation region and current is given by $I_D(sat) = \frac{\mu_n \cdot C_{ox}}{2} \cdot \frac{W}{L} \cdot (V_{GS} - V_T)^2$ $I_{DSsat} = \frac{150 \times 20 \times 16}{2} = 24mA$ • Correct equation 0.5 Mark • Correct answer 0.5 Marks (ii) When V_{DS}=2V and V_{GS} is 5V MOSFET is linear region and current is given by $I_D(lin) = \frac{\mu_n \cdot C_{ox}}{2} \cdot \frac{W}{L} \cdot [2 \cdot (V_{GS} - V_T)V_{DS} - V_{DS}^2]$ I_{DSlin}= 21mA • Correct equation 0.5 Mark • Correct answer 0.5 Marks

1d **Explain hot carrier effect.**



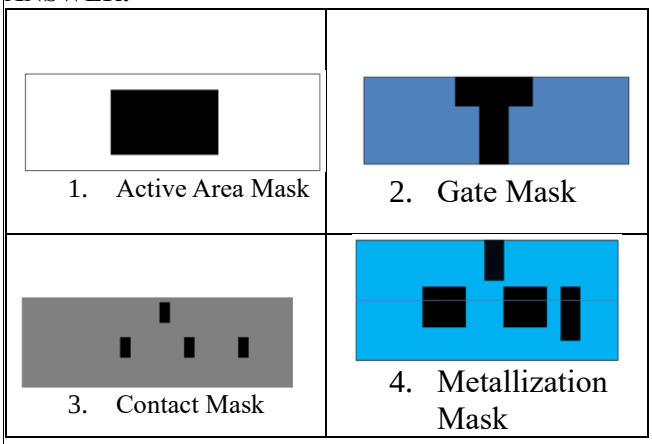


In short channel MOSFET due to aggressive scaling vertical electrical field and lateral electric field increases. Electric field near drain junction is high since drain is reversed biased for normal operation. High electric field increases velocity of electrons which causes increase in kinetic energy of elec. \trons. These high energy electrons which are called as hot electrons hit the oxide at the drain junction and damages the oxide near drain junction. Due to this threshold voltage of MOSFET increases which further lowers the performance of MOSFET. This effect is called as Hot Carrier effect.

Full correctness of answer as per this will get 2 Marks. Partial correctness will get partial marks and no relevance with this answer will get zero mark. If students draw only relevant sketches, then he/she will get partial marks

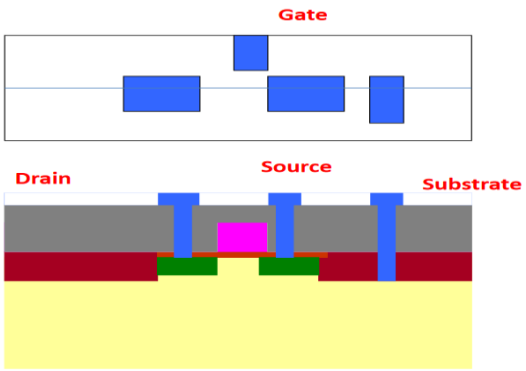
1e **List and draw various masks used in the fabrication process of NMOS transistor in the order of their use.**

ANSWER:



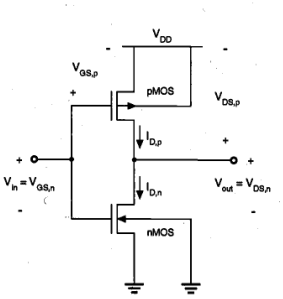
- Correct Mask name 0.25 Mark
- Correct sketch 0.25 Marks

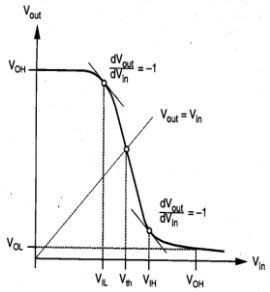
1f **Draw cross section of MOSFET after processing of Metallization Mask along with metallization mask**



- Mentalization Mask 0.5 Mark
- Cross section 1.5 Marks

2a **Draw CMOS inverter and derive expression for V_{IH} and V_{IL}**





Above Figures 1 Mark

Derivation for V_{IL}:

When Vin=V_{IL} slope of voltage transfer characteristics is -1.

At this point PMOS is in linear region and NMOS is in saturation. Therefore

$$\frac{k_n}{2}\cdot\left(V_{GS,n}-V_{T0,n}\right)^2=\frac{k_p}{2}\cdot\left[2\cdot\left(V_{GS,p}-V_{T0,p}\right)\cdot V_{DS,p}-{V_{DS,p}}^2\right]$$

Replacing V_{GS} and V_{DS} in terms of Vin and Vo

$$\frac{k_n}{2}\cdot\left(V_{in}-V_{T0,n}\right)^2=\frac{k_p}{2}\cdot\left[2\cdot\left(V_{in}-V_{DD}-V_{T0,p}\right)\cdot\left(V_{out}-V_{DD}\right)-\left(V_{out}-V_{DD}\right)^2\right]$$

To satisfy the derivative condition at VILE we differentiate both sides of above eqn with respect to Vin.

$$k_n\cdot\left(V_{in}-V_{T0,n}\right)=k_p\cdot\left[\left(V_{in}-V_{DD}-V_{T0,p}\right)\cdot\left(\frac{dV_{out}}{dV_{in}}\right)+\left(V_{out}-V_{DD}\right)-\left(V_{out}-V_{DD}\right)\cdot\left(\frac{dV_{out}}{dV_{in}}\right)\right]$$

Substituting $V_{in}=V_{IL}$ and $(dV_{out}/dV_{in})=-1$ in above equation we obtain

$$k_n\cdot\left(V_{IL}-V_{T0,n}\right)=k_p\cdot\left(2\,V_{out}-V_{IL}+V_{T0,p}-V_{DD}\right)$$

Rearranging terms gives

$$V_{IL}=\frac{2\,V_{out}+V_{T0,p}-V_{DD}+k_R\,V_{T0,n}}{1+k_R}$$

Each correct equation gets 0.5 Marks. Max marks will be 2

Derivation for V_{IH}:

When the input voltage is equal to V_{IH}, the nMOS transistor operates in the linear region, and the pMOS transistor operates in saturation.

$$\frac{k_n}{2}\cdot\left[2\cdot\left(V_{GS,n}-V_{T0,n}\right)\cdot V_{DS,n}-{V_{DS,n}}^2\right]=\frac{k_p}{2}\cdot\left(V_{GS,p}-V_{T0,p}\right)^2$$

$$\frac{k_n}{2}\cdot\left[2\cdot\left(V_{in}-V_{T0,n}\right)\cdot V_{out}-{V_{out}}^2\right]=\frac{k_p}{2}\cdot\left(V_{in}-V_{DD}-V_{T0,p}\right)^2$$

$$k_n\cdot\left[\left(V_{in}-V_{T0,n}\right)\cdot\left(\frac{dV_{out}}{dV_{in}}\right)+V_{out}-V_{out}\cdot\left(\frac{dV_{out}}{dV_{in}}\right)\right]=k_p\cdot\left(V_{in}-V_{DD}-V_{T0,p}\right)$$

Substituting $V_{in}=V_{IH}$ and $(dV_{out}/dV_{in})=-1$ in

$$k_n\cdot\left(-V_{IH}+V_{T0,n}+2\,V_{out}\right)=k_p\cdot\left(V_{IH}-V_{DD}-V_{T0,p}\right)$$

$$V_{IH}=\frac{V_{DD}+V_{T0,p}+k_R\cdot\left(2\,V_{out}+V_{T0,n}\right)}{1+k_R}$$

Each correct equation gets 0.5 Marks. Max marks will be 2

2b **Define CVS and explain its impact on MOSFET performance by deriving necessary equations**

- In constant voltage scaling lateral and vertical dimensions of MOSFET are scaled by factor S while all voltages V_{GS}, V_{DS}, V_T are kept constant.

Impact on Drain Current

Drain current before scaling is given by

$$I_{DS}=\frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS}-V_T)^2$$

Drain current after constant field scaling is given by

$$I_{DS}^{'}=\frac{1}{2}\mu_n SC_{ox}\frac{W/S}{L/S}(V_{GS}-V_T)^2=S\times I_{DS}$$

Drain current increases by factor S

Impact on Power

Power before scaling is given by

$$P=V_{DS}x\,I_{DS}$$

After scaling power is given by

$$P^{'}=V_{DS}*S\times I_{DS}=P=S\times P$$

Power increases by factor S

Impact of MOSFET Area

Area before scaling is given by

A= WxL

Area after scaling is given by

$$A^{'}=\frac{W}{S}\times\frac{L}{S}=\frac{A}{S^2}$$

Area reduces by factor S^2

Impact on Power Density

Power density before scaling is given by

$$\frac{P}{A}=\frac{V_{DS}\times I_{DS}}{W\times L}$$

Power density after constant field scaling is given by

$$\frac{P^{'}}{A^{'}}=\frac{V_{DS}\times S\times I_{DS}}{\frac{W}{S}\times\frac{L}{S}}=S^3\times\frac{P}{A}$$

Power desnsity after constant voltage scaling increases by factor S^3

Impact on Delay

Delay before scaling is given by

$$\tau=\frac{C\times V}{I}=\frac{W\times L\times C_{ox}\times V_{DS}}{I_{DS}}$$

Delay after scaling is given by

$$\tau^{'}=\frac{\frac{W}{S}\times\frac{L}{S}\times S\times C_{ox}\times V_{DS}}{S\times I_{DS}}$$

$$\tau^{'}=\frac{\tau}{S^2}$$

Dealy after constant field scaling reduces by factor S^2

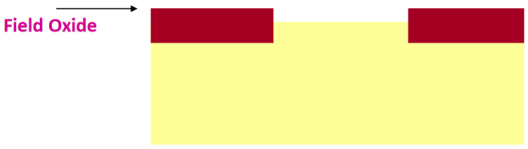
Explanation and derivation of each effect gets 1 Mark

3a **Give process flow of NMOS fabrications with the help of various masks and cross-section after each process**

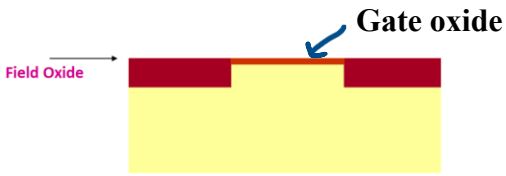
1. **Oxidation**

2. **Photolithography with Active area mask**

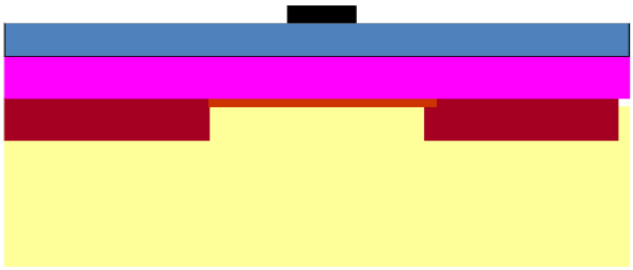
3. **Field Oxidation**



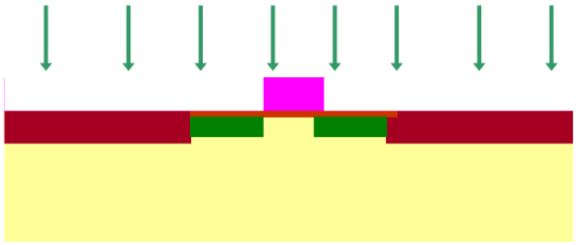
4. **Thin Gate Oxide**



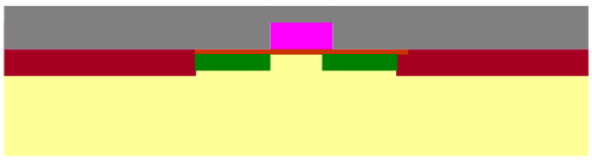
5. **Photolithography Gate Mask**

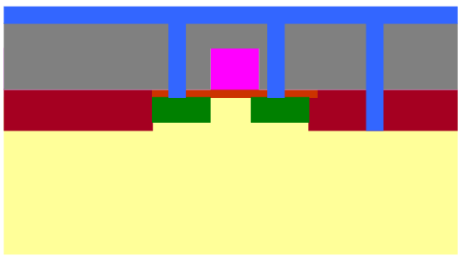
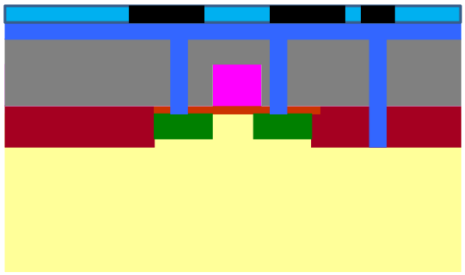
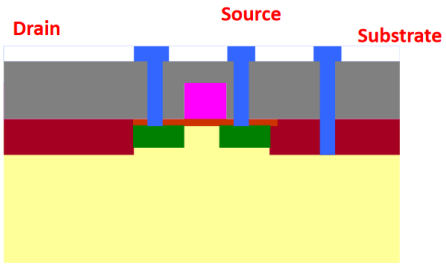


6. **N+ Source Drain Implant**



7. **Contact Mask**



	8. Metallization Process  **9. Photolithography Metallization Mask**   **10. After Photolithography and etching**  **Each step gets 0.5 Marks**
3b	**Give process flow of PMOS fabrications with the help of various masks and cross-section after each process** **Same as above**

After successful completion of the course student will be able to:

ECC503.1: Know various tools and processes used in VLSI Design (Knowing)
ECC503.2: Explain working of various CMOS combinational and sequential circuits used in VLSI Design (Understanding)
ECC503.3: Derive expressions for performance parameters of basic building blocks like CMOS inverter. (Applying)
ECC503.4: Relate performance parameters with design parameters of VLSI circuits. (Analysing)
ECC503.5: Select suitable circuit and design style for given application. (Evaluating)
ECC503.6: Design and realize various combinational and sequential circuits for given specifications. (Designing)