CSE-511 COMPUTER ARCHITECTURE

End-Semester Group Project Evaluation: (Group-10)

Group Members:

- Aanya Trehan (aanya20419@iiitd.ac.in)
- Apoorva Arya (apoorva20032@iiitd.ac.in)
- Jayan Pahuja (jayan20071@iiitd.ac.in)
- Yashika Singh (yashika20161@iiitd.ac.in)

Mid-Semester Deliverables:

We have elaborated the mid-project deliverables for your convenience, which can be found only after reading the aforementioned project's details.
Following are deliverables for MPE:
1. Your simulator must read and interpret the traffic file.
2. Your simulator must be able to read and interpret the delays file.
3. Your simulator must also support at least one of the routing algorithms.
4. Your simulator must also be able to inject packets as per the traffic file.
5. A working simulator that can generate the log file for at least PVA mode.
6. A working simulator that can generate the report file for at least PVA mode.
7. The log file should include the cycle count and the flits received in that cycle.

End-Semester Deliverables:
Please ensure the following are completed by EPE:
1. Whatever you could not implement in MPE has to be completed before EPE.
2. All the modes, i.e., the PVS and PVA, must be implemented and run on the same input files – traffic and delays.
    i. The delays file is directly used for PVA mode, but delays have to be derived and independently modified in PVS mode without changing the original delays file.
    ii. Apple-to-apple performance comparison has to be clearly shown for PVS and PVA.
3. The two types of graphs must be generated for both PVA and PVS modes.

Github Repository Link:

https://github.com/Yashika01Singh/CA_Project

Files used:

- File: clock.py -
  In this file, we have initialized the clock structure in which we have 3 functions for update, start and stopping the clock cycle. Also, the implementation for Gaussian Distribution is implemented in this file. We ensure that the clock frequency remains unchanged for both PVS and PVA modes, and the delays for each router are processed and sent as gaussian_delays.txt

- File: main.py
  This is the main file from which we control the simulation. In this, we see that we first instantiate the logger file, and then use the traffic and delays file to extract the output. Then for each of the elements, we process the flits, and transmit them from the start router into the mesh.

- File: mesh.py
  In this file, we define the system of routers, as a 3x3 mesh, in which routers are connected as follows:

  A - (0,0)
  B - (1,0)
  C - (2,0)
  D - (0,1)
  E - (1,1)
  F - (2,1)
  G - (0,2)
  H - (1,2)
  I - (2,2)

  We then define the connections and functions for update and injection.

- File: packet.py
  In this file, we define each of the flits, deriving it from the 96 bits, where 32 bits of header, body and tail flit are divided.

- File: port.py
  In this file, we define the output and input edge for each port, and define a function for input and output edge.

- File: processing_entity.py

- File: router.py
  In this define the intricate connections of the router, for each of the directions, 5 input ports, 5 output ports, and make the connections as well. We define the switch allocator function, which defines the coordinates to go next depending on the routing algorithm.