Project Seminar

Development of a analog-digital converter board for an ECG application in KiCad 8 and programming ESP32-S3 micro-controller for data transmission to a data sink

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Date: 1st July 2024

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1 Introduction of Kicad

KiCad is an open-source software suite for electronic design automation (EDA), primarily used for the creation of schematics and printed circuit board layouts. It provides tools for schematic capture, PCB layout, and 3D viewing of the PCB. KiCad is a popular choice among professionals in the electronics industry due to its open-source nature, extensive capabilities, and active user community. With a user-friendly interface and a wide range of features, KiCad has become a versatile and powerful tool for electronic design and prototyping. Here is a detailed step-by-step guide for designing a PCB with KiCad:**I used this Version: 8.0.3-8.0.3-0~ubuntu22.04.1(release build) throughout this project.**

1. Schematic Design:

- Launch KiCad, create a new project, and open the schematic editor.
- Design the circuit by placing components from the library onto the schematic sheet.
- Connect the components using wires to represent the electrical connections.
- Label components and connections appropriately for clarity.
- Add any necessary documentation like titles, values, and annotations.

2. Generate Netlist:

- After finalizing the schematic design, generate a netlist that captures the connections between components.

3. PCB Layout Design:

- Open the PCB layout editor and import the netlist generated from the schematic.
- Assign footprints to components, ensuring they match the physical components planned for the PCB.
- Place and orient components on the PCB layout canvas, arranging them according to the circuit design and space constraints.
- Route traces between components using the PCB editor's routing tools, following design best practices for signal integrity and EMI considerations.

4. Design Verification:

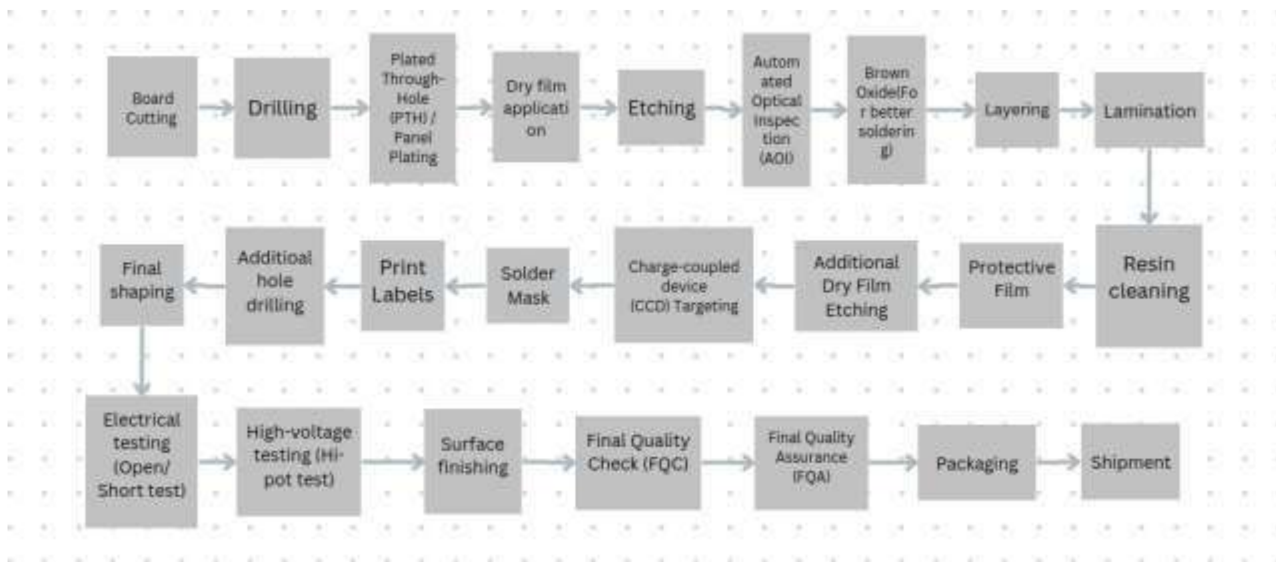
- Run a Design Rule Check (DRC) to ensure the layout meets minimum clearances, trace widths, and other design constraints.
- Perform a design review to verify the layout against the original circuit requirements.

5. Generate Manufacturing Files:

- After finalizing the PCB layout, generate manufacturing files such as Gerber files for PCB fabrication and assembly. Create drill files that specify the locations and sizes of holes to be drilled in the PCB.

2. Manufacturing Process of a PCB

The process of manufacturing a Printed Circuit Board (PCB) consists of numerous steps aimed at producing the PCB board. Here's a comprehensive breakdown of each stage:



Graph 1 :- Show the Manufacturing Process of a PCB

Once we have cut the copper PCB material and drilled holes according to the design, we will plate these holes with copper for connections and cover the surface with a special film that allows us to make copper traces and pads by exposing it to UV light and then etching (removing unwanted copper) away the rest. After this step, we check for mistakes with special machines (AOI Automated Optical Inspection), and if necessary may treat the copper with brown oxide for better soldering. For design that require multiple layers, everything is stacked up together tightly so as to form just one board.

We will then clean off any extra materials before protecting it with another film; sometimes additional pattern might be made via adding more films followed by etching.

Cameras are used next which ensures perfect alignment of everything before adding protective layer called solder mask; labels are also printed on board surface along other information too. Finally any last holes needed are drilled into it then we cut the board into its final shape.

We check the board's electrical connections to ensure they're good and that it can handle high voltages. Then, we add a coating to protect the copper and make it easier to solder. We carefully inspect every board to make sure it meets our quality standards.

Once we're sure everything is good, we pack up the boards nice and safe and send them off to where they're needed.

Chapter 3: Assembly Technologies and Packages of PCB Components

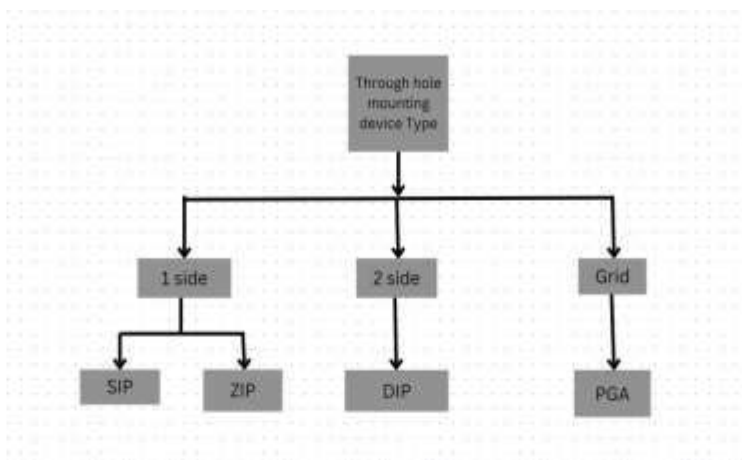
Assembly technologies and packages of PCB (Printed Circuit Board) components play a crucial role in determining the functionality, performance, and reliability of electronic devices. In this chapter, we delve into the various assembly technologies and packages commonly used in PCB manufacturing, exploring their applications.

There are two main type of assembly technologies in PCB design :

1. ThroughHole Technology

Insertion mounting basically means putting components onto a circuit board by sticking their leads or pins through holes in the board and then soldering them down. It's what we usually call through-hole mounting. These components have those little metal legs that poke through holes in the board, which gives them both support and an electrical connection. Before everyone started using surface mount technology (SMT), this through-hole method was the big thing. But SMT took over because it lets us make things smaller, pack more components onto the board, and it's way easier to do with machines.

There are three main types of insertion mounting:



Graph 2 :- Show the Assembly Technologies

1.1 One Side

Single-Sided Insertion Mounting (SIP)

SIP packages are pretty straightforward – they've got leads on just one side of the component. These are handy when we have tight on space and need to keep things compact.

Zero Insertion Pressure (ZIP).

ZIP packages typically utilize a mechanism that requires very low or zero force to insert the component, making it easier and safer to handle delicate components. This design feature is particularly important in applications where components need to be inserted and removed frequently without causing wear or damage to the connection points. ZIP packages are often found in applications where the components require frequent replacement or where there are concerns about mechanical stress during assembly.

1.2 Two side

Dual In-Line Package (DIP):

Dual In-line Package have pins on both sides for through-hole mounting on PCB. It is versatile,accommodating various components like ICs. Available in different sizes and pin configurations, DIP packages offer straightforward handling and secure soldering for reliable connections on the PCB.

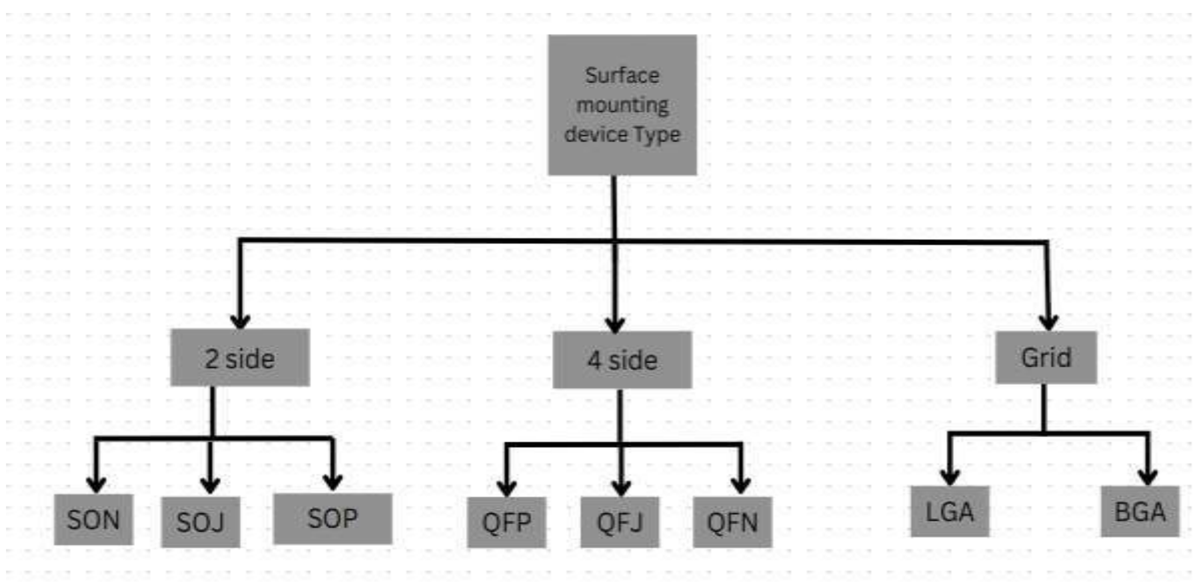
1.3 Grid

Pin Grid Array (PGA):

PGA packages feature pins arranged in a grid pattern on the underside of the component. PGAs offer good thermal performance,high pin counts and are commonly used for microprocessors and other high-performance ICs.

Through-hole technology boasts superior mechanical strength and durability, making it ideal for applications exposed to mechanical stress or vibration. Additionally, its larger lead sizes enable higher power handling capabilities compared to surface mount components. Moreover, through-hole assemblies are easier to repair or modify using standard soldering tools. However, its drawbacks include larger component sizes, longer assembly times, and limited suitability for high-density PCB designs.

2. Surface mount devices



Graph 3 :- Show the Type of Surface mount devices

SMD are electronic components designed as mounted directly onto the surface of a PCB. As opposed through-hole components that are inserted into holes on the PCB, SMD are soldered onto pads on the board surface.

There are three main types of SMT:

2.1 Two side

SOP, Small Outline J-Lead (SOJ), and Small Outline No-Lead (SON):

SOP packages have leads extending from two sides of the component in a gull-wing configuration.

SOJ packages have J-shaped leads extending from two sides of the component.

SON Components with terminals that make contact with the PCB pads directly, omitting leads.

2.2 Four-sided

Quad Flat Package (QFP): QFPs are rectangular or square packages with leads extending from all four sides. They offer high lead counts and are suitable for applications requiring medium to high-density integration.

Quad Flat J-Lead (QFJ): Similar to QFP but with J-shaped leads for increased reliability.

Quad Flat No-Lead (QFN): Components with no leads(not have any typical metal pins or wires) but pads on all four sides for direct surface mounting.This design saves space and allows for a more compact and efficient layout of components on the board.

1.3 Grid

Land Grid Array (LGA): its feature an array of metal pads on the underneath of the component, which are soldered directly onto corresponding pads on the PCB which increase thermal and electrical properties.

Ball Grid Array (BGA): **A BGA has** solder balls arranged in a grid pattern on the underside of the package.They offer good thermal and electrical performance, making them perfect for high-speed and **power** applications.

In wrapping up,All in all, it is clear that the assembly of PCB components really makes a big difference in the performance of our electronic devices.Surface mount technology has taken the lead because it's about saving space,making mounting easier through automation and lowering costs.But let's not forget through-hole technology it still has its place, especially when it comes to heavy-duty applications that require additional mechanical support or power handling.After all,knowing the ins and outs of various assembly methods and component packages is key to designing printed circuit boards that meet the diverse needs of today's electronics.

Chapter 4: Important Aspects of PCB Design for Hardware Developers and PCB Assemblers

In this chapter, we discuss the critical aspects of circuit board design from the perspective of both hardware developers and circuit board assemblers. Understanding the needs and requirements of both parties is essential to creating efficient, cost-effective and reliable electronic devices. Here are the main points from each perspective:

From the Perspective of a Hardware Developer:

Component Orientation: Consider the orientation of components to ensure consistency, ease of installation, testing, and inspection by the manufacturer.

Component Spacing: Avoid placing components too close together to allow sufficient room for routing with copper tracks, ensuring proper connections and preventing signal interference.

Grouping Components: Aligning components like capacitors and diodes in the same direction simplifies installation, testing, and inspection processes, ensuring efficiency for manufacturers.

Soldering Process Consideration: Keep in mind that the board will pass through a soldering oven for component connection, ensuring taller components do not obstruct smaller ones to prevent poorly connected solder joints.

Three-Dimensional Aspect: Be mindful of the size and height of components in the three-dimensional space to prevent conflicts and ensure optimal stacking and assembly.
Thermal Management: Managing heat dissipation is critical for component longevity and overall system reliability. Hardware developers must consider thermal constraints and incorporate appropriate cooling solutions in the design.

From the Perspective of a PCB Assembler:

1. Ensure that bulk (buffer) and bypass capacitors are positioned in close proximity to the supply pins of each IC to optimize power distribution efficiency.

2. Use 45-degree angles when routing tracks instead of sharp 90-degree angles to enhance signal integrity by reducing signal reflection and impedance mismatches.

3. Minimize signal distortion and interference by keeping track lengths as short as feasible on the PCB layout.

4. Choose the width of conductor tracks according to the amount of current they need to carry within the circuit. This ensures that the tracks can adequately handle the required current without overheating or causing voltage drops due to excessive resistance. The track width directly affects the amount of current that can pass through without generating excessive heat, so it's crucial to match the track width with the current requirements of the circuit components.

5. Use vias thoughtfully to link traces between PCB layers, ensuring signal integrity and impedance control in the circuit design. Proper via placement is crucial to maintain signal quality and prevent impedance mismatches.

6. Position mounting holes and connectors strategically for ease of installation and handling.

7. Keep enough distance between components, particularly inductors, to avoid interference and potential damage caused by electromagnetic coupling.

8. Segregating analog and digital signal paths involves keeping them physically separated to prevent interference. This practice ensures that noise from digital signals does not degrade the quality of analog signals, maintaining signal integrity in electronic circuits.

9. Conduct a final design rule check (DRC) to verify layout accuracy and adherence to manufacturing requirements.

10. Taking into account these essential factors in PCB design from the viewpoints of both hardware developers and PCB assemblers ensures that electronic devices are built and produced efficiently and cost-effective.

Chapter 5:Electrocardiography (ECG) of the Human Heart

5.1 Basic of Human Heart

Human Heart pumps blood around your body as your heart beats.This blood sends oxygen and nutrients to all parts of your body, and carries away unwanted carbon dioxide and waste products. understanding the components of this system is crucial for comprehending how the heart functions rhythmically.[**10]**

RightAtrium:Right atrium: one of the four chambers of the heart. The right atrium receives blood low in oxygen from the body and then empties the blood into the right ventricle.[11]

Sinoatrial (SA) Node:The SA node is considered the pacemaker of the heart. Its electrical signals normally cause the atria of an adult's heart to contract at a rate of about 60 to 100 times a minute. Disturbance anywhere along this electrical pathway can cause irregular heartbeats (arrhythmia).[11]

Atrioventricular (AV) Node: The atrioventricular node (AVN) is **a complex structure that performs a variety of functions in the heart**. The AVN is primarily an electrical gatekeeper between the atria and ventricles and introduces a delay between atrial and ventricular excitation, allowing for efficient ventricular filling.

Bundle of His:The bundle of His is an elongated segment connecting the AV Node and the left and right bundle branches of the septal crest. It is approximately 1.8 cm long in an adult heart[4] and is primarily located deep within the dense connective tissue

Right and left bundle branches: The left bundle branch conducts impulses to the left ventricle, and the right bundle branch conducts impulses to the right ventricle. Conduction may be blocked in the left or right bundle branch. The left bundle branch further divides into two branches, called the anterior and posterior fascicles.[12]

Purkinje Fibers: Purkinje fibers or Purkinje cardiomyocytes are part of the whole complex of the cardiac conduction system, which is today classified as specific heart muscle tissue responsible for the generation of the heart impulses.[13]

ECG Application

The electrical current that is produced during the depolarization and repolarization of the heart travels throughout the body.Electrodes arrayed on the body surface allow for quantification of changes in electric activity caused by heart. The recorded trace is known as an electrocardiogram (ECG).[14]

5.2 How to measure heart activity?

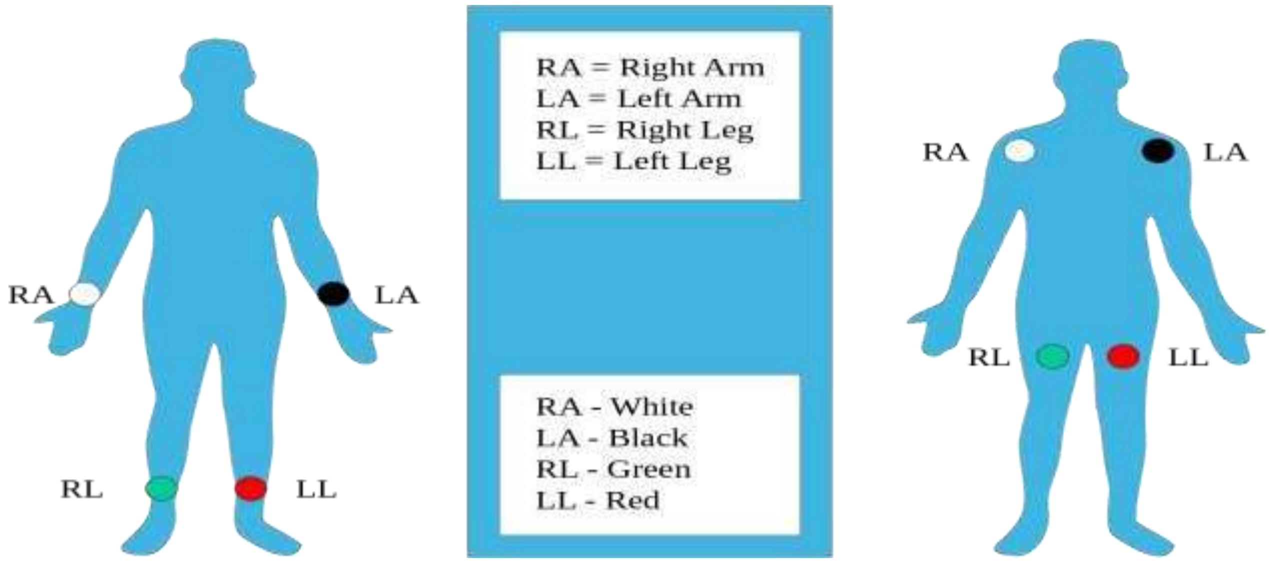


Figure 4 :- Show the heart activity measure[15]

ECG is a device for registering heart's electrical activity which originates from the depolarizations of myocardium, that is basically negative shift of electric charge. Almost these signals move to skin as oscillating waves. Despite its small magnitude usually measured in microvolts (uV), they can be reliably detected using electrodes placed on the skin.

Normally a complete ECG setup will have at least four electrodes placed either on a person's chest or on their extremities such as right arm, left leg, right leg and left arm though variations may exist to meet several recording requirements with flexibility and less intrusion.For instance, electrodes can be placed solely on the forearms and legs. ECG electrodes, often wet sensors, require the application of a conductive gel to enhance the connection between the skin and electrodes, ensuring accurate readings.[15]

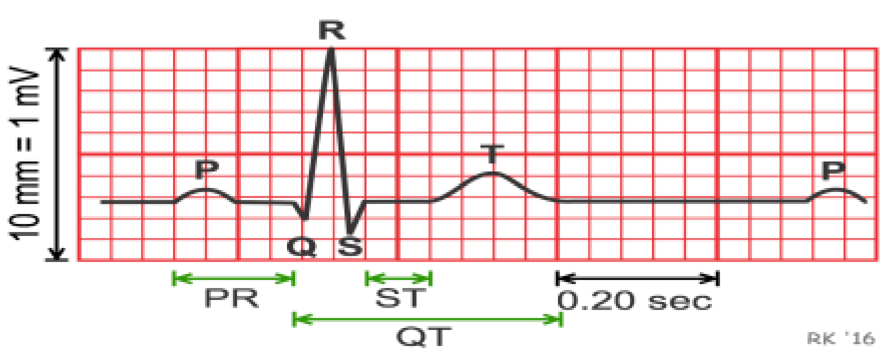


Figure 5 :- Show the ECG Tracing[14]

Above is a typical ECG tracing. The sequence of atria and ventricles' depolarization and repolarization is represented by the various waves which make in the ECG. The voltages are calibrated so that 1 mV = 10 mm (2 large squares) in the vertical axis, and the ECG is recorded at a speed of 25 mm/sec (5 large squares/sec). Consequently, a voltage of 0.10 mV and a time interval of 0.04 sec (40 msec) are represented by each tiny 1-mm square. The intervals between various waves can be used to calculate heart rate because the recording speed is standardized.[15]

P wave (atrial depolarization)

The wave of depolarization known as the P wave, which typically lasts 0.08 to 0.10 seconds (80 -100 ms), propagates throughout the atria from the SA node.The impulse is moving through the bundle of His and the AV node, where the conduction velocity is slowed, during the brief isoelectric (zero voltage) period that follows the P wave. The time interval between P waves can be used to calculate the atrial rate.[15]

The period of time from the onset of the P wave to the beginning of the QRS complex is termed the PR interval, which normally ranges from 0.12 to 0.20 seconds in duration. This interval represents the time between the onset of atrial depolarization and the onset of ventricular depolarization. If the PR interval is >0.20 sec, there is an AV conduction block, which is called a first-degree heart block if each impulse from the atria can still be conducted into the ventricles.[15]

QRS complex (ventricular depolarization)

QRS complex includes the Q wave, R wave, and S wave. These three waves occur in rapid succession. The QRS complex represents the electrical impulse as it spreads through the ventricles and indicates ventricular depolarization. As with the P wave, the QRS complex starts just before ventricular contraction.

It is important to recognize that not every QRS complex will contain Q, R, and S waves. The convention is that the Q wave is always negative and that the R wave is the first positive wave of the complex. If the QRS complex only includes an upward (positive) deflection, then it is an R wave. The S wave is the first negative deflection after an R wave.[16]

T Wave

A T wave follows the QRS complex and indicates ventricular repolarization. Unlike a P wave, a normal T wave is slightly asymmetric; the peak of the wave is a little closer to its end than to its beginning. T waves are normally positive in leads When a T wave occurs in the opposite direction of the QRS complex, it generally reflects some sort of cardiac pathology. If a small wave occurs between the T wave and the P wave, it could be a U wave. The biological basis for a U wave is unknown.[16]

ST segment

The ST segment is the isoelectric period following the QRS and ending at the beginning of the T wave.

This represents the period at which both ventricles are completely depolarized.

QT interval

The QT interval represents the time for both ventricular depolarization and repolarization to occur, and therefore roughly estimates the duration of an average ventricular action potential. This interval can range from 0.20 to 0.40 seconds, depending upon heart rate.[16]

5.3 Essentials for Capturing Electromagnetic Biosignals

Recording electromagnetic biosignals demands careful attention to detail for precise and reliable measurements.

It is essential, when recording electromagnetic biosignals, that the process of capturing them should not interfere with their reading too much. The aim is to keep things as close to their natural state as possible so that precise results can be obtained.

Non-invasive methods are preferable for patient's comfort and safety. This implies coming up with ways of recording signals without causing any harm or discomfort.

We have to be clever about where we put our recording equipment if we want to get the best signal. Separating the wanted signal from early interferences will ensure reliable data.

The role played by substances such as transition metals, electrolytes and polarization voltages in affecting the process of recording signals should be known. This information will guide us during the recording exercise.

Polarization voltage stability and impact on the body are important considerations. We must ensure that this voltage remains stable so that it does not disrupt natural signals.

For recording biosignals, Ag/AgCl electrodes which have good electrical properties may be used since they are popularly known for such a purpose. These electrodes help in creating strong connection with skin which leads to accurate

Commonly used for recording biosignals, electrodes such as Ag/AgCl are popular because of their good electric properties. These electrodes make a good contact with the skin and hence provide accurate readings.

Polarization voltages can be affected by temperature variations. However, Ag/AgCl electrodes only undergo small changes in voltage when temperatures change. This should be taken into consideration so that measurements are done correctly.

Modern methods use capacitively coupled and dry electrodes which are more advanced types of electrodes for capturing signals efficiently. With these inventions signal recordings are enhanced.

Sometimes invasive methods are used to derive signals where fine needle-shaped probes are involved. These probes which have a very tiny diameter allows for closer examination through direct accessibility to limited regions.

5.4 Signal amplification and filtering

In order to maintain accuracy and precision of measurements, guidelines must be followed when increasing the amplitudes of signals in electromagnetic biosignal recording.

A preamplifier is used to increase signal amplitudes to ~1V at the body leak off point.

The amplifier should have high input impedance (>1000 x R source in the body + contact resistance).

OPV with FET input (input impedance up to ~10^13 Ohm) or MOSFET (input impedance up to ~10^16 Ohm) can be considered as good options.

Active linear filters should be used for both high-pass and low-pass filters; while selecting consider slew rate so as not only isolated but also attenuate undesired signals.

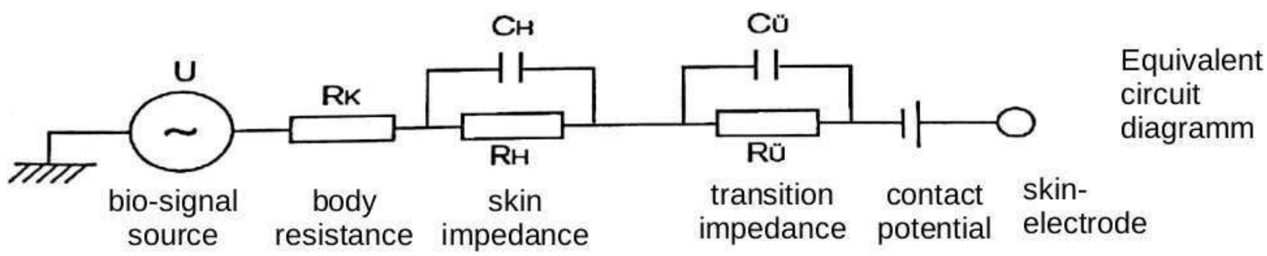


Figure 6 :- Signal amplification and filtering process[2]

When it comes to measuring electromagnetic biosignals, there are four main factors at play; the body's resistance, the skin impedance, the transition impedance at the electrode-skin interface and the contact potential between the electrode and skin. The human body's resistance (which is affected by things like hydration and condition of our skin) determines how electric currents will flow through us. Skin impedance – which has a capacitive part and a resistive part – changes depending on moisture content as well as other qualities of our skin; this alters how well signals can be transmitted through it. Transition impedances need to be as low as possible so that they act more like conductors than insulators – otherwise signals won't get through clearly enough! Finally there's also what happens when an electrode makes contact with your epidermis: any voltage offset caused by this contact potential difference could mess up all recorded bioelectricity unless taken into account.

5.5 Sources of interference and how to minimize them

It is very important to recognize and source the causes of interference when recording electromagnetic biosignals. The right positioning of the recording electrodes is necessary since signals like electroencephalograms (EEGs) are much smaller in amplitude than electrocardiogram (ECG) signals. Recordings can be disturbed by body activities such as muscle potentials thus patients should be immobilized and relaxed during the process. Proper electrode selection may minimize polarization that improves the accuracy of signal acquisition too. In addition, shielding and increasing signal-to-noise ratio as well can enhance recorded data quality more than expected. Early identification and intervention into these issues will enable researchers or medical practitioners achieve better fidelity in their signals while also creating favorable conditions for analysis reliability in electromagnetic biosignal studies.

5.6 ECG measurement board AD8232 EVALZ

The AD8232 EVALZ evaluation board is indeed designed for the AD8232, a single-lead, heart rate monitor front end IC, specifically for measuring electrocardiogram (ECG) signals. This evaluation board is equipped with components like amplifiers, filters, and ADCs that are essential for processing the ECG signals picked up by the electrodes.

The AD8232-EVALZ evaluation board ships with a default configuration for applications that involve three electrodes connected to the hands. The LA, RA, and RL terminals serve as the signal inputs and the right leg drive electrode connections, respectively.[21]

The in-amp has a fixed gain of 100, and the op amp is set for a gain of 11. The overall gain is 1100 V/V, which limits the maximum differential input signal to approximately 2.7 mV p-p. Exceeding this amplitude does not damage the AD8232; however, the signal at the output appears distorted. Due to the high-Q of the filter, additional peaking sets the maximum observed gain more than 1100 V/V at approximately 15 Hz. The total gain can be changed by adjusting the R16 and R17 resistors, but doing so has a direct impact on the Q of the low-pass filter. Note that the in-amp has a fixed gain of 100.

A single-supply configuration is used to implement the entire signal chain. For this purpose, the reference buffer is set to a ratiometric level at midsupply using two 10 MΩ resistors (R14 and R15). The integrated reference buffer output provides a midsupply dc level for the system. The signal at the output rides on top of this midsupply level. This voltage is available at the REFOUT pin (TP19) to serve as a reference level for the subsequent signal acquisition stages.[21]

Chapter 6:Schematic Editor

The schematic editor in KiCad allows users to design electronic circuits by providing a platform to place components,connect them with wires, and annotate the design with descriptive text. It typically includes features such as a library of electronic symbols, the ability to create and modify component footprints, and tools for organizing and structuring complex circuit designs. The schematic editor is an essential component of the KiCad EDA suite, enabling engineers and hobbyists to create accurate and standardized representations of their electronic circuits.

6.1 Symbol Editor

The symbol editor is a tool within KiCad that allows users to create and modify schematic symbols for electronic components. This feature is essential for customizing symbol representations to accurately reflect the characteristics of specific components not found in standard libraries. With the symbol editor, users can define the pinout, graphics, and electrical properties of each symbol, ensuring precise representation in the schematic editor. This capability makes KiCad versatile and adaptable to a wide range of electronic design requirements.

Creating a symbol in KiCad involves using the Symbol Editor tool to define the schematic representation of an electronic component. Here's a brief overview of the steps involved:

1. Launch the Symbol Editor within KiCad.
2. Define the graphic representation of the symbol using lines, shapes, and other drawing tools.
3. After that we can add various components to the symbol sheet by using the symbol editor tools and features
4. Assign pin numbers,value, pin names, and electrical properties (input,output,power) to create a functional symbol.
5. Save the symbol to the component library for reuse in schematics.
6. The symbol we made in the symbol editor can finally be used in the schematic.

Here is the symbols that we used in our project.

Solder Nail (RTM1_3)

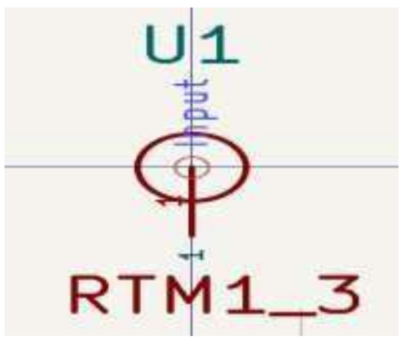


Figure 7 :- Show the symbol of Soldering nail denoted by U1 ,U2

Creating symbols for soldering nails in KiCad is an essential step in the design process, providing a clear and standardized way to represent physical connections in an electronic circuit. It aids in communication, collaboration, and the successful translation of a schematic design into a physical PCB layout.

KiCad symbols for mechanical support points visually document the integration of physical components, aiding collaboration and ensuring effective coordination between electronic and mechanical design aspects.

AKL Terminal Block

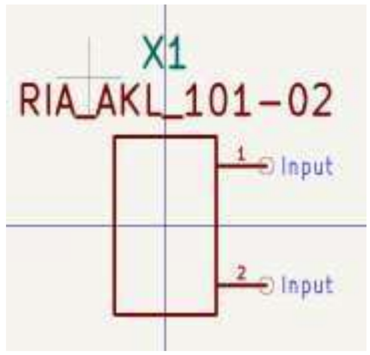


Figure 8 :- Show the symbol of Terminal Block denoted by X1,X4 and X3

Screw terminals,also known as terminal blocks,are typically used to make electrical connections in a printed circuit board(PCB).it is provide a convenient way to connect and disconnect wires without soldering.They consist of a metal block with a threaded hole and a captive screw. Wires are inserted into the terminal,and the screw is tightened to establish a secure electrical connection.

This design facilitates easier maintenance and repairs,as connections can be easily adjusted or replaced.its commonly used in industrial application,power suplies,and other electronic systems where robust connections are crucial.

WE632723300011

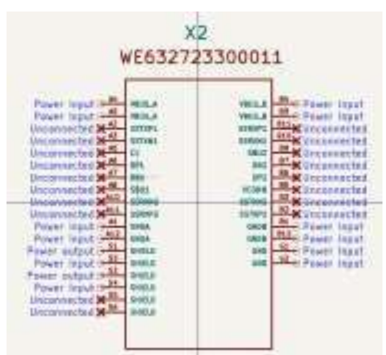


Figure 9 :- Show the symbol of USB type C receptacle connector denoted by X2

The WE632723300011 USB type C receptacle connector serves as the interface for external power supply in our project, facilitating power distribution and grounding. It receives the main supply voltage through designated pins and ensures reliable connectivity for power and data transfer. Additionally, it feature grounding connections and electromagnetic interference shielding for stability. This component contributes to the overall functionality and performance of our project by enabling reliable power delivery and connectivity.[17]

LT1761IS5-3V3 and LT1762EMS8-2V5

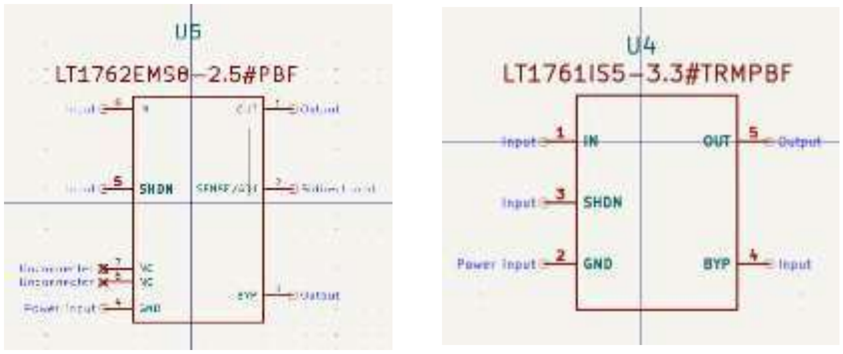


Figure 10 :- Show the symbol of regulators denoted by U5 and U4

The LT1761 series regulators are micropower, low noise, low dropout regulators designed for a wide range of applications. With an external 0.01µF bypass capacitor, output noise drops to 20µVRMS over a 10Hz to 100kHz bandwidth. The devices are capable of operating over an input voltage from 1.8V to 20V, and can supply 100mA of output current with a dropout voltage of 300mV. Quiescent current is well controlled, not rising in dropout as it does with many other regulators. The LT1761 regulators are stable with output capacitors as low as 1µF. Small ceramic capacitors can be used without the series resistance required by other regulators. Internal protection circuitry includes reverse battery protection, current limiting, thermal limiting and reverse current protection. The device is available in fixed output voltages of 1.2V, 1.5V, 1.8V, 2V, 2.5V, 2.8V, 3V, 3.3V and 5V, and as an adjustable device with a 1.22V reference voltage.

IN (Pin 1):Input. Power is supplied to the device through the IN pin. A bypass capacitor is required on this pin if the device is more than six inches away from the main it is advisable to include a bypass capacitor in battery-powered circuits. A bypass capacitor in the range of 1µF to 10µF is sufficient.input filter capacitor.

GND (Pin 2): Ground.

SHDN(pin Fixed/-SD Devices) :- Shutdown. The SHDN pin is used to put the LT1761 regulators into a low power shutdown state. The output will be off when the SHDN pin is pulled low. The SHDN pin can be driven either by 5V logic or open-collector logic with a pull-up resistor. The pull-up resistor is required to supply the pull-up current of the open-collector gate, normally several microamperes, and the SHDN pin current, typically 1µA. If unused, the SHDN pin must be connected to VIN. The device will not function if the SHDN pin is not connected. For the LT1761-BYP, the SHDN pin is internally connected to VIN.

BYP (Pins 3/4, Fixed/-BYP Devices): Bypass. The BYP pin is used to bypass the reference of the LT1761 regula- tors to achieve low noise performance from the regulator. The BYP pin is clamped internally to ±0.6V (one VBE) from ground. A small capacitor from the output to this pin will bypass the reference to lower the output voltage noise. A maximum value of 0.01µF can be used for reducing output voltage noise to a typical 20µVRMS over a 10Hz to 100kHz bandwidth. If not used, this pin must be left unconnected.

OUT (Pin 5): Output. The output supplies power to the load. A minimum output capacitor of 1µF is required to prevent oscillations. Larger output capacitors will be required for applications with large transient loads to limit peak volt- age transients. See the Applications Information section for more information on output capacitance and reverse output characteristics.

LTC6655LNCHMS8-4.096

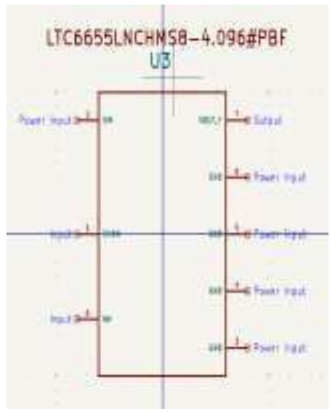


Figure 11 :- Show the symbol of reference voltage denoted by U3

The LTC6655 voltage reference offers exceptional precision, low noise, and drift performance, making it ideal for high-resolution measurements in instrumentation and test equipment. Its wide temperature range of -40°C to 125°C ensures suitability for demanding automotive and industrial applications. The LTC6655LN variant includes a noise reduction pin for even lower wideband noise with a single capacitor. It can be powered from as low as 500mV above the output voltage to 13.2V, with superior load regulation and shutdown mode for low power applications.[19]

SHDN (Pin 1): Shutdown Input. This active low input powers down the device to <20µA. If left open, an internal pull-up resistor puts the part in normal operation. It is recommended to tie this pin high externally for best performance during normal operation.
VIN (Pin 2): Power Supply. Bypass VIN with a 0.1µF, or larger, capacitor to GND.
GND (Pin 4): Device Ground. This pin is the main ground and must be connected to a noise-free ground plane.
GND (Pins 3, 5, 8): Internal Function. Ground these pins.
NR (Pin 6 – LTC6655): Noise Reduction Pin. To band limit noise, connect a capacitor between this pin and ground. See Applications Information section.
VOUT_F (Pin 7 – LTC6655): VOUT Force Pin. This pin sources and sinks current to the load. An output capacitor of 2.7µF to 100µF is required.

LTC2368IMS-16
The LTC2368IMS-16 is a 16-bit high-speed SAR ADC by Linear Technology. It offers precise analog-to-digital conversion with low power consumption.

Figure 12 :- Show the symbol of LTC2368IMS-16 denoted by U6

6.2 Footprint Editor

Footprint Editor as part of its tools for PCB design. In KiCad, the Footprint Editor allows you to create, modify, and manage footprints for components that will be placed on our printed circuit board. a footprint refers to the physical layout and arrangement of pads or other connection points on a PCB for a specific electronic component. The footprint defines the space and configuration needed to solder a particular component onto the PCB.Footprints are crucial for ensuring accurate and reliable PCB assembly. When designing a PCB, engineers select or create footprints for each component to match the physical characteristics of the component's package.

Solder Nail (RTM1_3)

Figure 13 :- Show the Footprint of Soldering nail

The square uses the F.courtyard layer. Through-hole type a pad have an oval shape of 1.43mm and 3.5mm with hole shape of circular a diameter of 1.4mm.Circle with 2.2mm radius uses F. silkscreen layer with 0.1mm line width.it is associated with the symbols U1, U2 in the schematic.

AKL Terminal Block

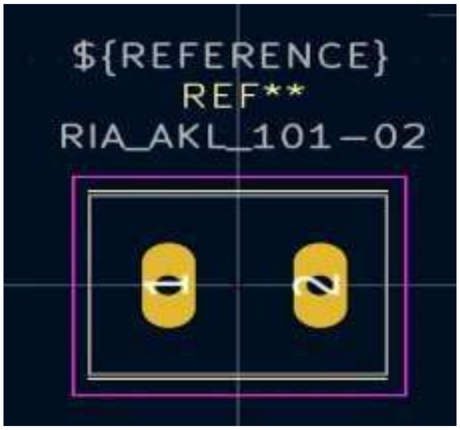


Figure 14 :- Show the Footprint of Terminal Block

The larger rectangle is outlined on the F.courtyard layer, while the smaller rectangle is outlined on the F.fab layer. Additionally, two lines are marked on the F.silkscreen layer, each measuring 10mm in length. Furthermore, two Through-hole pads are defined, each with an oval shape measuring 1.8mm by 3.8mm and featuring a circular hole with a diameter of 1.2mm.
it is associated with the Footprint X1,X3,X4 in the PCB design.

WE632723300011

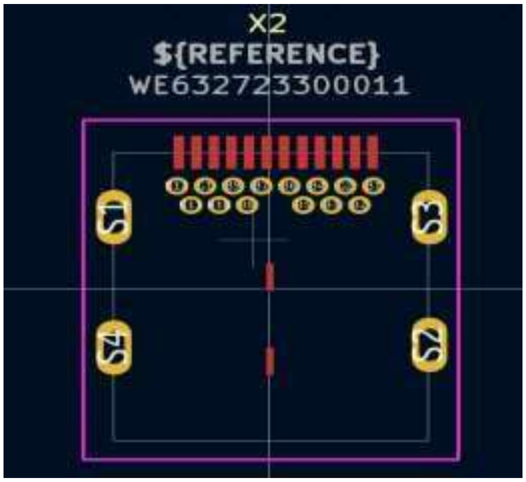


Figure 15 :- Show the Footprint of USB type C receptacle connector

It is denoted with the Footprint X2 in the PCB design.A larger rectangle is defined on the F.courtyard layer, while a smaller rectangle is outlined on the F.fab layer, measuring 10.58mm in height and 8.94mm in width. Adjacent to the smaller rectangle, shield components S1 to S4 are positioned, featuring oval-shaped Through-hole pads with dimensions of 1mm by 2mm and a circular hole diameter of 0.6mm to 1.2mm. The spacing between S1 and S4 is precisely 4.780mm. On the top side of the smaller rectangle, SMD pads labeled A1 to A12 are arranged with dimensions of 1.2mm by 0.3mm, spaced 0.5mm apart. Following the setup of these pads, Through-hole pads labeled B1 to B12, along with circular pads numbered 25 and 26, are established, each featuring a circular shape with a diameter of 0.65mm and a hole diameter of 0.4mm.

LT1761IS5-3.3

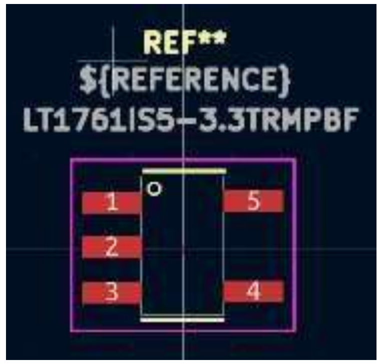


Figure 16 :- Show the Footprint of 3.3V regulators

It is denoted with the footprint U4 in the PCB design. The larger rectangle is outlined on the F.courtyard layer, while the smaller square is outlined on the F.fab layer.Two solid lines are drawn on the F.silkscreen layer, each with a length of 3,3528mm and line width is 0,1524. There are five SMD pads, each with a rectangular shape measuring 1.22mm by 0.45mm. The distance between pad 1 and pad 2 is 0.950mm, and the spacing between pad 5 and pad 4 is 1.9mm.

LT1762EMS8-2.5

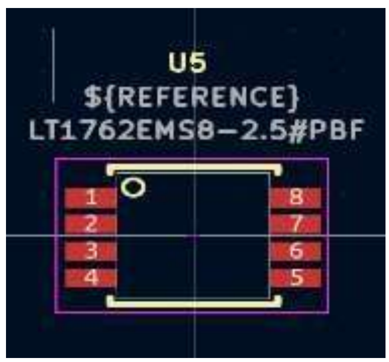


Figure 17 :- Show the Footprint of 2.5V regulators

It is denoted with the footprint U5 in the PCB design. The larger rectangle is outlined on the F.courtyard layer, while the smaller square is outlined on the F.fab layer.Two solid lines are drawn on the F.silkscreen layer, each with a length of 1.625mm. There are 8 SMD pads, each with a rectangular shape measuring 1.016mm by 0,458mm. The distance between two pad is 0.650mm

LTC6655LNCHMS8.4.096

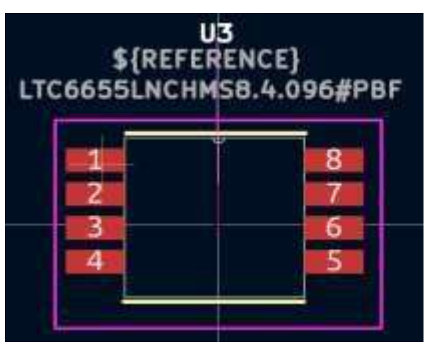


Figure 18 :- Show the Footprint of reference voltage

It is denoted with the footprint U3 in the pcb Design.The larger rectangle is outlined on the F.courtyard layer, while the smaller square is outlined on the F.fab layer.Two solid lines are drawn on the F.silkscreen layer, each with a length of 3,08mm and line width of 0.09mm. There are 8 SMD pads, each with a rectangular shape measuring 1,016mm by 0,458mm. The distance between two pad is 0.650mm

LTC2368IMS-16

Figure 19 :- Show the Footprint of LTC2368IMS-16

It is denoted with the footprint U6 in the PCB design.The larger rectangle is outlined on the F.courtyard layer, while the smaller square is outlined on the F.fab layer.Two solid lines are drawn on the F.silkscreen layer, each with a length of 3,1mm and line width of 0,1mm.There are SMD pads, each with a rectangular shape measuring 1,016mm by 0,343mm. The distance between two pad is 0.500mm

Esp32-S3

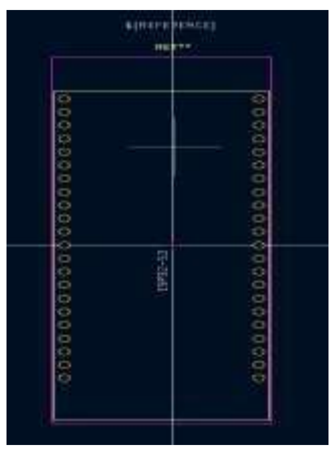


Figure 20 :- Show the Footprint of Esp32-s3 microcontroller

It is denoted with the footprint U7 in the Footprint.The larger rectangle is outlined on the F.courtyard layer, while the smaller square is outlined on the F.fab layer and the height of this small square of 62,74mm and width of 25.5mm.There are 44 Through-hole pads are defined, each with an circular shape measuring 1.53mm and featuring a circular hole with a diameter of 1,02mm.

6.3 Schematic Design

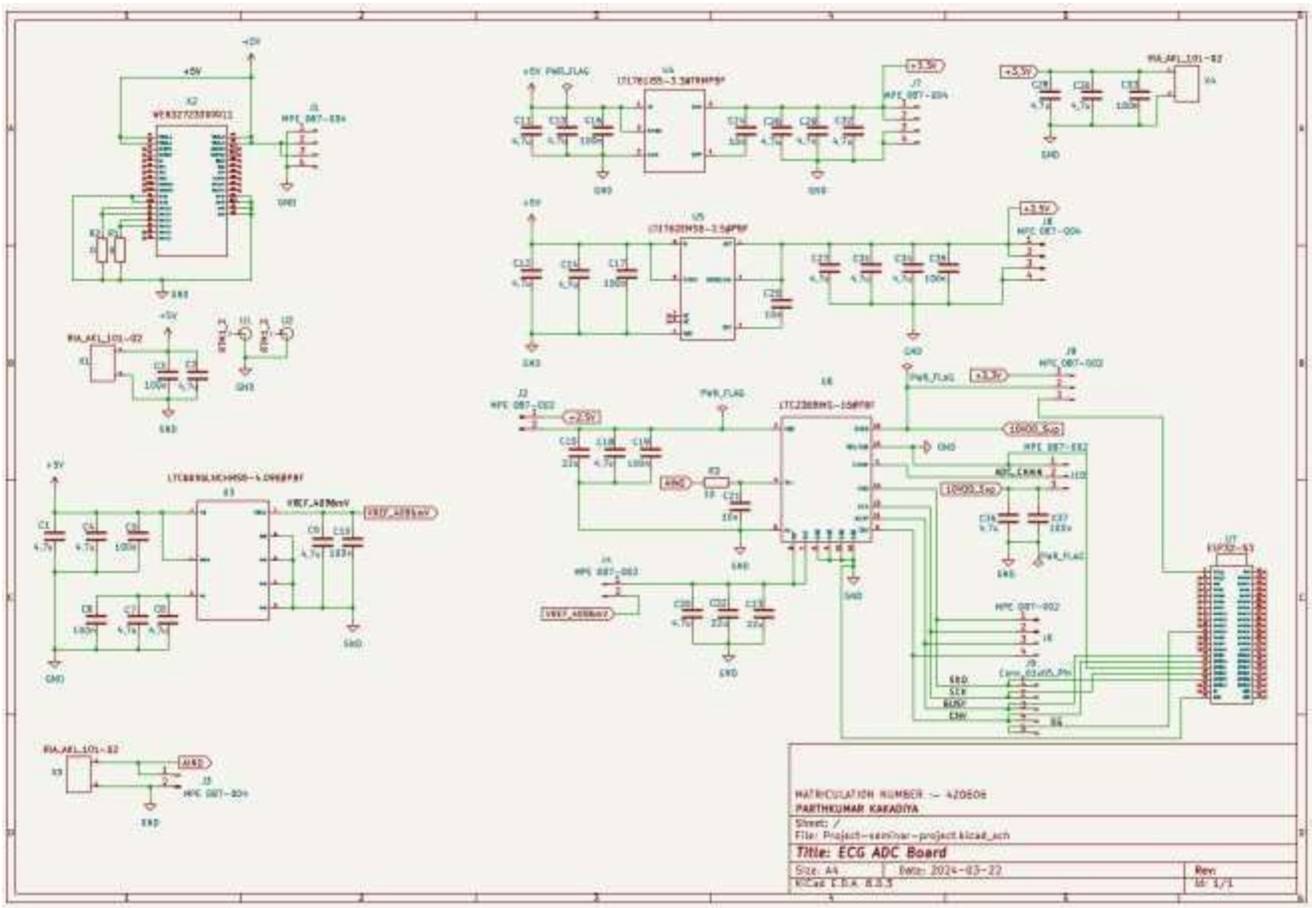


Figure 21:- Schematic Design of the Development of a Analog-Digital Converter Board

Above Figure is the schematic design of the development of a analog-digital converter board for an ECG application which has electronics component such as register,capacitor,WE632723300011, J1 to J10 , RIA_AKL_101-02(2-Pole Connection Screw Terminal), RTM1_3 , LT1761IS5-3.3TRM , LT1762EMS82.5 , LTC6655LNCHMS8.4.096,LTC2368IMS-16PBF and ESP32.

Overall Workflow of the ADC Board

When the board is powered on, the USB power supply (WE632723300011) provides a 5V input. The LT1761 and LT1762 regulators convert this 5V supply to 3.3V and 2.5V, respectively, powering various components. The LTC6655 provides a stable 4.096V reference voltage essential for the ADC's accuracy.

We then connect the reference voltage output (1VREF_4096mV) from the precision voltage reference (LTC6655LNCHMS8.4.096#PBF) to the reference input of the ADC for accurate conversion. For the ADC, we connect the analog input signals to be converted and provide the necessary supply voltages (AINO and OVDD_Sup) to power the ADC and ensure proper operation. The ADC converts these analog signals to digital form and communicates the data to the ESP32 via SPI.

This entire setup ensures precise and reliable analog-to-digital conversion, suitable for applications such as ECG signal processing.

Transfer function and Basic Calculation

According to our schematic The LTC6655LNCHMS8 provides a precise reference voltage of 4.096V.This voltage is used as a reference for the ADC to convert analog signals into digital values.

The LTC2368IMS-16PBF is a 16-bit ADC, meaning it can represent analog input signals with 16 bits of resolution.where each bit represents a fraction of the reference voltage.

The resolution of an ADC determines the number of discrete levels it can represent, which is 2^N, where N is the number of bits.

With a 4.096V reference voltage and a 16-bit resolution, each LSB (Least Significant Bit) of the ADC represents a voltage of **(4.096V / 2^16) ≈ 62.5µV**.

This means that the ADC can distinguish between analog input voltages with a resolution of approximately 62.5µV.

We use **GND(Ground)** for common reference point for all voltages in a circuit. It provides a return path for electric current, helps reduce noise, and enhances safety by directing fault currents to the earth.

Various resistors and capacitors (R1, R2, R3, C1 to C35) are used throughout the circuit for filtering, stabilizing voltages, and ensuring clean signal paths. These components are crucial for reducing noise and improving signal integrity.This improves the overall precision and reliability of our analog-to-digital conversion process.

We use the +5V symbol to indicate a 5-volt power rail. This label connects various components to the 5V power supply, ensuring consistent voltage throughout the circuit.

In our schematic, we are using J1 to J10, with different pin configurations (1*2, 1*3, 1*4). it is serve as as flexible connection points that allow us to easily configure and interface various parts of the circuit. By using it, we can quickly modify connections and integration with other components.

We use the RIA_AKL_101-02 terminals (referred to as x1, x2, x3) in our project. They're establishing secure and reliable electrical connections. The 2-pole screw terminals facilitate easy assembly and maintenance by allowing straightforward connection and disconnection of wires. Additionally, they offer flexibility in the circuit design, ensuring stable connectivity for external components and sources of power supply.

Global labels such as +3.3V, +2.5V, 1VREF_4096mV, AINO, and OVDD_Sup are used to clearly identify and manage key power and signal connections across the schematic. These global labels ensure consistent and accurate routing of power supplies and signals, simplifying the design process and enhancing readability.

The schematic use global labels for efficient power distribution and signal referencing. +3.3V and +2.5V supply stable voltages to components, while 1VREF_4096mV is reference voltage of 4.096V for analog-to-digital converters and OVDD_Sup provides stable power for digital components.

e WE632723300011 USB type C receptacle connector serves as the interface for external power supply in our project, facilitating power distribution and grounding.

The LT1761IS5-3.3 (5 pin configuration) and LT1762EMS8-2.5(8 pin configuration)regulator serves as a voltage regulator in our project, ensuring stable and regulated power supply. It takes an input voltage and regulates it to provide a consistent 3.3 volt output for LT1761IS5 -3.3TRMPBF and 2.5 volt output for LT1762EMS8-2.5 . By connecting this regulator with capacitors connected across its input and output pins , noise is filtered out while also stabilizing the voltage . It makes sure that every other component gets a steady flow of current which will contribute to its overall performance.This regulator plays a crucial role in maintaining the reliability and performance of our circuit by providing consistent power to other components, contributing to overall functionality.[18]

LTC6655LNCHMS8-4.096 serves as a crucial component in our project, providing precise voltage reference. Its 8-pin configuration enables stable voltage regulation and accuracy. By managing input, shutdown, and noise reduction, this IC ensures consistent and reliable performance. This voltage reference is essential for accurate measurements and reliable operation of our project, ensuring optimal performance in various applications.[19]

LTC2368IMS-16

The LTC2368-16 is a low noise, low power, high speed 16-bit successive approximation register (SAR) ADC. Operating from a 2.5V supply, the LTC2368-16 has a 0V to VREF pseudo-differential unipolar input range with VREF ranging from 2.5V to 5.1V. The LTC2368-16 consumes only 13.5mW and achieves ±0.75LSB INL maximum, no missing codes at 16 bits with 94.7dB SNR.The LTC2368-16 has a high speed SPI-compatible serial interface that supports 1.8V, 2.5V, 3.3V and 5V logic while also featuring a daisy-chain mode.The LTC2368-16 automatically powers down between conversions, leading to reduced power dissipation that scales with the sampling rate.[20]

The LTC2368IMS-16PBF is a vital 16-bit analog-to-digital converter (ADC) in our project, responsible for converting analog signals from sensors into high-resolution digital data. It interfaces with the ESP32 microcontroller through the SPI communication protocol, ensuring precise and accurate data acquisition. This IC enables detailed and reliable signal representation, crucial for applications like ECG measurements, by providing stable power, reference voltages, and grounding, and effectively integrating with the overall circuit.[20]

Pin Number	Pin name	Pin Function
1	CHAIN	Chain Mode Selector Pin.When low, the LTC2368-16 operates in normal mode and the RDL/SDI input pin functions to enable or disable SDO. When high, the LTC2368-16 operates in chain mode and the RDL/SDI pin functions as SDI
2	VDD	2.5V Power Supply. The range of VDD is 2.375V to 2.625V. Bypass VDD to GND with a 10μF ceramic capacitor.
3	GND	Ground
4	IN+	Analog Input. IN+ operates differential with respect to IN– with an IN+-IN– range of 0V to VREF.
5	IN-	Analog Ground Sense. IN– has an input range of ±100mV with respect to GND and must be tied to the ground plane or a remote ground sense.
6	GND	Ground
7 8	REF REF	Reference Inputs. The range of REF is 2.5V to 5.1V.
9	CNV	Convert Input. A rising edge on this input

		powers up the part and initiates a new conversion. Logic levels are determined by OVDD.
10	GND	Ground
11	BUSY	BUSY Indicator. Goes high at the start of a new conversion and returns low when the conversion has finished. Logic levels are determined by OVDD.
12	RDL/SDI	When CHAIN is low, the part is in normal mode and the pin is treated as a bus enabling input. When CHAIN is high, the part is in chain mode and the pin is treated as a serial data input pin where data from another ADC in the daisy chain is input.
13	SCK	Serial Data Clock Input. When SDO is enabled, the conversion result or daisy-chain data from another ADC is shifted out on the rising edges of this clock MSBfirst.
14	SDO	Serial Data Output. The conversion result is output on this pin on each rising edge of SCK MSB first. The output data is in straight binary format.
15	OVDD	I/O Interface Digital Power. The range of OVDD is 1.71V to 5.25V.
16	GND	Ground

Pin configuration table of LTC2368IMS-16

Some information and Function of LTC2368IMS-16

The LTC2368-16 operates in two phases. During the acquisition phase, the charge redistribution capacitor D/A converter (CDAC) is connected to the IN+ and IN– pins to sample the pseudo-differential analog input voltage. A rising edge on the CNV pin initiates a conversion. During the conversion phase, the 16-bit CDAC is sequenced through a successive approximation algorithm, effectively comparing the sampled input with binary-weighted fractions of the reference voltage (e.g. VREF/2, VREF/4 … VREF/65536) using the differential comparator. At the end of conversion, the CDAC output approximates the sampled analog input. The ADC control logic then prepares the 16-bit digital output code for serial transfer.

The analog inputs of the LTC2368-16 are pseudo-differen- tial in order reduce common-mode noise by sampling the difference between the IN+ signal and a fixed reference at IN–, enhancing accuracy without the complexity of true differential inputs.[20]

Input Filtering

The noise and distortion of the buffer amplifier and signal source must be considered since they add to the ADC noise and distortion. Noisy input signals should be filtered prior to the buffer amplifier input with an appropriate filter to minimize noise.

Another filter network consisting of LPF2 should be used between the buffer and ADC input to both minimize the noise contribution of the buffer and to help minimize disturbances reflected into the buffer from sampling transients. Long RC time constants at the analog inputs will slow down the settling of the analog inputs. Therefore, LPF2 requires a wider bandwidth than LPF1. A buffer amplifier with a low noise density must be selected to minimize degradation of the SNR.High quality capacitors and resistors should be used in the RC filters since these components can add distortion.[20]

ADC Reference

The LTC2368-16 requires an external reference to define its input range.With its small size, low power and high accuracy, the LTC6655-5 is particularly well suited for use with the LTC2368-16. The LTC6655-5 offers 0.025% (max) initial accuracy and 2ppm/°C (max) temperature coefficient for high precision applications. The LTC6655-5 is fully specified over the H-grade temperature range and complements the extended temperature operation of the LTC2368-16 up to 125°C. Bypass the LTC6655-5 with a 47µF ceramic capacitor close to the REF pin.

The REF pin of the LTC2368-16 draws charge (Qconv) from the 47μF bypass capacitor during each conversion cycle. The reference replenishes this charge with a DC current, IREF = QCONV/tCYC.
The DC current draw of the REF pin, IREF, depends on the sampling rate and output code. If the LTC2368-16 is used to continuously sample a signal at a constant rate, the LTC6655-5 will keep the deviation of the reference voltage over the entire code span to less than 0.5LSBs.[20]

CNV Timing

The conversion process of the LTC2368-16 is initiated by a rising edge on the CNV pin, which also powers up the device. Once a conversion starts, it must complete before a new conversion can begin. For best performance, CNV should be driven by a clean, low-jitter signal. The BUSY output signal indicates the conversion status, remaining high during the conversion. To ensure accurate digitized results, any additional CNV transitions should occur within 40ns of starting the conversion or after the conversion has finished. After the conversion, the LTC2368-16 powers down and starts acquiring the input signal again.
After completing a conversion, the LTC2368-16 automatically powers down until a new conversion is started. It's suggested to disable SDO and turn off SCK during power-down to minimize power consumption. This feature efficiently reduces power dissipation, particularly at lower sampling frequencies.[20]

By using the precise reference voltage provided by the LTC6655LNCHMS8-4.096 and the high-resolution ADC capabilities of the LTC2368IMS-16PBF, accurate and reliable analog-to-digital conversion can be achieved.

Bill of Materials (BOM) list (incl. ordering information)[23][24]

Ref.	Value	Reichelt and mouser No.	Manufacturer No.	Manufacturer Name:	Price per unit	Quantity
c1,c2,c4,c7,c8,c9,c11,c12,c13,c14,c18,c20,c26,c27,c28,c29,c30,c31,c32,c34,c36	4,7uF Packaging/ housing:0603 (1608 metrics)	581-600S4R7BW250T	600S4R7BW250T	KYOCERA AVX	€0.921	21
c3,c5,c6,c10,c16,c17,c19,c33,c35,c37	Capacity:100 pF Packaging/ housing:0603 (1608 metric)	581-600S101JT250T	600S101JT250T	KYOCERA AVX	€0.877	10
c15,c22,c23	Capacity:22pF Packaging/housing: 0805 (2012 metric)	581-600F220FT250XTV	600F220FT250XTV	KYOCERA AVX	2,06 €	3
c21,c24,c25	Capacity:10pF Packaging/housing: 0603 (1608 metric)	581-600S100JT250T	600S100JT250T	KYOCERA AVX	0,967 €	3
R1,R2	Resistance:0 Ohms Housing Code - Inch:0402Housing code - mm:1005	594-MCS0402HZ0000ZE1	MCS0402HZ0000ZE100	Vishay / Beyschlag	0,716 €	2
R3	Resistance:10 ohms Housing Code - Inches:0603Housing code - mm:1608	71-RCP0603W10R0GEB	RCP0603W10R0GEB	Vishay / Dale	€2.39	3
RTM_1_3	O 1.3mm length 10mm	RTM 1,3-100	RTM 1,3-100	reichelt	€2,15	2

AKL 101-02	Connection terminal, 2-pole, Ø 2 mm, RM 5.08	AKL 101-02	AKL 101-02	reichelt	€0.26	3
WE632723300011(USB Type C Connectors USB 3.1)	Rated current:3 A Insulation resistance:1 Gohms Nominal voltage:5 V	710-632723300011	632723300011	Wurth Elektronik	4,06 €	1
J1,J5,J6,J7,J8 MPE 087-1-004 Pin headers 2.54 mm, 1X04, straight	Number of poles:4 Grid dimension:2.54mm	MPE-087-004	MPE-087-004	reichelt	0.11	5
J2,J3,J4,J9 MPE 087-1-002 Pin headers 2.54 mm, 1X02, straight	Number of poles:2 Grid dimension:2.54mm	MPE-087-002	MPE-087-002	reichelt	0,06 €	4
J10 MPE 087-1-003 Pin headers 2.54 mm, 1X03, straight	Number of poles:3 Grid dimension:2.54mm	MPE-087-003	MPE-087-003	reichelt	0,07 €	1
LTC6655LNCHMS8-4.096#PBF(voltage reference)	VREF Series - Input Voltage - Max.:4.296V to 13.2V Output voltage:4,096 B	584-L6655LNCHMS84096	LTC6655LNCHMS8-4.096#PBF	Analog Devices	9,63 €	1
LT1761IS5-3.3TRMPBF(LDO voltage regulator)	Output voltage:3.3V Output current:100mA Input voltage, min.:1.8VInput voltage, max.:20V	584-1761IS5-3.3TMPF	LT1761IS5-3.3#TRMPBF	Analog Devices	€4.06	1
LT1762EMS8-2.5PBF(voltage regulator)	Output voltage:2.5V Output current:150mA Input voltage, min.:1.8V Input voltage, max.:20V	584-1762EMS8-2.5PBF	LT1762EMS8-2.5#PBF	Analog Devices	€4.05	1
LTC2368IMS-16PBF	Resolution:16 bits Amount of channels:1 channel Sampling rate:1MS/s Analog supply voltage:2.5V	584-LTC2368IMS-16PBF	LTC2368IMS-16#PBF	Analog Devices	32,55 €	1

6.4 PCB assembly plan

A circuit board is referred to as a prototype circuit board (PCB) before electrical components are assembled on it. Printed circuit board assembly, also known as PCB board assembly (PCBA), is the process of assembling different components, such as integrated circuits, resistors, and capacitors, and soldering paste on the printed circuit board (PCB).[22]

Design the PCB layout in a design software to create the schematic and layout design. Define the dimensions of the board, place component on it and route traces. Perform an ERC(electrical rule checks) and DRC(design rule checks) check to verify that your design is correct. Export Gerber files of the design including drill file and BOM and send these to a PCB manufacturer. The manufacturer will make board layers, apply solder mask and add silkscr

Here is a step-by-step process of PCB board assembly:

Step 1: Apply solder paste to circuit board: - Place thin stainless steel stencil on circuit board using mechanical device. Solder paste should be applied evenly onto the circuit board in the exact positions needed.

Step 2: Pick and place the machine: - SMD or surface mount components must be placed on the PCB prepared by the robotic device.Then the components need to be soldered to the circuit board surface.

Step 4: Inspect the PCB assembly

Once the reflow process is complete and the mounting components are soldered, testing of the PCB takes place.The assembled board must be inspected and tested for functionality.Ways to inspect PCBA for quality control include:

Manual inspection: Visual inspection performed directly by the designer to ensure the quality of the PCB.

Automated Optical Inspection: An inspection method more suitable for larger batches of PCBA. The automatic optical inspection machine, also known as the AOI machine, uses high-power cameras, placed at different angles to view welds.[22]

X-ray Inspection: Inspection is used for more complex PCBs by examining the layers of the PCB and identifying potential problems

Step 5: Install a Plated Through-Hole Component A plated through-hole component, or PTH, is a hole in the PCB that is plated through the board. Instead of solder paste, a more specialized soldering method is needed for PTH.

Manual soldering : With manual through-hole insertion

Wave Solder: Automatic version for manual soldering where a wave of molten solder solders all the holes at the bottom of the board at once. A solder paste tool, transfer machine, high-speed chip thrower and infrared oven installed in a conveyor configuration can apply soldering.

Step 6: Perform Final Testing Once the soldering of the PCB assembly is complete, it's time to Finally, perform final quality testing and functional testing. Run power and signal simulation to test the electrical characteristics of the PCB. A sign that the PCB is defective is when it shows fluctuations in electrical signals during testing.If the PCB fails the final inspection, it must be scrapped. And the process starts again until the PCB is successfully produced.[22]

6.5 PCB Design of ADC Board

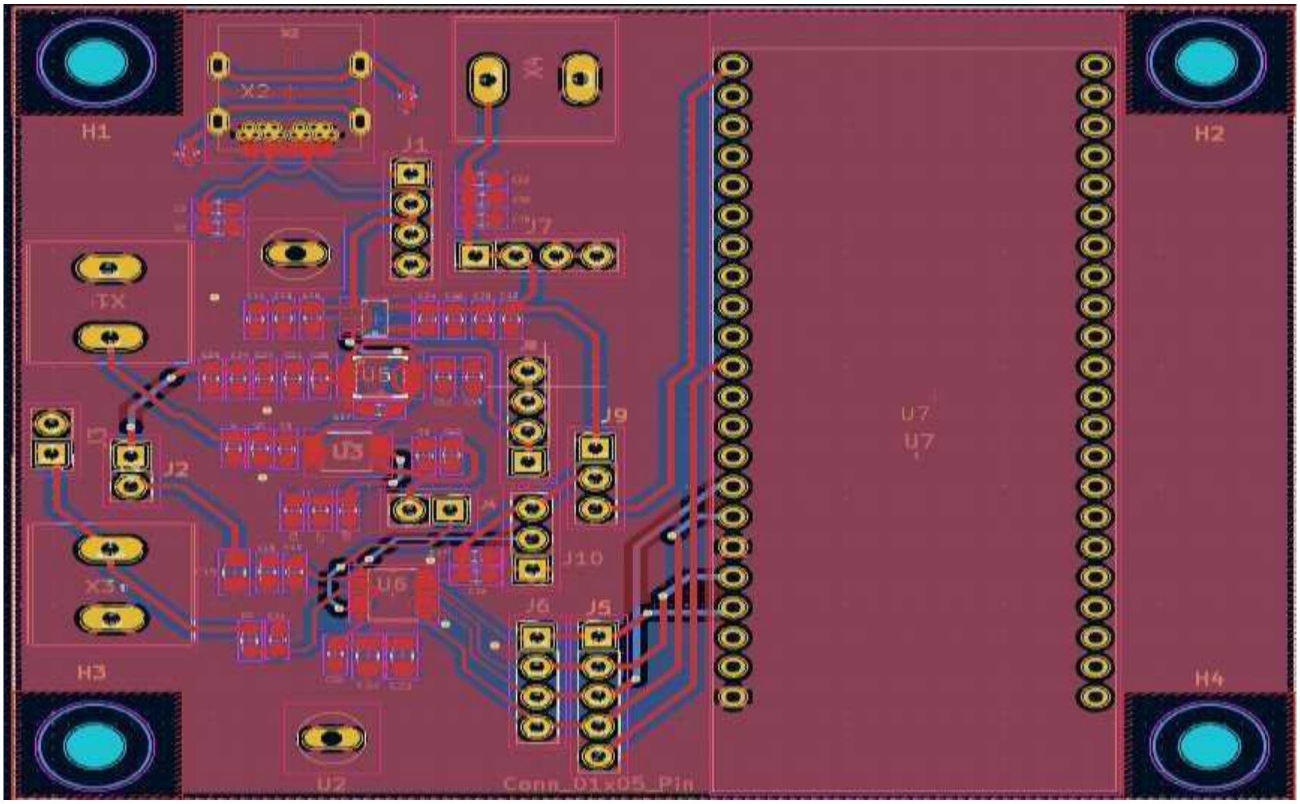


Figure 22: PCB Design of ADC Board

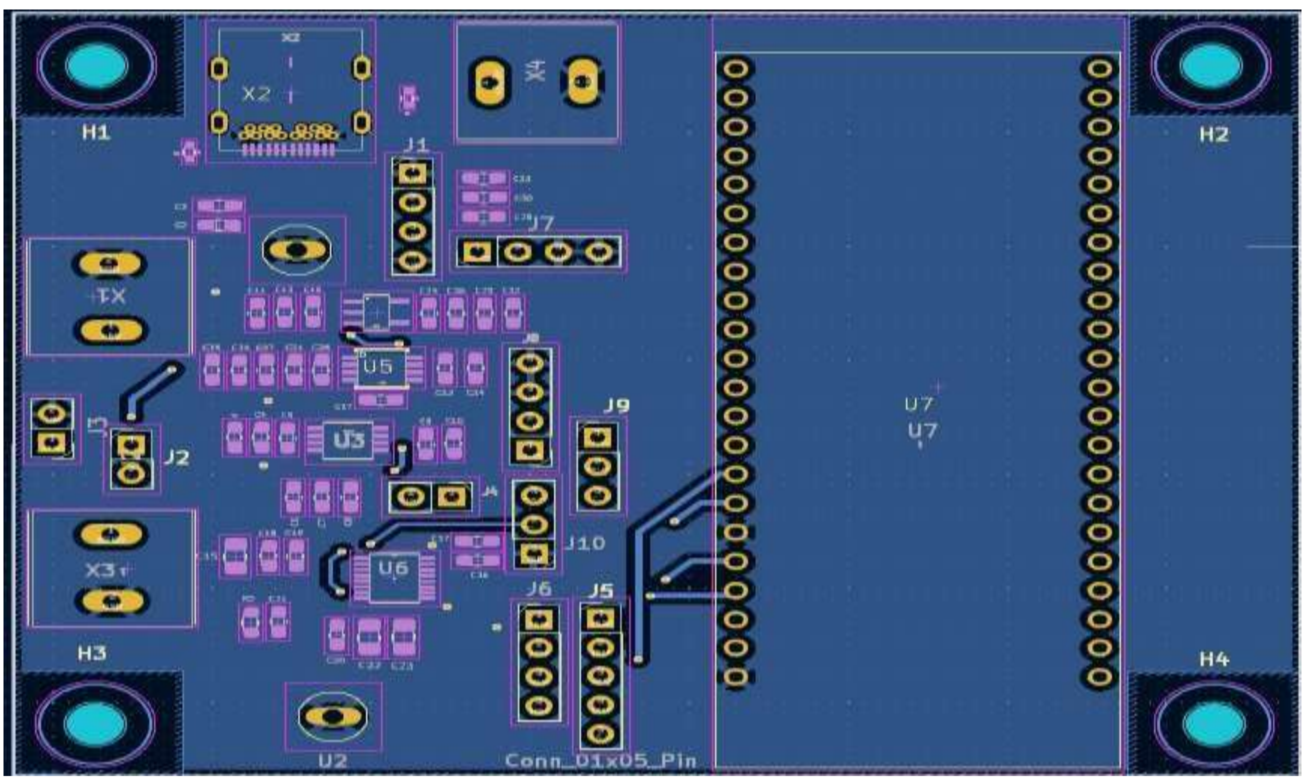


Figure 23: Bottom Layer PCB Design of Analog-Digital Converter Board

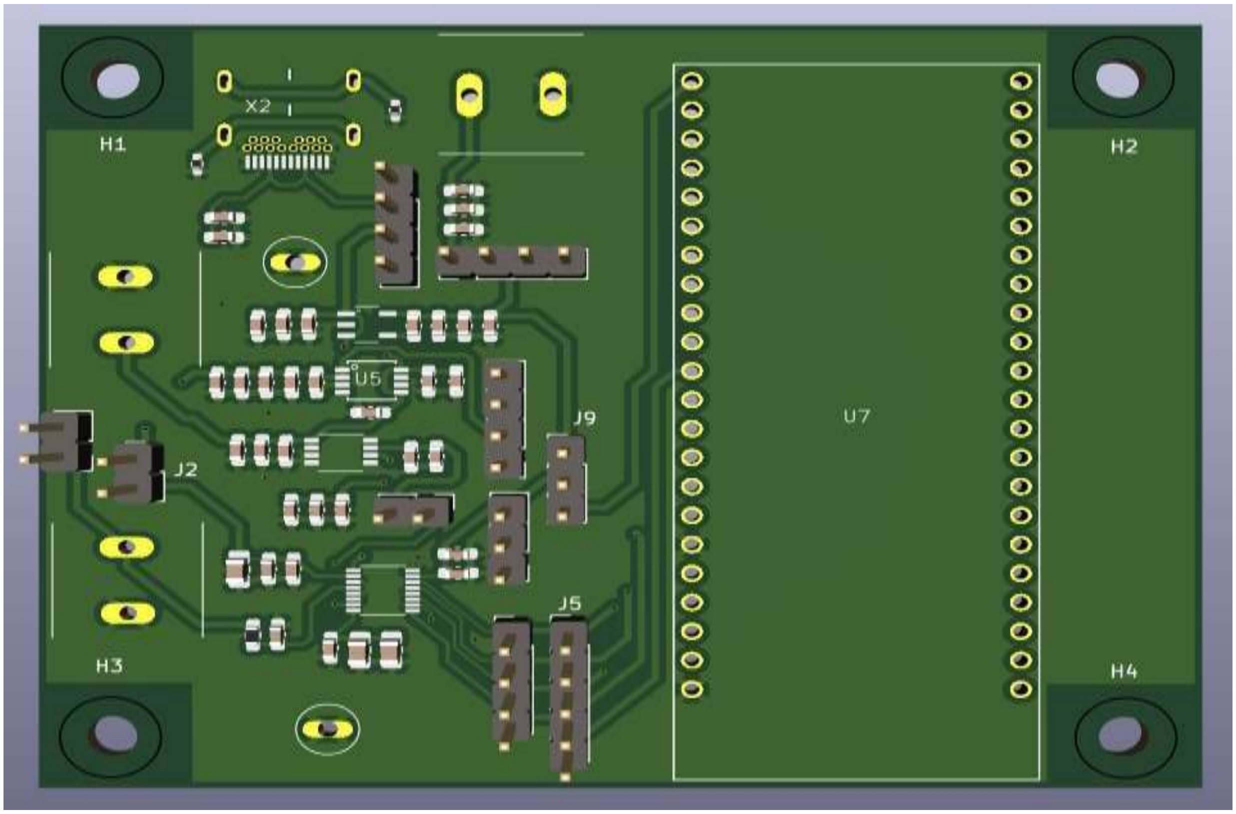


Figure 24:- Top view of 3D design of PCB Figure 23:- Top view of 3D design of PCB

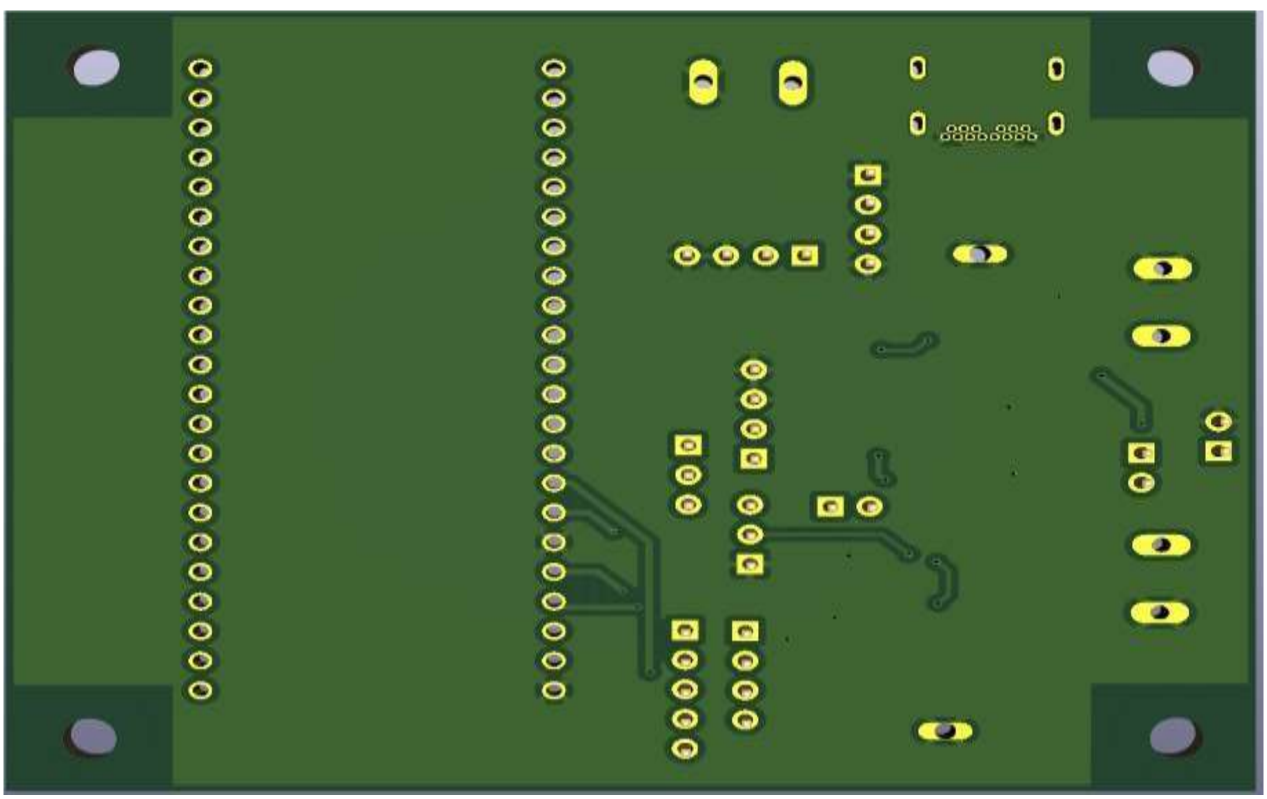


Figure 25:- Bottom view of 3D design of PCB

important of alignment and placement of the components in the layout design

A proper placement of components plays a critical role in PCB layout design and therefore it impacts performance, reliability. Consider the following factors:

1. Keep components as close together as possible to reduce the length of interconnecting traces and place critical components where they will cause minimal noise or interference.

2. Power and Ground: Establishing a reliable power and ground connection should be the primary focus in your design. Position decoupling capacitors near the power pins to ensure stability, and Optimize ground plans for low-impedance return paths.

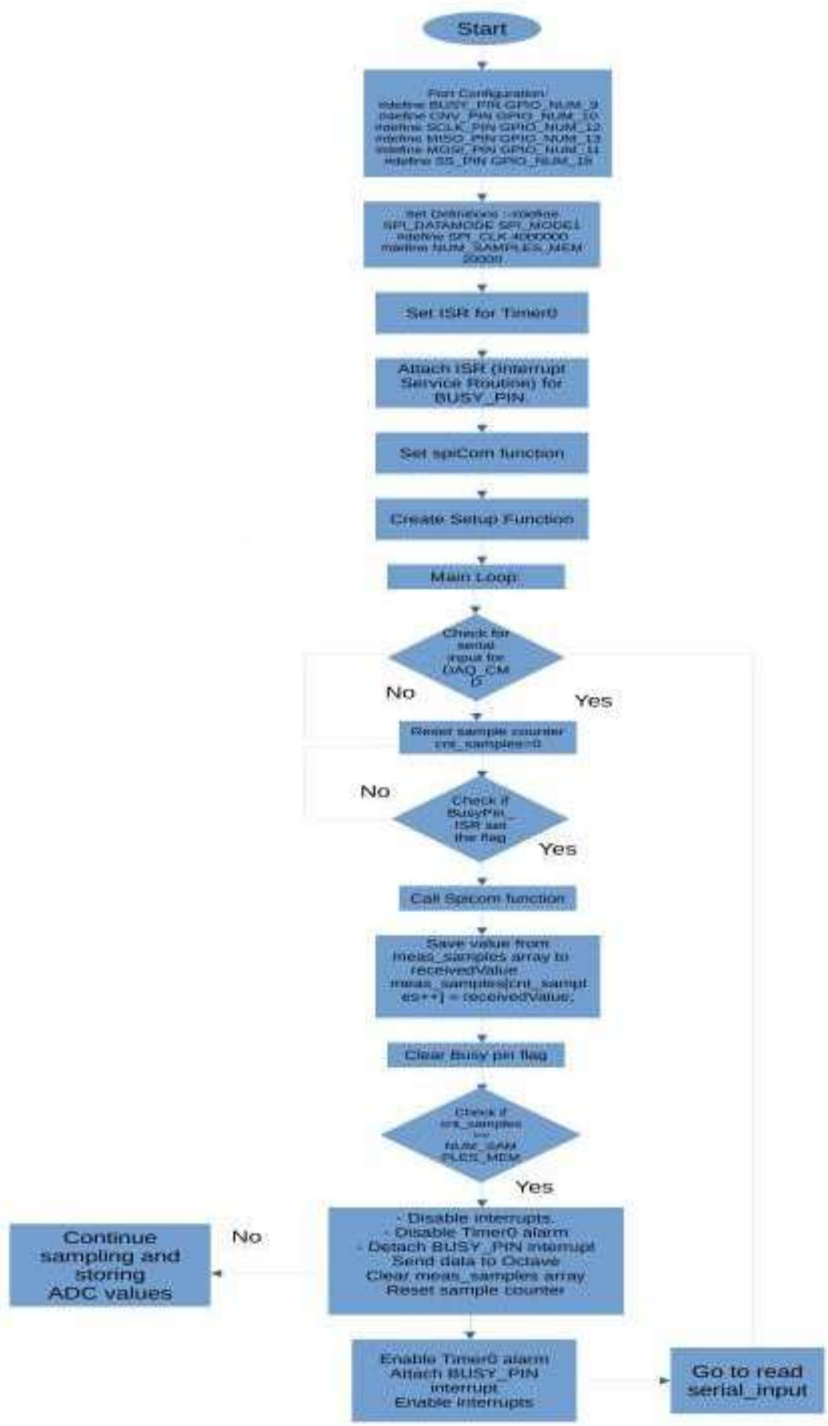
3. Thermal Considerations:When placement of heat-generating components, plan for effective heat dissipation by using thermal vias and heat sinks.

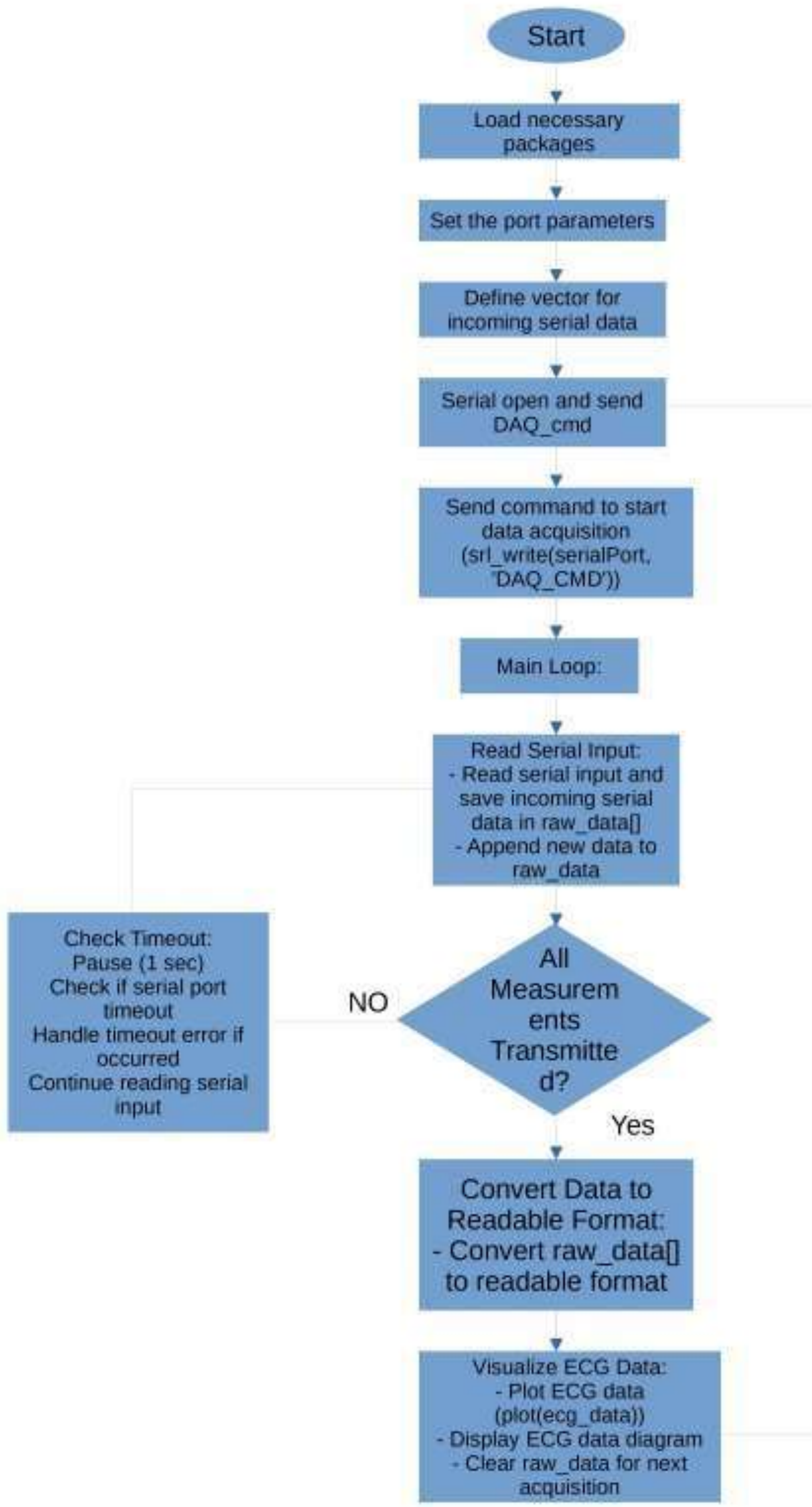
4. Manufacturing Constraints: Provide enough space for soldering, assembly, and testing activities; try to aligning footprints with industry guidelines.

5. Mechanical Constraints: when making the layout which involves fitting within available space, aligning with connectors or mounting holes, and ensuring mechanical stability.

Chapter 7: ADC-board Software

The flowchart outlines the key steps in the ADC-board software (plateform.io IDE and Octave)




Start
Load necessary packages
Set the port parameters
Define vector for incoming serial data
Serial open and send DAQ_cmd
Send command to start data acquisition (srl_write(serialPort, 'DAQ_CMD'))
Main Loop:
Read Serial Input:
- Read serial input and save incoming serial data in raw_data[]
- Append new data to raw_data
All Measurements Transmitted?
NO
Check Timeout:
Pause (1 sec)
Check if serial port timeout
Handle timeout error if occurred
Continue reading serial input
Yes
Convert Data to Readable Format:
- Convert raw_data[] to readable format
Visualize ECG Data:
- Plot ECG data (plot(ecg_data))
- Display ECG data diagram
- Clear raw_data for next acquisition

In this chapter, i discuss the software part for the ADC-board.I use Plateform.io for as IDE,octeve for data visualization and some other packages.The flow chart indicate the overall process software part in our project starting with configuring the ports, sampling data, communicating via SPI, processing the data, transferring the data, interacting with Matlab/Octave, and presenting the data.

Initialize the hardware timer, serial communication, and SPI Communication is the first phase in the ADC programming flowchart.While SPI communication is configured, the GPIO pins that we set in Schematic will set like CNV_PIN, BUSY_PIN, SCLK_PIN, MISO_PIN, MOSI_PIN, and SS_Pin are configured to interface with the LTC2368-16 ADC.Timer0 is set up for periodic ADC sampling, and an Interrupt Service Routine (ISR) is attached to the BUSY_PIN to find when the ADC data is ready.

In the loop of this program it checks first any incoming command from octave instance run on our laptop through serial port. When DAQ_CMD command is received, then DAQ_CMD flag will be set and cnt_samples is reset to zero indicating the start of the data acquisition process.

The program then enters in a data acquisition loop where it checks the ISR flags. If the Timer0 ISR flag is set perfectly then it triggers an ADC conversion by toggling the CNV_PIN.If the BUSY_PIN interrupt service routine flag is set then the program reads the ADC result via SPI, stores the data in the meas_samples array, and increase the sample counter. If the sample counter reaches NUM_SAMPLES_MEM = 20000, interrupts are disabled, the data is sent to the Octave script using the sendtoOctave() function, the meas_samples array is cleared, and interrupts are re-enabled, ready for the next acquisition cycle.

Serial communication is initialized with the COM port (COM3) via an Octave script, at a baud rate of 115200. Byte size, parity, stop bits and timeout are set in order to ensure reliability. The microcontroller sends ADC values to the raw_data array while expecting num_samples_mem samples.

Upon sending 'DAQ_CMD', the script enters a loop to gather data blocks (newData1, newData2) until reaching NUM_SAMPLES_MEM * 2 bytes. It Convert raw_data to uint16 value to ASCII and send it for ADC values, plots ECG data graphically, clears raw_data for next acquisition, and triggers another 'DAQ_CMD' for continuous data collection.The flowchart includes timeout handling, issuing error messages if data reception exceeds specified limits, ensuring robust data acquisition and visualization from the microcontroller.

7.2 SPI Communication

In our project Serial Peripheral Interface (SPI) communication between the ESP32-s3 microcontroller and the LTC2368IMS16 ADC. The SPI protocol we used for its high-speed data transfer capabilities and reliable full-duplex communication. Here’s a detailed description of how SPI communication works in our context:[25]

1.**Master-Slave Configuration**: The ESP32 works as the master device, while the LTC2368IMS-16 ADC acts as the slave. The master start and controls the communication process.

2. **SPI Pins**: The communication have four main SPI lines:

MOSI (Master Out Slave In): it is Used to send data from the ESP32 to the ADC.

MISO (Master In Slave Out):it is Used to receive data from the ADC to the ESP32.

CLK (Serial Clock): Generated by the ESP32 to synchronize data transfer.

SS (Slave Select): Also called as CS (Chip Select), this pin is used by the ESP32 to enable the ADC. When SS is low, the ADC is selected and communication can occur.

3. **Data Transfer**: During SPI communication, data is transferred in a synchronous manner. The ESP32 generates clock pulses on the SCLK line,

3. Data Transfer: During SPI communication, data transfer synchronously manner. Every clock pulse on SCLK line generated by ESP32 and with each pulse, data is simultaneously sent from the master to the slave (via MOSI) and from the slave to the master (via MISO).

4. Communication Process:

The ESP32 pulls the SS line low to select the ADC.

The ESP32 sends a data to the ADC via the MOSI line, synchronized with the SCLK pulses.

The ADC give response by sending data back to the ESP32 through the MISO line.

After the data transfer is finish, the ESP32 pulls the SS line high to unselect the ADC.

Data Integrity: For good signal conditioning , noise reduction such as filtering and shielding have been implemented so that integrity of data can be maintained thereby reducing errors during this communication.

By using SPI communication, our project ensures proper data transfer between the ESP32 and the LTC2368IMS-16 ADC, enabling accurate analog-to-digital conversion data processing.

PROGRAMMING in plateform.io in C++ :-

main.cpp

```
#include <Arduino.h>

#include <SPI.h>

#include <stdlib.h>

#include <stddef.h>

#define SPI_DATAMODE SPI_MODE1

#define BUSY_PIN GPIO_NUM_9

#define CNV_PIN GPIO_NUM_10

#define SCLK_PIN GPIO_NUM_12

#define MISO_PIN GPIO_NUM_13

#define MOSI_PIN GPIO_NUM_11

#define SS_PIN GPIO_NUM_18

#define SPI_CLK 4000000

#define NUM_SAMPLES_MEM 20000
```

```
void spiCom(SPIClass *spi, uint16_t data, uint8_t mode);
int sendtoOctave(uint16_t fields[], int n_fields);
// Variables
uint16_t meas_samples[NUM_SAMPLES_MEM] = {0};
volatile uint8_t myISR_Flags = 0x00; // Interrupt flags
uint16_t ecgData = 0; // Pre-processed ECG data
uint16_t receivedValue = 0; // Data container for spiCom()
SPIClass *fspi = NULL; // Instance of SPI class object
int cnt_samples = 0; // To count number of samples
bool DAQ_CMD = false; // Flag to track if DAQ command is received
// Hardware timer definition
hw_timer_t *Timer0_Cfg = NULL; // Timer0 configuration
// ISR for Timer0
void IRAM_ATTR Timer0_ISR() {
  digitalWrite(CNV_PIN, HIGH);
  myISR_Flags |= 0x01; // Set Timer0 flag
  digitalWrite(CNV_PIN, LOW);
}
// ISR for Busy pin
void IRAM_ATTR BusyPin_ISR() {
  myISR_Flags |= 0x02; // Set Busy pin flag
}
// SPI communication function
void spiCom(SPIClass *spi, uint16_t data, uint8_t spi_mode) {
  spi->beginTransaction(SPISettings(SPI_CLK, MSBFIRST, spi_mode));
  digitalWrite(spi->pinSS(), LOW);
  receivedValue = spi->transfer16(data);
  digitalWrite(spi->pinSS(), HIGH);
  spi->endTransaction();
}
void setup() {
```

```
  Serial.begin(115200);
  // Initialize SPI
  fspi = new SPIClass(FSPI);
  fspi->begin(SCLK_PIN, MISO_PIN, MOSI_PIN, SS_PIN);
  pinMode(fspi->pinSS(), OUTPUT);
  digitalWrite(fspi->pinSS(), HIGH);
  pinMode(CNV_PIN, OUTPUT);
  pinMode(BUSY_PIN, INPUT);
  // Attach ISR for the busy pin
  attachInterrupt(digitalPinToInterrupt(BUSY_PIN), BusyPin_ISR, FALLING);
  // Timer0 configuration
  Timer0_Cfg = timerBegin(0, 40, true); // Prescaler of 40 for 1us ticks
  timerAttachInterrupt(Timer0_Cfg, &Timer0_ISR, true);
  timerAlarmWrite(Timer0_Cfg, 1000, true); // 1ms interval
  timerAlarmEnable(Timer0_Cfg);
  cnt_samples = 0;
}
void loop() {
  // Check for serial input for DAQ_CMD
  if (Serial.available() > 0) {
    String input = Serial.readStringUntil('\n');
    if (input == "DAQ_CMD") {
      DAQ_CMD = true;
      cnt_samples = 0; // Reset sample counter
    }
  }
// Continue only if DAQ_CMD is received
  if (!DAQ_CMD) return;

  // Marking (2)
  if (myISR_Flags & 0x01) { // Check if Timer0_ISR set the flag
```

```
        myISR_Flags &= ~0x01; // Clear Timer0 flag
        // Start ADC conversion
        digitalWrite(CNV_PIN, HIGH);
        delayMicroseconds(1);
        digitalWrite(CNV_PIN, LOW);
    }
    if (myISR_Flags & 0x02) { // Check if BusyPin_ISR set the flag
        // Read ADC result
        spiCom(fspi, 0, SPI_DATAMODE);
        meas_samples[cnt_samples++] = receivedValue;
        myISR_Flags &= ~0x02; // Clear Busy pin flag
        if (cnt_samples >= NUM_SAMPLES_MEM) {
            cnt_samples = 0; // Reset sample counter
            // Disable interrupts
            noInterrupts();
            timerAlarmDisable(Timer0_Cfg);
            detachInterrupt(digitalPinToInterrupt(BUSY_PIN));
            // Send data to Octave or process it further
            sendtoOctave(meas_samples, NUM_SAMPLES_MEM);
            // Clear array fields
            memset(meas_samples, 0, sizeof(meas_samples));
            // Enable interrupts
            timerAlarmEnable(Timer0_Cfg);
            attachInterrupt(digitalPinToInterrupt(BUSY_PIN), BusyPin_ISR, FALLING);
            interrupts();
        }
    }
}
int sendtoOctave(uint16_t fields[], int n_fields) {
    for (int i = 0; i < n_fields; i++) {
        float ecgData = fields[i] * (3.3 / 65536); // Scale the ECG data to voltage
```

```
        Serial.write((uint8_t*)&ecgData, sizeof(float));
    }
    return 0;
}
```

Octave Configuration :-

```
% Load packages
pkg load instrument-control
% Instantiate the Serial Port
serialPort = serial("\\\\.\\COM3", 115200); % Adjust "COM3" to your port
pause(1); % Wait for device to wake up
% Set the port parameters
set(serialPort, 'baudrate', 115200);
set(serialPort, 'bytesize', 8);
set(serialPort, 'parity', 10);
set(serialPort, 'stopbits', 1);
set(serialPort, 'timeout', 3.8);
% Define vector for incoming serial data
raw_data = [];
% Serial open and send DAQ_cmd
srl_flush(serialPort); % Flush serial port buffers
srl_write(serialPort, 'DAQ_CMD');
disp('DAQ_CMD sent, waiting for data...');
NUM_SAMPLES_MEM = 20000; % Number of samples to acquire
% Read incoming data
while true
    % Read serial input and save incoming serial data in raw_data[]
    newData1 = srl_read(serialPort, NUM_SAMPLES_MEM); % Read first 8 bytes
    newData2 = srl_read(serialPort, NUM_SAMPLES_MEM); % Read next 8 bytes
 if ~isempty(newData1) && ~isempty(newData2)
raw_data = [raw_data; newData1'; newData2']; % Append new data to raw_data (transpose to match row-wise storage)
    end
```

```
% Condition: all measurements transmitted? (Check if enough data is received)
    if length(raw_data) >= NUM_SAMPLES_MEM * 2 % Assuming 2 bytes per sample
        % Convert raw_data[] to readable & printable format (ASCII)
        ecg_data = typecast(uint8(raw_data), 'uint16'); % Convert bytes to uint16
        % Convert each uint16 value to ASCII and send it
        ascii_data = char(ecg_data); % Convert to ASCII characters
        fprintf('Received ASCII data: %s\n', ascii_data); % Display ASCII data
        % Clear raw_data for next acquisition
        raw_data = [];
        % Go to marking (1)
        disp('Data acquisition complete, ready for next command.');
% Optional: Add a delay before sending the next command
        pause(1); % Adjust delay as needed
        srl_flush(serialPort); % Flush serial port buffers
        srl_write(serialPort,   'DAQ_CMD');
        disp('DAQ_CMD sent again, waiting for data...');
    else
        % No then: Check for timeout
        pause(1); % Wait for 1 second before checking again
        if get(serialPort, 'timeout')
            % Yes then: Error handling
            disp('Error: Serial port timeout.');
            break;
        end
    end
end
```

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