Intel Altera tools for FPGA Design

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***Abstract*—In today's modern world FPGAs (Field Programmable Gate Arrays), play a key role in several sophisticated industries. The advantages of FPGAs are faster time to market, parallelism, efficiency and programmablity have resulted in their greater demand and wider applications. FPGAs are used in industries such as Communications, Aeronautics , Defence, etc. To design for various applications various semiconductor companies have released wide range of design tools.**

This paper explains Intel Altera tools for FPGA designing and dives deeper into overview of Intel FPGAs , Intel Altera tool chain and Analysis. A comparative research between Intel Altera and AMD Xilinx designing tools.

***Index Terms*—FPGA, Intel, Altera , Quartus, Soc (system on chip), Vivado**

I. Introduction

There are many companies that produce FPGAs in the semiconductor integrated chip production industry. One of the dominating company in this field is Intel Semiconductor corporation. The company was founded in 1968 and is currently located in Santa Clara , California , USA. [1] Altera was founded in 1983. Altera was producing several types of cutting edge FPGAs. It entered in an agreement on February 2013 with Intel to use Intel's foundry services to produce its 14-nm node for the future manufacturing of its FPGAs. Intel entered the FPGA sector in 2015 when it acquired Altera as its business unit. [2]

II. Overview of Intel Altera FPGAs

A. Intel Altera FPGA Portfolio

INTEL produces a wide range of FPGA products for applications based on custom logic solution. Intel has categorized FPGAs in 5 major categories. [3] The categorization is based on various factors such as IC performance , cost effectiveness and time to market. The following subsections will give an in depth information about each category and respective specific attributes of the FPGA devices.

B. Intel Agilex FPGAs and SoCs

Intel has produces the Agilex FPGAs for **full breath of programmable logic needs**. It is use cases are in industries such as communication and data centers. Intel Agilex FPGAs provide the flexibility needed to tackle challenges such as increasing demand for integrating multiple functions, adopt evolving standards and changing market requiremnts.

Intel Agilex FPGAs have 4 generations. Agilex 3,5,7 and 9. The generations 7 is highest performance FPGAs delivering industry-leading fabric and I/O speeds, ideal for the most bandwidth- and compute-intensive applications. The Agilex 7 FPGA are integrated with SoC technologies and further classified into :

- F series of SoC FPGAs- Designed for wide range of applications across many markets and transceiver rates up to 58Gbps .
- I series of SoC FPGAs - bandwidth-intensive applications with highest performance I/O interfaces, transceiver rates up to 116 Gbps. 4,000,672 logic elements.
- M series of SoC FPGAs- optimized for compute and memory-intensive applications, Network-onChip (NoC) to maximize memory bandwidth. [3]

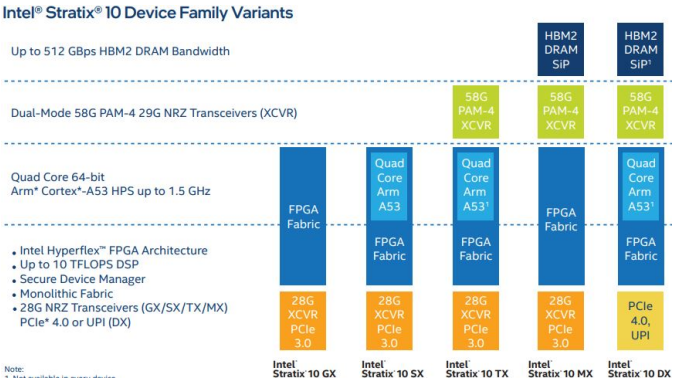

Fig. 1. Intel Stratix 10 FPGAs sub catagories specifications

C. Intel Stratix 10 FPGA and SoC

1) The Stratix 10 FPGA is built on the Intel 14 nm Tri-Gate process and Stratix 10 devices deliver 2 times core performance gains over previous-generation.
2) There is a 70 percent reduction in power consumption.
3) Stratix 10 FPGAs are used in **application which require heavy computing** since they have the highest density FPGA with up to 10.2 M logic elements.
4) Integrated quad-core 64 bit Arm Cortex-A53 hard processor system up to 1.5 GHz.
5) Stratix 10 FPGAs are further classified in 5 categories. [3] The specifications of the variants of Stratix 10 FPGAs are presented in figure 1.

D. Intel Arria 10 FPGA and SoC

- The intel Arria 10 FPGAs are produced by TSMCs foundry on a 20nm fabric making it one speed-grade performance advantage over competing devices. The Arris 10 FPGA is with speeds up to 1,500 giga floating-point operations per second (GFLOPS). This makes the Arria

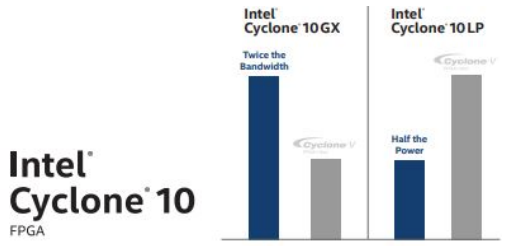

Fig. 2. INTEL Cyclone 10 FPGA generation 10 progression

10 FPGAs an ideal use case for **end market applications because of its high speed**s. Its applications are as follows

- Remote radio head
- Mobile back haul
- Data center server acceleration
- Encoder/decoder

E. Intel Cyclone 10 FPGA and SoC

Intel Cyclone 10 FPGAs are designed for low cost and powers saving applications. There are two variants of the Cyclone 10 FPGAs.

1) **Intel Cyclone 10 GX FPGA**s : The Cyclone 10 GX variant is **optimized for high-bandwidth** applications such as industrial robotics, embedded vision cameras and machine vision. They provide high bandwidth via 12.5G transceiver-based functions.
2) **Intel Cyclone 10 LP FPGAs** : The Cyclone 10 LP variant is **designed for low cost and power sensitive applications**. They are enabled with embedded Nios II soft processor support. Its applications are in sensor fusion, industrial motor control and I/O expansion.

Figure 2 show the generation 10 progression as compared to previous genrations.

F. Intel MAX 10 FPGA and SoC

Intel MAX 10 FPGAs are optimized for a **wide range of high-volume and cost-sensitive applications**. Intel MAX 10 FPGAs are produced by TSMCs foundry on 55nm flash technology. The MAX 10 FPGAs include FPGA capabilities such as Digital Signal Processing, analog functionality, Nios II Gen2 embedded soft processor support and memory controllers.

Its major applications are as follows:

- Electric Vehicle - The signal processing acceleration allow use cases such as motor control, battery management, and power conversion.
- Industrial applications - efficient real-time controls for motor control and I/O modules. Use cases in Internet of things (IOT) applications because enables accurate environmental condition sensing.
- Communications - Analog functionality allows integration system-monitoring circuitry in a single device.

INTEL ALTERA FPGAS DESIGN TOOLS

G. FPGA designing challenges introduction

FPGAs designing process faces many challenges such as RTL code analysis, physical synthesis for earlier timing and parallel data processing. To solve these challenges an integrated approach based FPGA designing tool is required. This will simplify the designing process as well as provide solutions to increasing demand for complex data processing requirements.

H. Intel Quartus Prime Design Software

The Intel Quartus Prime Design software is a premium software from Intel used to design entry, synthesis to optimization, verification, simulation, and binary generation for Intel FPGAs. The software is available to the user in three editions : pro version, standard version and lite version. The lite versions is free to use while the pro and standard versions require a paid licence. The Quartus Prime Design software supports Agilex, Stratix, Cyclone , Max and Arria series FPGAs.

The following subsections will give an overview of the various tools within Quartus Prime Design software.

1) Platform Designer: The Platform Designer saves time and reduces workload in the FPGA design process by automatically generating interconnect logic to connect intellectual property (IP) functions and subsystems. The platform designer uses a hierarchical framework to offer fast response times and provides support for blackbox entities. The platform designer uses various design tools to create register transfer level (RTL) languages, block-based design entry and schematic entry. [4]

2) Block based design workflows: The block based design workflows allow the user to create designs faster and add the possibility for re-usability of the block in future. This feature allow the user to add 3rd party IPs and pre designed blocks. It also allow geographically diverse teams to collaborate together as group within the team can work on a specific block at a time. The designed blocks and can be integrates together at the final stage of the project. [5]

3) Partial reconfiguration: Partial reconfiguration creates the ability to reconfigure a part of the FPGA design dynamically while the rest of the FPGA design continues to function. This allows to have implementation of complex FPGA design systems. [5]

4) Creating a design partition: A design partition is a logical, named, hierarchical boundary that can be assigned to an instance in the FPGA design. This design partitioning can optimize and lock down results for individual blocks. This provides the ability to reuse the results of individual blocks in another projects. Figure 3 shows an example of design partitioning. [5]

5) Chip Planner: Chip planner allows you to view floorplanning of the FPGA resources in a FPGA design. The chip planner can be used to modify the logic placement, connections, and routing paths after running the Fitter. [5]

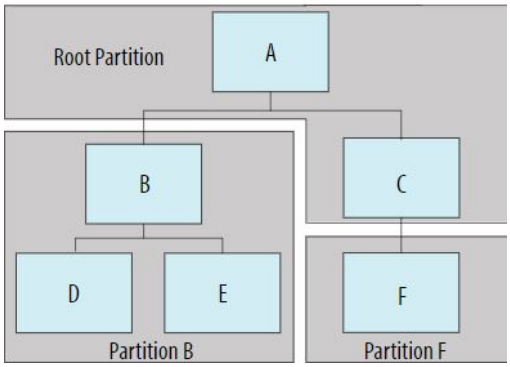

Fig. 3. Design Partition

6) Interface planner: The interface planner explores the FPGA devices peripheral architecture and assigns appropriate interfaces. This results in prevention of illegal pin assignments by performing fitter and legality checks in real time. This process eliminates complex error messages and speed up I/O design. [5]

7) Logic Lock regions: A Logic Lock region is logic placement and routing constraint. You can define any physical resource of the device as logic lock region. Then assign design nodes and other properties to the region. This gives a more predictable result with each design iteration. [5]

8) Fitter (Place and Route) : The fitter process all levels of design place and route, including the Plan, Early Place, Place, Route, and re-time stages. [5]

9) Register re-timing: The register re-timing stage of the fitter can balance register chain by moving them into hyper registers in the routing fabric itself. The register re-timing stage can also move the register chain across combinational logic to provide optimized solutions. [5]

10) Timing Analyser: The timing analyser is an ASCI style timing analysis tool that analysis the timing performance of a FPGA design. The timing analyser checks the timing for design paths, evaluates the propagation delay along each path and checks for any timing constrain violations. It reports timing results as either a positive slack or negative slack. [5]

11) The Design Space Explorer II tool : The design Space Explorer tool processes the design using a group of settings and constraints. The tool reports the best combination of setting and constraints. This allow the FPGA design to have the most optimal project setting for resource, performance and power consumption. [5]

12) Power analyzer: The power analyser can analyse the power consumption up to the field-programmable gate level. This allows it to produce highly accurate power reports as it has access to the design routing and configuration information. [5]

13) Signal Tap Logic Analyzer: The signal tap logic analyzer reads and reports real-time signal behaviour in a FPGA design. The tool gives you a sight of internal signal without the requirement of any I/O pins or external devices. This allow to debug more efficiently. [5]

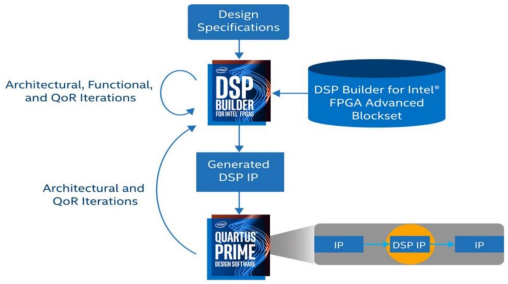

Fig. 4. DSP Builder for intel FPGAs

14) Transceiver Toolkit: The transceiver toolkit allow designer real-time transceiver settings and reduces board bring-up time. It can run link tests across many board and devices. It also provides channel manager to track and monitor for testing multiple channels simultaneously. [5]

15) Intel Advanced Link Analyzer: The Intel advanced link analyzer tool allow designers to evaluate high-speed serial link performance. It can also be used in post design debug and validation processes. [5]

I. Digital Signal Processing Builder for Intel FPGAs

The Digital Signal Processing (DSP) Builder for Intel FPGAs is a tool that generates hardware description language (HDL) for DSP algorithms form Mathworks and simulink tools on Intel FPGAs. The tool generates highly systhesizable VHDL/ Verilog code from matlab functions and simulink models. The following are some features of DSP builder tools [6]:

1) From high-level schematic to low-level optimized VHDL targeted for Intel FPGAs.
2) Co-simulation and code generation by importing RTL into matlab/simulink.
3) Allows access to advanced math.h functions and multi-channel data.

Figure 4 gives an visual overview of the DSP Builder.

J. High Level Synthesis compiler

The high level synthesis compiler (HLS) takes in untimed C++ code and produces a production quality register-transfer level (RTL) code. This tool also helps you to explore multiple architectures through high level directives. It also generates reusable intellectual property (IP) for system integration using the Platform Designer. This tool supports inference of streaming, memory mapped, or wire interfaces, device-specific timing-driven schedule optimization and technology mapping .

It also helps user analyze area utilization, loop structure, memory usage, system data flow, clusters, and surrounding logic [5]

K. Ashling RiscFree IDE

Ashling RicsFree IDE is a integrated developing environment specially designed for intel ARM based processors FPGA and nios 5 soft processors. It is also included with the

Intel Quartus Prime Software Pro version 22.2. It comprises of an entire tool chain including IDE, Compiler, Debugger and Trace. [5]

L. Intel Simics simulator for Intel FPGAs

This is a full-system simulation tool that supports definition, development and deployment on virtual platforms. This ensures early product development and reduces product time to market. It also eliminated the need for a physical FPGA board for development purposes. This simulator provides a software and hardware simulation in parallel and hence provides a co-related visibility. The platform also offers its user teams a virtual environment to collaborate in real-time to increase productivity. [5]

M. Intel FPGA AI Suite

The intel FPGA Artificial intelligence platform was created to ease the use of AI on intel FPGAs. The suite enables FPGA designers, machine learning engineers, and software developers to create optimal artificial intelligence based applications for the customer requirements. [5]

III. Intel and AMD Xilinx FPGA tools

A. Vivado

Vivado Xilinx FPGA design tool is a powerful software that has been designed to create various complex functionalities in an easy to use fashion. It supports various HDLs such as VHDL, Verilog, and SystemVerilog. It has several capabilites such as :

- High-level synthesis
- Integrated logic simulation
- IP integration
- Design reuse
- Hierarchical design
- Timing analysis
- Power optimization
- Debugging tools [7]
-

1) Strengths of Vivado :

1) The Vivado software is capable of handling complex designs with ease. It is created in a way that produces scalable designs and can handle designs of all sizes.
2) Another advantage is that its ability to integrate with other tools. The software is designed to work swiftly with other Xilinx tools such as Vivado HLS tool and the SDSoC development environment. This integration allows the Vivado tool to design optimal solution to a specific hardware design problem.
3) The third advantage is the Vivado software has several features and tools within itself to fine tune the details of your software design to maximize end product quality and reliability. [7]

B. Comparison Between Vivado and Intel Quartus

This comparison is based on 4 key factors that play a crucial role in choosing the best FPGA design software for developing a FPGA design;

- **Ease of use** : Both softwares have a very high degree of ease of usability since they are designed to create complex designs. However they vary in specific cases where the designer's experience is taken into consideration. The vivado software is ideal for designers with less experience or new designers in the FPGA designing industry. This is because vivado has more modern and intuitive user interfaces as compared to intel quartus. The intel quartus on the other hand has more steep learning curve but has more customizable options for advanced users.
- **Design flow** : Vivado offers a more streamlined process for FPGA design development than intel Quartus by having faster compile times and faster implimentation times. The intel quartus has more complex design flow but comprises of other qualities such as more flexibility in terms of design optimization and customization.
- **Performance**: The intel Quartus offers a slight advantage in performance in some aspects. The vivado on the other hand has the ability to support newer FPGA architectures allowing it to develop more cutting edge designs.
- **Cost**: Vivado is more expensive than Quartus but also provides more advance features. Quartus is cheaper than Vivado but provides a balance between cost and the available features. [7]

Both Vivado and Quartus are unique tools and provide best designing platforms as per the user requirements.

IV. Conclusion

To conclude, this paper provides a brief description and explanation of the FPGA products by Intel such as Agilex, Stratix, Arria, Cyclone and Max series FPGAs. It encompasses a detailed view of numerous software design tools provided by Intel such as Quartus and others. It describes there uses and key features. The paper also gives a short overview of AMD Xilinx FPGA design tool that is Vivado. It provides a comparison between Vivado and Quartus on 4 key factors.

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