

~~ELL - 604~~

~~System Design~~

~~Electronic~~

SYLLABUS

Unit-I: Design of Power Supply System, Unregulated DC power supply system with rectifier and filter, Consideration regarding ripple, Design of emitter follower regulator (series pass transistor regulator), Design of SMPS, Step up and step down, IC voltage regulator, Positive & negative voltage regulator, Adjustable regulators, High current short circuit protection.

Unit-II: Design of Single Stage and Two stage amplifiers (R-C Coupled) using BJT, Design and analysis of power amplifier: class A, class B, class AB, Design of transformer coupled class A power amplifier.

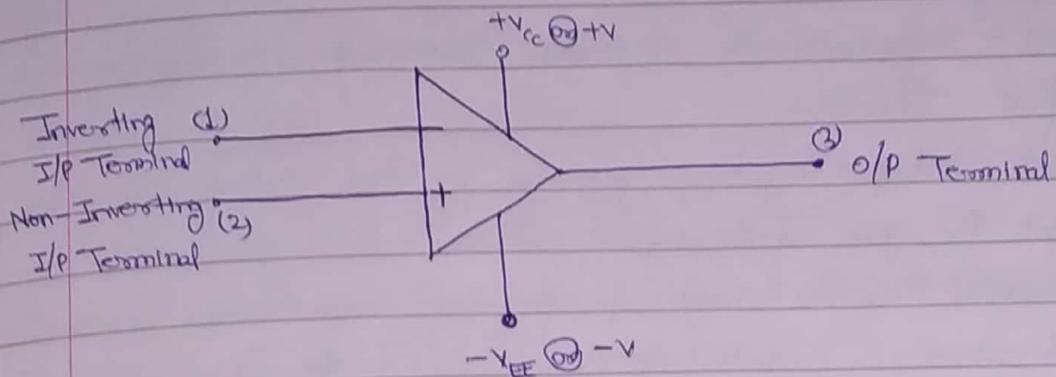
Unit-III: Design of Oscillators using BJT: Frequency of oscillation and condition for sustained oscillation, Sine wave oscillators, Audio frequency and radio frequency oscillators.

Unit-IV: Operational Amplifier: Basics of an OP-Amp, OP-Amp parameters, their basic application, Inverting amplifier, Non-Inverting amplifier, Differential Amplifier, Integrator, Differentiator, Voltage follower, Adder, Subtractor, V to I and I to V converter, Design of Butterworth, Chebyshev filters.

Unit-V: Design of Digital System: flip-flops, registers, counters, A to D converters and D to A converters and Digital voltmeter.

A. OPERATIONAL AMPLIFIER

(A)



IC 741

- It is a linear IC.
- It has very high voltage gain, high input impedance, low output impedance.
- Inverting Terminal: It produces the opposite polarity, (by 180° phase shift) to output signal.
- Non-Inverting Terminal: It produces the same polarity ($0^\circ/360^\circ$ phase shift) to output signal.

* OP-Amp Parameters

- i) Gain
- ii) Output Impedance (Resistance)
- iii) Input Impedance (Resistance)
- iv) Input Offset Voltage
- v) Output Offset Voltage
- vi) Input Bias current
- vii) Slew Rate
- viii) Bandwidth
- ix) CMRR (Common Mode Rejection Ratio)
- x) Input Offset current

* Characteristics & Properties of an Ideal OP-Amp

i) Voltage gain = ∞

ii) Input Impedance = ∞ , it means, I (current in OP-Amp) = 0

iii) Output Impedance = 0

iv) Offset Voltage = 0, it is zero for an ideal OP-Amp, this means zero output for zero input signal voltage.

v) Bandwidth = ∞ ; the range of frequency over which the amplifier performance is satisfactory, is called its bandwidth. The bandwidth of ideal OP-Amp is infinite. This means operating frequency range is from zero to infinite.

* CMRR (Common Mode Rejection Ratio; S)

$$S = \frac{A_d}{A_{cm}} = \infty \text{ (For ideal op-amp)}$$

where, A_d = Differential gain

A_{cm} = Common Mode gain

Because of the common mode noise off $V_{lg} = 0$ for an ideal OP-Amp.

* Slew Rate

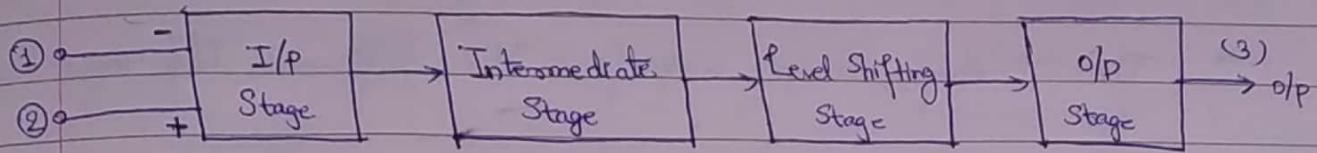
$$\text{Slew Rate} = \infty \text{ (For ideal OP-Amp)}$$

This ensures that the change in the output voltage simultaneously with changes in the input voltage.

S.No.	Characteristics	Representation	Values
1.	Voltage Gain	A	∞
2.	I/P Impedance	$Z_i \approx R_i$	∞
3.	O/P Impedance	$Z_o \approx R_o$	0
4.	Offset Voltage	$V_{off(las)}$	0
5.	Bandwidth	B.W.	$\infty (0-\infty)$
6.	Slew Rate	S.P.	∞
7.	CMRR	S	0

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* Idea Basic Block Diagram of an OP-Amp



I/P Stage → Dual input balanced amplifier
output differential

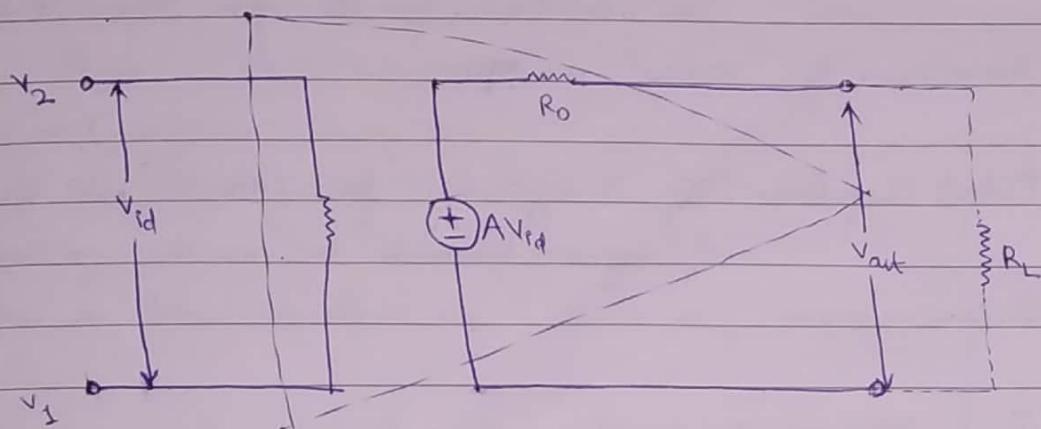
Intermediate Stage → Dual input unbalanced output differential amplifier

Level Shifting Stage → Emitter follower constant current source

O/P Stage → Complementary Symmetry Push-Pull Amplifier

* PRACTICAL OP-AMP

- Characteristics



Equivalent Ckt. of Practical OP-Amp

$$\begin{aligned} v_{out} &= A V_{id} \\ &= A(v_1 - v_2) \end{aligned}$$

→ In practical OP-Amp which has finite output & input resistance and a finite open-loop voltage gain.

→ In practical OP-Amp, i/p impedance $\neq \infty$ & o/p impedance $\neq 0, \infty$, output voltage is given by

$$v_{out} = A V_{id} = A(v_1 - v_2)$$

where, $A = \text{open loop gain with o/p terminal}$

→ The OP-Amp always amplifies the difference b/w input voltage.

- Properties

i) Open loop gain: It is v/g gain of the OP-Amp when no feedback is applied. Practically, it is several thousands gm in dB.

$$\text{Gain in dB} = 20 \log_{10} \left(\frac{V_o}{V_i} \right)$$

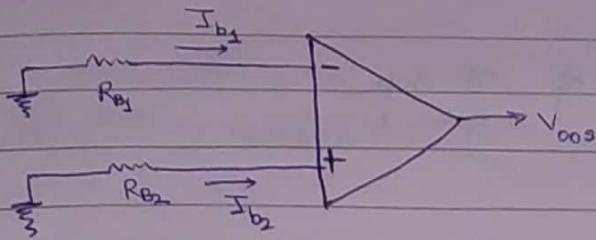
ii) Input Impedance: It is finite & typically greater than $1M\Omega$. If we use FETs, for the input stage it can be increased to several $100M\Omega$.

iii) Output Impedance: It is typically few 100Ω , with the application of negative feedback it can be reduced to 1Ω .

iv) Bandwidth: It is in open loop configuration, it is very small. If we apply negative feedback, bandwidth increases to a desired value.

v) Input Offset Voltage: The D.C. voltage which makes the output v/g (V_{ios}) zero when the other terminals is grounded is known as input offset voltage. Input offset voltage depends on temperature.

vi) Output Offset Voltage: When o/p obtained with both i/p terminals are grounded, is the output offset voltage.



It is produced due to input offset voltage V_{ios} & also due to input bias current I_b .

$$V_{oos} = V_{out} \text{ due to } V_{ios} + V_{out} \text{ due to } I_b$$

$$\therefore V_{oos} = \left(1 + \frac{R_f}{R_1}\right) V_{ios} + I_b \cdot R_f$$

Now, the input bias current I_b which is the average of I_{b1} & I_{b2} .
Let assume $I_{b1} = I_{b2}$

$$\text{Hence, } I_{b1} = I_{b2} = I_b$$

then, eq. becomes

$$V_{oos} = \left(1 + \frac{R_f}{R_1}\right) V_{ios} + I_b \cdot R_f$$

This is the op offset vlg without any compensating network used.

18.01.19

vii) Input Bias Current: It is the average of two bias current flowing into the two input terminals.

$$I_b = \frac{|I_{b1}| + |I_{b2}|}{2}$$

viii) Input offset Current: Difference b/w the two bias currents flowing towards the input of Op-Amp is input offset current.

$$I_{pos} = |I_{b1} - I_{b2}| \quad (20 - 60 \mu A)$$

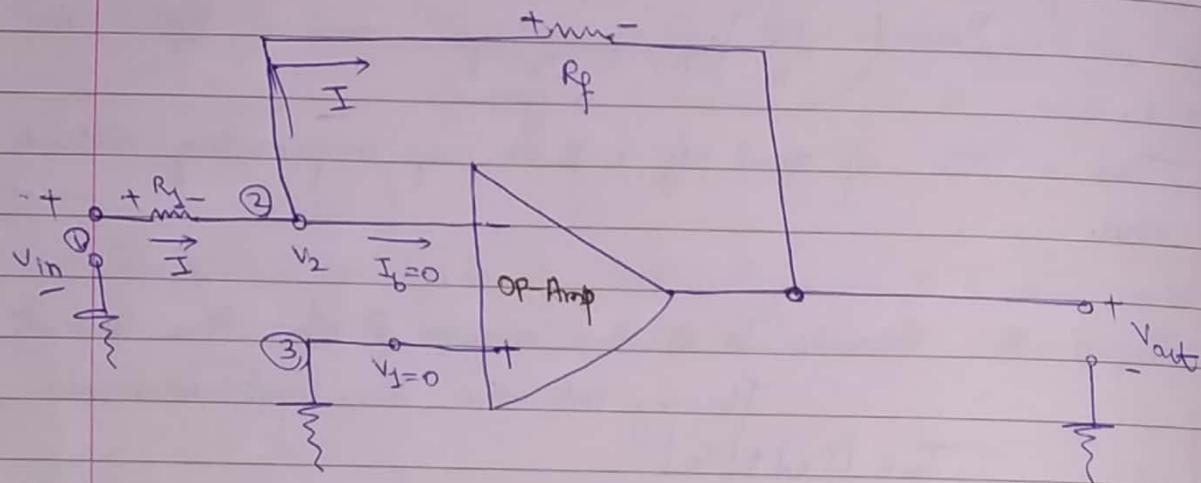
* Linear Applications of OP-Amp

- i) Adder
- ii) Subtractor
- iii) Integrator
- iv) Differentiator
- v) Voltage follower
- vi) Instrumentation Amplifier

* Non-Linear Applications of OP-Amp

- i) Comparator
- ii) Anti-logarithmic Amplifier
- iii) Logarithmic Amplifier
- iv) Schmitt Trigger

* Ideal Inverting Amplifier



→ The op of an ideal inverting amplifier

→ An amplifier which provides a phase shift of 180° b/w i/p & o/p is known as inverting amplifier.

Apply KCL at pt. ②,

$$\frac{v_2 - v_{in}}{R_1} + \frac{v_2 - v_o}{R_f} = 0$$

Here, $V_1 = V_2 = 0$

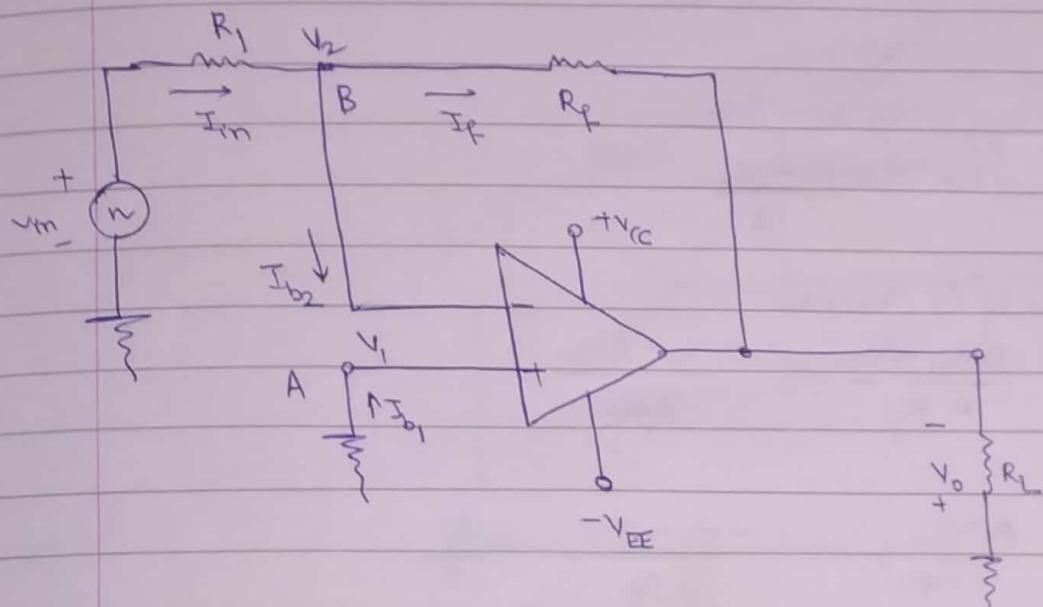
$$\frac{0 - V_{in}}{R_1} + \frac{0 - V_o}{R_f} = 0$$

$$\frac{-V_{in}}{R_1} - \frac{V_o}{R_f} = 0$$

$$\frac{V_o}{R_f} = \frac{-V_{in}}{R_1}$$

$$A = \text{Gain} = \frac{V_o}{V_{in}} = -\frac{R_f}{R_1}$$

* Practical Inverting Amplifiers



Expression for Voltage Gain

→ The closed loop vlg gain is denoted as A_{fg} , i.e., the ratio of op vlg to s/p vlg with feedback.

Apply KCL at node B,

$$I_{in} = I_f + I_{b2}$$

Input resistance $R_{in} \neq \infty$, it is very very large & hence $I_{b2} = 0$
 (negligible) & small can be neglected.

$$\therefore I_{in} \approx I_p$$

$$\frac{V_2 - V_{in}}{R_i} + \frac{V_2 - V_o}{R_f} = 0$$

$$\frac{V_{in} - V_2}{R_i} = \frac{V_2 - V_o}{R_f} \quad \text{--- (1)}$$

From eqⁿ ckt. of op-Amp, we can write

$$\begin{aligned} V_o &= A V_{id} \\ &= A(V_1 - V_2) \end{aligned}$$

$$V_1 = 0$$

$$V_o = -AV_2$$

$$\text{i.e. } V_2 = \frac{-V_o}{A}$$

So, eqⁿ(1) becomes

$$\frac{AV_{in} + V_o}{A R_i} = -\frac{V_o - AV_o}{A R_f}$$

$$\frac{AV_{in}}{R_i} = -\frac{V_o - AV_o}{R_f} - \frac{V_o}{R_i}$$

$$\frac{AV_{in}}{R_i} = -\frac{V_o(1-A)}{R_f} - \frac{V_o}{R_i}$$

$$R_f AV_{in} = -V_o R_i (1-A) - V_o R_f$$

$$R_f AV_{in} = -V_o (R_i - R_i A - R_f)$$

$$A_f = \frac{V_o}{V_{in}} = \frac{-R_f A}{R_1 + R_1 A - R_f}$$

$$A_f = \frac{+R_f A}{R_f + R_1(A-1)}$$

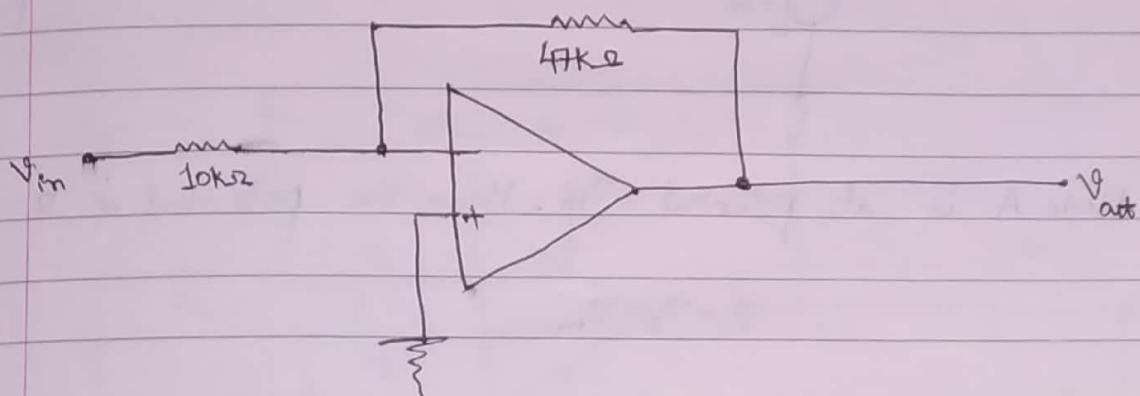
$$A_f = \frac{A}{1 + \frac{R_1}{R_f}(A-1)}$$

$\frac{V_o}{V_{in}}$	$= \frac{-AR_f}{R_f + R_1 + AR_1}$
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24.01.19(A)

Prob.

Determine the voltage gain of OP-Amp Ckt. as shown in figure.



Sol →

$$\frac{V_{out}}{V_{in}} = \frac{-47k\Omega}{10k\Omega} = -4.7 \text{ Ans}$$

Prob. For an inverting amplifier ckt., using OP-Amp, the desired voltage gain is -60. If R_1 is selected as 4.7kΩ. Select the proper value of R_f .

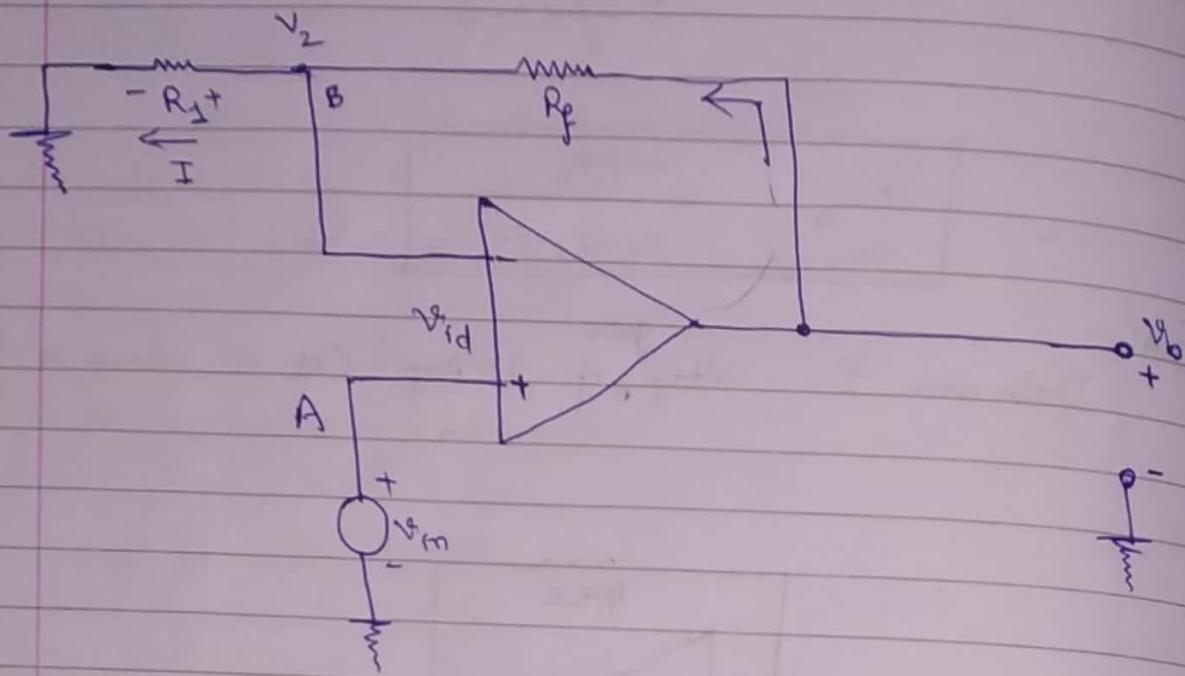
Sol →

$$-60 = \frac{-R_f}{R_1} \Rightarrow R_f = 60 \times 4.7 = 282k\Omega$$

Ans

* Ideal Non-Inverting Amplifier

→ An amplifier which amplifies the input without producing any phase-shift between input & output is called as non-inverting amplifier.



→ Node A is at potential V_m . Hence, the potential of B is

$$\therefore V_1 = V_2 = V_m$$

Apply KCL,

$$\frac{V_2 - 0}{R_1} + \frac{V_2 - V_o}{R_f} = 0$$

$$V_2 \left(\frac{1}{R_1} + \frac{1}{R_f} \right) = \frac{V_o}{R_f}$$

$$A = \frac{V_o}{V_m} = 1 + \frac{R_f}{R_1}$$

* Comparison of Inverting & Non-Inverting Amplifier

Inverting Amplifier

$$i) A = -\frac{R_f}{R_1}$$

$$ii) \text{Gain} = (-)ve$$

iii) Phase Shift of 180°
b/w i/p & o/p

iv) Voltage gain can be
adjusted as $>, =, < 1$.

v) I/p impedance = R_1

Non-Inverting Amplifier

$$i) A = 1 + \frac{R_f}{R_1}$$

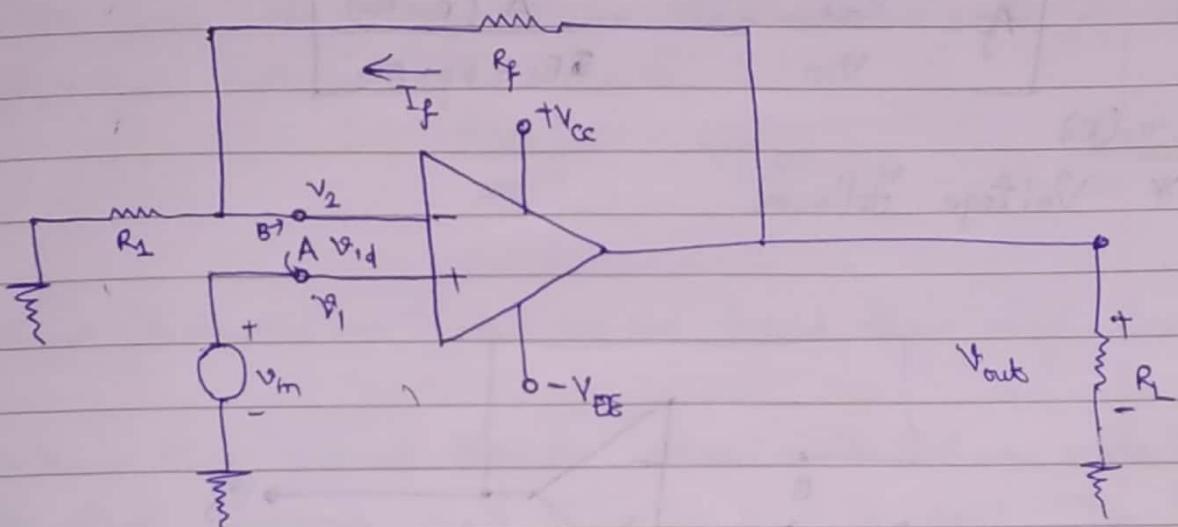
$$ii) \text{Gain} = (+)ve$$

iii) Phase shift of 0°
b/w i/p & o/p

iv) Voltage gain is always
greater than 1.

v) I/p impedance is extremely
large.

* Practical Non-Inverting Amplifier



→ The closed loop voltage gain is A_f which is the ratio of
o/p v_o to i/p v_m with feedback.

$$\therefore A_f = \frac{\text{v}_o}{\text{v}_m}$$

$$\begin{aligned} V_{\text{out}} &= A V_{\text{in}} \\ &= A(V_1 - V_2) \end{aligned} \quad \text{--- (1)}$$

$$V_1 = V_{\text{in}}$$

$$V_2 = V_f$$

Using voltage-divider rule,

$$V_f = \left(\frac{V_{\text{out}}}{R_1 + R_f} \right) R_1$$

$$V_{\text{out}} = A \left(V_{\text{in}} - \frac{R_1 V_{\text{out}}}{R_1 + R_f} \right)$$

$$V_{\text{out}} \left(1 + \frac{A R_1}{R_1 + R_f} \right) = A V_{\text{in}}$$

$$A_f = \frac{V_{\text{out}}}{V_{\text{in}}} = \frac{A (R_1 + R_f)}{R_1 + R_f + A R_1}$$

24.01.19 (B)

* Voltage Follower

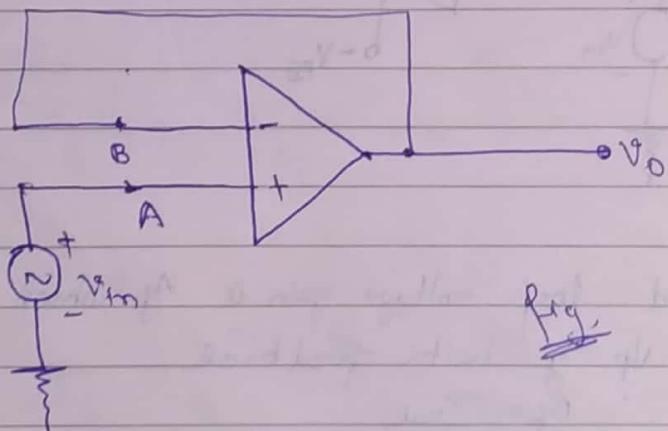


Fig.

→ Circuit in which the output voltage follows the input voltage is called as voltage follower circuit.

$$V_1 = V_2 = V_{in}$$

→ The node A is at potential V_{in} . Now, node B is also at the same potential.

$$\therefore V_A = V_B = V_{in}$$

— ①

Now, node B is directly connected to o/p, so,

$$V_{out} = V_B$$

— ②

From ① & ② +

$$V_{out} = V_{in}$$

→ For this ckt, voltage gain is unity.

→ It is also known as source follower, unity gain amplifier, buffer amplifier.

* Slew Rate for Inverting Amplifier

→ It may be defined as the maximum rate of change of output voltage with time.

$$S = \left. \frac{dV_{out}}{dt} \right|_{max.} \quad V/\mu s$$

$$\frac{dV_o}{dt} = \frac{I}{C}$$

Note → For distortionless o/p, OP-Amp should have high slew rate.

→ We know that internal capacitor voltage can't change suddenly.

→ for high charging rate, capacitor must be small. Therefore, the slew rate for the OP-Amp whose maximum internal capacitor charging current is known as

$$S = \frac{I_{max.}}{C}$$

* Slew Rate for Non-Inverting Amplifier

- Ideally must be infinite
- Higher Slew Rate, Better performance of OP-Amp
- Let the input voltage v_i is purely sinusoidal & the output voltage v_o will also be purely sinusoidal.

From fig., op vlg follows slp vlg. ∴ we have

$$v_m = v_m \sin \omega t$$

$$v_{out} = v_m \sin \omega t$$

$$S = \frac{dv_{out}}{dt} = v_m \omega \cos \omega t \quad (1)$$

But, $\left(\frac{dv_{out}}{dt} \right)_{max}$ is nothing but is slew rate for maximum $\cos \omega t$, i.e. 1.

$$\therefore S = v_m \omega$$

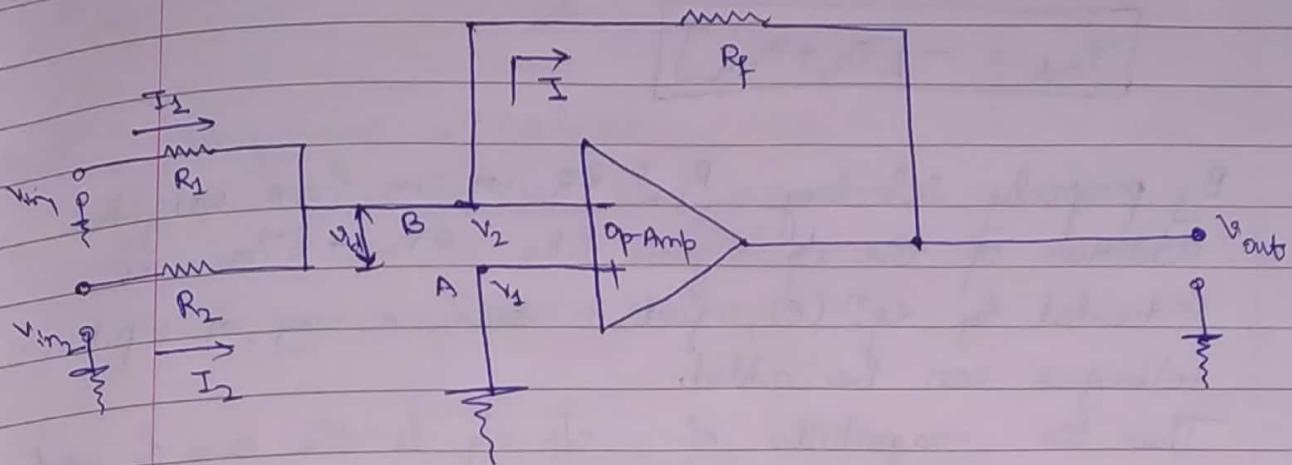
$$\textcircled{a} \quad S = v_m (2\pi f)$$

$$f_m = \frac{S}{2\pi v_m}$$

where, $f_m = \text{Max. frequency}$

* SUMMER/ADDER

Since, the input impedance of an OP-Amp is extremely large, more than one input signal can be applied to the inverting amplifier. Such ckt. gives the addition of applied signal at the output. Hence, it is called as Summer/adder as shown in figure.



→ At point A is grounded. Due to virtual ground concept, the node B is also grounded.

$$V_1 = V_2 = 0 \quad \text{--- (1)}$$

From (1),

$$I_1 = \frac{V_{in1} - V_2}{R_1} = \frac{V_{in1}}{R_1} \quad \text{--- (2)}$$

$$I_2 = \frac{V_{in2} - V_2}{R_2} = \frac{V_{in2}}{R_2} \quad \text{--- (3)}$$

$$I = I_1 + I_2 \quad \text{--- (4)}$$

Now, apply KCL at node B,

$$\therefore I = \frac{V_2 - V_{out}}{R_f} = -\frac{V_{out}}{R_f} \quad \text{--- (5)}$$

$$I = \frac{V_{in1}}{R_1} + \frac{V_{in2}}{R_2}$$

$$-\frac{V_{out}}{R_f} = \frac{V_{in1}}{R_1} + \frac{V_{in2}}{R_2}$$

$$V_{out} = \left[\frac{R_f}{R_1} V_{in1} + \frac{R_f}{R_2} V_{in2} \right] \quad \text{--- (6)}$$

If $R_f = R_1 = R_2$

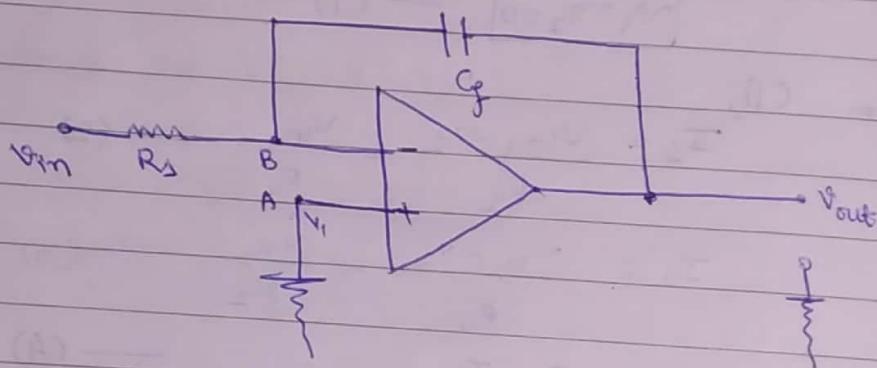
$$V_{out} = -[V_{in_1} + V_{in_2}]$$

By properly selecting $R_f, R_1 \& R_2$ we can have weighted addition of the o/p signals like $aV_{in_1} + bV_{in_2}$ as indicated by eq. (6), in fact, in such a way, n input voltages can be added.

Thus, the magnitude of o/p v/g is the sum of input voltages & hence ckt. is called as summer/adder ckt.

30.01.19

* ACTIVE OP-AMP INTEGRATOR



The node A is grounded & node B is also at the ground by the virtual ground condition.

$$V_1 = V_2 = 0$$

As i/p current of Op-Amp is zero, the entire current I flowing through R_1 is also flows through C_f from i/p side.

$$I = \frac{V_{in} - V_2}{R_1} = \frac{V_{in}}{R_1} \quad (1)$$

$$I = C_f \frac{d(V_2 - V_{out})}{dt} = -C_f \frac{dV_{out}}{dt} \quad (2)$$

Comparing eq. (1) & (2):

$$\frac{V_{in}}{R_1} = -C_f \frac{dV_{out}}{dt}$$

Integrating both the sides:

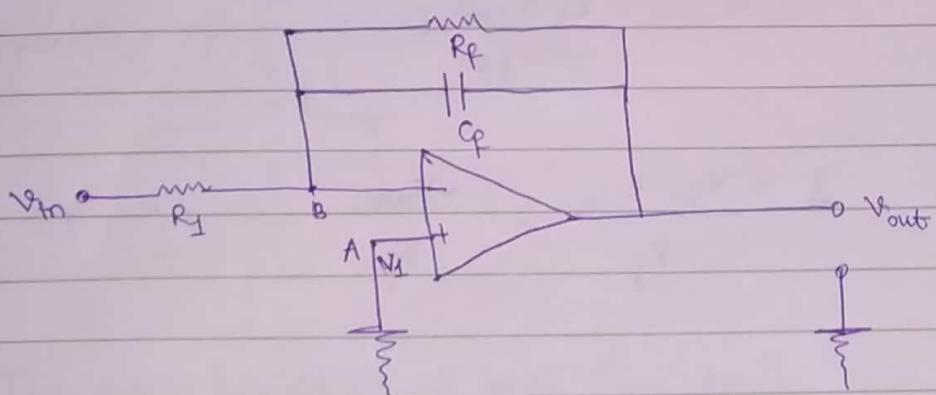
$$\int_0^t \frac{V_{in}}{R_1} dt = C_f \int \frac{dV_{out}}{dt} dt$$

$$\int_0^t \frac{V_{in}}{R_1} dt = -C_f V_{out}$$

$$V_{out} = \frac{-1}{C_f R_1} \int_0^t V_{in} dt + V_{out}(0) \quad (4)$$

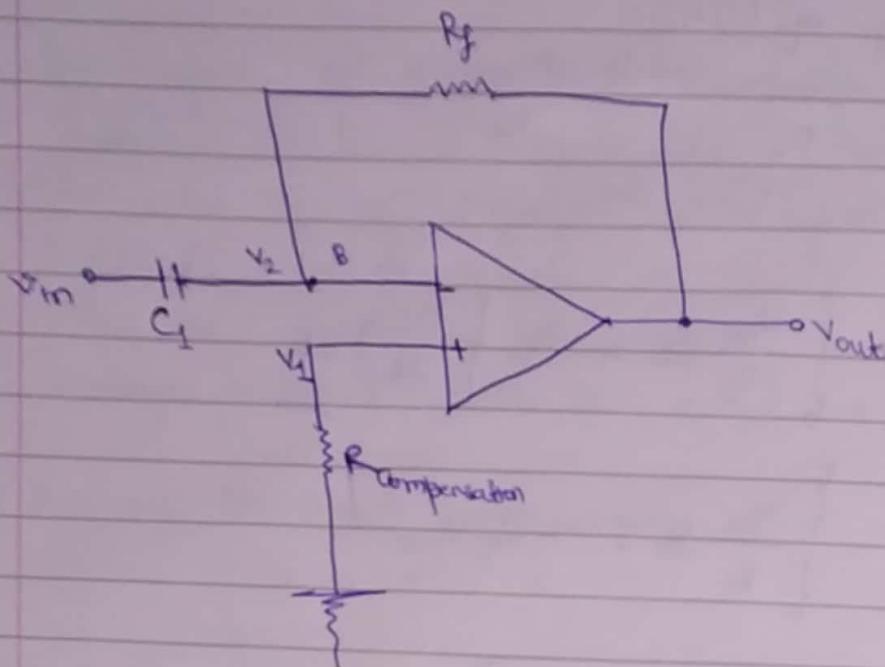
Eq. (4) shows that the o/p is $\frac{-1}{C_f R_1}$ times the integral of I/P & $R_1 C_f$ is called as time constant of the integrator.

* PRACTICAL OP-AMP INTEGRATOR



31.01.19

* ACTIVE OP-AMP DIFFERENTIATOR



Exchange the position of R and C from differentiator ckt. can be obtained from Integrator circuit.

As input current of OP-Amp is zero, entire current I_1 flows through R_f .

$$\begin{aligned} I_1 &= C_1 \frac{d}{dt} (V_{in} - V_2) \\ &= C_1 \frac{dV_{in}}{dt} \end{aligned}$$

$$\left\{ \begin{array}{l} V_2 = 0 \text{ (Virtual Ground)} \end{array} \right\} \quad (1)$$

$$I = \frac{V_2 - V_{out}}{R_f} = \frac{-V_{out}}{R_f} \quad (2)$$

Comparing eq. (1) & (2),

$$C_1 \cdot \frac{dV_{in}}{dt} = -\frac{V_{out}}{R_f} \quad \text{--- (3)}$$

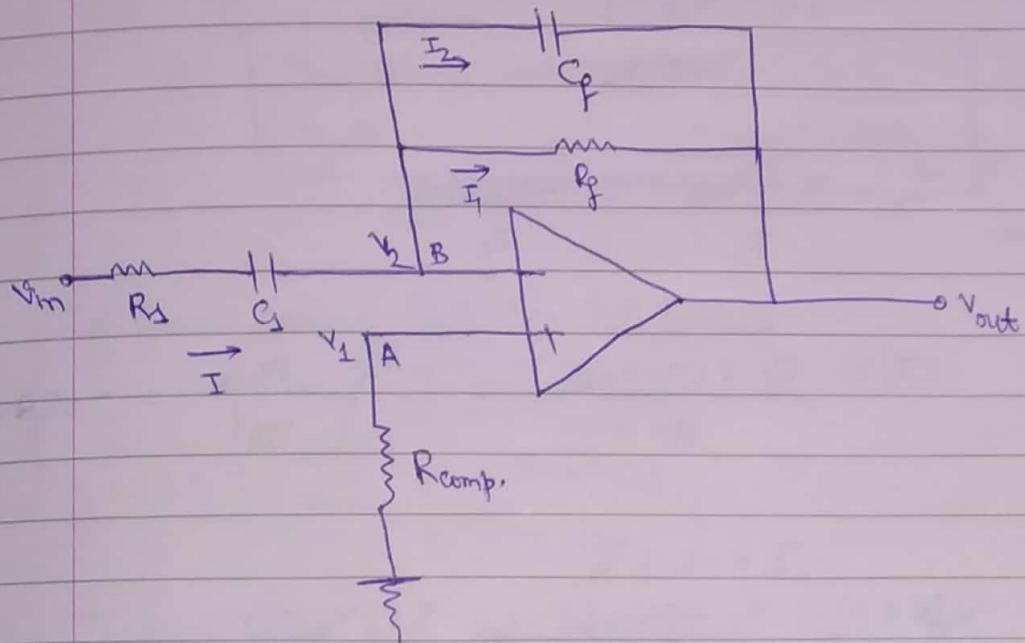
$$V_{out} = -C_1 R_f \frac{dV_{in}}{dt}$$

--- (4)

This eq. shows that output is $C_1 R_f$ times the differentiation of input voltage. Product $C_1 R_f$ is called time constant of the differentiator.

The main advantage of such an active differentiator is the small time constant required for differentiation.

* PRACTICAL Op-Amp DIFFERENTIATOR



→ The noise & stability at high freq. can be corrected in the

practical differentiator ckt. using the resistance R_1 in series with C_1 & capacitor C_f in parallel with resistance R_f .

R_{comp} is used for voice compensation.

For current I , $I = I_1 + I_2$

$$I = \frac{V_2 - V_m}{Z_1} = \frac{V_m}{Z_1} \quad (\because V_2 = 0, \text{Virtual Ground}) \quad (1)$$

where, $Z_1 = R_1$ in series with C_1

So, in Laplace domain we can write

$$\begin{aligned} Z_1 &= R_1 + \frac{1}{SC_1} \\ &= \frac{1 + SC_1 R_1}{SC_1} \end{aligned} \quad (2)$$

$$\therefore I = \frac{V_m(s) SC_1}{1 + SC_1 R_1} \quad (3)$$

$$I_1 = \frac{V_2 - V_{out}}{R_f} = \frac{-V_{out}(s)}{R_f}$$

$$I_2 = \frac{C_f d(V_2 - V_{out})}{dt} = -C_f \frac{dV_{out}}{dt} = -SC_f V_{out}(s)$$

$$\begin{aligned} I &= I_1 + I_2 \\ \frac{V_m(s) SC_1}{1 + SC_1 R_1} &= -\frac{V_{out}(s)}{R_f} - S C_f V_{out}(s) \end{aligned}$$

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{-SC_1}{1 + SC_1 R_f} \times \left(\frac{1}{R_f} + SC_F \right)$$

$$= \frac{-SC_1}{1 + SC_1 R_f} \times \frac{1 + SC_F R_f}{R_f}$$

$$= \frac{-SC_1 R_f}{(1 + SC_1 R_f)(1 + SC_F R_f)}$$

$\frac{V_{out}(s)}{V_{in}(s)} =$	$\frac{-SC_1 R_f}{1 + S(C_1 R_f + C_F R_f) + S^2 C_1 R_f C_F R_f}$
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If $R_f C_F = R_1 C_1$, then we have

$\frac{V_{out}(s)}{V_{in}(s)} =$	$\frac{-SC_1 R_f}{1 + S^2 C_1 R_f C_F R_f + 2SC_F R_f}$
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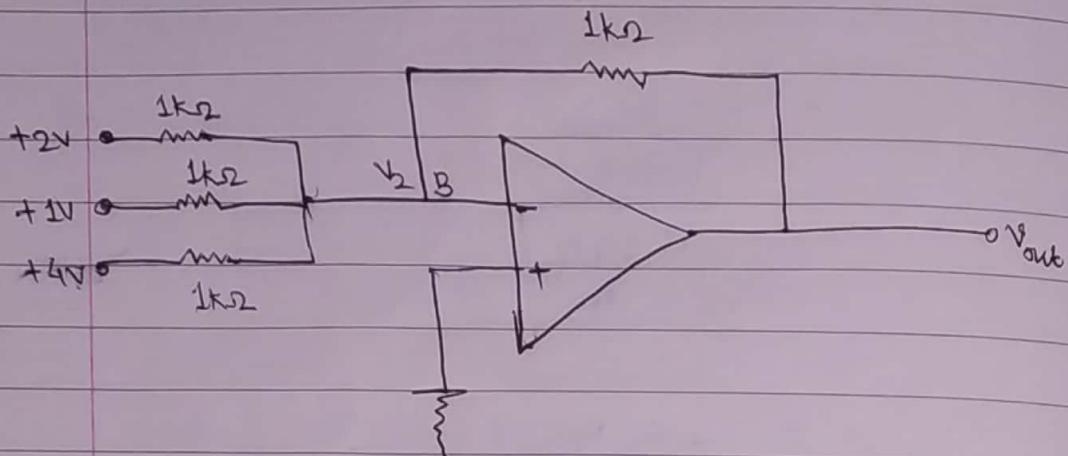
If time constants $R_f C_F \gg R_1 C_1$ or $R_f C_F \gg R_1 C_1$

$$\therefore \left\{ \frac{V_{out}(s)}{V_{in}(s)} = -SC_1 R_f \right\}$$

Taking I.L.T. on both the sides

$$V_{out}(t) = -R_f C_1 \frac{dV_{in}}{dt}$$

Prob: Determine the output voltage for configuration shown in figure:



$$\text{Ans} \rightarrow \frac{V_{\text{out}} - V_2}{1k\Omega} = I$$

$$I = \frac{V_{\text{out}}}{1k}$$

~~$$I = -\left(\frac{2}{1k} + \frac{1}{1k}\right) + \frac{4}{1k}$$~~

$$I = -\left\{\left(2/1k\right) + \left(1/1k\right) + \left(4/1k\right)\right\}$$

$$I = -7/1k$$

$$V_{\text{out}} = -7V \quad \text{Ans}$$

* VOLTAGE TO CURRENT CONVERTOR

- 1) Floating Type
- 2) Grounded Type

→ In floating type V to I converter, R_L is not connected to the ground.

- In ground type, one end of R_L is connected to ground.
- V to I converter with floating load

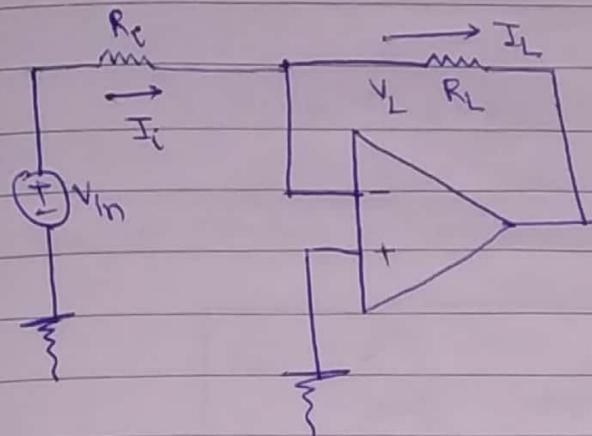


Fig. (a)

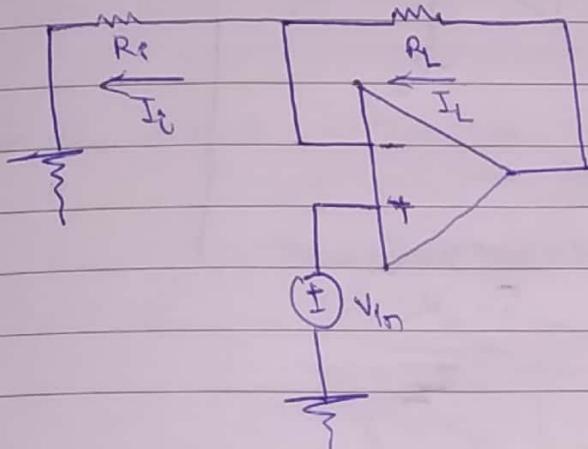


Fig. (b)

$$I_L = I_E = \frac{V_{in}}{R_1}$$

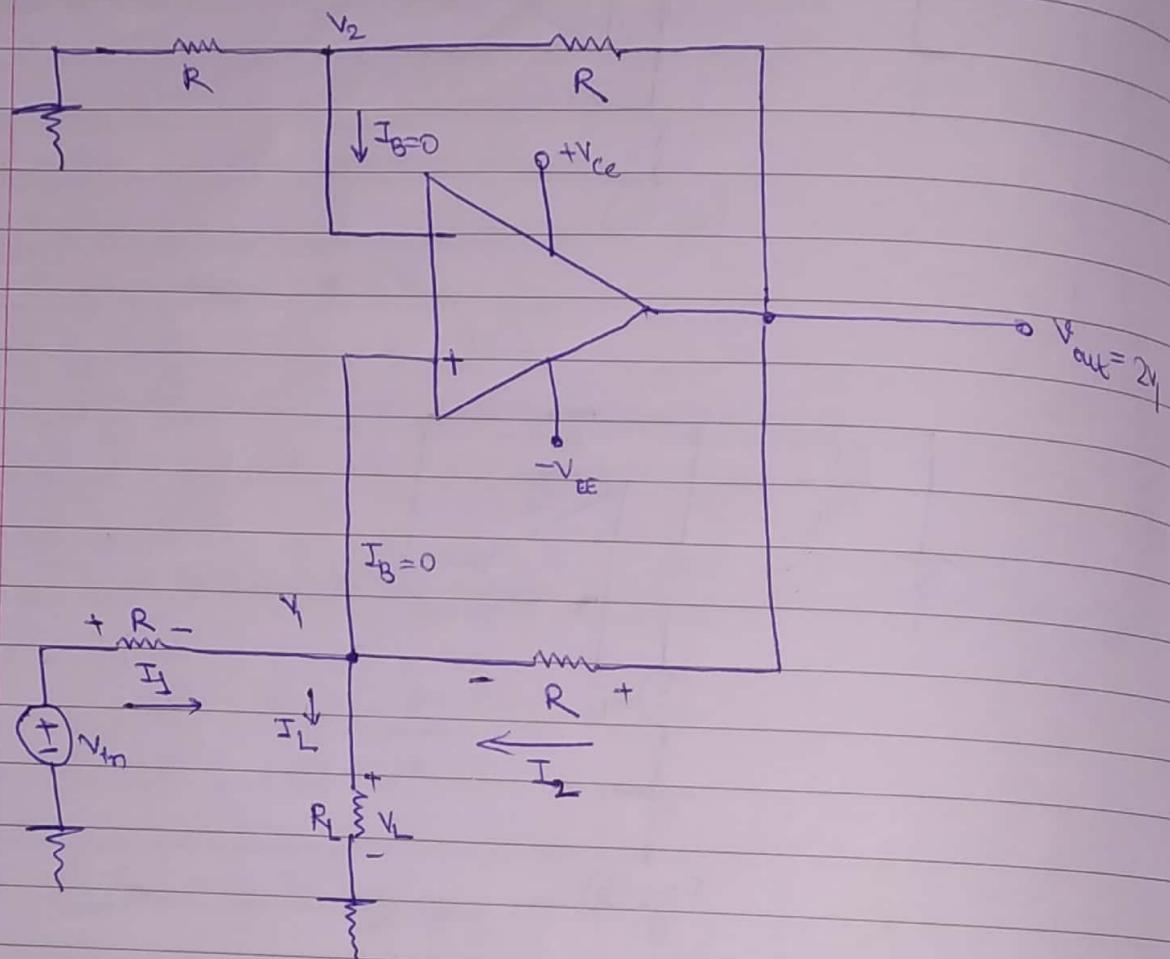
$I_L \propto V_{in}$

— (1)

As input current of OP-Amp is zero, thus, the load current is always proportional to input voltage & circuit works

as voltage to current converter.

→ V to I converter with grounded load



First determining voltage V_1 at non-inverting terminal & then the relationship between V_1 & the load current is taken out.

Apply KCL at node of V_1 ,

$$I_1 = I_1 + I_2$$

$$I_L = I_1 + I_2 \\ = \frac{V_{in} - V_1}{R} + \frac{V_{out} - V_1}{R}$$

$$R I_L = V_{in} + V_{out} - 2V_1$$

$$V_1 = \frac{V_{in} + V_{out} - R I_L}{2} \quad (1)$$

The gain of OP-Amp in non-inverting mode,

$$A = 1 + \frac{R_f}{R_i}$$

$$= 1 + \frac{R}{R}$$

$$= 1+1 \\ \boxed{A = 2}$$

Hence, the output voltage is $V_{out} = 2V_1 = V_{in} + V_{out} - R I_L$

$$V_{out} = V_{in} + V_{out} - R I_L$$

$$0 = V_{in} - R I_L$$

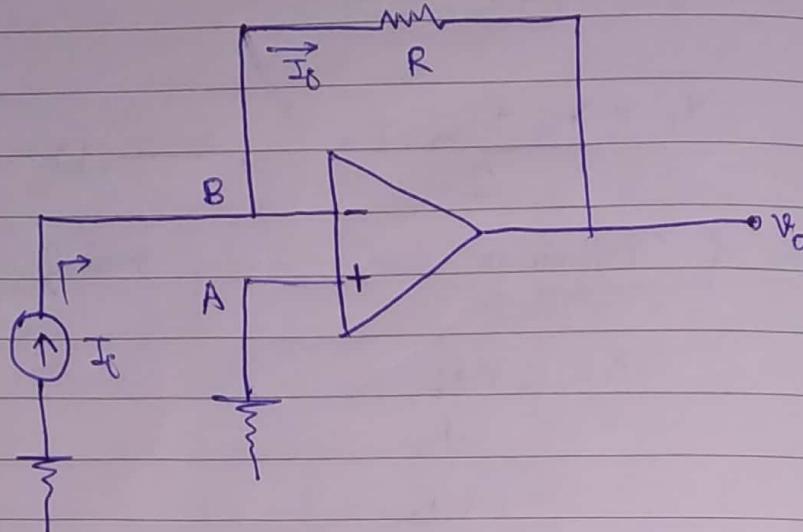
$$V_{in} = I_L R$$

$$\boxed{I_L = \frac{V_{in}}{R}}$$

* CURRENT TO VOLTAGE CONVERTER

- 1) Floating Type
- 2) Grounded Type

→ I to V converter with grounded load



$$V_B = 0$$

* Node B is virtual ground as node A is grounded, i.e.,
 $V_B = 0$,

$$\therefore I_i = \frac{V_B - V_{out}}{R} = -\frac{V_{out}}{R} \quad \text{--- (1)}$$

$$V_{out} = -I_i R$$

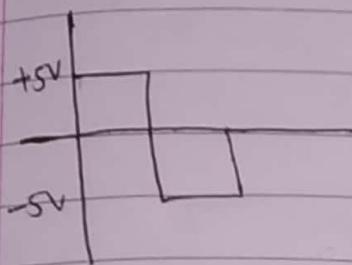
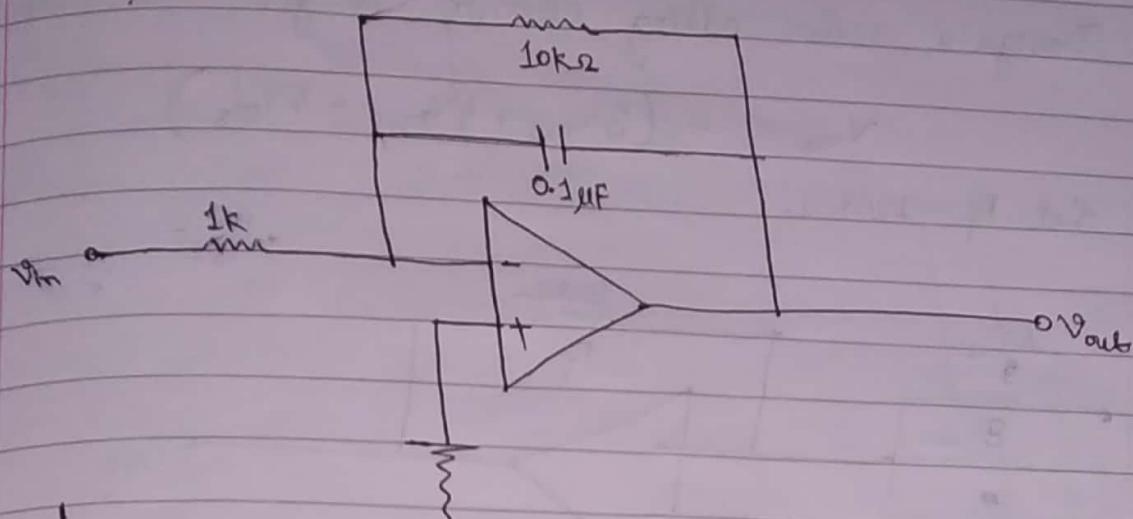
(D)

$$V_{out} \propto I_i \quad \text{--- (2)}$$

Ckt. works as current to voltage converter. This ckt. is also known as current controlled voltage source (CCVS).

If the resistance in ckt. is replaced by impedance z , ckt. is called trans-impedance amplifier.

01.02.19
Prob:



In the output voltage. Determine the slew rate.

$$f = 1 \text{ kHz}$$

$$T = \frac{1}{f} = 1 \text{ ms}$$

$$\Delta V_{\text{out}} = V_{\text{in}} T$$

$$\begin{aligned} &= \frac{2R_1 C_f}{2 \times 10^3 \times 0.1 \times 10^{-6}} \\ &= 5(10^{-3}) \end{aligned}$$

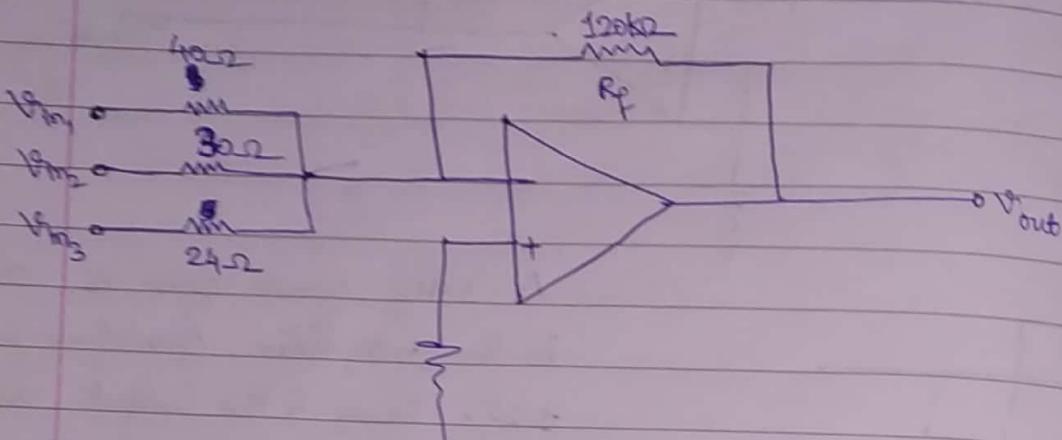
$$= 25 \text{ V} \quad \underline{\text{Ans}}$$

$$\begin{aligned} \text{Slew Rate} &= 2\pi f_m V_m \xrightarrow{\text{I/P Max V/g}} \\ &= 2\pi(10^3)(25) / \text{second} \\ &= 157 \text{ kV/s} \quad 31.41 \text{ kV/s} \\ &\approx 0.03141 \text{ V/μs} \quad \underline{\text{Ans}} \end{aligned}$$

Prob: Design a scalar adding circuit to give the output:

$$V_{out} = -(3V_{in_1} + 4V_{in_2} + 5V_{in_3})$$

Let $R_f = 120\text{k}\Omega$.



$$\frac{R_f}{R_1} = 3$$

$$R_1 = 40\text{k}\Omega$$

$$\frac{R_f}{R_2} = 4$$

$$R_2 = 30\text{k}\Omega$$

$$\frac{R_f}{R_3} = 5$$

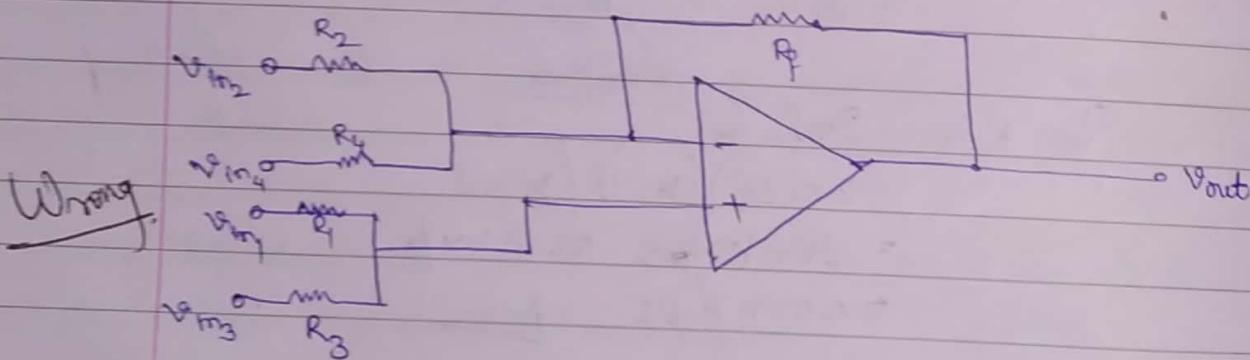
$$R_3 = 24\text{k}\Omega$$

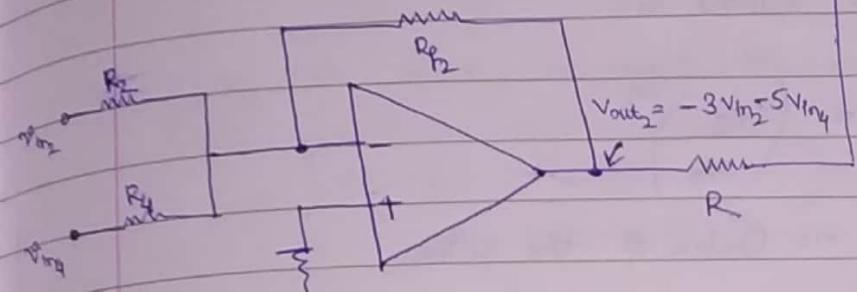
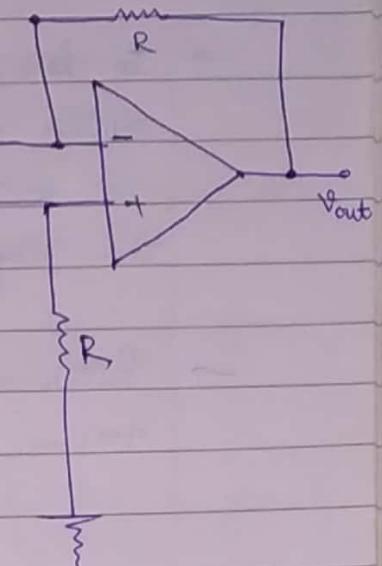
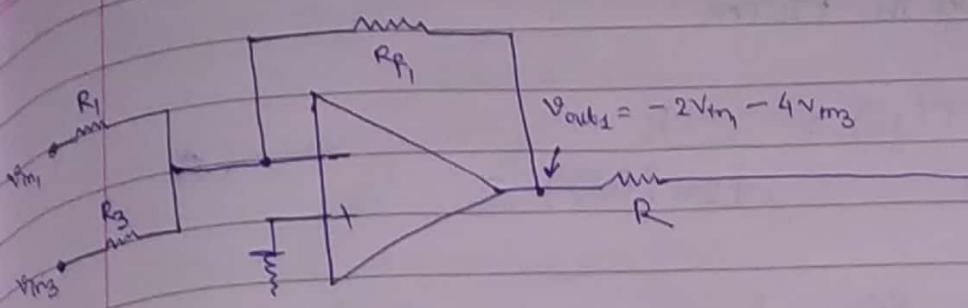
Prob: Design an Op-Amp ckt. which can give the output as

$$V_{out} = 2V_{in_1} - 3V_{in_2} + 4V_{in_3} - 5V_{in_4}$$

Sol:

$$V_{out} = (2V_{in_1} + 4V_{in_3}) - (3V_{in_2} + 5V_{in_4})$$





$$\begin{aligned}
 V_{out} &= V_{out_2} - V_{out_1} \\
 &= -3V_{in_2} - 5V_{in_4} - (-2V_{in_1} - 4V_{in_3}) \\
 &= 2V_{in_1} + 4V_{in_3} - 3V_{in_2} - 5V_{in_4}
 \end{aligned}$$

Prob. For a practical integrator, the component values are $R_1 = 120\text{k}\Omega$, $R_f = 1.2\text{M}\Omega$ and $C_f = 10\text{nF}$. i) Draw the circuit diagram. ii)

Determine the safe frequency above which true integration will take place. iii) Determine the d.c. gain. iv) Find the peak of the output voltage for a sine wave input with 5V peak & 10kHz frequency.

06.02.19

* BUTTERWORTH FILTER

$$T(j\omega) = \frac{k}{[1 + f(\omega)]^{1/2}} \quad (1)$$

- In low pass filter design, assuming all the zeros of the system function are at infinity, amplitude function can be written as eq.(1), where, k = d.c. gain constant as it is the magnitude at $\omega=0$.
- Butterworth suggested that the polynomial for the amplitude response can be selected as:

$$f(\omega^2) = \left(\frac{\omega}{\omega_0} \right)^{2n}$$

where, n = Order of the filter.

Let $R=1$, then, the amplitude function can be written as

$$T(j\omega) = \frac{1}{[1 + f(\omega)]^{1/2}}$$

$$\therefore T(j\omega) = \frac{1}{\left[1 + \left(\frac{\omega}{\omega_0} \right)^{2n} \right]^{1/2}} \quad (2)$$

- To get normalised response for LPF, assume that the frequency is normalised such that $\omega_0 = 1$, then, the response function is given by

$$T(j\omega) = \frac{1}{[1 + \omega^{2n}]^{1/2}} \quad \text{--- (3)}$$

→ The response function given in eq. (3) is called n^{th} order Butterworth response.

- Properties of Butterworth Filter

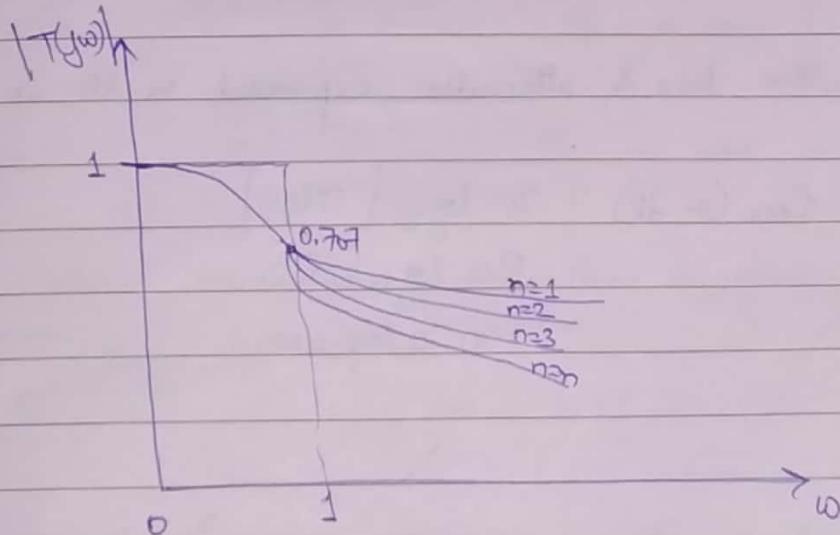
- For any value of n , at $\omega=0$, the amplitude function is given by

$$|T(j0)| = \frac{1}{(1 + (0)^{2n})^{1/2}} = 1 \quad [\text{For all } n]$$

- For any value of n , at $\omega=1$, the amplitude function is given by

$$|T(j1)| = \frac{1}{(1 + (1)^{2n})^{1/2}} = \frac{1}{\sqrt{2}} = 0.707 \quad [\text{for all } n]$$

- As the order of the filter increases, the approximate characteristic approaches to the ideal characteristics. This clearly indicates that for higher values of n or higher orders filter approximation is better for large ω .



v) Using Binomial series expansion, we can rewrite equation no. 12

$$|T(j\omega)| = \frac{1}{(1+\omega^{2n})^{1/2}} = (1+\omega^{2n})^{-1/2}$$

$$= 1 - \frac{1}{2} \omega^{2n} + \frac{3}{8} \omega^{4n} - \frac{5}{16} \omega^{6n} + \dots$$

vi) In the pass band, the value of ω^{2n} should be very small compared to 1, then the amplitude function can be written as:

$$|T(j\omega)| \approx 1$$

While in the stop band, ω^{2n} should be much greater than 1, then the amplitude function decreases as ω increases.

vii) In stop band, $\omega^{2n} \gg 1$, then the amplitude response can be written as

$$|T(j\omega)| = \frac{1}{(\omega^{2n})^{1/2}} = \frac{1}{\omega^n} = \omega^{-n} \quad (5)$$

where, n = order of the filter

Then, the loss & attenuation expressed in dB is given by

$$\begin{aligned} \text{Loss (in dB)} &= 20 \log_{10} |T(j\omega)| \\ &= 20 \log_{10} (\omega^{-n}) \\ &= -n 20 \log_{10} \omega \end{aligned} \quad (6)$$

Transfer function of Butterworth Filter

The amplitude function for the Butterworth filter is given by

$$|T(j\omega)| = \frac{1}{(1+\omega^{2n})^{1/2}}$$

$$\therefore |T(j\omega)|^2 = \frac{1}{(1+\omega^{2n})} = \frac{N(s)}{D(s)}$$

The poles of the function can be obtained by equating denominator polynomial to zero. Hence,

$$D(s) = (1+\omega^{2n}) = 0$$

$$\text{Here, } \omega = \frac{s}{j}$$

$$\text{So, } D(s) = 1 + \left(\frac{s}{j}\right)^{2n} = 0$$

$$1 + (-js)^{2n} = 0 \quad 1 + (-s^2)^n = 0 \quad -(7)$$

$$1 + j^{2n} s^{2n} = 0$$

$$1 + (js)^{2n} = 0$$

Then, the pole location for amplitude function is given by

$$s_k = e^{j\left(\frac{(2k-1)\pi}{n}\right)} \quad , \text{if } n \text{ even} \quad \left. \begin{array}{l} \\ \end{array} \right\} -(8)$$

$$e^{j\left[\frac{2k\pi}{n}\right]\frac{\pi}{2}} \quad , \text{if } n \text{ odd}$$

Combining above results, the pole location in general are given by

$$s_k = e^{j\left(\frac{2k+n-1}{2n}\right)\pi} \quad , \text{where, } k = 1, 2, \dots, n \quad -(9)$$

But, the complex frequency variable s can be expressed in terms

of real part & imaginary part.

$$s_k = \sigma_k + j\omega_k$$

$$\text{where, } \sigma_k = \cos\left(\frac{2k+n-1}{2n}\pi\right) = \sin\left(\frac{2k-1}{n}\pi\right)$$

$$\& \omega_k = \sin\left(\frac{2k+n-1}{2n}\pi\right) = \cos\left(\frac{2k-1}{n}\pi\right)$$

From eq.(8) & (9), it is observed that all the poles are located at unit circle in the S-plane, then, the transfer function for the Butterworth filter for different-ordered filters is given by

$$T(s) = \frac{1}{(s-s_1)(s-s_2)(s-s_3)\dots} \quad (10)$$

07.02.19

- First Order Butterworth Filter

$n=1$ & $R=1$ putting in eq. (9),

$$s_1 = e^{j\left(\frac{\frac{2(1)+1-1}{2(1)} - \frac{\pi}{2}}{2(1)}\right)\pi}$$

$$\text{i.e., } s_1 = e^{j\pi}$$

$$s_1 = \cos\pi + j\sin\pi$$

$$\boxed{s_1 = -1}$$

Putting the value of s_1 in eq.(10) +

$$T(s) = \frac{1}{s - (-1)} = \frac{1}{s+1}$$

Second Order Filter

$$n=2, k=1, 2$$

$$n=2, k=1$$

$$s_1 = e^{j\left(\frac{2(0)+2-1}{2(2)}\pi\right)}$$

$$\text{i.e. } s_1 = e^{j\frac{3\pi}{4}}$$

$$= \cos(3\pi/4) + j \sin(3\pi/4)$$

$$= -\frac{1}{\sqrt{2}} + j \frac{1}{\sqrt{2}}$$

$$s_1 = -\frac{1+j}{\sqrt{2}}$$

$$n=2, k=2$$

$$s_2 = e^{j\left(\frac{2(2)+2-1}{2(2)}\pi\right)}$$

$$= e^{j5\pi/4}$$

$$= \cos 5\pi/4 + j \sin 5\pi/4$$

$$= -\frac{1}{\sqrt{2}} - j \frac{1}{\sqrt{2}}$$

$$s_2 = -\frac{(1+j)}{\sqrt{2}}$$

Putting these value in eq. (10)†

~~$$T(s) = \frac{1}{s+1}$$~~

~~$$(s+1-j)(s+1+j)$$~~

~~$$\text{i.e. } T(s) =$$~~

~~$$\frac{2}{(j+(s-1))(j+(s+1))}$$~~

~~$$\frac{2}{(s+(j-1))(s+(j+1))}$$~~

~~$$= \frac{2}{s^2 - (j-1)^2}$$~~

~~$$= \frac{2}{s^2 + 2s + 1 + 1}$$~~

~~$$= \frac{2}{s^2 - (j^2 + 1 - 2j)}$$~~

~~$$= \frac{2}{s^2 + 2s + 2}$$~~

~~$$= \frac{2}{s^2 + 2j}$$~~

Putting these value in eq. (10) \downarrow

$$T(s) = \frac{1}{(s + \frac{1}{\sqrt{2}} - j\frac{1}{\sqrt{2}})(s + \frac{1}{\sqrt{2}} + j\frac{1}{\sqrt{2}})}$$

$$= \frac{1}{\left(\frac{s+1}{\sqrt{2}}\right)^2 - \left(\frac{j}{\sqrt{2}}\right)^2}$$

$$= \frac{1}{s^2 + \frac{1}{2} + \sqrt{2}s + \frac{1}{2}}$$

$$\therefore T(s) = \frac{1}{s^2 + \sqrt{2}s + 1}$$

• Third Order Filter

$$n=3; K=1, 2, 3$$

$$s_1 = e^{j\left(\frac{2(0)+3-1}{2(3)}\right)\pi} \\ = e^{j\frac{2\pi}{3}}$$

$$= \cos\left(\frac{2\pi}{3}\right) + j \sin\left(\frac{2\pi}{3}\right)$$

$$= \frac{-1}{2} + j \frac{\sqrt{3}}{2}$$

$$s_1 = \frac{\sqrt{3}j - 1}{2}$$

$$s_2 = e^{j\left(\frac{2(2)+3-1}{2(3)}\right)\pi}$$

$$= e^{j\pi}$$

$$s_2 = -1$$

$$\begin{aligned}
 s_3 &= e^{\int \left(\frac{2(s)+3-1}{2(s)} \right) \pi} \\
 &= e^{\int 4\pi/3} \\
 &= \cos 4\pi/3 + j \sin 4\pi/3 \\
 &= -\frac{1}{2} - j \frac{\sqrt{3}}{2}
 \end{aligned}$$

$$\boxed{s_3 = -\frac{(1-\sqrt{3}j)}{2}}$$

$$\begin{aligned}
 T(s) &= \frac{1}{\left(s + \frac{1-\sqrt{3}j}{2}\right)(s+1)\left(s + \frac{1+\sqrt{3}j}{2}\right)} \\
 &= \frac{1(4)}{(2s+1-\sqrt{3}j)(s+1)(2s+1+\sqrt{3}j)} \\
 &= \frac{4}{(s+1)((2s+1)^2 - (\sqrt{3}j)^2)} \\
 &= \frac{4}{(s+1)(4s^2 + 4s + 1 + 3)} \\
 &= \frac{4}{(s+1)(4s^2 + 4s + 4)} \\
 &= \frac{1}{(s+1)(s^2 + s + 1)} \\
 &= \frac{1}{s^3 + s^2 + s + s^2 + s + 1} \\
 \boxed{T(s) = \frac{1}{s^3 + 2s^2 + 2s + 1}}
 \end{aligned}$$

Generalised Transfer Function for Butterworth LPF

$$T(s) = \frac{1}{a_n s^n + a_{n-1} s^{n-1} + a_{n-2} s^{n-2} + \dots + a_1 s + 1}$$

- * Some important observations of Butterworth polynomial are:
- i) Coefficient of the highest power of s is always one for any order of filter.
 - ii) Lowest order term i.e. constant is always one for any order of filter.
 - iii) For all odd order filters, one of the factors is always $(s+1)$, while the remaining factors are quadratic in nature.
 - iv) For all even order filters, all factors are quadratic in nature.
 - v) All the poles of Butterworth polynomial are located in left half of s -plane on a circle with radius equal to one & centre at origin.

→ The polynomial in the denominators of the above equation is known as Butterworth polynomial. For different order filters, Butterworth polynomial factored form are as given in Table (1).

n	
1	$(s+1)$
2	$(s^2 + \sqrt{2}s + 1)$
3	$(s^2 + s + 1)(s + 1)$
4	$(s^2 + 0.76536s + 1)(s^2 + 1.84776s + 1)$
5	$(s+1)(s^2 + 0.6180s + 1)(s^2 + 1.6180s + 1)$
6	$(s^2 + 0.5176s + 1)(s^2 + \sqrt{2}s + 4)(s^2 + 1.9318s + 1)$
7	$(s+1)(s^2 + 0.4450s + 1)(s^2 + 1.2456s + 1)(s^2 + 1.8022s + 1)$
8	$(s^2 + 0.3986s + 1)(s^2 + 1.11405s + 1)(s^2 + 1.6630s + 1)(s^2 + 1.9620s + 1)$

Note: For Chebyshen Approximations, refer Pg.no.66 to Pg.no.72.

4. OPERATIONAL AMPLIFIER

(B)

- * **Chebyshev Approximation**
 - Let us consider an approximation which ripples about the normalised magnitude i.e. unity in the passband, & the magnitude decreases very rapidly in the stop band, beyond the cut-off frequency ω_0 . This approximation can be realised using the Chebyshev cosine polynomials, hence the approximation is called Chebyshev approximation.
 - This approximation is equally good at $\omega=0$ & $\omega=1$. Thus, Chebyshev approximation which ripples about the normalised magnitude is also called equal ripple approximation.
 - The Chebyshev cosine polynomial of n^{th} order is defined as
- $$\begin{aligned} C_n(\omega) &= \cos(n \cos^{-1}\omega) \quad \text{in pass band, i.e. } |\omega| \leq 1. \\ &= \cos n(\cos^{-1}\omega) \quad \text{in stop band, i.e. } |\omega| > 1 \end{aligned} \quad \text{①}$$
- The higher order polynomials can be obtained easily by using recursive formula given as
- $$C_n(\omega) = 2\omega C_{n-1}(\omega) - C_{n-2}(\omega) \quad \text{②}$$

Let us find Chebyshev cosine polynomials for different values of n :

$$n=0 ; C_0(\omega)=1$$

$$n=1 ; C_1(\omega)=\omega$$

$$n=2 ; \text{ Using recursive formula given in eq. ②,}$$

$$C_2(\omega) = 2\omega C_1(\omega) - C_{2-2}(\omega) = 2\omega C_1(\omega) - C_0(\omega)$$

Substituting values of $C_1(\omega)$ & $C_0(\omega)$, we get

$$C_2(\omega) = 2\omega C_1(\omega) - 1 = 2\omega^2 - 1$$

$n=3$, using recursive formula,

$$\begin{aligned} C_3(\omega) &= 2\omega C_{3-1}(\omega) - C_{3-2}(\omega) \\ &= 2\omega C_2(\omega) - C_1(\omega) \end{aligned}$$

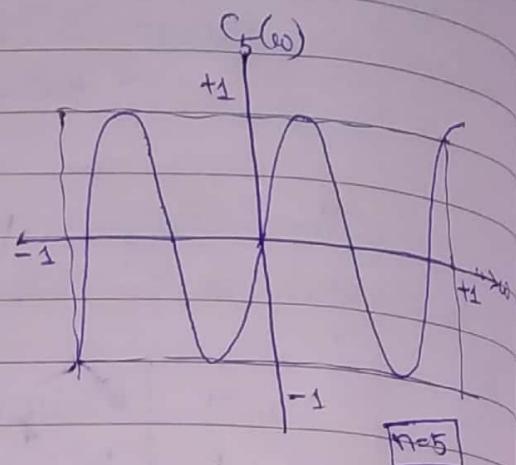
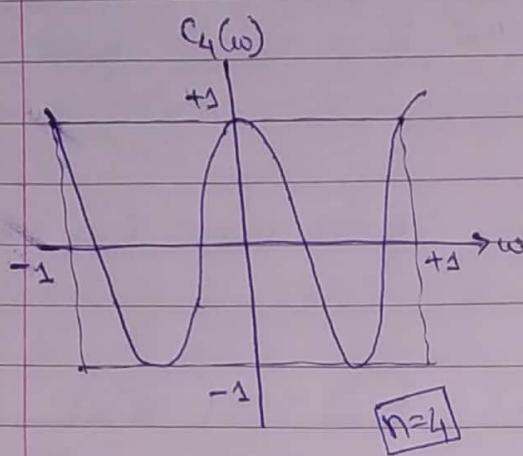
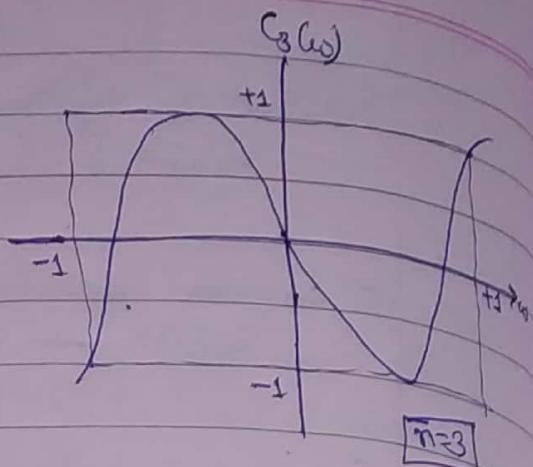
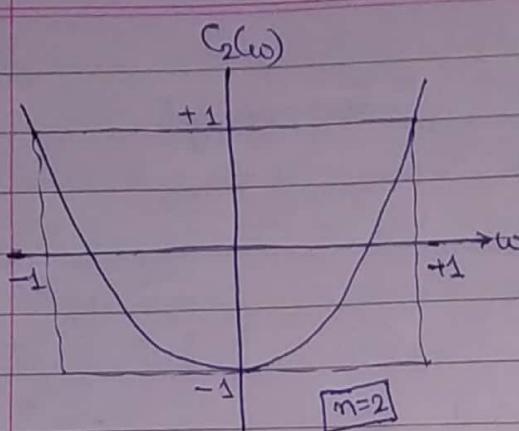
Substituting values of $C_2(\omega)$ & $C_1(\omega)$, we get

$$\begin{aligned} C_3(\omega) &= 2\omega(2\omega^2 - 1) - \omega = 4\omega^3 - 2\omega - \omega \\ &= 4\omega^3 - 3\omega \end{aligned}$$

The Chebyshev polynomials for different values of n are as given in the table.

n	Chebyshev Polynomials : $C_n(\omega) = \cos(n \cos^{-1} \omega)$
0	1
1	ω
2	$2\omega^2 - 1$
3	$4\omega^3 - 3\omega$
4	$8\omega^4 - 8\omega^2 + 1$
5	$16\omega^5 - 20\omega^3 + 5\omega$
6	$32\omega^6 - 48\omega^4 + 18\omega^2 - 1$
7	$64\omega^7 - 112\omega^5 + 56\omega^3 - 7\omega$
8	$128\omega^8 - 256\omega^6 + 160\omega^4 - 32\omega^2 + 1$
9	$256\omega^9 - 576\omega^7 + 432\omega^5 - 120\omega^3 + 9\omega$
10	$512\omega^{10} - 1280\omega^8 + 1120\omega^6 - 400\omega^4 + 50\omega^2 - 1$

→ The behaviour of Chebyshev polynomial with the variation of ω is as shown in figure:



→ Some important properties of Chebyshev polynomials useful in low pass filter approximation are as follows:

- (1) From the plots of Chebyshev polynomials, it is clear that the zeros of the polynomials are located in the interval $w = -1$ to $w = +1$, that is, $|w| \leq 1$.
- (2) Within the interval from $w = -1$ to $w = +1$, the magnitude of Chebyshev polynomial is always less than or equal to unity, i.e., $|C_n(w)| \leq 1$ for $|w| \leq 1$.
- (3) Outside interval $|w| \leq 1$, magnitude of Chebyshev polynomial rapidly increases with increase in w .

Consider the function $\epsilon^2 C_n^2(w)$, where, ϵ is the real number which is very small compared to unity. As seen from

above properties, $\epsilon^2 C_n^2(\omega)$ will vary between 0 & ϵ^2 in the interval $|\omega| \leq 1$, as $C(\omega) = 1$. Let us add 1 to this function, making it $1 + \epsilon^2 C_n^2(\omega)$. The new function will vary between 1 & $1 + \epsilon^2$ for $|\omega| \leq 1$, where, $(1 + \epsilon^2)$ is slightly greater than 1. Inverting this new function & relating it to the square of the magnitude, we get

$$|T(j\omega)|^2 = \frac{1}{1 + \epsilon^2 C_n^2(\omega)} \quad \rightarrow ③$$

The distance between maximum & minimum in the passband is called ripple height & it is given by

$$\text{Ripple} = 1 - \frac{1}{\sqrt{1 + \epsilon^2}} \quad \rightarrow ④$$

In the stop-band, i.e., for $|\omega| > 1$, as ω increases $\epsilon^2 C_n^2(\omega)$ becomes very large as compared to 1, then,

$$|T(j\omega)|^2 = \frac{1}{\epsilon^2 C_n^2(\omega)}$$

$$\therefore |T(j\omega)|^2 \approx \frac{1}{\epsilon C_n(\omega)} \quad \rightarrow ⑤$$

In the stop-band, the loss or attenuation expressed in dB is given by

$$\text{Loss} = -20 \log_{10} |T(j\omega)|$$

$$\therefore \text{Loss} = -20 \log_{10} \frac{1}{\epsilon C_n(\omega)}$$

$$\therefore \text{Loss} = -20 \log_{10} [e^{-1} C_n(\omega)^{-1}]$$

$$\therefore \text{Loss} = 20 \log_{10} \epsilon + 20 \log_{10} C_n(\omega) \quad \text{--- (6)}$$

But, for large ω , $C_n(\omega)$ can be expressed as
 $C_n(\omega) = 2^{n-1} \omega^n \quad \text{--- (7)}$

Substituting value of $C_n(\omega)$ in the expression for loss, we get

$$\text{Loss} = 20 \log_{10} \epsilon + 20 \log_{10} (2^{n-1} \cdot \omega^n)$$

$$\therefore \text{Loss} = 20 \log_{10} \epsilon + 20(n-1) \log_{10} 2 + 20n \log_{10} \omega$$

$$\therefore \text{Loss} = 20 \log_{10} \epsilon + 6(n-1) + 20n \log_{10} (\omega) \quad \text{--- (8)}$$

From above expression, it is observed that Chebyshev response falls-off at the rate of $20n$ dB/decade after initial loss of $[20 \log_{10} \epsilon + 6(n-1)]$ dB.

* Transfer Function of Chebyshev Approximation to Ideal Low Pass Filter

Let us define a design parameter β_K given by

$$\beta_K = \frac{1}{n} \sin^{-1} \left(\frac{1}{\epsilon} \right) \quad \text{--- (9)}$$

where, n = degree of Chebyshev polynomial

ϵ = factor deciding ripple

The poles of the function $H(s)$ of Chebyshev approximation are given by

$$s_K = \sigma_K + j\omega_K$$

--- (10)

It is observed that these poles are located on an ellipse in the s-plane, where the ellipse is given by

$$\frac{\sigma^2}{\omega_0^2} + \frac{\omega_0^2}{\cosh^2 \beta_K} = 1 \quad \text{--- (11)}$$

The locus of poles of Chebyshev filter is as shown in the figure.

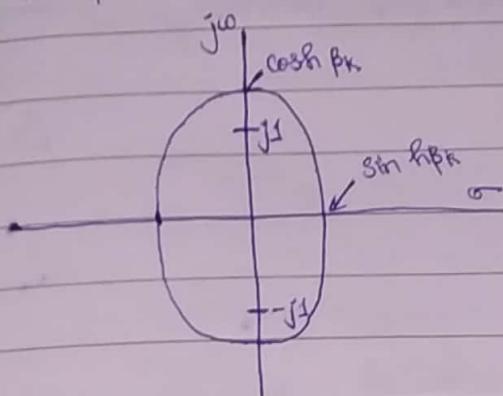


Fig. Locus of poles of Chebyshev filter

Let us normalise poles of Chebyshev response s_K , such that the poles of the Chebyshev response also occur at $\omega=1$, instead of at $\omega=\cosh \beta_K$. Selecting a normalising factor, $\cosh \beta_K$, such that normalised poles are given by

$$s_K' = \frac{s_K}{\cosh \beta_K}$$

$$s_K' = \frac{\sigma_K}{\cosh \beta_K} + \frac{j\omega_K}{\sinh \beta_K} = \sigma_K' + j\omega_K' \quad \text{--- (12)}$$

The normalised pole locations of Chebyshev response can be given by

$$\sigma_K' = \tan \beta_K \cdot \sin \left(\frac{2K-1}{n} \right) \frac{\pi}{2} \quad \text{--- (13)}$$

$$\omega_k = \cos \left(\frac{(2k-1)\pi}{n} \right) \quad \text{--- (14)}$$

Finally, to obtain denormalised poles of Chebychev response, multiply real & imaginary parts of s_k by a normalising factor $\cos \beta_k$.
So,

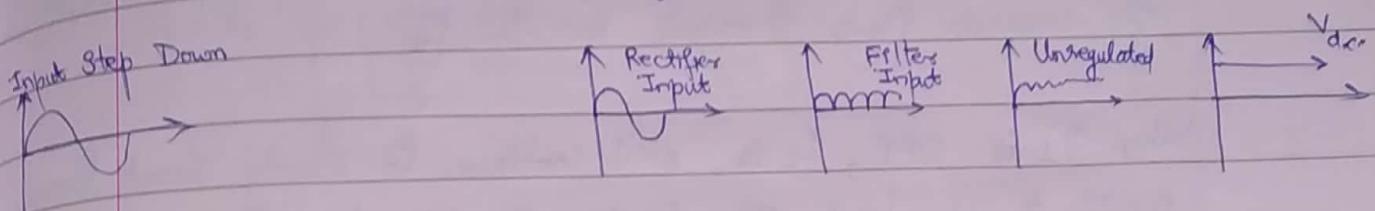
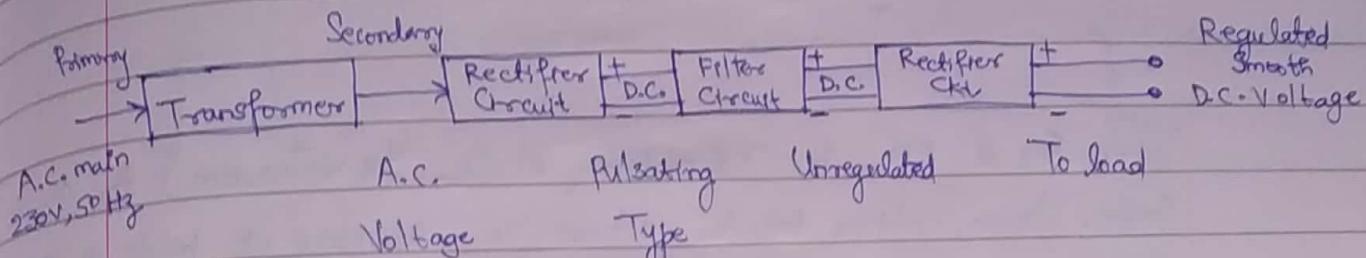
$$s_k = s_k' \cdot \cos \beta_k$$

$$s_k = (\sigma_k + j\omega_k) \cos \beta_k \quad \text{--- (15)}$$

4th chapter over.

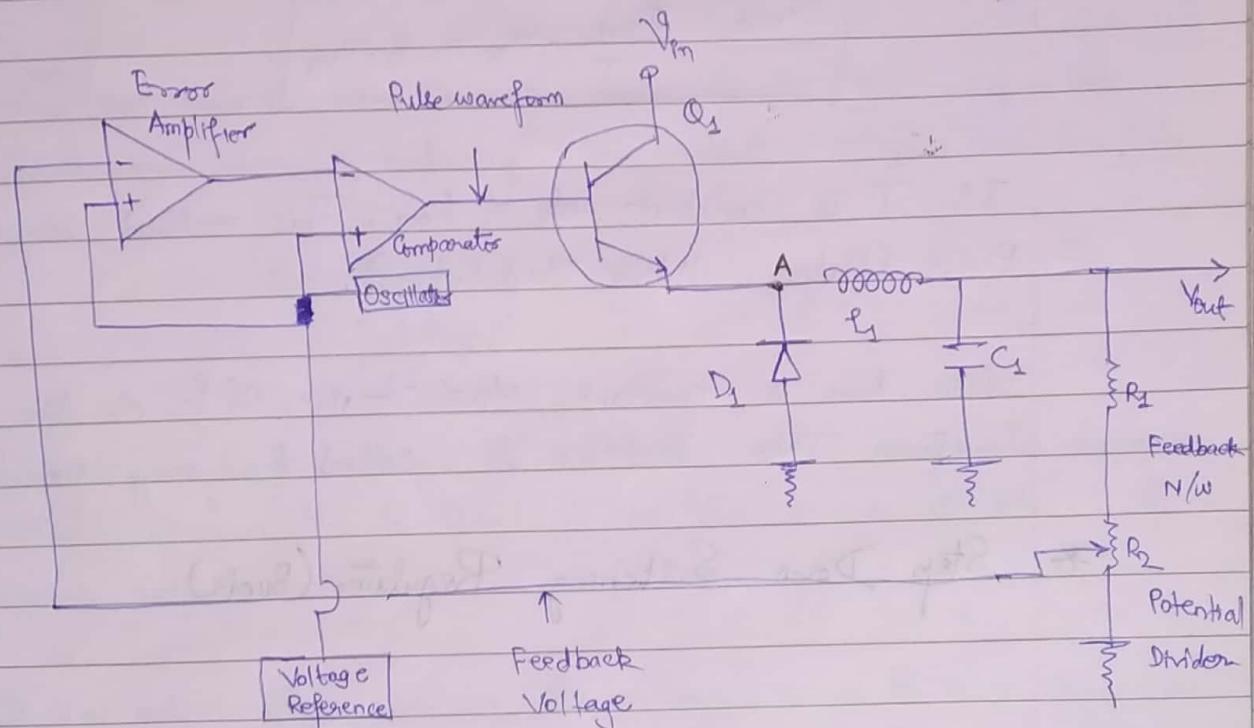
1. ELECTRONICS APPLICATIONS

* Regulated Power Supply



→ A voltage regulator ckt. is the one which is designed to keep the output voltage of a power supply nearly constant under varying input voltage conditions & varying load conditions.

* SMPS (Switch Mode Power Supply)



$$\text{Coefficient of Duty Cycle} \rightarrow S = \frac{t_{on}}{T} \text{ or } t_{on} f$$

$$V_{out} = \frac{t_{on}}{T} \cdot V_{in} = S \cdot V_{in}$$

When Q_1 is ON, in saturation state, V_{ce} (saturation) for Q_1 is zero. Hence, entire input voltage V_{in} appears at point A, thus, the current flows through inductor L_1 .

When Q_1 is OFF, L_1 is still continue to supply current through itself to the load. The diode D_1 provides the return path for the current. The capacitor C_1 acts to ~~smooth~~ smooth out the voltage & the voltage at the output is ~~almost~~ always d.c. in nature. The voltage V_{out} of the switching regulator is a function of duty cycle & the input voltage V_{in} , mathematically it is expressed as

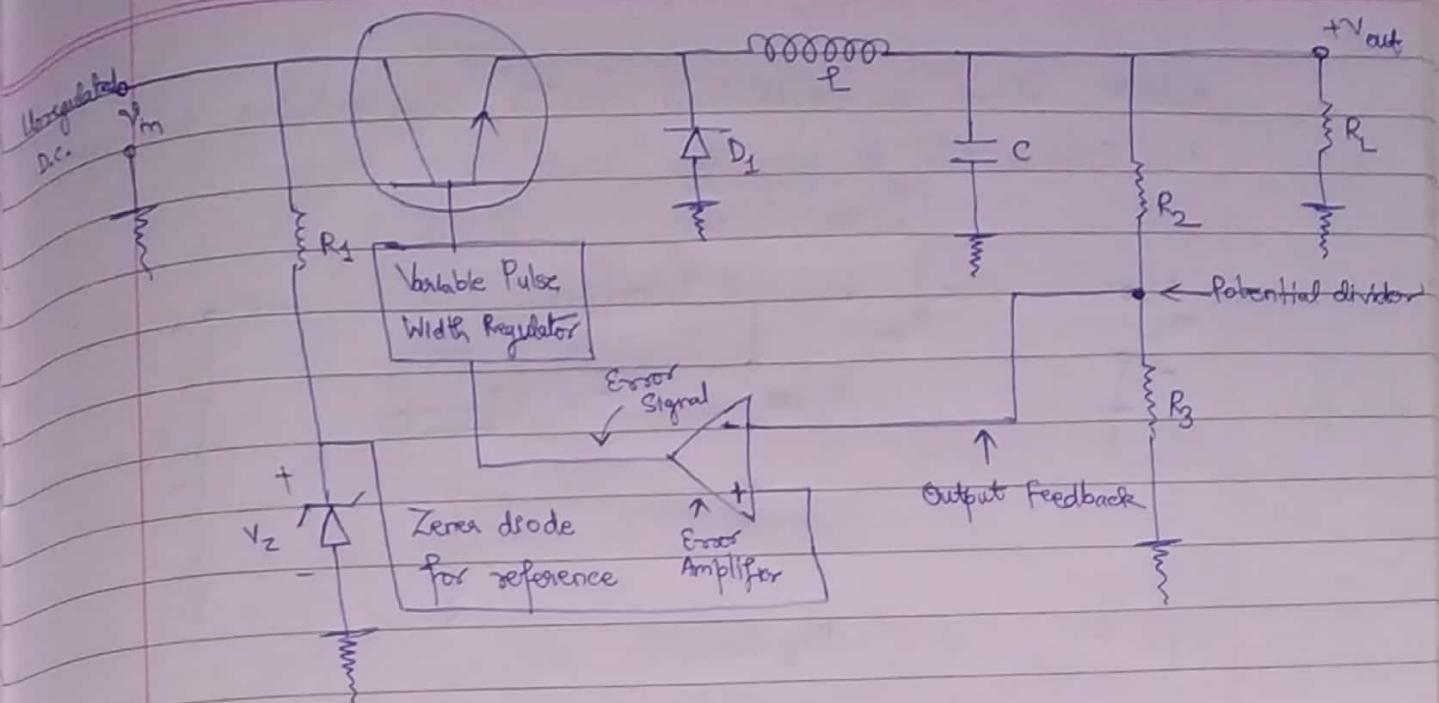
$$V_{out} = \frac{t_{on}}{T} \cdot V_{in} = S \cdot V_{in}$$

If T is constant, $o/p \propto t_{on}$. This method is called PWM (Pulse Width Modulation).

When t_{on} is constant, $o/p \propto \frac{1}{T}$, i.e., $\propto f$ of the pulse waveform. This method is called frequency modulation.

* Step Down Switching Regulators (Buck)

Q1



- When Q_1 is ON, the capacitor charges through it and when Q_1 is OFF, the capacitor discharges through the load resistance as shown in figure. The variable pulse width oscillator controls ON/OFF period of Q_1 . When ON time is more compared to OFF time, the capacitor charges more & increasing the output voltage.
- When OFF time is more than ON time, for Q_1 , the capacitor discharges more & reducing the output voltage. Thus, the duty cycle:

$$S = \frac{t_{on}}{t_{on} + t_{off}} > \frac{t_{on}}{T} = t_{on,f}$$
- If the output voltage decreases, the voltage across R_3 decreases. The reference V_z is fixed. Thus, the error at input of error amplifier is more.
- If the output voltage increases, the voltage across R_3 increases. Thus, the error at the input of error amplifier decreases. Hence,

Output voltage is maintained constant by controlling duty cycle.

Q. Output v/g is given by

$$V_{out} = \delta V_{in}$$

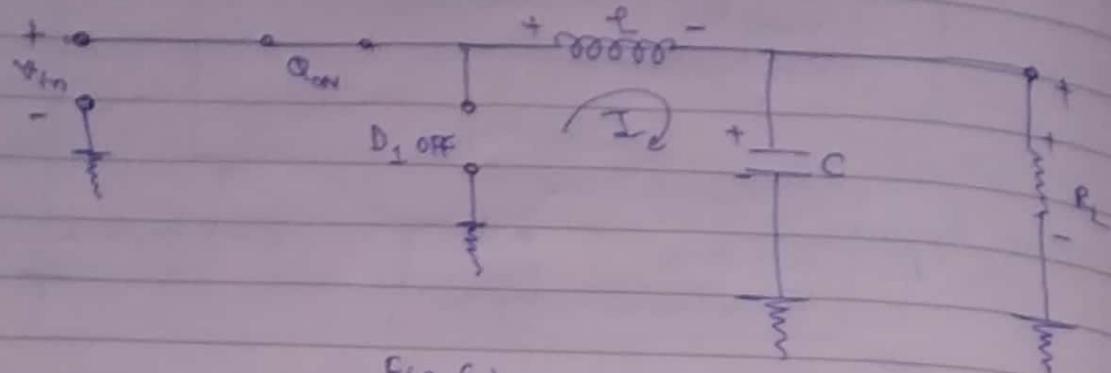


Fig. (a)

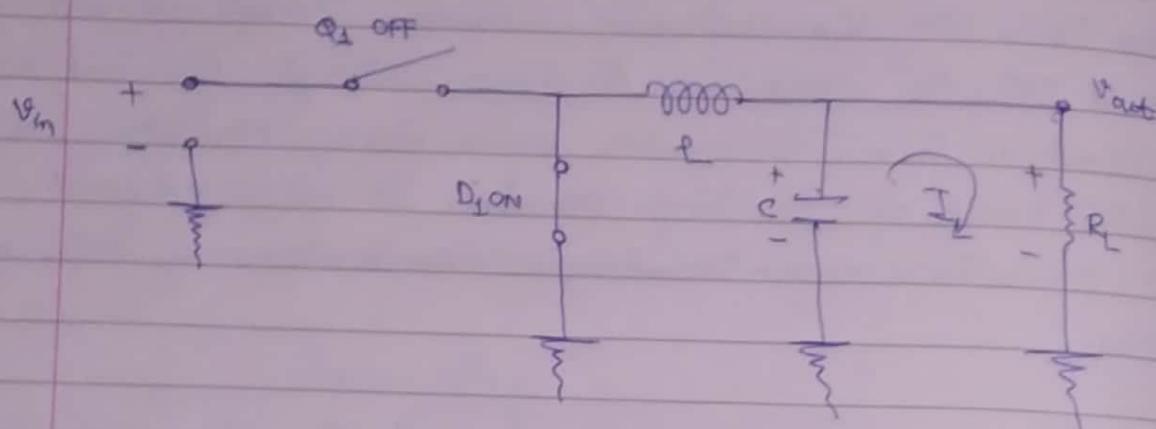
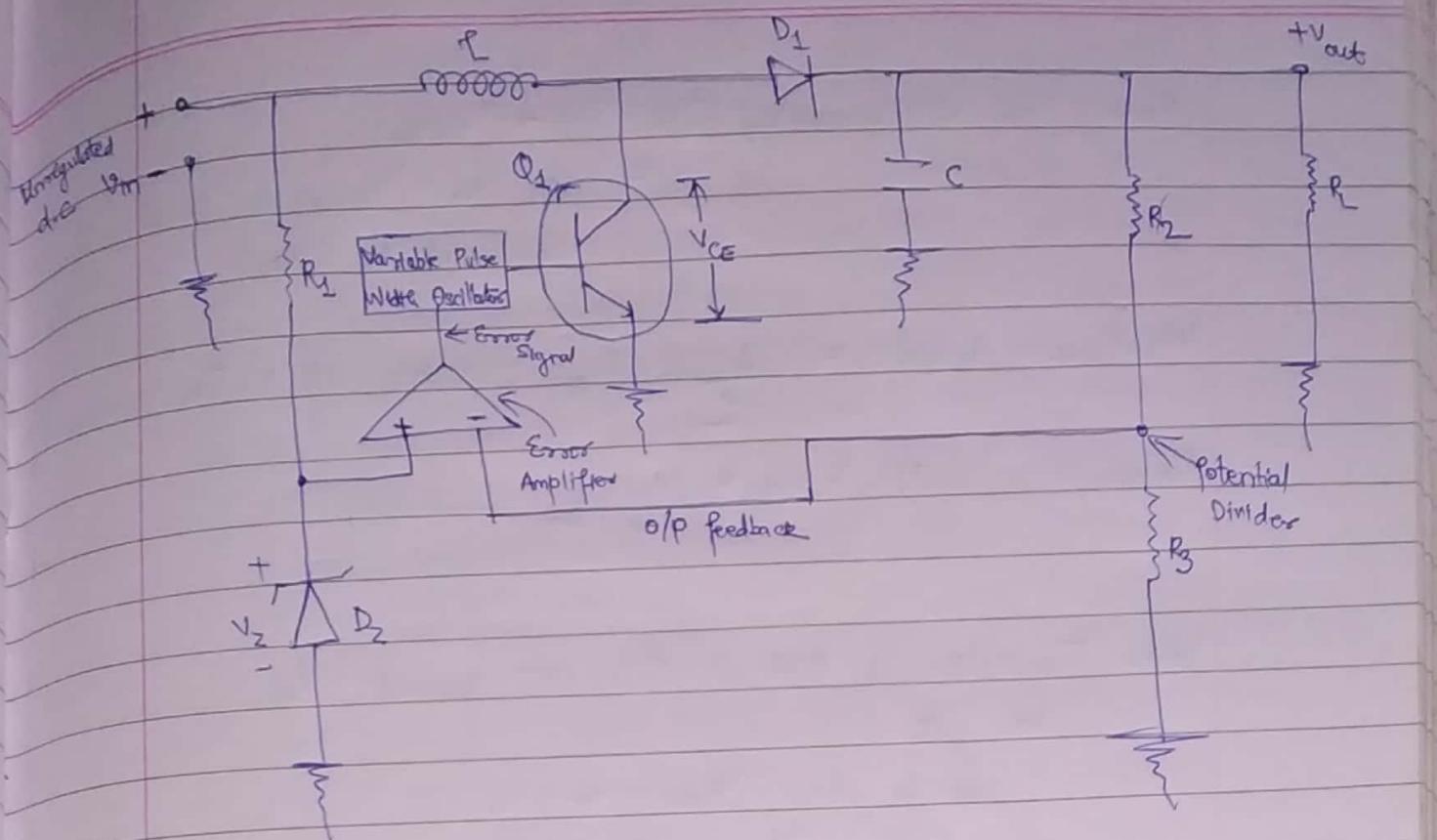


Fig. (b)

* Step-up Switching Regulator (Boost)

- The transistor Q₁ works as an ON-OFF switch.
- When Q₁ is driven into saturation, V_{CE} is very very small & it acts as short-ckt.
- When Q₁ is driven into cut-off, it is off & it acts as open ckt.

Case 1: Let Q₁ is ON, i.e., driven to saturation. When Q₁ is on, V_{CE} is denoted as V_{CE(sat)} & the voltage across L suddenly becomes (V_{in} - V_{CE}). This expands the



magnetic field around the inductor very quickly. During ON time (t_{on}) of Q_1 , the voltage across the inductor starts decreasing exponentially from its maximum value $V_{in} - V_{CE(sat)}$.

The longer the ON-time of Q_1 , the smaller will be the voltage across L .

Case 2: Let Q_1 is switched OFF, i.e., cut-off region. When Q_1 is OFF, the magnetic field of the inductor L collapses & it's polarity gets reversed. This is because the inductor current cannot change instantly. Thus, value of I_L attended after exponential decreases, when Q_1 is ON, now gets reversed.

Expression for the Output Voltage

The current through inductor is given by

$$i_L = \frac{1}{L} \int v_L dt$$

For t_{on} (ON-period), $V_L = V_{in} - V_{CE(sat)}$
 $\approx V_{in}$ as $V_{CE(sat)}$ is small compared to V_{in} .

We have $i_{L(on)} = \frac{1}{L} V_{in} \int dt$, but $\int dt = t_{on}(V_{in} \text{ constant})$,
 hence, $\therefore i_{L(on)} = \frac{V_{in}}{L} t_{on}$ — (1)

When transistor is OFF, i.e. for OFF period t_{off}
 we get

$$\begin{aligned} V_{out} &= V_{in} + V_L \\ (02) \quad V_{out(OFF)} &= V_{out} - V_{in} \end{aligned}$$

Also, $i_{L(off)} = \frac{1}{L} V_L(t_{off}) \int dt$, but, $\int dt = t_{off}$

$$\therefore i_{L(off)} = \frac{1}{L} (V_{out} - V_{in}) t_{off} \quad (2)$$

Comparing eq. (1) & (2) \downarrow

$$\frac{V_{in}}{L} t_{on} = \frac{1}{L} (V_{out} - V_{in}) t_{off}$$

$$\therefore V_{out} - V_{in} = V_{in} \cdot \frac{t_{on}}{t_{off}}$$

$$V_{out} = V_{in} \left(1 + \frac{t_{on}}{t_{off}} \right)$$

$$= V_{in} \left(\frac{t_{off} + t_{on}}{t_{off}} \right)$$

$$\text{But } T = t_{on} + t_{off}$$

$$t_{off} = T - t_{on}$$

$$\begin{aligned} V_{out} &= \frac{V_{in} T}{T - t_{on}} \\ &= \frac{V_{in}}{1 - \frac{t_{on}}{T}} \end{aligned}$$

$$V_{out} = \frac{V_{in}}{1 - S} \quad \left(S = \frac{t_{on}}{T} \text{ (Duty cycle)} \right)$$

Thus, if $S = 0.5$, i.e., duty cycle of 50% .

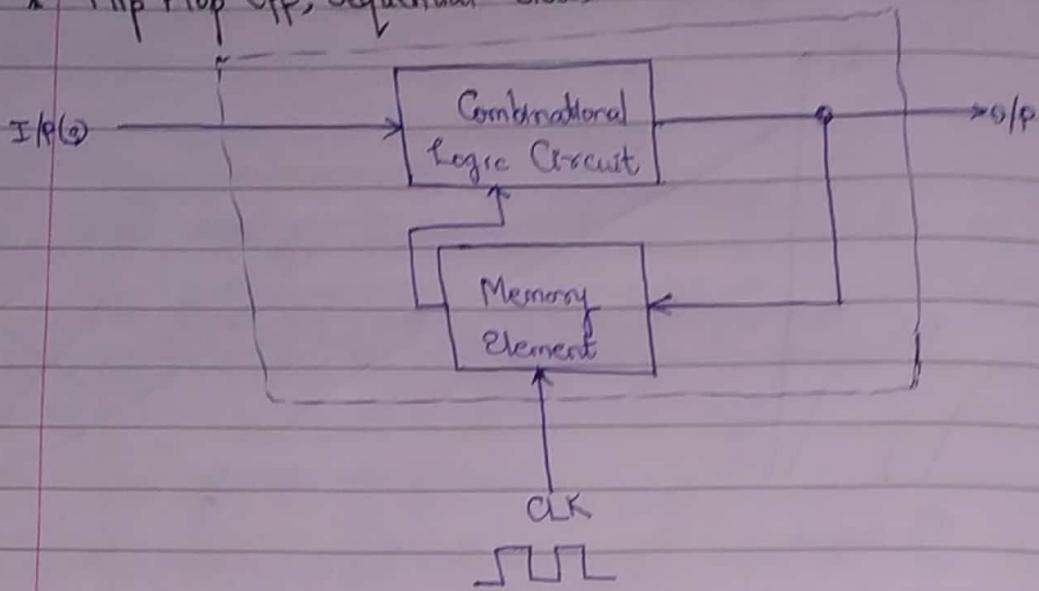
$$\therefore V_{out} = 2V_{in}$$

Output voltage is twice the input voltage.

5. DESIGN OF DIGITAL SYSTEM

(A)

* Flip-Flop (ff; Sequential ckt.)



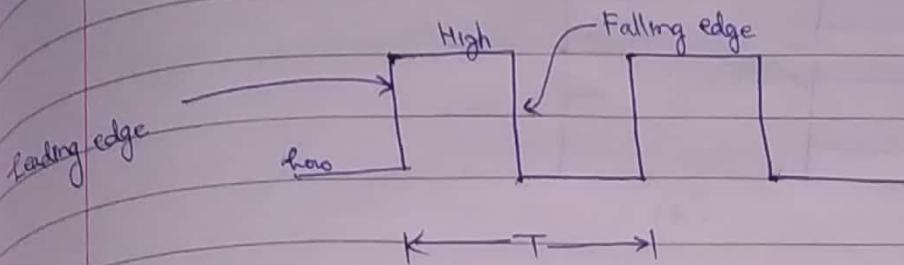
- Its output depend on present input and previous output. Unit of sequential circuit is flip-flop. In order to provide the previous input or output a memory element is required to be used. Thus, a sequential ckt. needs a memory element.

- Present State of Sequential Circuit
 - The data stored by memory element at any given instant of time is called as the present state of sequential circuit.
- Next State of Sequential Circuit
 - The combinational circuit operates on the external inputs & the present states to produce new output. Some of these new output(s) are stored in the memory element & called as the next state of the sequential circuit.

Clock Signal

- It is a rectangular signal with a duty cycle equal to 50%.
- The CLK signal repeats itself after every T (sec). Hence, the CLK frequency is:

$$f = \frac{1}{T}$$



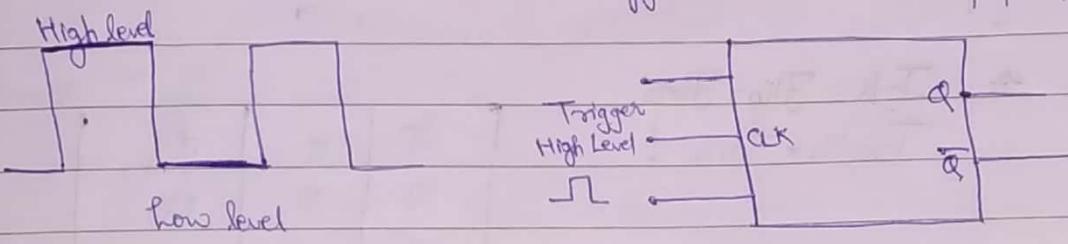
CLK is an extra control of flip-flop.

* TRIGGERING METHODS

- In the latches & flip-flops, we use the additional signal called CLK signal.
- There are two types of triggering methods:
 - i) Level triggering ckt.
 - ii) Edge triggering ckt.

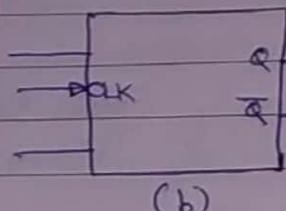
(i) Concept of Level Triggering

- The latch and flip-flop ckt.s. which respond to their inputs only if their enable input (E) held at an Active high or low level are called as level triggered latch or flip-flop.



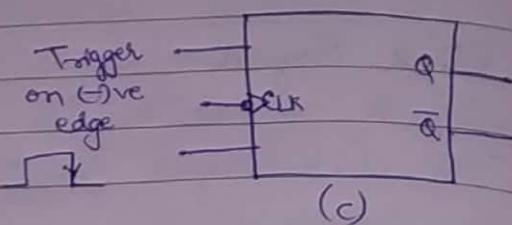
(a)

Trigger on
low level



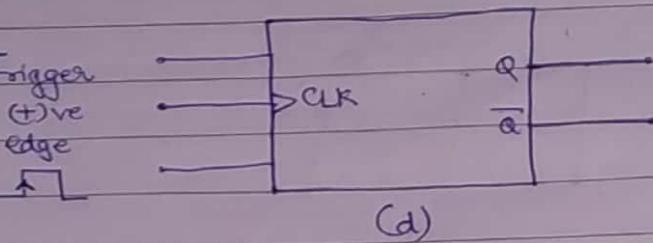
(b)

Trigger
on (↑)ve
edge



(c)

Trigger
on (+)ve
edge



(d)

(ii) Concept of Edge Triggering

→ The flip-flop which change their output corresponding to the positive or negative edge of the CLK I/p are called as edge-triggered flip-flops.

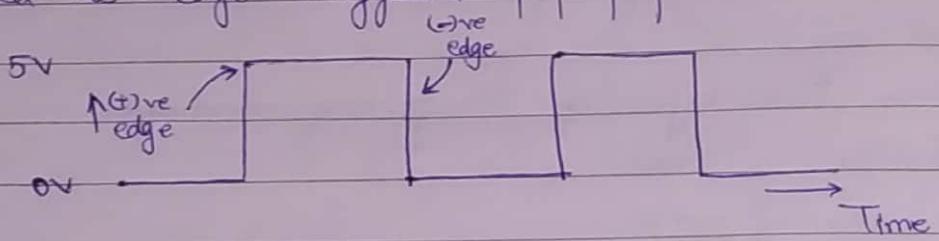
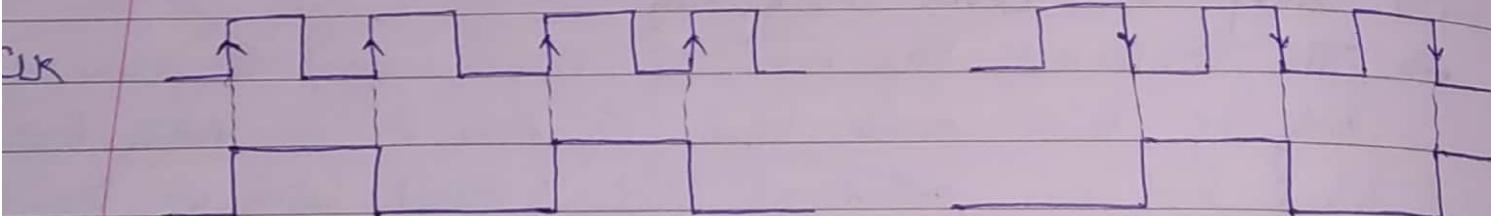
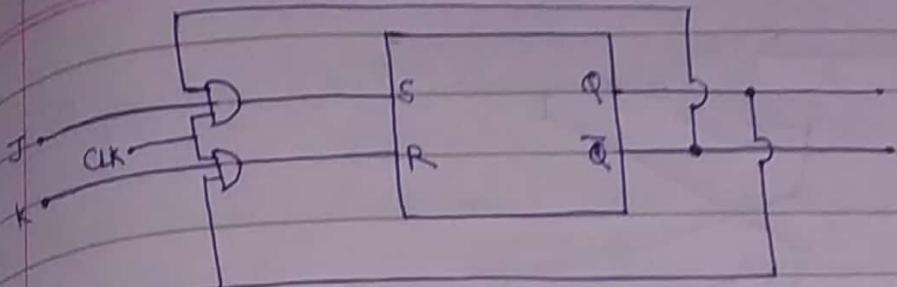


Fig.: CLK pulse transition



* JK Flip-Flop Truth-Table:

J	K	Q
0	0	NC
0	1	0
1	0	1
1	1	Toggle



Toggle Condition: If output receive again 1 again 0 to 1 (or) 1 to 0 is called toggling condition.

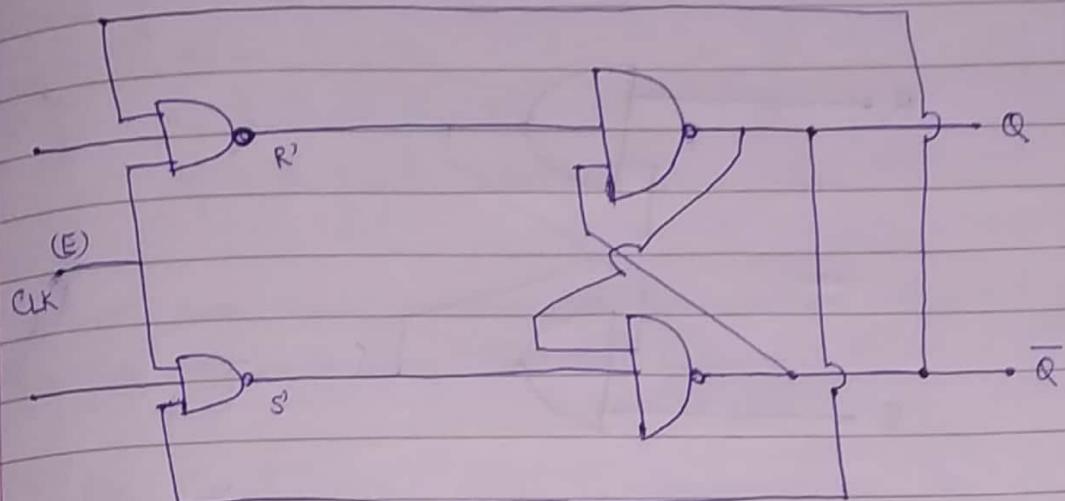


Fig.: J-K flip-flop using NAND Gate

* S-R Flip-Flop (Set-Reset)

→ It consist of 2-NOR (or) 2-NAND gates. It has only 2 input & 2 output.

Truth Table

	S	R	Q	\bar{Q}
	0	0	N.C.	No change
	0	1	0	1
	1	0	1	0
	1	1	Invalid	Invalid

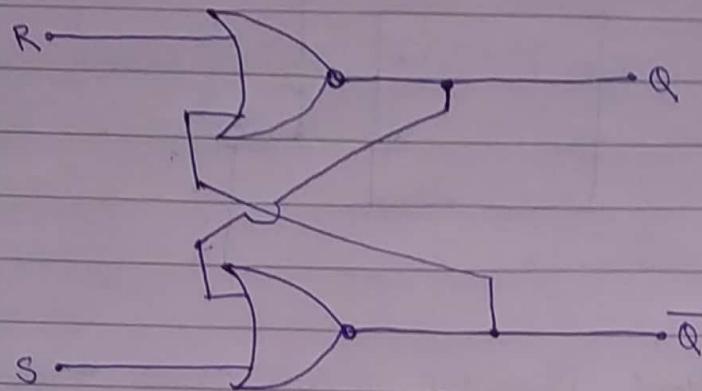


Fig.(a) using NOR Gate

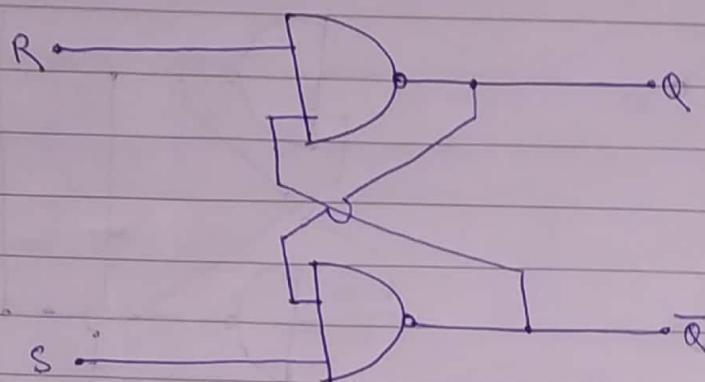
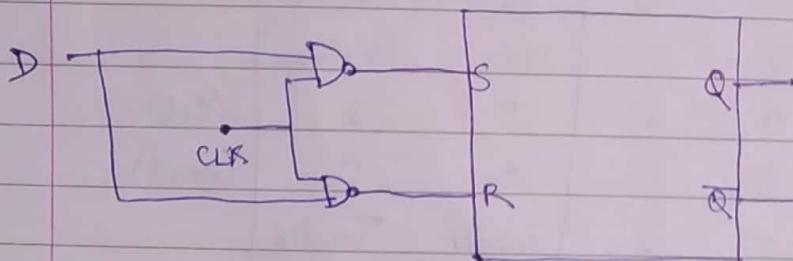


Fig.(b) using NAND Gate

→ By default, it is NOR, if it is not specified. If it is specified, then clear it is NOR (or) NAND.

* D Flip-Flop (Delay)

→ If 2 input S&R connect with one input & the CLK is present and output do not change is called D flip-flop.



Truth Table

I/P	O/P
0	0
1	1

→ D flip-flop is also storage or latch device.

• Race-around Condition (Toggle Condition)

→ We receive 0-1-0-1 means toggle condition, this problem is called race-around condition.

Q. Why this problem come in any flip-flop?

- Because of some delay propagation delay in any circuit i.e. $t_c > t_p$.

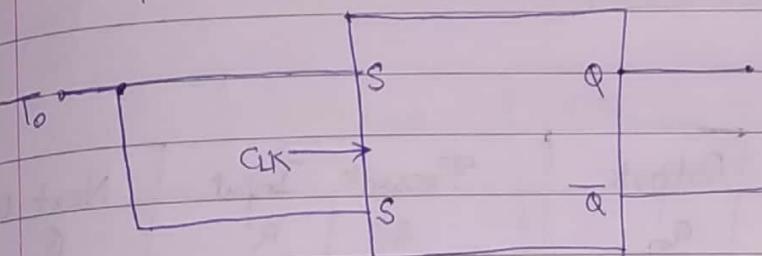
- Clock period is less than or equal to propagation delay of any circuit i.e. $t_c \leq t_p$.

$t_c \rightarrow$ Clock period

$t_p \rightarrow$ Propagation delay

→ To avoid race-around condition, we can use the edge-triggered J-K flip-flop OR Master-Slave J-K flip-flop.

* T Flip-Flop (Toggle)



Truth Table

T	Q
0	N.C.
1	Toggle

→ Toggle flip-flop is basically a J-K flip-flop with J-K terminals permanently connected together. It has only one input denoted by T.

22/02/19

* CHARACTERISTIC TABLE OF FLIP-FLOP

i) S-R Flip-Flop

Output Q_n	Present		Input R	Next Output Q_{n+1}
	S	R		
0	0	0	0	0
0	0	1	0	0
0	1	0	0	1
0	1	1	1	X
1	0	0	0	1
1	0	1	1	0
1	1	0	0	1
1	1	1	1	X

SO
S R Q_n

R	00	01	11	10
0	0	0	X	1
1	1	0	X	1

$$Q_{n+1} = \overline{R}Q_n + S$$

ii) J-K Flip-Flop

Output Q_n	Present		Input R	Next Output Q_{n+1}
	S	J		
0	0	0	0	0
0	0	1	1	0
0	1	0	0	1
0	1	1	1	1
1	0	0	0	1
1	0	1	1	0
1	1	0	0	1
1	1	1	1	0

J_1	K_1	S_1
0	0	0
1	1	0
1	0	1
0	1	0

$$Q_{out} = \bar{J}_1 K_1 + J_2 K_2$$

a) D Flip-Flop

Output Q_n	Present Input D	Next Output Q_{out}
0	0	0
0	1	1
1	0	0
1	1	1

Q_n	D	Q_{out}
0	0	1
1	0	0

$$Q_{out} = D$$

b) T Flip-Flop

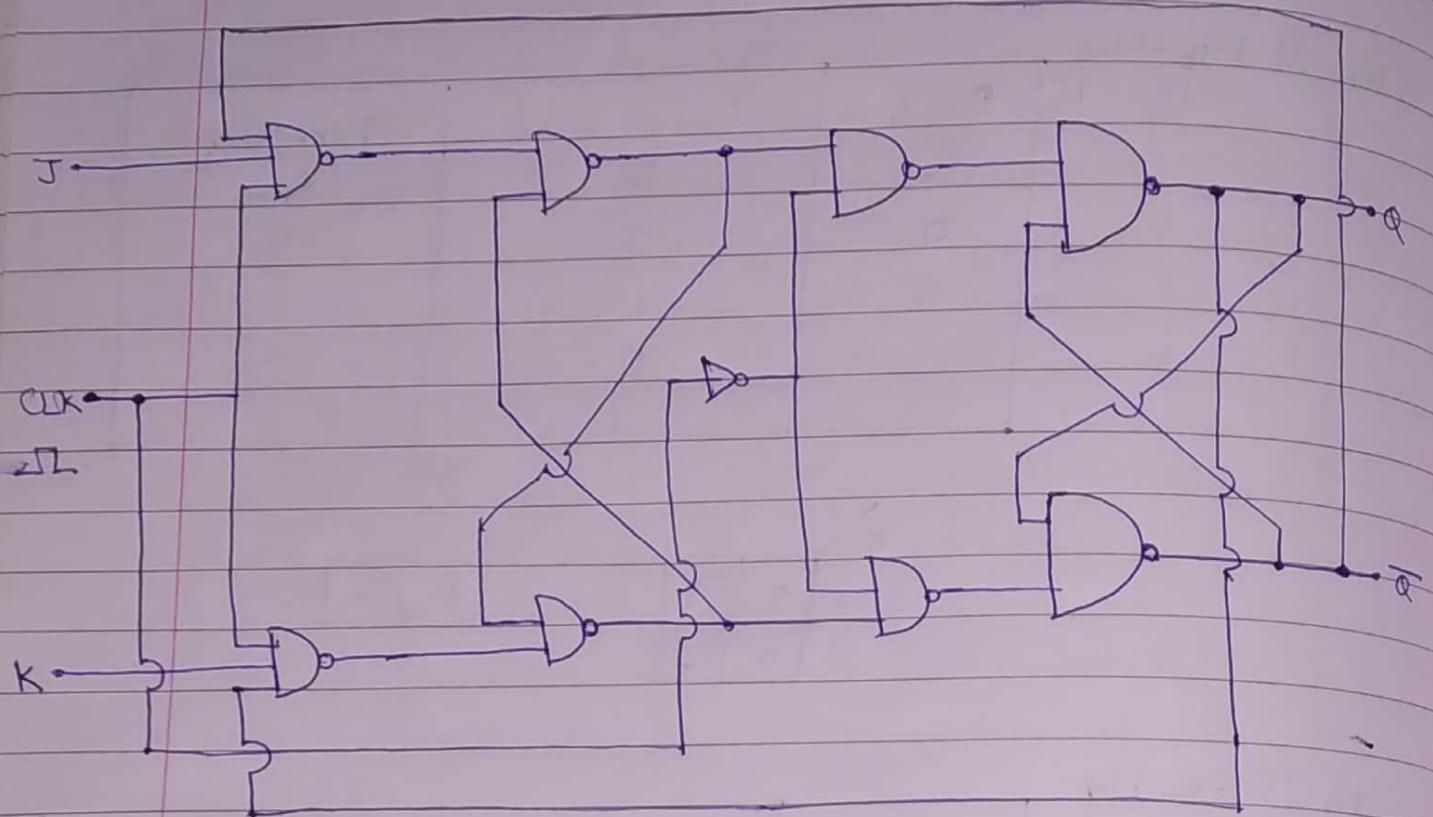
Output Q_n	Present Inputs T	Next Output Q_{out}
0	0	0
0	1	1
1	0	1
1	1	0

Q_n	T	Q_{out}
0	0	1
1	1	0

$$\begin{aligned} Q_{out} &= Q_n \bar{T} + \bar{Q}_n T \\ &= Q \oplus T \end{aligned}$$

* MASTER-SLAVE J-K FLIP FLOP
→ Solution for Race Around Condition

→ Out of the two JK flip-flop one is only active at a time.



27.02.19

* Excitation Table of S-R Flip-Flop

Q_n	Q_{n+1}	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

Truth Table of SR ff		
S	R	Q_n
0	0	N.C.
0	1	0
1	0	1
1	1	Invalid

* Excitation Table of J-K Flip-Flop

Q_n	Q_{n+1}	J	K
0	0	0	x
0	1	1	x
1	0	x	1
1	1	x	0

Truth Table of J-K ff		
J	K	Q_n
0	0	N.C.
0	1	0
1	0	1
1	1	Toggle

* Excitation Table of D Flip-Flop

Q_n	Q_{n+1}	D
0	0	0
0	1	1
1	0	0
1	1	1

Truth Table of D ff

Input	Output
0	0
1	1

* DIFFERENCE B/W LATCH & FLIP-FLOP

→ Latch & Flip-Flop both are basically the bistable element.

→ A latch has got an enable input. As long as it is active, the latch output will keep changing according to the input.

→ In other words, latch is the level-triggered flip-flop, but flip-flop is a sequential ckt which generally samples its input & changes its output only at particular instant of time.

→ The flip-flop are therefore said to be edge sensitive or edge-triggered rather than being levelled.

for 5(B), refer Pg.no. 48-52.

for 5(A), refer Pg.no. 73 onwards.

& Come back to this page to Pg. 55 & then back to Pg. 72

5. DESIGN OF DIGITAL SYSTEM

(B)

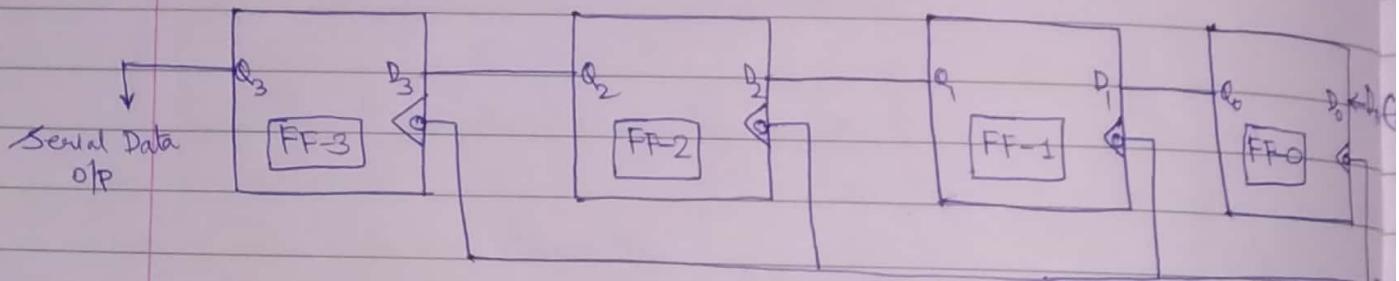
* Shift Register

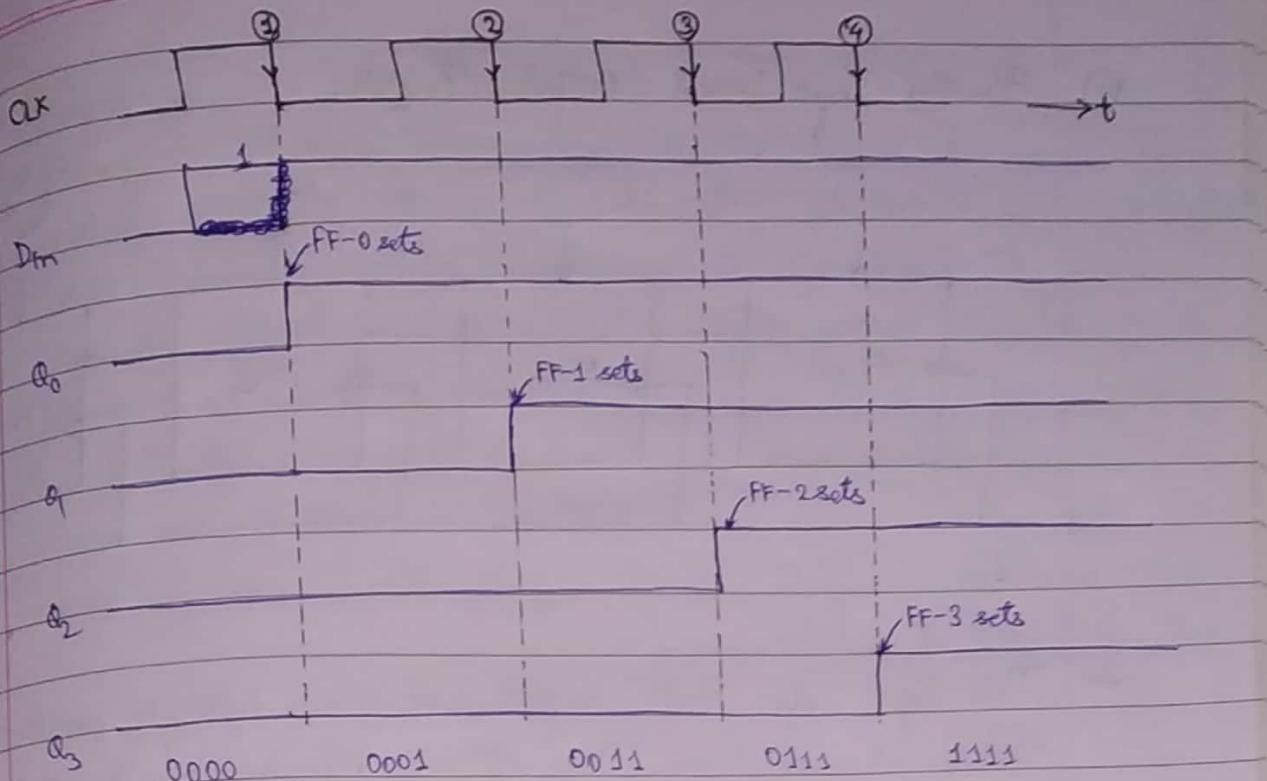
- Flip-flop is a one-bit memory cell which can be used for storing the digital data. To increase the storage capacity in terms of no. of bits we have to use a group of flip-flops known as a register. The register is a group of flip-flops.
- The n-bit register will consist of n no. of flip-flops & it is capable of storing n-bit word. These no. of bits are the no. of flip-flop in the register. This register is also called as the buffer register.
- Buffer registers are used for temporary storage of digital words. There are 4 types of shift registers:

 - i) SISO (Serial In Serial Out) Register
 - ii) SIPO (Serial In Parallel Out) Register
 - iii) PISO (Parallel In Serial Out) Register
 - iv) PIPO (Parallel In Parallel Out) Register

- Shift registers are used for data storage, data transfer & certain arithmetic and logic operations.

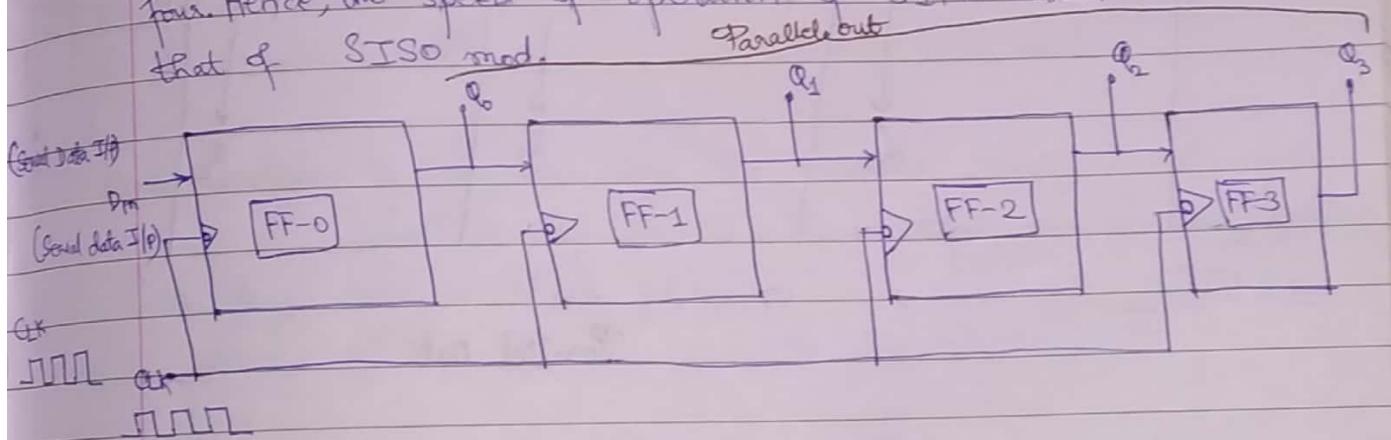
i) Serial Input Serial Output Register



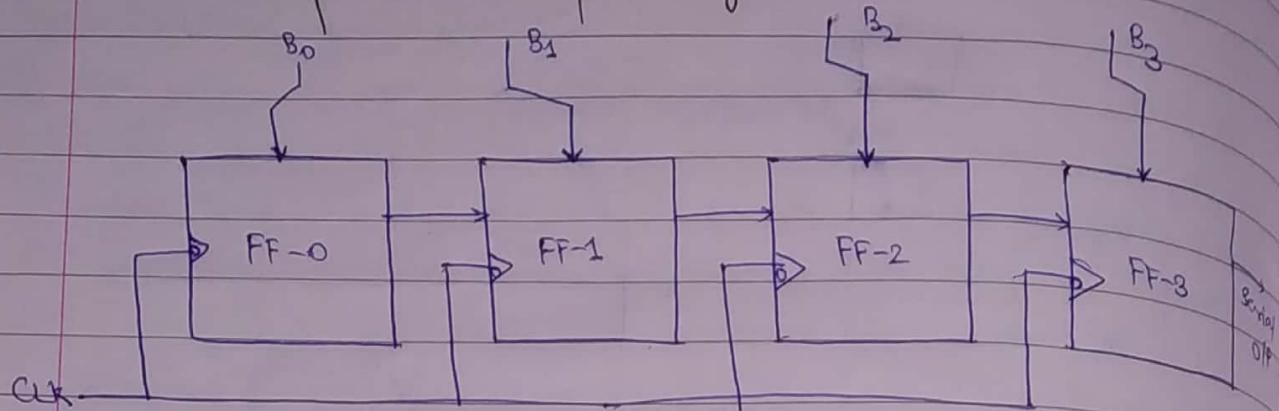


i) Serial Input Parallel Output Register

- First the data is loaded bit by bit.
- The outputs are disabled as long as the loading is taking place.
- As soon as the loading is complete & all the flip-flops contain their required data, the outputs are enabled so that all the loaded data is made available over all the output lines simultaneously.
- No. of clock cycles required to load a four-bit word is four. Hence, the speed of operation of SIPO mod is same as that of SISO mod.



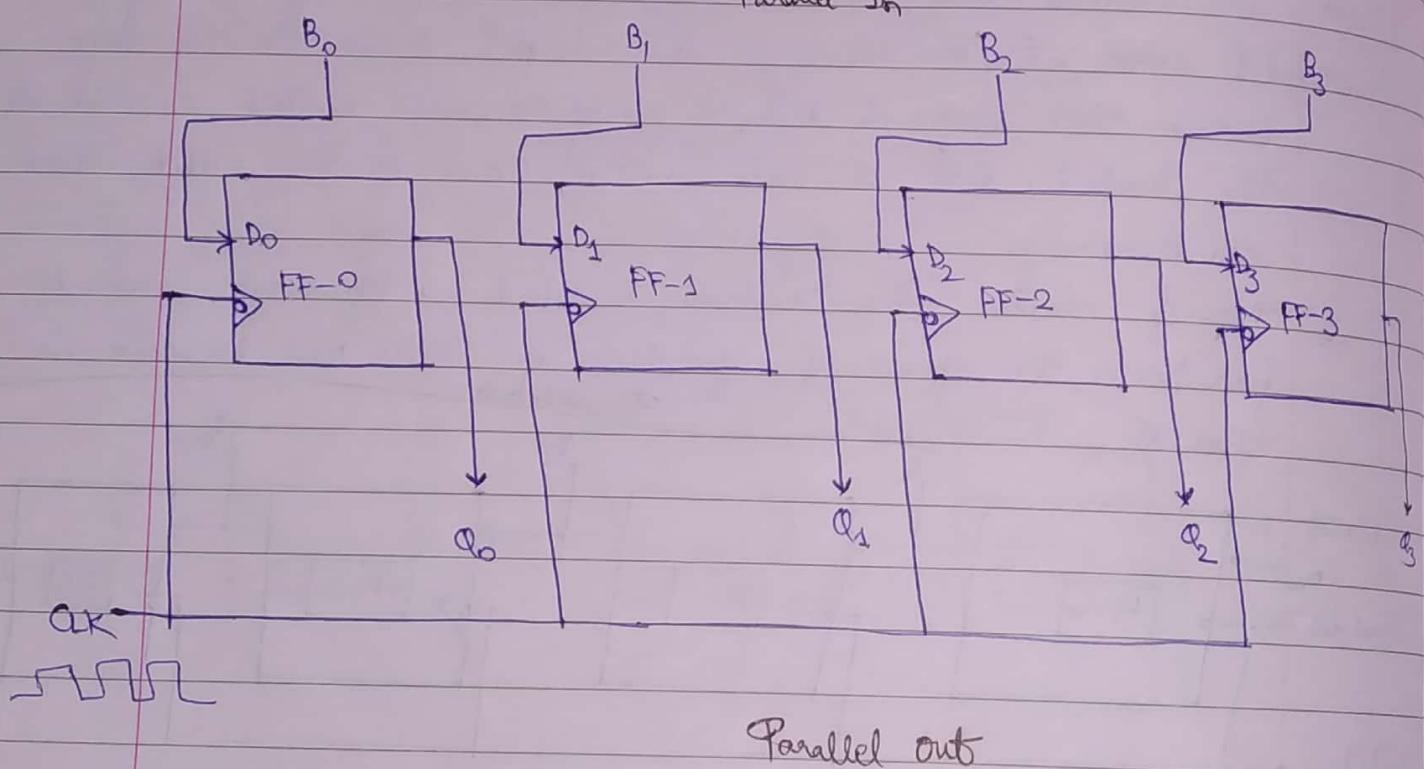
ii) Parallel-Input Serial Output Register



→ This type of shift register accepts data in parallel all bits at a time. The stored information is outputted in serial form.

iii) Parallel-Input Parallel Output Register

Parallel In



Parallel out

COUNTERS

- * These counters are binary counters. The digital clk. used for counting pulses is known as counter. It is a sequential clk.
- Counters is the widest application of flip-flops. It is a group of flip-flops with clock signal applied. Counters count the no. of clock pulses, hence, with some modifications, it can be used for frequency & time-period measurement.
- There are 2 types of counter:
- i) Asynchronous Counter / Ripple Counter - Only one external CLK applied to ^{one} flip-flop but other flip-flop share this CLK with each other.

- ii) Synchronous Counter - There are 2 types of synchronous counter:
 - i) Ring Counter
 - ii) Johnson (Switch-Tail) Counter

Each flip-flop provide only one CLK externally.

- Depending on the way in which the counting progresses, the synchronous & asynchronous counters are classified as follows:

- i) Up counters
- ii) Down counters
- iii) Up / Down counters

- i) Up counters - Up counters are the counters that count from small to big count. Their output goes on increasing as they receive clock pulses.

Eg. Output of an up-counter will be 0-1-2-3, ...

- ii) Down counters - Down counters are the counters that

Count from large to small count. Their output goes on decreasing as they receive CLK pulses. The output of a down counter will be 7-6-5-4-

(ii) Up-Down Counter It is the combination of up counter & down counter.

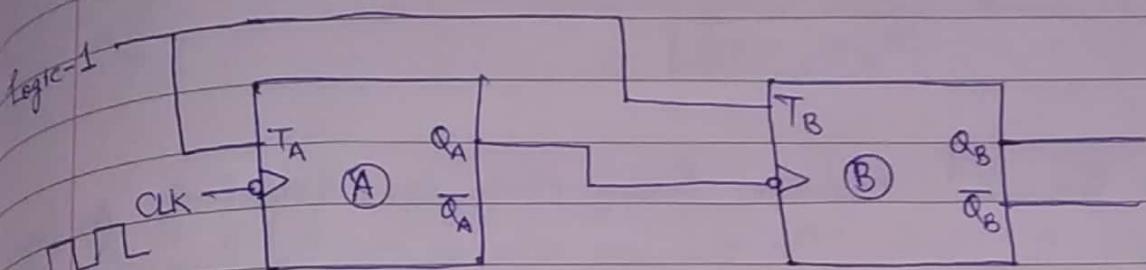
$$\text{No. of states} = 2^n$$

$$\text{Max. count} = 2^n - 1$$

5. DIGITAL SYSTEM DESIGN

(c)

* 2-bit Asynchronous (Ripple up counter)



Table

Clock	Counter Output	State no.	Decimal equivalent of counter output
	Q_B (MSB) Q_A (LSB)		
Initially	0 0	-	0
1 st ↓	0 1	1	1
2 nd ↓	1 0	2	2
3 rd ↓	1 1	3	3
4 th ↓	0 0	4	0

On the 1st negative going CLK edge, the first falling edge of the CLK hits flip-flop A; the no. of flip-flop used is 2. Thus, the no. of bits will always be equal to no. of flip-flops. The toggle (T) flip-flops are being used but we can use J-K flip-flop also with J and K connected permanently to logic 1.

External CLK is applied to the CLK input of flip-flop A and Q_A output is applied to the CLK input of the next flip-flop, i.e., flip-flop B.

On the 1st negative going clock edge, the first falling edge of the CLK hits flip-flop A. It will toggle as $T_A = 1$. Hence, Q_A will be equal to 1. Hence, after the first CLK pulse, counters output are

$$\boxed{Q_B Q_A = 01}$$

At the 2nd negative falling clock edge, flip-flop A toggles again to make Q_A zero. The change in Q_A from 1 to 0 acts as a negative CLK edge for flip-flop B. So, it will also toggle & Q_B will become 1. Hence, after second CLK pulse, counters output are

$$\boxed{Q_B Q_A = 10}$$

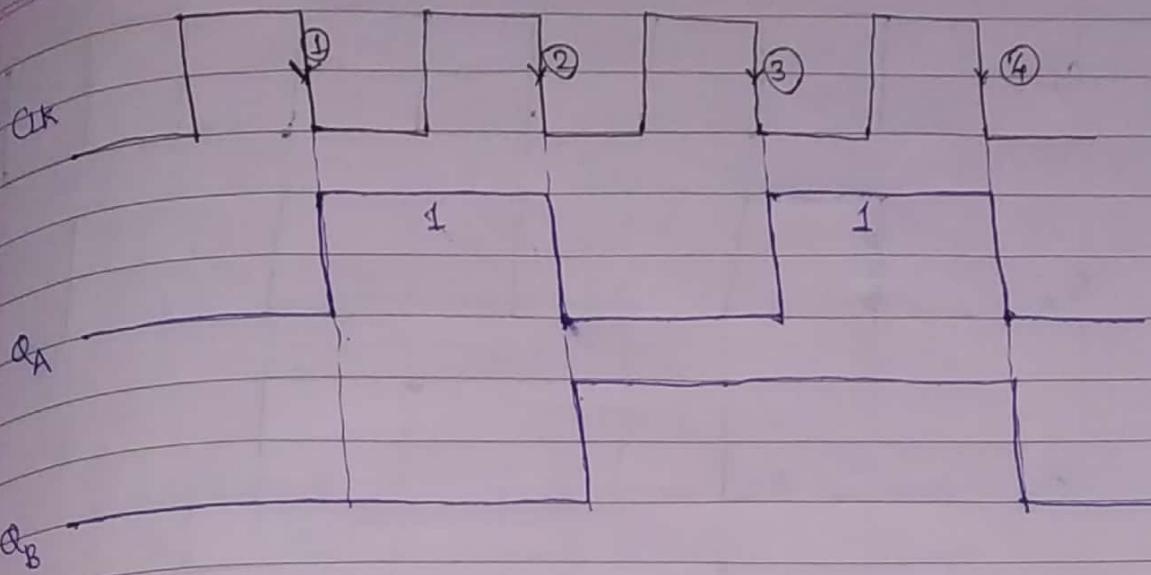
At the 3rd falling edge of clock, flip-flop A toggles again & Q_A becomes 1 from 0. Since, this is a positive going change, flip-flop B doesn't respond to it & remaining inactive so Q_B doesn't change & continue to be equal to 1. Therefore,

$$\boxed{Q_B Q_A = 11}$$

At the 4th negative CLK edge, flip-flop A toggles & Q_A changes

$$\boxed{Q_B Q_A = 00}$$

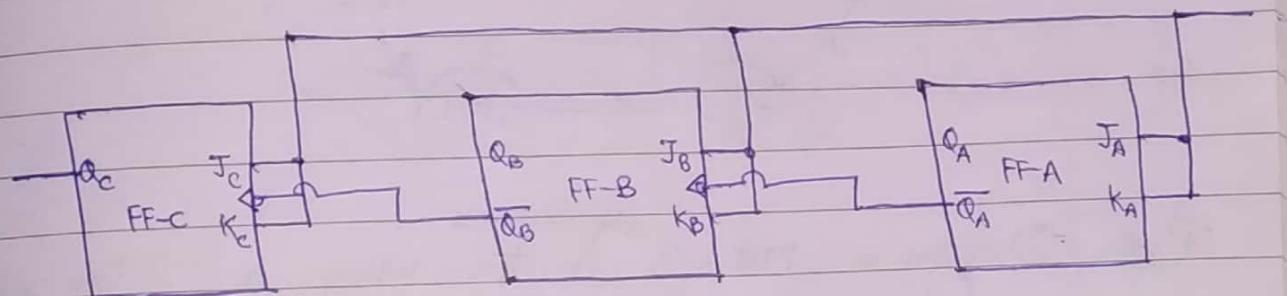
from 1 to 0. This negative change in Q_A acts as CLK pulse for flip-flop B. Hence, it toggles to change Q_B from 1 to 0.

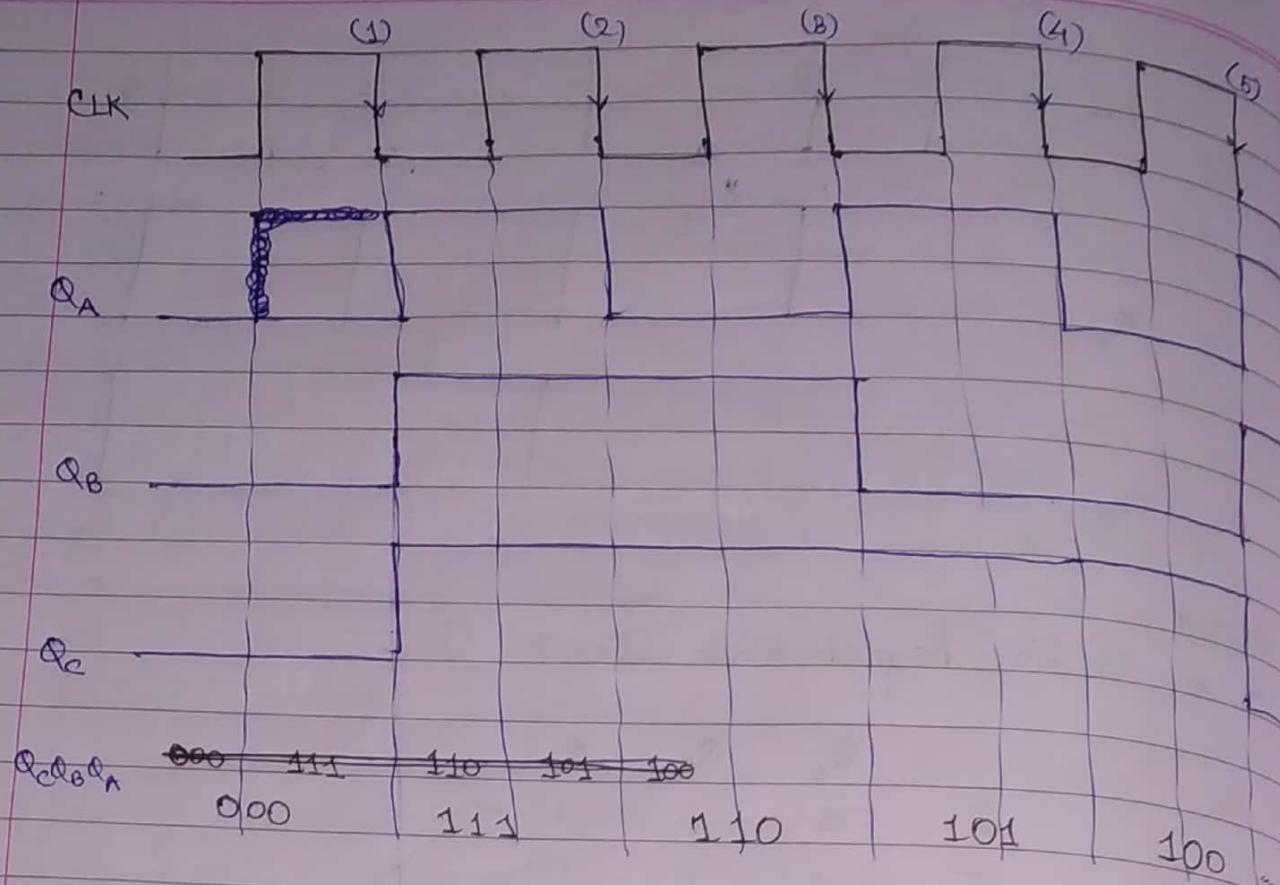


* 01.03.19
* 3-bit Asynchronous Down Counter

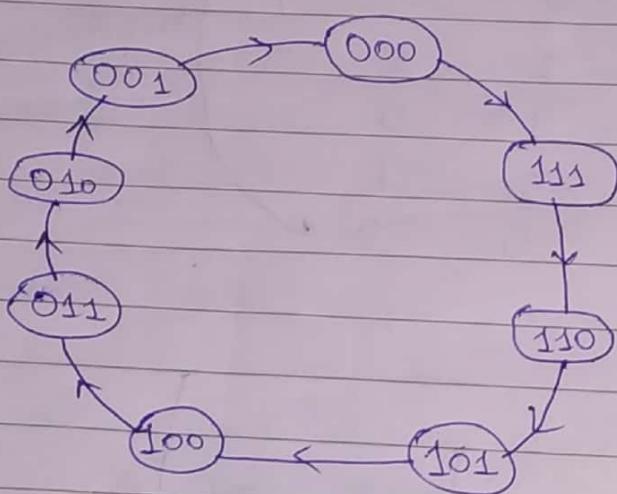
	Q_c	Q_b	Q_a	
7	1	1	1	↑
6	1	1	0	
5	1	0	1	
4	1	0	0	
3	0	1	1	
2	0	1	0	
1	0	0	1	
0	0	0	0	↓

Recycle

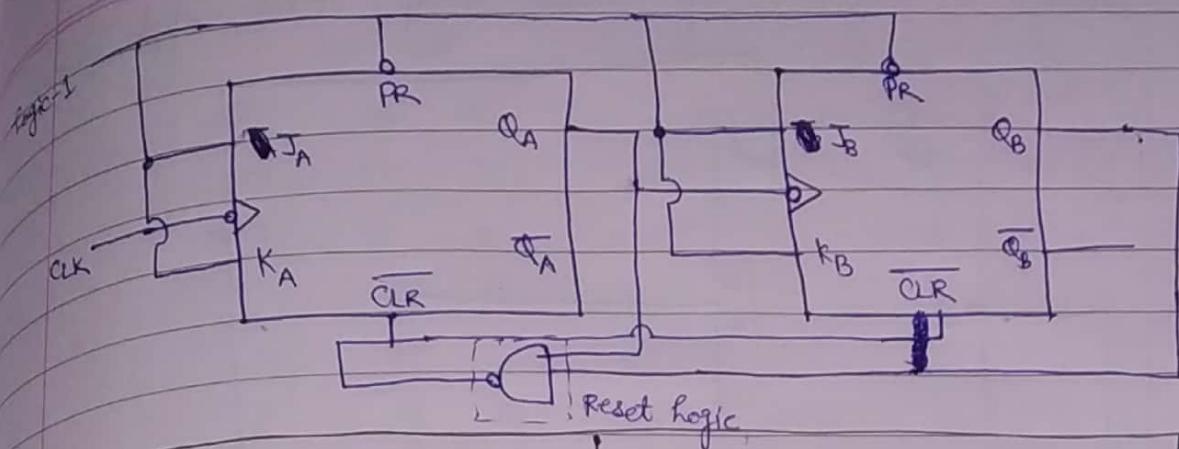




State Diagram



Prob: Design a Mod-3 ^{asynchronous} Counter using a 2-bit ripple counter.

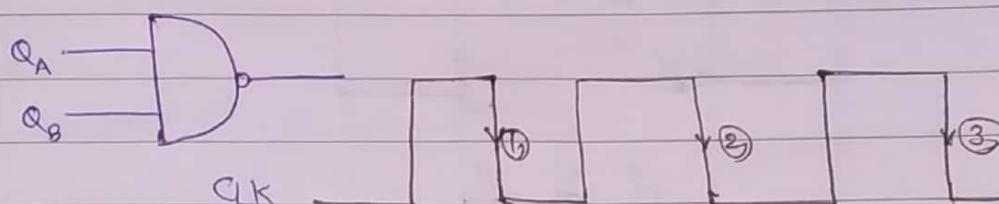


FF Output		O/P of reset logic Y
Q _B	Q _A	
0	0	1
0	1	1
1	0	1
1	1	0

$$\overline{Q_B} \cdot \overline{Q_A}$$

Q _B	Q _A	0	1
0	1	1	1
1	1	1	0

$$(Y) O/P = \overline{Q_A} + \overline{Q_B} = \overline{Q_A} \cdot \overline{Q_B} \quad (\text{DeMorgan's law})$$



Prob. Design a MOD-5 up counter using 3-bit ripple counter.

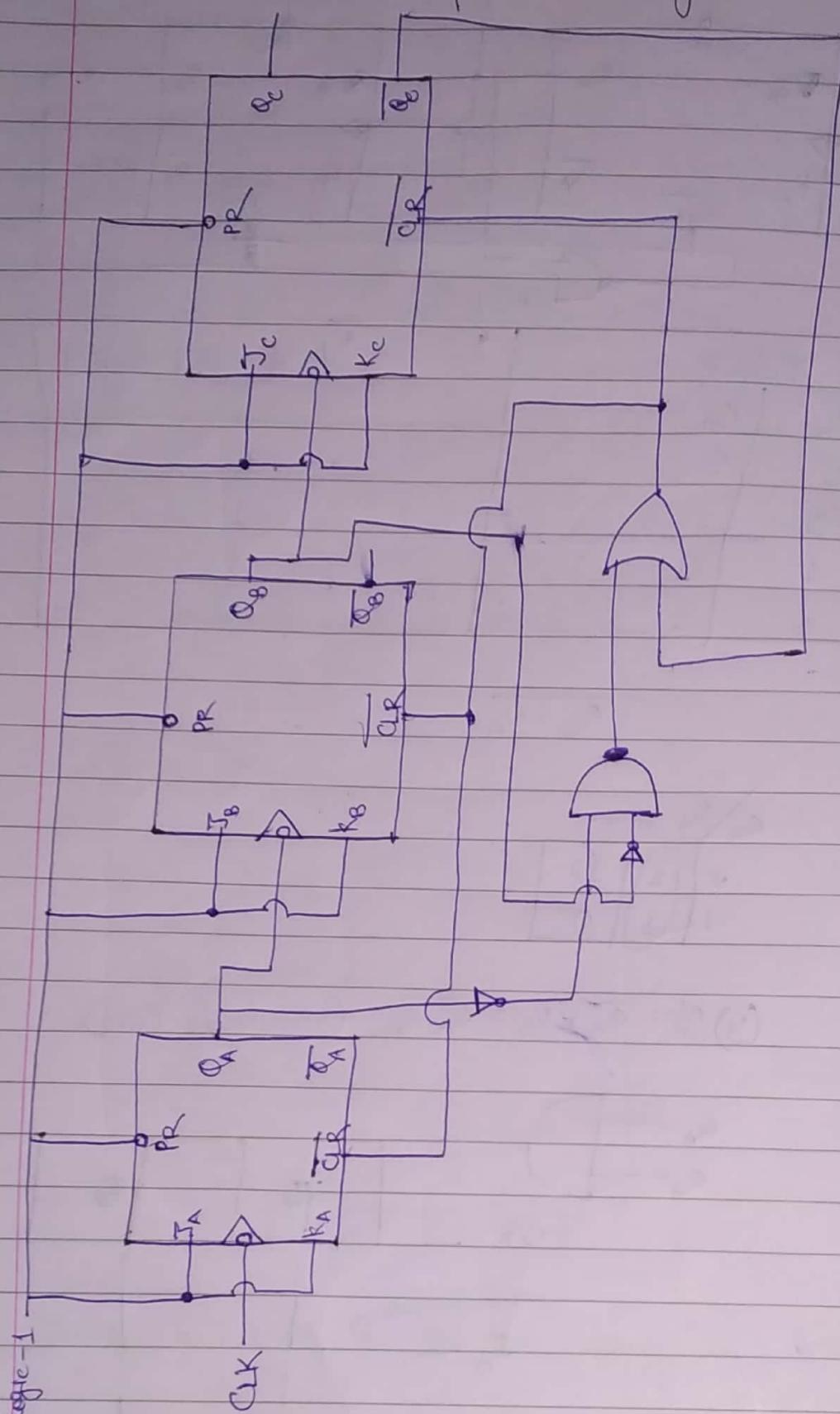


Figure-1

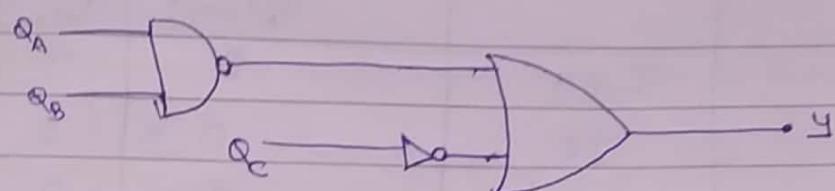
FF- o/p

Q_c	Q_B	Q_A	
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

o/p of next
logic Y1
1
1
1
0
0
0

Q_c	Q_B	Q_A	0	1	11	10
0	(1)	1	1	1	1	1
1	1	0	0	0	0	0

$$\text{o/p } (Y) = \overline{Q_c} + \overline{Q_A} \cdot \overline{Q_B}$$



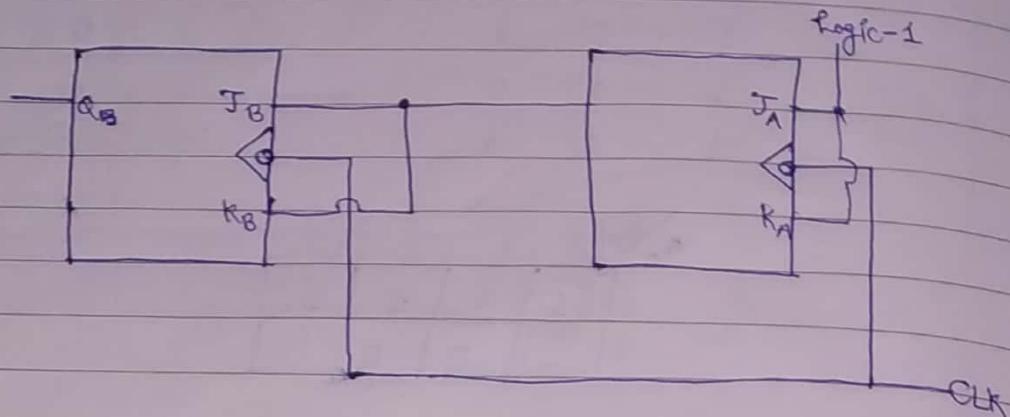
Mod of Counters

- 1) Mod of ripple counter = 2^n
- 2) Mod of Johnson Counter = $2m$
- 3) Mod of ring counter = n
- 4) n-bit parallel counter Mod = 2^n

* SYNCHRONOUS COUNTER

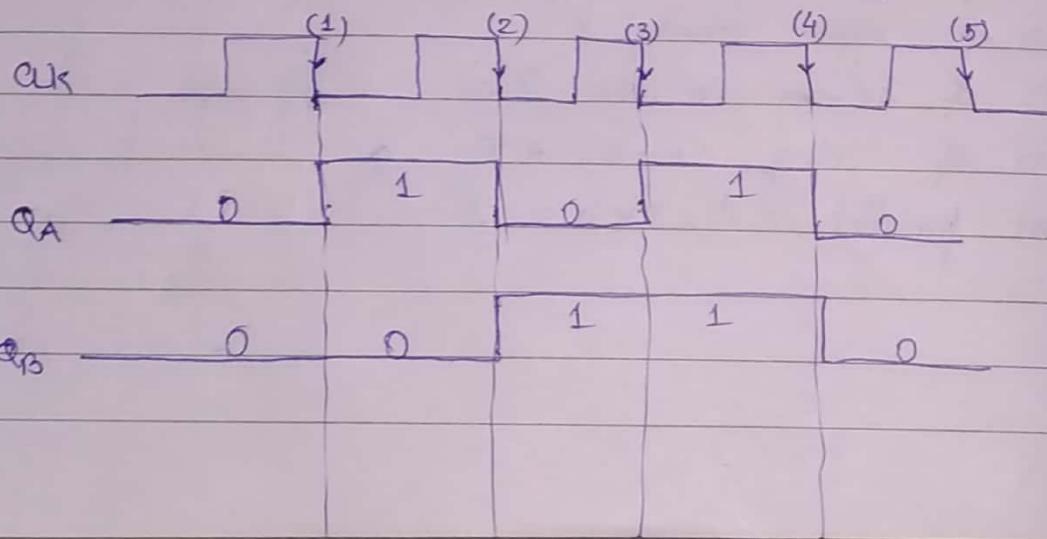
→ If the CLK pulses are applied to all the flip-flops in a counter simultaneously then such a counter is called a synchronous counter.

* 2-bit Synchronous Up-Counter



Table

Clock	Counter		o/p(Q)
	Q_B (MSB)	Q_A (LSB)	
Initial	0	0	
1↑	0	1	
2↓	1	0	
3↓	1	1	
4↑	0	0	



Difference between Synchronous & asynchronous counter

Parameter	Asynchronous	Synchronous
i) Ckt. complexity	Simple logic circuit	With increase in no. of states, logic ckt. becomes complicated.
ii) Connection pattern	Output of the preceding flip-flop is connected to CLK of next flip-flop	There is no connection b/w output of preceding flip-flop & CLK of next one.
iii) CLK Input	All the flip-flops are not clocked simultaneously	All flip-flops receive CLK signal simultaneously
iv) Propagation Delay	$P.D. = n \times t_d$ (t_d = Propg delay per ff) (n = No. of flip-flop)	$P.D. = (t_d)_{FF} + (t_d)_{gate}$ It is much shorter than that of asynchronous counter
v) Maximum Frequency of operation	Low because of long propagation delay	High due to shorter propagation delay

2. POWER AMPLIFIERS

(A)

- The power amplifier is capable of delivering power to the loud speaker. The power amplifier is an essential part of every electronic system. Similarly, in case of broadcast, transmitters & radio receivers power amplifiers are used.
- The power amplifiers are large-signal amplifiers which raise the power level of the signals. The power amplifier may also be defined as a device which convert d.c. power to a.c. power & whose action is controlled by the input signal.
- The power amplifier takes the power from d.c. power supply connected to the output ckt. & converts it into useful a.c. signal power. The d.c. power is distributed according to the relation:

$$dc\ power\ (P_d) = ac\ power\ (P_a) + losses$$

- There are two types of power amplifiers:

- i) Audio power amplifier
- ii) Radio power amplifier

- **Audio Power Amplifier**

- The audio power amplifier raise the power level of signals that have audio frequency range 20Hz to 20KHz.
- They are also known as small-power amplifiers.

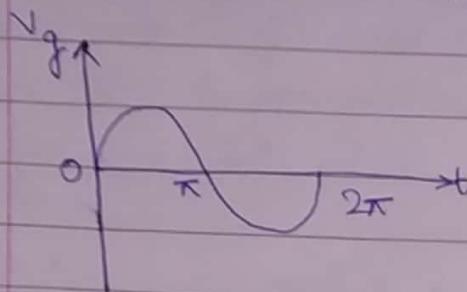
- **Radio Power Amplifier (Tuned, ^{Power}Amplifier)**

- These raise the power level of signal that have frequency range 20KHz - 300 GHz. They are also known as large signal power amplifiers.
- On the basis of the mode of operation, the power amplifier may be classified as:

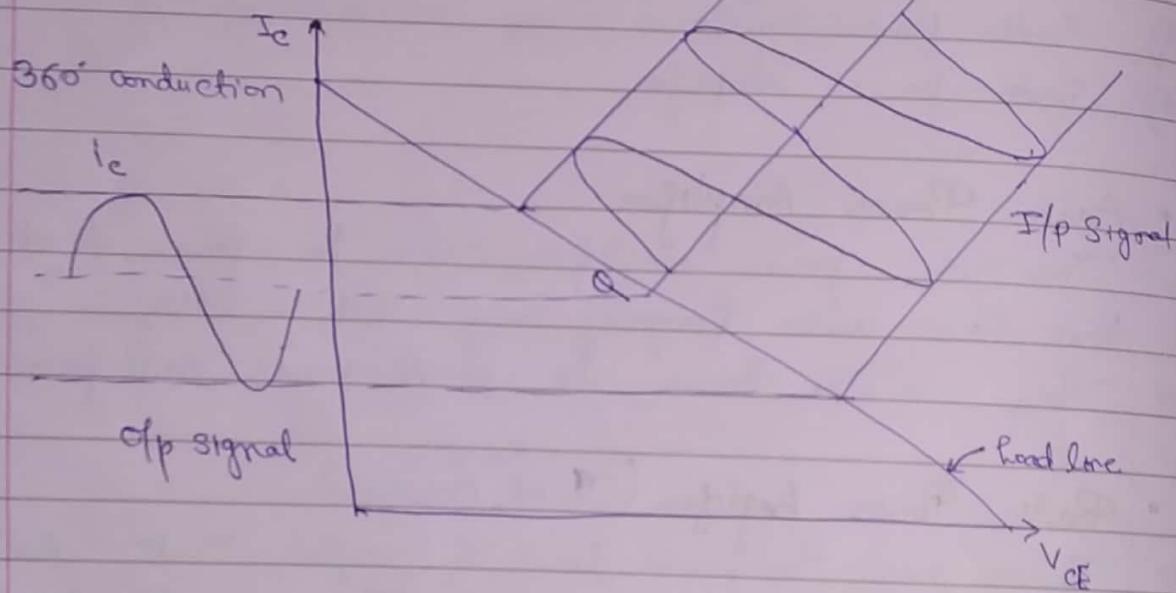
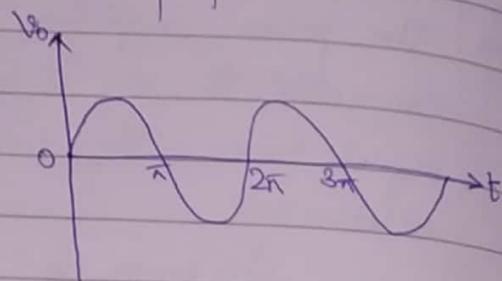
- i) Class A P.A.
- ii) Class B P.A.
- iii) Class C P.A.
- iv) Class AB P.A.

j) Class A P.A.

→ When the collector current flows at all times during the full cycle of input signal, the power amplifier is also known as class A power amplifier.



I/P Signal



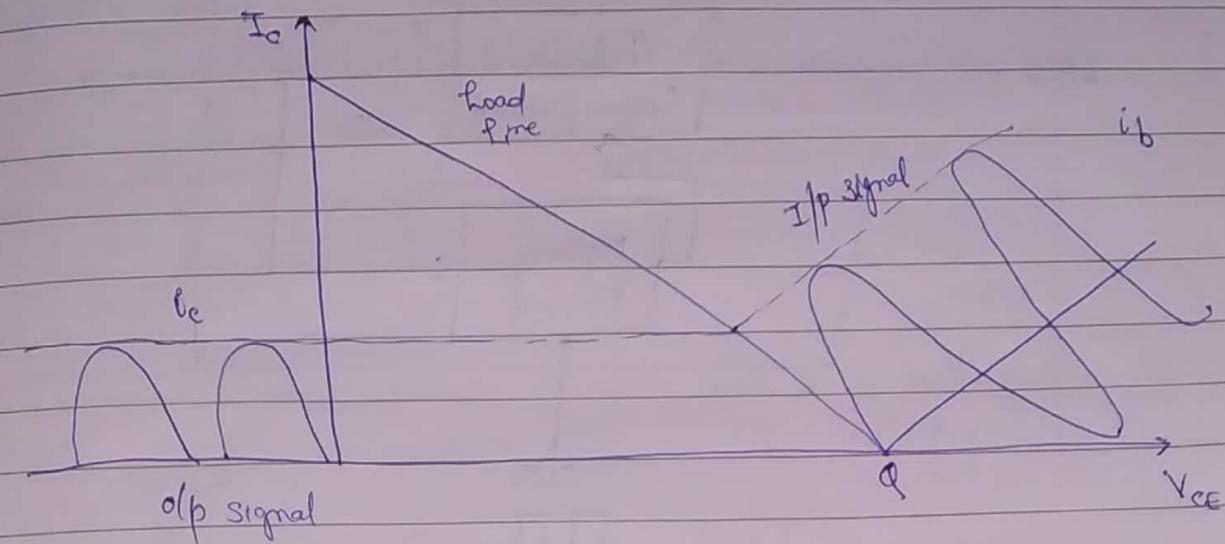
O/p Signal

Load line
 V_{CE}

→ The transistor is to be biased such that o/p current flows for the full cycle of i/p signal (360°) as shown in figure.

ii) Class B P.A.

→ When the collector current flows only during the positive half cycle of I_p signal - the p.a. is known as Class-B p.a.



iii) Class C P.A.

→ When the collector current flows for less than half cycle of I_p signal - the p.a. is known as Class-C p.a.

Note: For part (B) of this unit, refer Pg.no. 82.

2. POWER AMPLIFIERS

(B)

* Series-Fed Class-A Power Amplifier

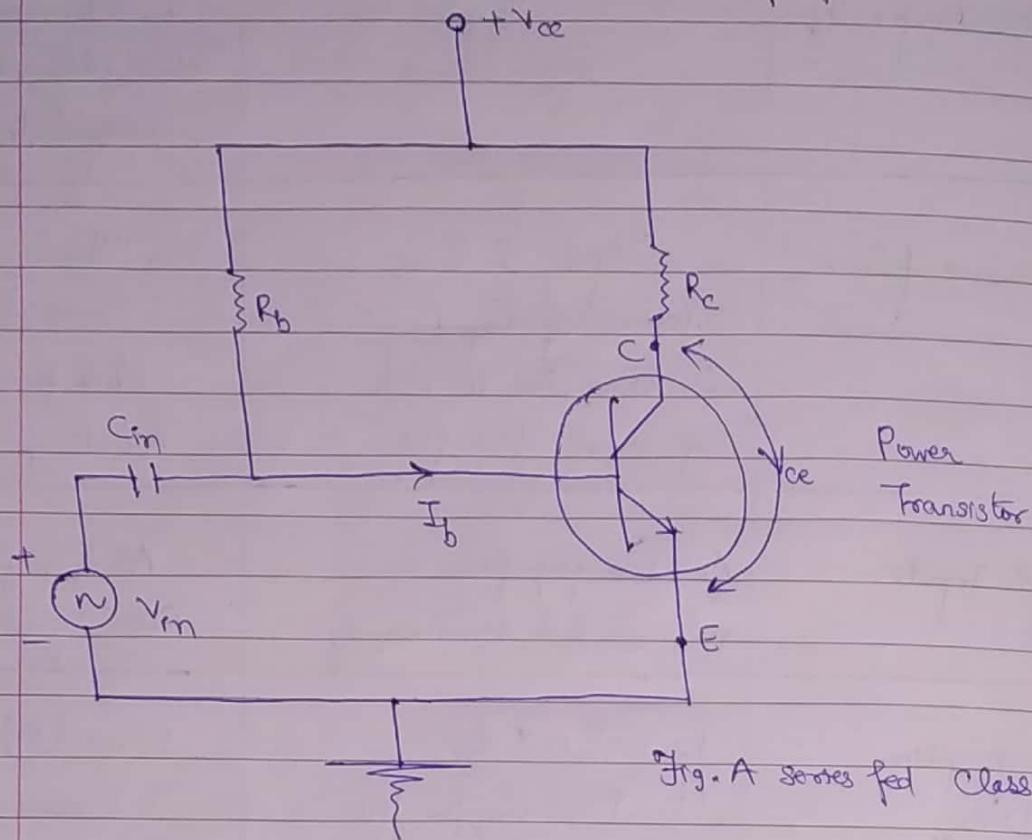


Fig. A series fed Class

→ Power Relations for Class A Power Amplifier

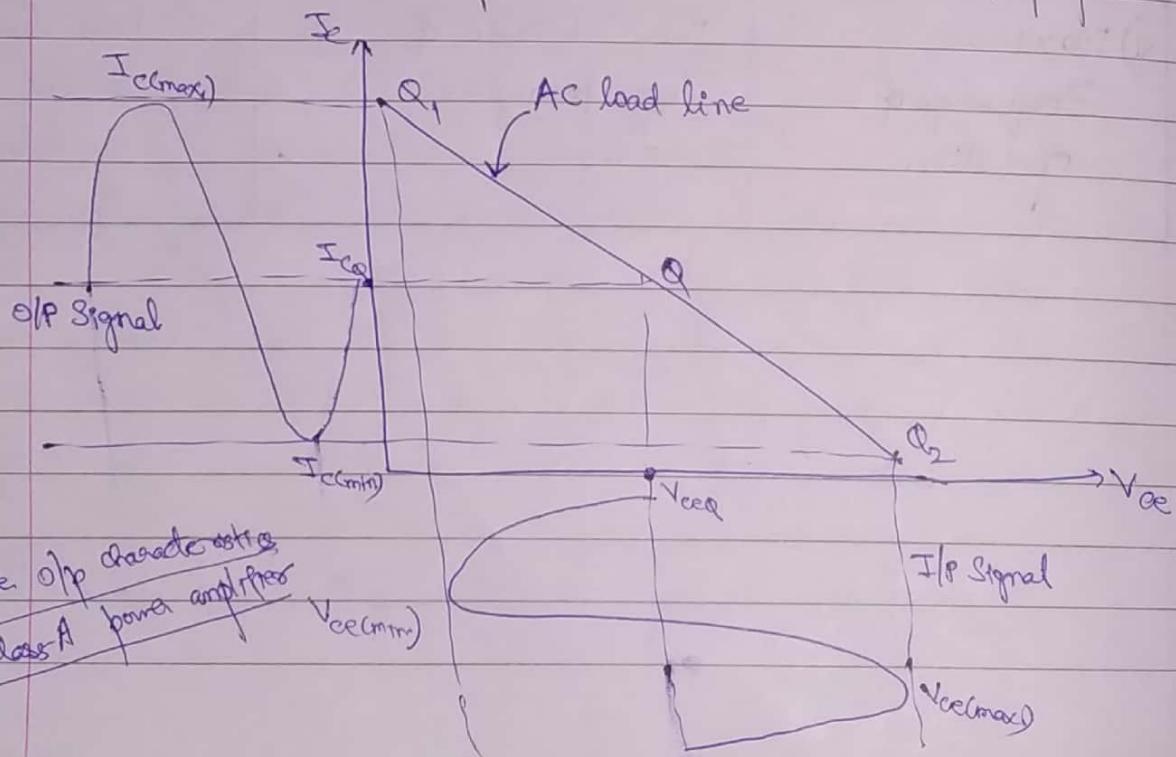


Fig.: The O/P characteristics
for Class A power amplifier

The input power from the collector power supply V_{cc} will be

$$P_{in(dc)} = V_{cc} \cdot I_{CQ} \quad \text{--- (1)}$$

where, I_{CQ} = No signal collector current

Now, this power drawn from the collector power supply is used in two components:

i) Power dissipated in the collector load resistor in the form of heat is given by

$$P_{RC(dc)} = I_{CQ}^2 R_C \quad \text{--- (2)}$$

ii) The power supplied to the transistor is given by

$$P_{tr(dc)} = P_{in(dc)} - P_{RC(dc)} \quad \text{--- (3)}$$

Now, using eq. (1) & (2),

$$P_{tr(dc)} = V_{cc} \cdot I_{CQ} - I_{CQ}^2 R_C \quad \text{--- (4)}$$

Now, this power supplied to the transistor is $P_{tr(dc)}$ is further divided in two parts:

(a) a.c power which is developed across the load resistor

constitute a.c. power output & is given by

$$P_{out(ac)} = \frac{I_c^2 R_C}{2} = \frac{V_{ce}^2}{2 R_C} \quad \text{--- (5)}$$

where, I_c = rms value of collector current

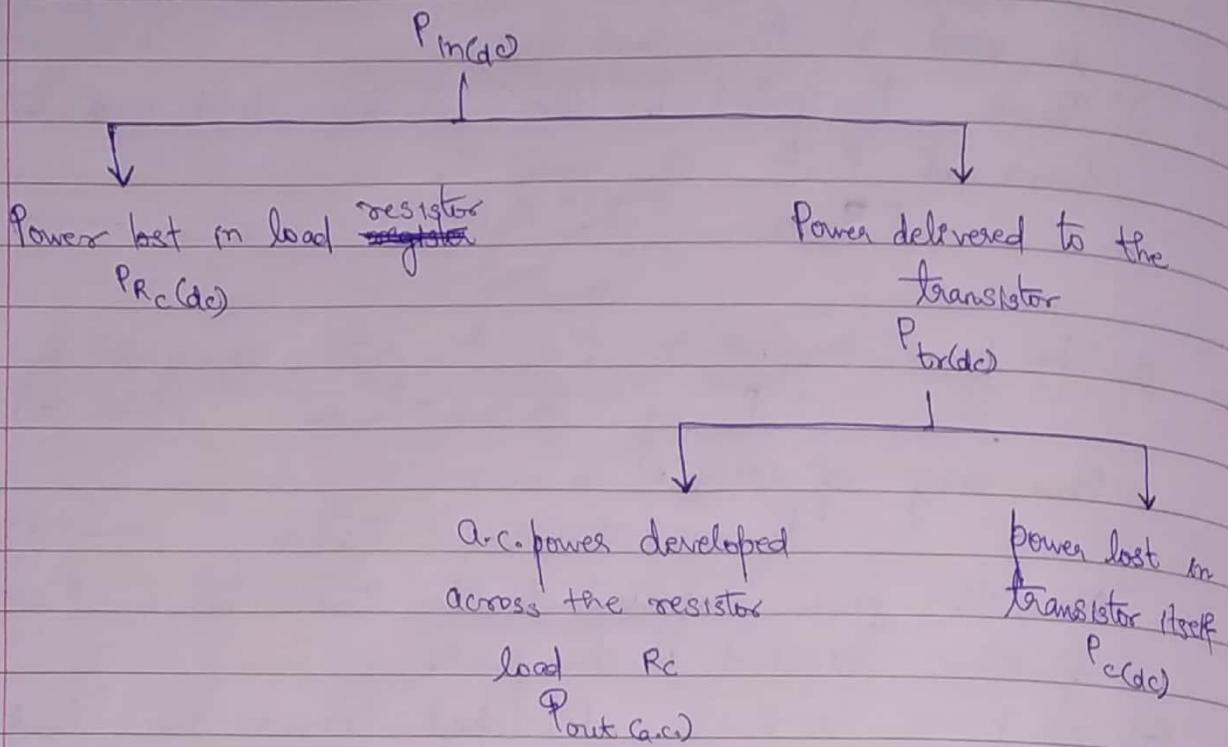
V_{ce} = rms value of collector to emitter voltage

$$\text{Therefore, } P_{out(ac)} = \left(\frac{I_c(\text{max})}{\sqrt{2}} \right)^2 R_C = \frac{V_{ce}(\text{max})^2}{2 R_C} \quad \text{--- (6)}$$

$$\text{Or } P_{out(ac)} = \frac{I_c^2(\text{peak to peak})}{8} = \frac{V_{ce}^2(\text{peak to peak})}{8 R_C} \quad \text{--- (7)}$$

$$\text{Or } P_{out(ac)} = \frac{I_c(\text{peak to peak}) \times V_{ce}(\text{peak to peak})}{8} \quad \text{--- (8)}$$

(b) Power dissipated in the form of heat by the transistor itself. The power distribution in class A power amplifier in the form of a power flow diagram as shown in figure.



Collector Efficiency:

$$\eta_{\text{collector}} = \frac{\text{Average a.c. power o/p} (P_{out(a.c.)})}{\text{Average d.c. power i/p to transistor} (P_{tr(dc)})}$$

14.03.19

- Expression for power efficiency of Class-A power amplifier
- A measure of the ability of an active device to convert the d.c. power of supply into the a.c. (signal). Power delivered to the load is known as the power efficiency or conversion efficiency or theoretical efficiency. It is simply denoted by η .

$\eta = \frac{\text{a.c. power delivered to the load, } P_{\text{out(a.c.)}}}{\text{Total power drawn from d.c. supply, } P_{\text{in(d.c.)}}} \quad (1)$

The a.c. power delivered to the load is equal to

$$P_{\text{out(a.c.)}} = \frac{I_c(\text{peak to peak}) \times V_{ce}(\text{peak to peak})}{8} \quad (2)$$

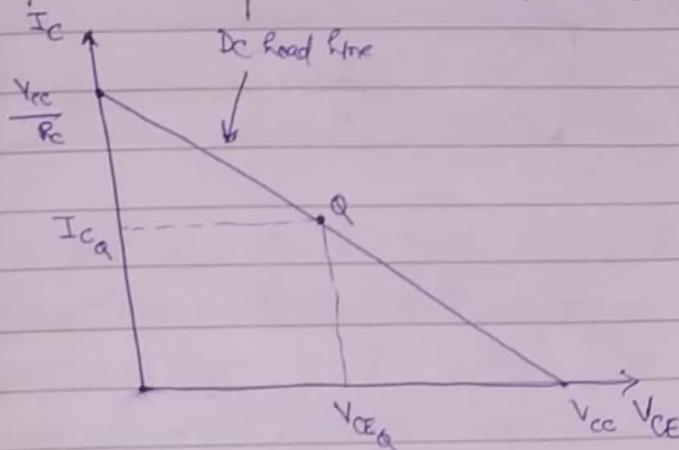
$$(2) \quad P_{\text{out(a.c.)}} = \frac{(I_{c_{\text{max}}} - I_{c_{\text{min}}}) \times (V_{c_{\text{emax}}} - V_{c_{\text{min}}})}{8} \quad (2)$$

$$P_{\text{in(d.c.)}} = V_{cc} \cdot I_{ca} \quad (3)$$

Comparing eq. (1), (2) & (3) we get

$$\eta = \frac{(I_{c_{\text{max}}} - I_{c_{\text{min}}}) \times (V_{c_{\text{emax}}} - V_{c_{\text{min}}})}{8 V_{cc} \cdot I_{ca}}$$

Evaluation of maximum power and efficiency



If the operating point Q is set at the mid-point of maximum signal swing, then the resulting max^m power condition can be obtained.

$$\text{Maximum } V_{ce}(\text{peak to peak}) = V_{cc}$$

$$\text{Maximum } I_{CE}(\text{peak to peak}) = \frac{V_{CC}}{R_C}$$

→ The maximum a.c. power developed across the load resistor will be

$$P_{out(a.c.)\max.} = \frac{1}{8} \cdot \frac{V_{CC}}{R_C} \times V_{CC} = \frac{V_{CC}^2}{8R_C} \quad (1)$$

For the Q-point, we have

$$I_{CQ} = \frac{V_{CC}}{R_C / 2} \quad (2)$$

& the d.c. power drawn from d.c. power supply will be

$$\begin{aligned} P_{in(d.c.)\max.} &= V_{CC} \cdot I_{CQ} \\ &= V_{CC} \times \frac{V_{CC}}{2R_C} \end{aligned}$$

$$P_{in(d.c.)\max.} = \frac{V_{CC}^2}{2R_C} \quad (3)$$

$$\therefore \eta_{\max.} = \frac{1}{4} = 0.25 = 25\%$$

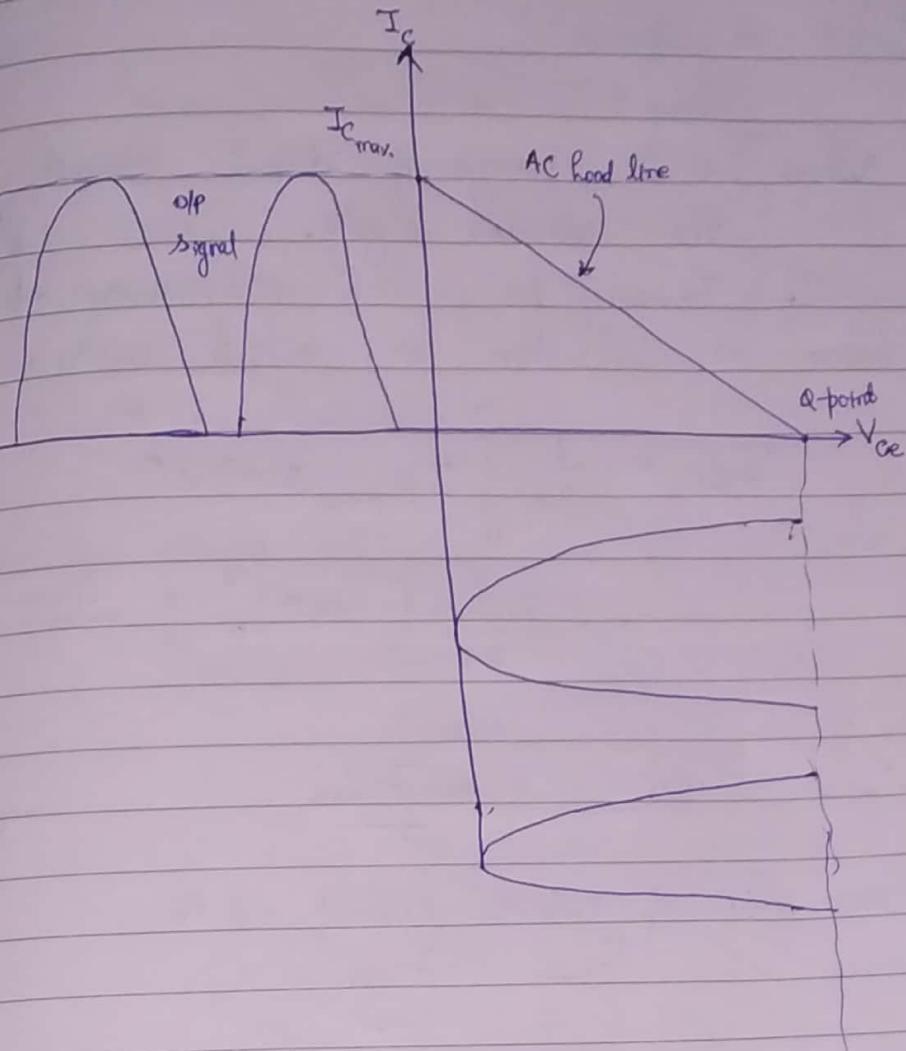
Thus, this is max. % efficiency for a series fed class-A power amplifier. Because, this max. efficiency would occur only when ideal conditions are fulfilled, & the max. a.c. signal swings. ∴ most series fed class-A power amplifier have power efficiency much less than 25%.

Prob:

A power transistor working in class A operation has zero signal power dissipation of 8 watts. If the a.c. power output is 2 watts, then, find the collector efficiency &

be power rating of ~~thyristor~~ transistor
25%.

CLASS-B POWER AMPLIFIER



→ In a class-B operation, the transistor is biased in such a way so that the zero signal collector current is zero. This means that the class-B operation doesn't need any biasing system. The operating point is set at cut-off as shown in figure. It remains forward-biased for only half cycle of the input signal. During the (+)ve half cycle of the input a.c. signal, the circuit is forward-biased and hence collector current flows. During the half cycle of the input a.c. signal, the circuit is reverse-biased & no

collector current flows.

- Calculation of Power and Efficiency of class-B power amplifier

→ Input d.c. power:

$$P_{\text{in dc}} = V_{\text{cc}} I_{\text{dc}}$$

Where, I_{dc} is Average of direct current taken from the collector supply.

If I_{cmax} is the maximum or peak value of collector or output current. Then,

$$\begin{aligned} I_{\text{dc}} &= \frac{1}{2\pi} \int_0^{\pi} I_{\text{cmax}} \sin \theta d\theta \\ &= \frac{I_{\text{cmax}}}{2\pi} [-\cos \theta]_0^{\pi} = \frac{I_{\text{cmax}}}{\pi} \end{aligned}$$

$$\therefore P_{\text{in dc}} = \frac{V_{\text{cc}} \cdot I_{\text{cmax}}}{\pi} \quad \text{--- (1)}$$

Rms value of collector current will be

$$I_{\text{c rms}} = \frac{I_{\text{cmax}}}{\sqrt{2}}$$

Rms value of output voltage will be

$$V_{\text{o rms}} = \frac{V_{\text{cc}}}{\sqrt{2}}$$

Hence, output power during half-cycle will be

$$P_{\text{out dc}} = \frac{1}{2} \frac{I_{\text{cmax}}}{\sqrt{2}} \times \frac{V_{\text{cc}}}{\sqrt{2}}$$

$$P_{\text{out dc}} = \left(\frac{1}{2}\right)^2 I_{\text{cmax}} \cdot V_{\text{cc}} = \frac{1}{4} I_{\text{cmax}} V_{\text{cc}} \quad \text{--- (2)}$$

In above equation factor $\frac{1}{2}$ is used because power is developed during first one half-cycle only.

d.c. power loss in load is given by

$$P_{R_{load}} = I_{dc.}^2 R_c = \left(\frac{I_{cmax}}{\pi} \right)^2 R_c \quad (3)$$

Also, d.c. power loss in collector region of transistor is given by

$$P_m(d.c) = P_{R_C(d.c)} + P_{out(d.c)} \quad (4)$$

Therefore, the overall efficiency can be calculated as

$$\begin{aligned} \eta_{overall} &= \frac{P_{out(d.c)}}{P_{m(d.c)}} \\ &= \frac{I_{cmax} V_{cc}/4}{I_{cmax} V_{cc}/\pi} = \frac{\pi}{4} \\ &= 0.785 \end{aligned}$$

$$\boxed{\eta_{overall} = 78.5\%}$$

A transformer coupled A-power amplifier draws a current of 200mA from a collector supply of 10V, when no signal is applied to it, determine

- Max. o/p power
- Max. collector efficiency
- Power rating of the transistor, if the load connected across the transformer secondary is of 2Ω & transformer turn ratio is 5:1.

Sol - i) Max. o/p power

$$(P_o)_{ac} = \frac{V_{ce} \times I_{Co}}{2}$$

$$= \frac{10V \times 200mA}{2}$$

$$\boxed{(P_o)_{ac} = 1W} \quad \text{Ans}$$

$$\text{ii) Max. collector efficiency} = \frac{(P_o)_{ac}}{(P_{tr})_{dc}}$$

$$= \frac{1W}{2 \times 1W}$$

$$\boxed{\eta_{\text{collector}} = 50\%} \quad \text{Ans}$$

iii)

$$n = 5:1$$

$$R_L = 2\Omega$$

$$R'_L = n^2 R_L$$

$$\boxed{R'_L = 50\Omega}$$

$$\text{Power rating} = I^2 R'_L$$

$$= (200mA)^2 \cdot 50\Omega$$

$$\boxed{P.R. = 2W} \quad \text{Ans}$$

15.03.19

* CLASS AB POWER AMPLIFIER

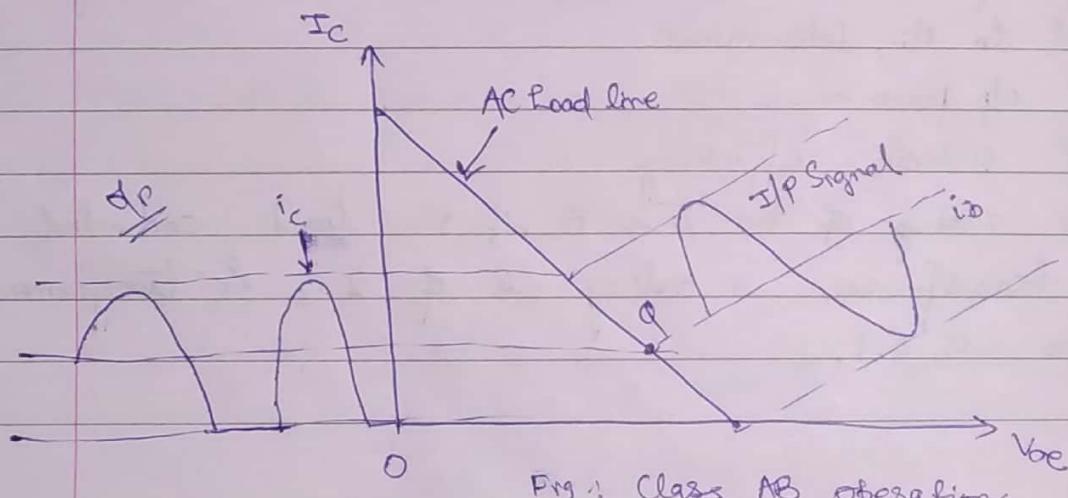


Fig : Class AB operation

In class AB power amplifier, the biasing ckt. is so adjusted that the operation point Q lies near the cut-off voltage. During small operation of the half cycle can or complete one half cycle of the signal the input ckt remain forward biased, hence, collector current flows, but during small portion C less than half cycle of the entire cycle, the input circuit is reverse biased & therefore no collector current flows during the period.

Class AB operation needs a push-pull connection to achieve a full output cycle.

Ques: A transformer coupled class-A large amplifier has maximum & minimum values of collector-emitter voltage of 25V & 2.5V. Determine its collector efficiency.

$$\eta_{\text{collector}} = 50 \times \frac{V_{c\text{emax}} - V_{c\text{emin}}}{V_{c\text{emax}} + V_{c\text{emin}}}$$

$$= 50 \times \frac{22.5V}{27.5V}$$

$$\boxed{\eta_{\text{collector}} = 40.9\%} \quad \underline{\text{Ans}}$$

Ques: A transformer-coupled class A power amplifier supplies the power to an 80Ω load connected across the secondary of a step-down transformer having turn ratio 5:1. Determine the maximum power off for a signal collector current of 120mA

$$R_L = 80\Omega$$

$$R'_L = 2000\Omega$$

$$\left(\frac{I^2 R'_L}{2} \right) = \frac{28.8 W}{2} = 14.4 W \quad \underline{\text{Ans}}$$