INDIAN INSTITUTE OF TECHNOLOGY KHARAGPUR

DEPARTMENT OF COMPUTER SCIENCE & ENGINEERING

Report

Verilog Assignment-1 : Part-2

Computer Organization and Architecture Laboratory

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1. 4-bit Carry Look-ahead Adder

Problem statement

- Design a 4-bit CLA. Clearly state, the Boolean equations of the Look-ahead carry generation for the 4 carry bits, C1, C2, C3, and C4 in terms of the generate and propagate signals, denoted as G0, . . . , G3 and P0 . . . , P3 respectively. Also state the equations for the corresponding generate and propagate signals.

Circuit Diagram

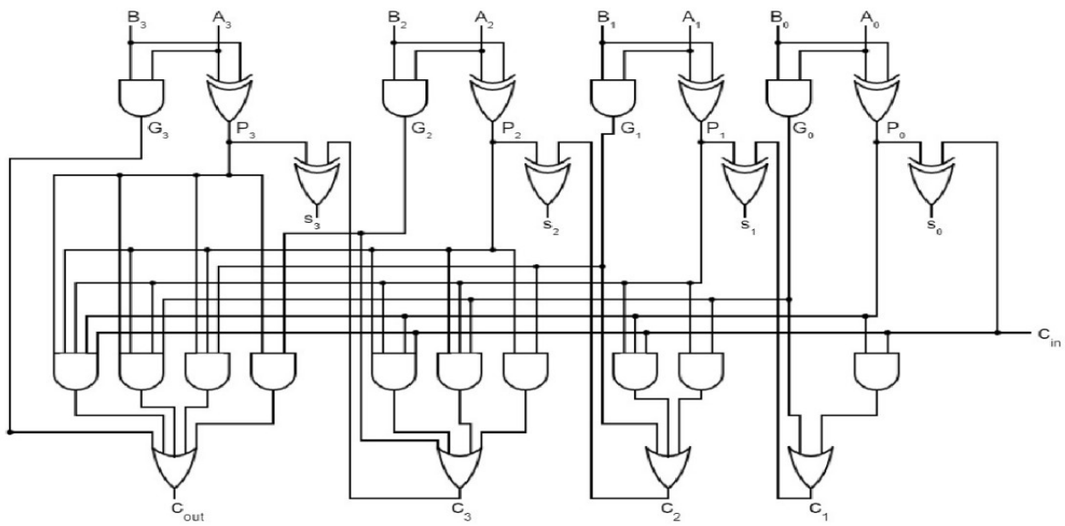

Figure 1: 4 bit CLA

Description

Boolean equations of the Look-ahead carry generation for the 4 carry bits:

$C_1 = G_0 + P_0 C_{in}$

$C_2 = G_1 + P_1 G_0 + P_1 P_0 C_{in}$

$C_3 = G_2 + P_2 G_1 + P_2 P_1 G_0 + P_2 P_1 P_0 C_{in}$

$C_{out} = G_3 + P_3 G_2 + P_3 P_2 G_1 + P_3 P_2 P_1 G_0 + P_3 P_2 P_1 P_0 C_{in}$

Equations for the corresponding generate and propagate signals:

for each i-th bit (i= 0,1,2,3) :

Carry generate $\Rightarrow \mathrm{G}_i = A_i \wedge B_i$

Carry propagate $\Rightarrow \mathrm{P}_i = A_i \oplus B_i$

2. Comparing the speed of 4-bit CLA with 4-bit RCA

Delay	**4-bit RCA**	**4-bit CLA**
Logic	0.249 ns	0.249
Route	1.874 ns	1.874
Total	2.123 ns	2.123

In the code of 4-bit CLA, we have used 'assign' function so its delay is more than expected. When we use simple gates instead of the 'assign' function, the delay will be lower as expected. Hence the delay for 4-bit Carry Look-ahead Adder will be less than 4-bit Ripple Carry Adder.

3. 16-bit Carry Look-ahead Adder

(i) 4-bit Carry Look-ahead Adder (Augmented)

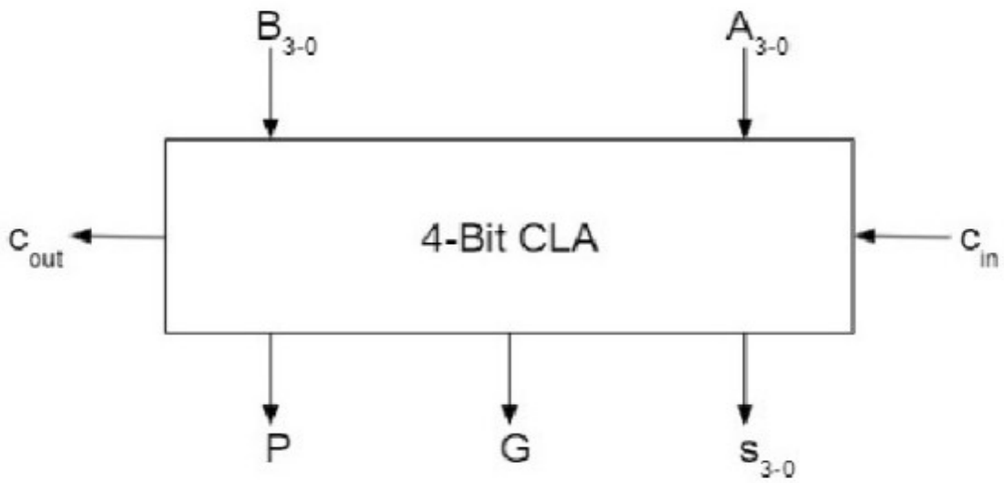

Figure 2: 4 bit CLA (Augmented)

(ii) The Hierarchical Structure of a 16-bit CLA

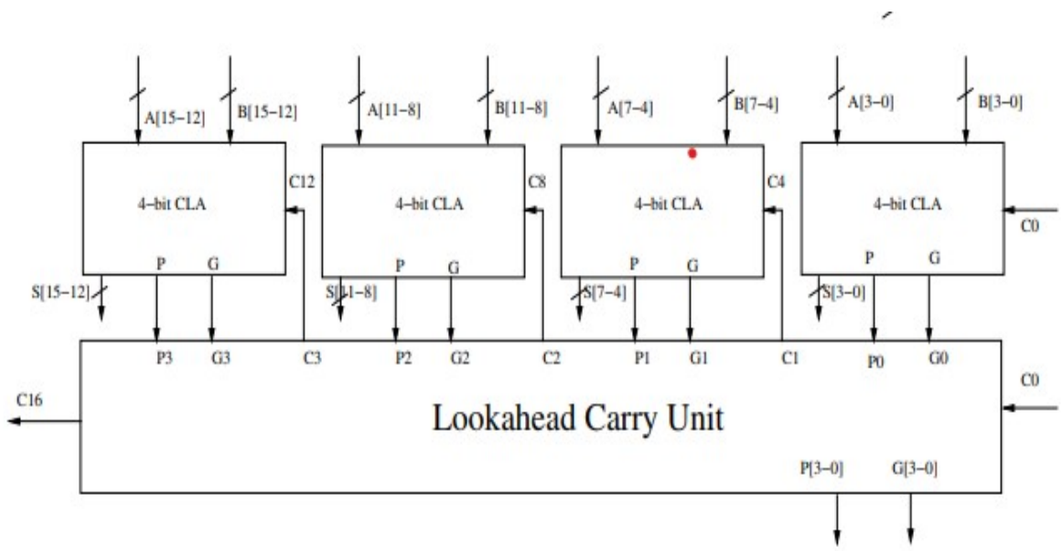

Figure 3: The Hierarchical Structure of a 16-bit CLA

(iii) 16-bit CLA (Ripple Carry out)

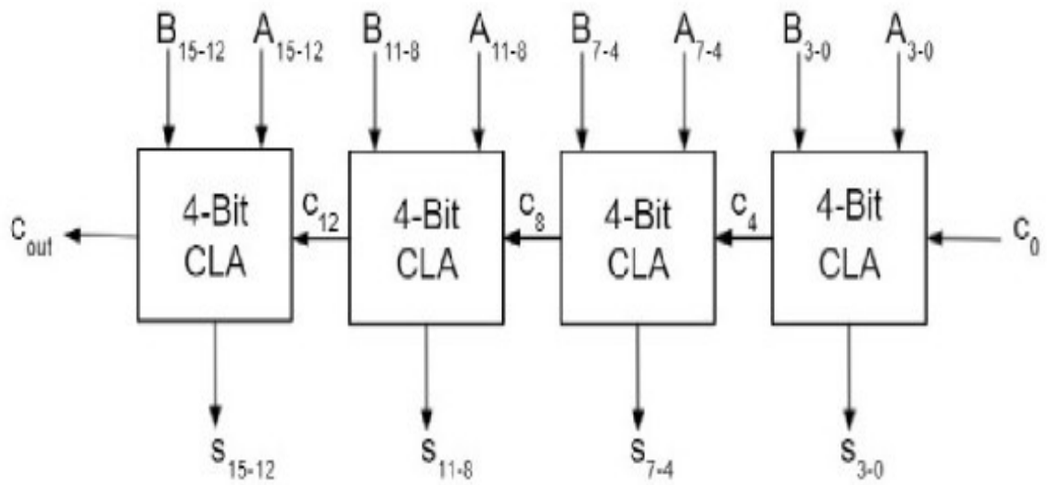

Figure 4: 16-bit CLA (Ripple Carry out)

Comparison		
	Delay	**Number of Slice LUTs**
16-bit CLA (Ripple carry-out)	6.197 ns	24
16-bit CLA (look-ahead carry unit)	5.513 ns	45

(iv) Speed Comparison

Comparing the 16-bit CLA with 16-bit RCA		
	Delay	**Number of Slice LUTs**
16-bit RCA	6.167 ns	24
16-bit CLA	5.513 ns	45

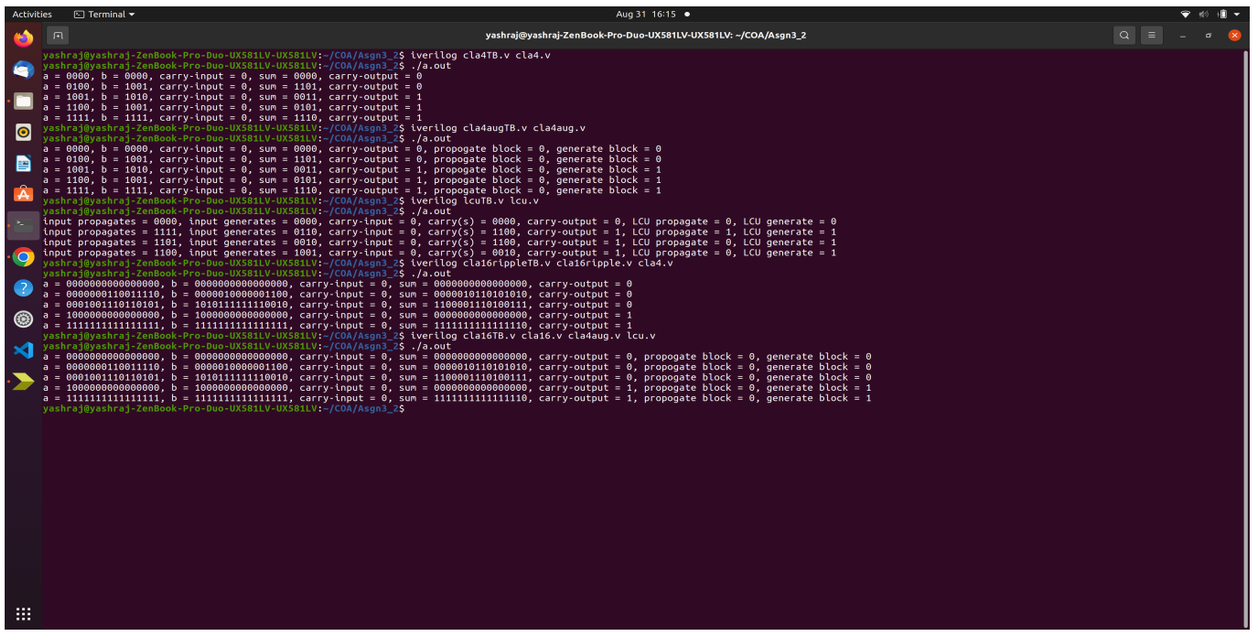

Figure 5: Output after executing Test Benches on all Verilog Files