INDIAN INSTITUTE OF TECHNOLOGY KHARAGPUR

DEPARTMENT OF COMPUTER SCIENCE & ENGINEERING

Report

Verilog Assignment-2

Computer Organization and Architecture Laboratory

Group No. 24

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1. Behavioral Design of Binary Counter

For this question, we have used the behavioral ideology to design the 4-bit Binary Up-Counter. Initially we designate “0” to our count variable and we keep incrementing it in every clock cycle. Also, we had a “reset” variable, which when set to “1” will again make out count variable “0”. We have also implemented the functionality that after the counter reaches 15, which is its maximum value, it again goes back to “0”.

To increment the counter value after every clock cycle, we have used the ’always’ block in our Verilog code. Inside it we have used the if-else-if construct of Verilog to either increment the counter value or make it ”0” again if the counter has reached its maximum value or it has been reset.

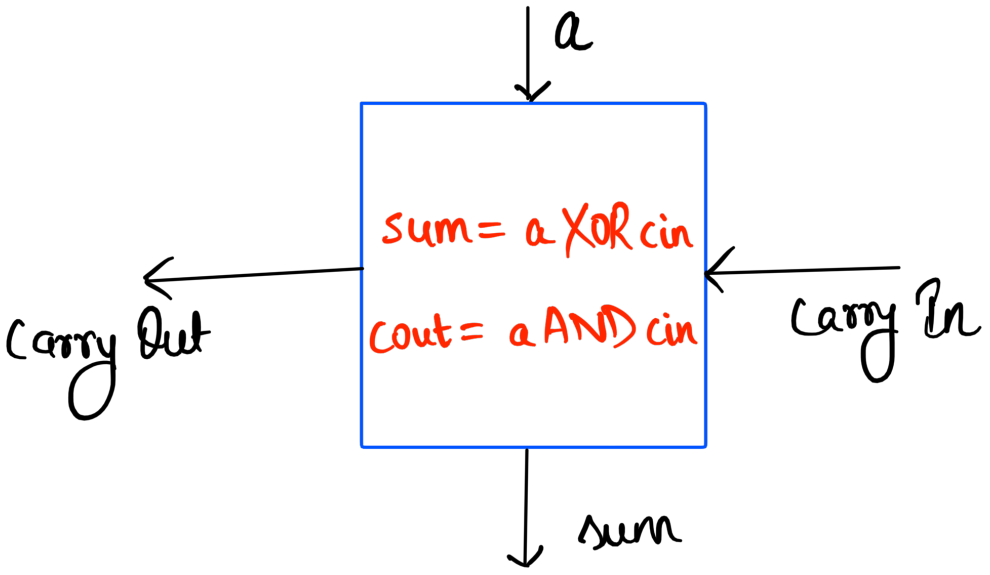
2. Structural Design of Binary Counter

We optimized the Ripple carry Adder to increment the count by one each time. For optimizing we solved the equations of the full adder.
$Sum = C_{in} \oplus A \oplus B$
$C_{out} = (A \wedge B) \vee (C_{in} \wedge (A \oplus B))$
Put $B = 0$ in this equations , we get
$Sum = C_{in} \oplus A$
$C_{out} = C_{in} \wedge A$

Following pages shows the Architecture of our 4-Bit asynchronous binary up counter....

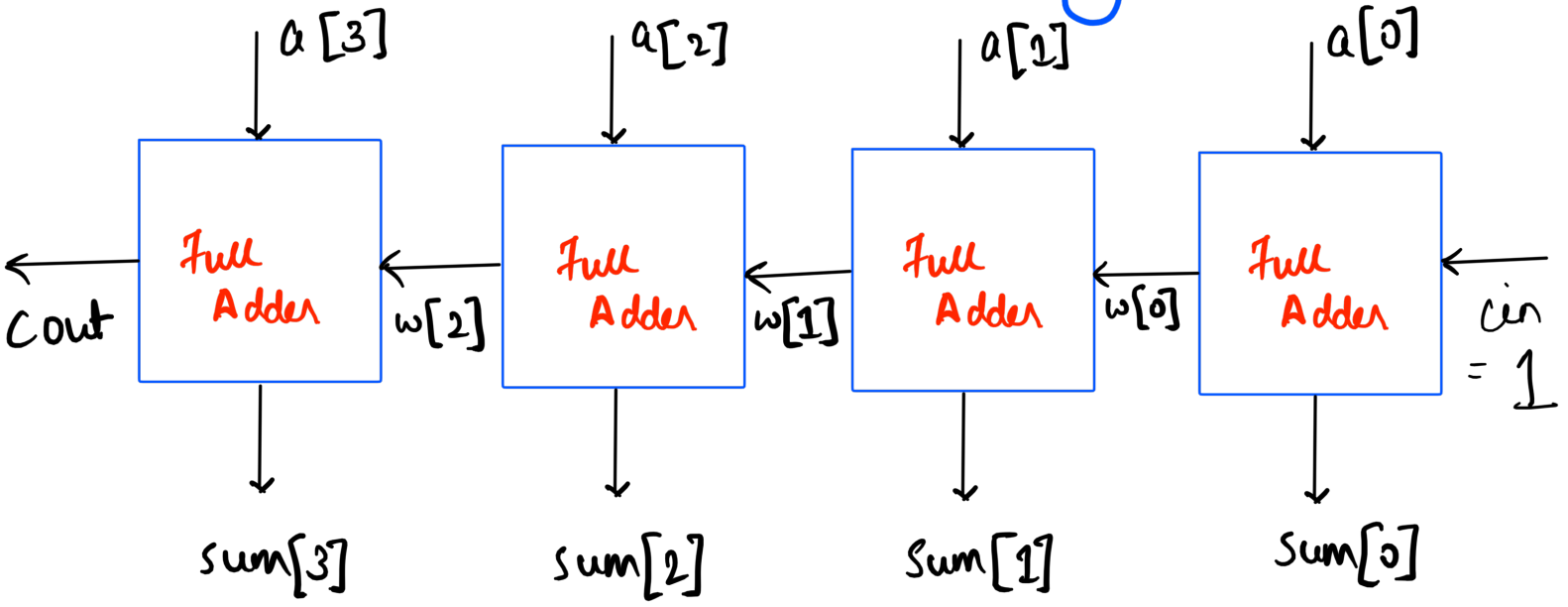
- Full Adder

  Optimised for adding 1



- Ripple Carry Adder

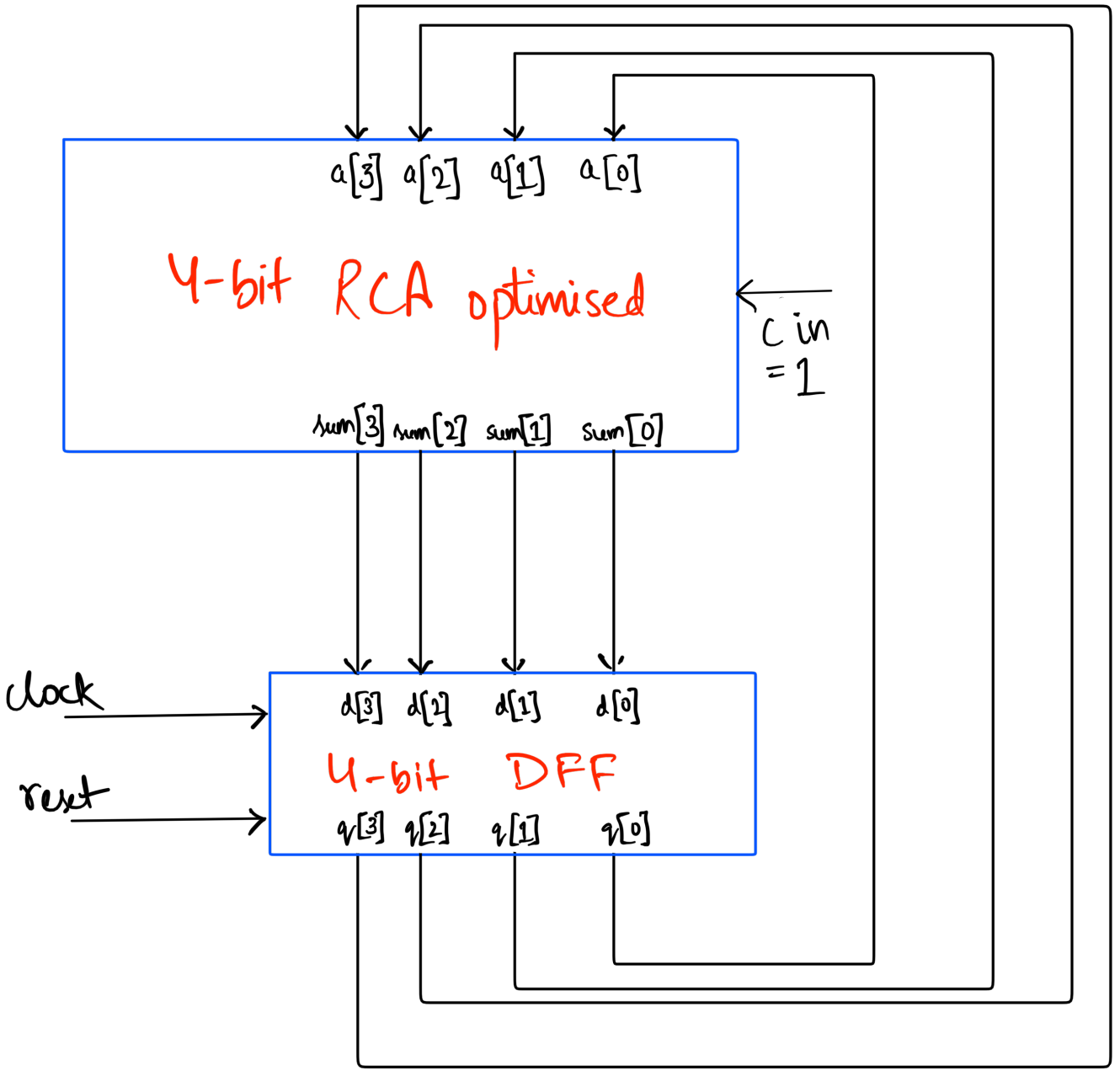
  Optimised for adding 1 in a 4-bit binary number



- Binary Upcounter

In this we have used a 4-bit D-Flip Flop designed by us.

It is same as a 1-bit D-FlipFlop but has a 4-bit input 'd' and a 4-bit output 'q'.



- The Top module along with the clock divider