National University of Computer and Emerging Sciences

Karachi Campus

Digital Logic Design (EE1005)

Final Exam

Date: May 26th , 2025

Total Time: 3Hrs

Total Marks: 50

Total Questions: 6

Course Instructor(s)

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Roll No _____ Section _____ Student Signature _____

Attempt all the questions.

CLO # 1 Understand the knowledge of number systems and their operations [5 marks]

Q1(a) Convert decimal 28_{10} and 31_{10} to Gray code. [2]

- **28_{10} → Gray code = 10010_2**
- **31_{10} → Gray code = 10000_2**

(b) Express the decimal number -239 as an 8-bit number in the sign-magnitude, 1's complement, and 2's complement forms. [3]

ign-Magnitude 111101111 ❌ (9 bits, invalid!)

✅ So: **239 can't be represented in 8-bit sign-magnitude!**

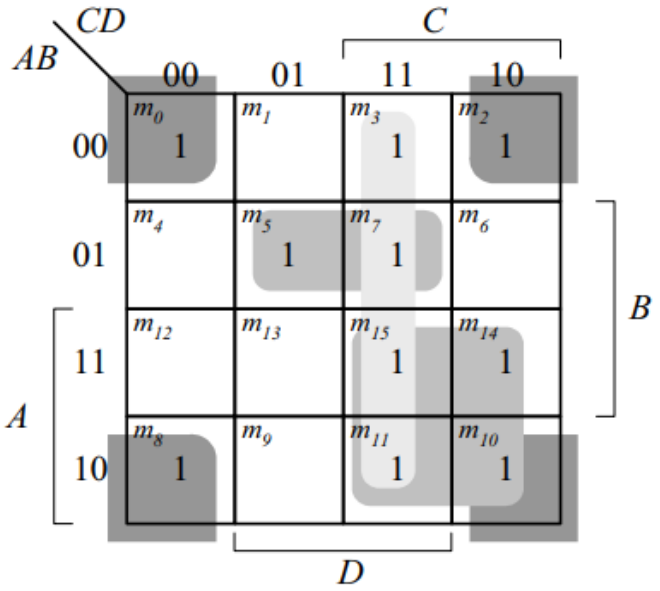
1's Complement 00010000

2's Complement 00010001

CLO # 2 Techniques to design logic circuits. [10 marks]

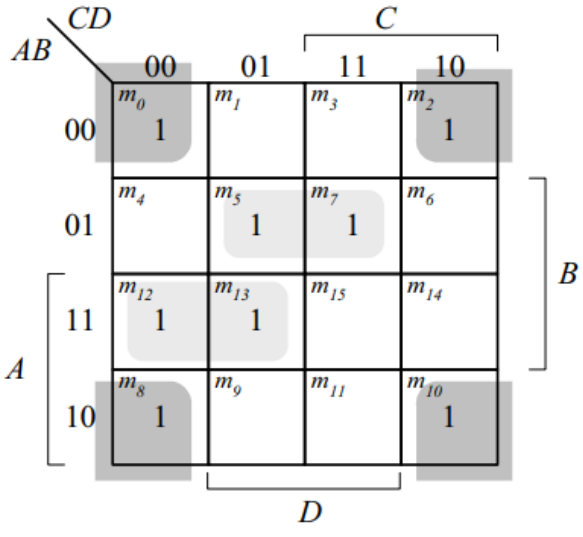
Q2:(a) Simplify the following Boolean expressions, using four-variable K-maps only, without creating truth table: [3]

i) $A\bar{B}C + \bar{B}\bar{C}\bar{D} + BCD + AC\bar{D} + \bar{A}\bar{B}C + \bar{A}B\bar{C}D$



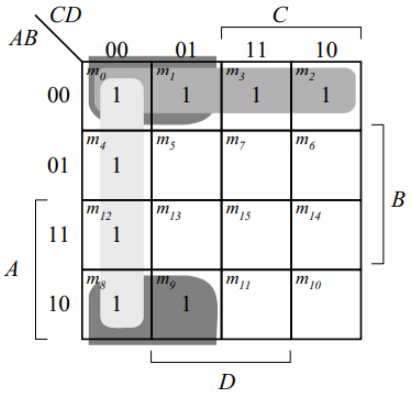
(c) $F = B'D' + AC + A'BD + CD \text{ (or } B'C)$

ii) $\bar{A}\bar{B}\bar{C}\bar{D} + A\bar{C}\bar{D} + \bar{B}C\bar{D} + \bar{A}BCD + B\bar{C}D$

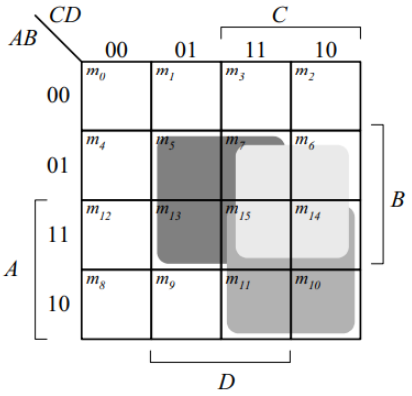


(a) $F = B'D' + A'BD + ABC'$

b) Implement NAND-NAND and OR-NAND for the following function: [3]
F[A, B, C, D] = ∑{0, 1, 2, 3, 6, 10, 11, 14}

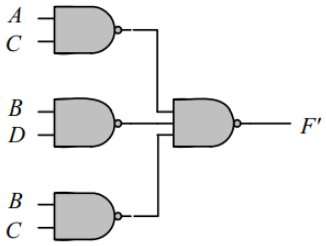


$F = A'B' + C'D' + B'C'$



$F' = BC + AC + BD$

$F = (BC)'(AC)'(BD)'$

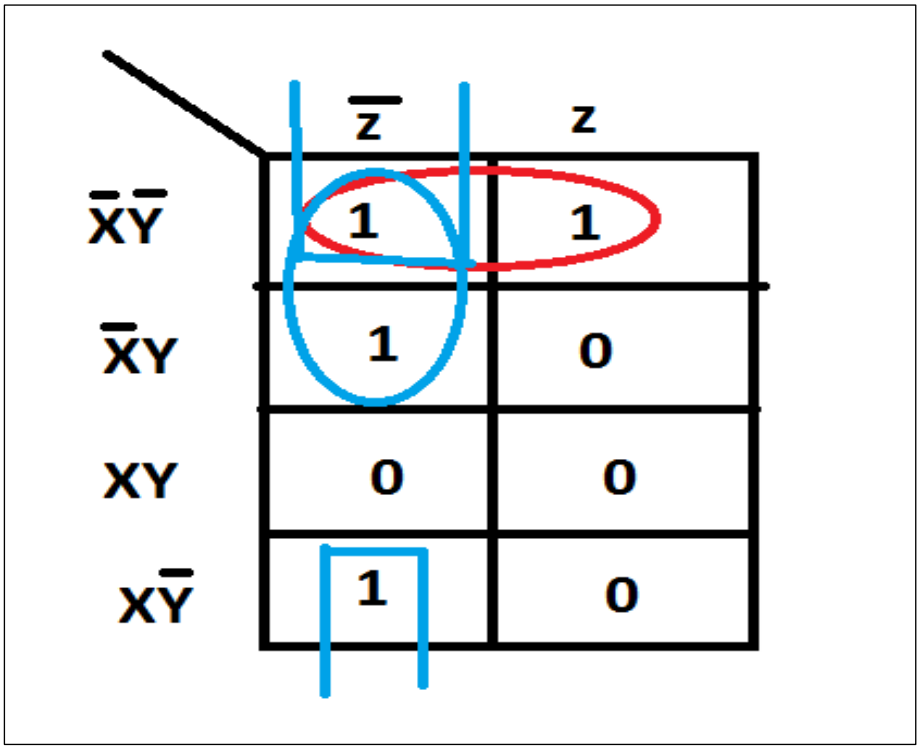


c) In a water pumping station there are three pumps (x, y, z) that are to be monitored. If x=1 it implies that pump x is on and working. You are required to design a combinational circuit to raise an alarm when the majority of the pump fails. Derive the minimal Boolean expression for this combinational circuit using K-map and construct the logical circuit diagram. [4]

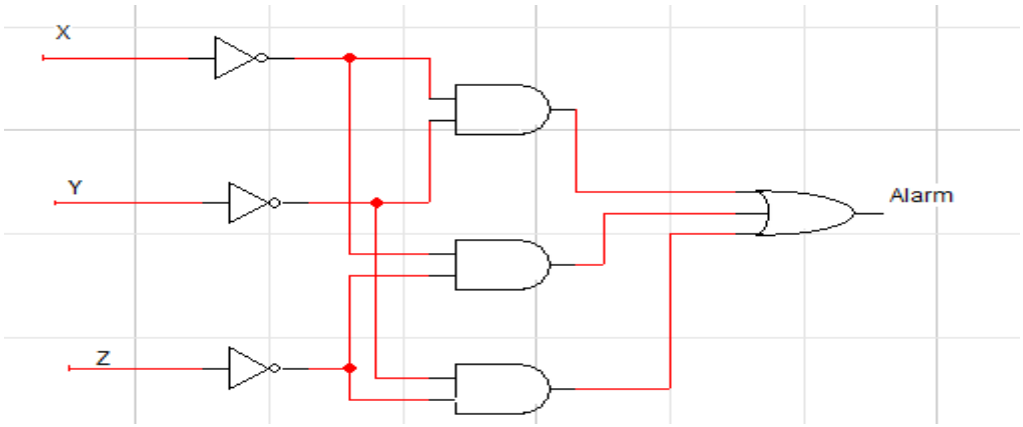
Truth Table

X	Y	Z	Alarm
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	0

K-map



Equation: X'Y' + X'Z' + Y'Z'

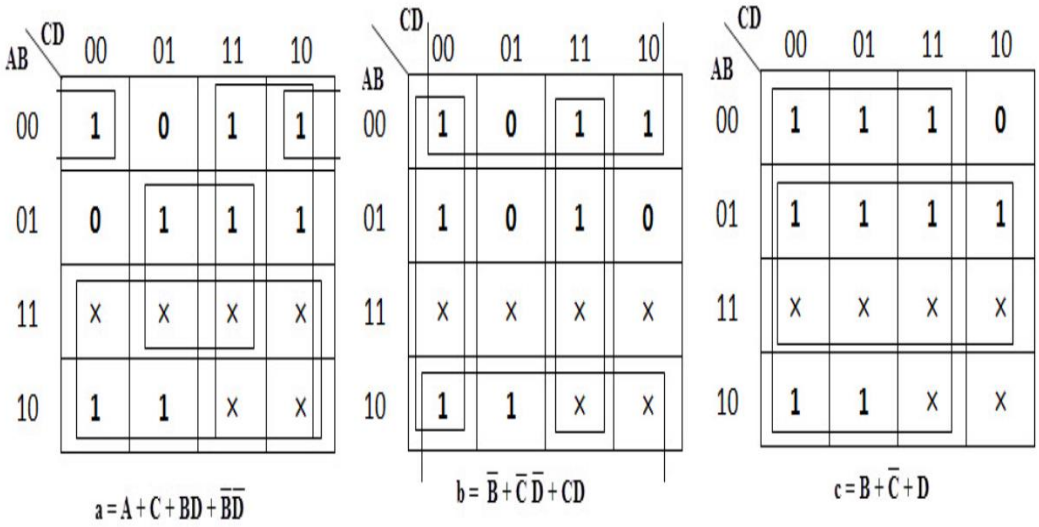


CLO # 3 Analyze small –scale combinational digital circuits. [10 marks]

Q3 (a) Design a simplified Digital Logic Circuit for a BCD to 7-Segment Decoder. [3]
Following steps are required.
(i) Find the truth table. (Input variables are D3 D2, D1 and D0)
(ii) Plot the K-Maps ONLY for outputs segment a,b and c.
(iii) Simplify the K-Maps output functions in sum of product (SOP) form.

Truth Table for 7 Segment Decoder

Decimal Digit	Input lines				Output lines							Display pattern
	A	B	C	D	a	b	c	d	e	f	g	
0	0	0	0	0	1	1	1	1	1	1	0	
1	0	0	0	1	0	1	1	0	0	0	0	
2	0	0	1	0	1	1	0	1	1	0	1	
3	0	0	1	1	1	1	1	1	0	0	1	
4	0	1	0	0	0	1	1	0	0	1	1	
5	0	1	0	1	1	0	1	1	0	1	1	
6	0	1	1	0	1	0	1	1	1	1	1	
7	0	1	1	1	1	1	1	0	0	0	0	
8	1	0	0	0	1	1	1	1	1	1	1	
9	1	0	0	1	1	1	1	1	0	1	1	



(b) The full-adder in Fig-1 is tested under all input conditions with the input waveforms shown. From your observation of the $\sum$ and C_{out} waveforms, is it operating properly, and if not, what is the most likely fault? [2]

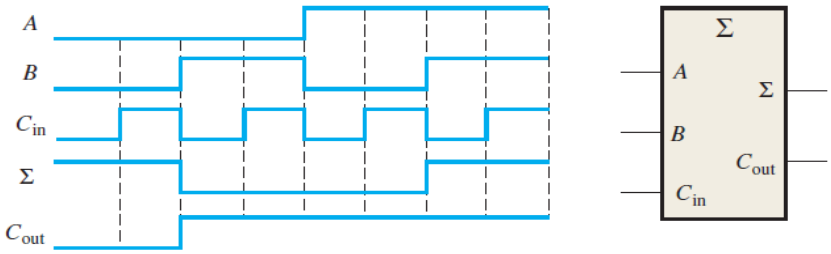
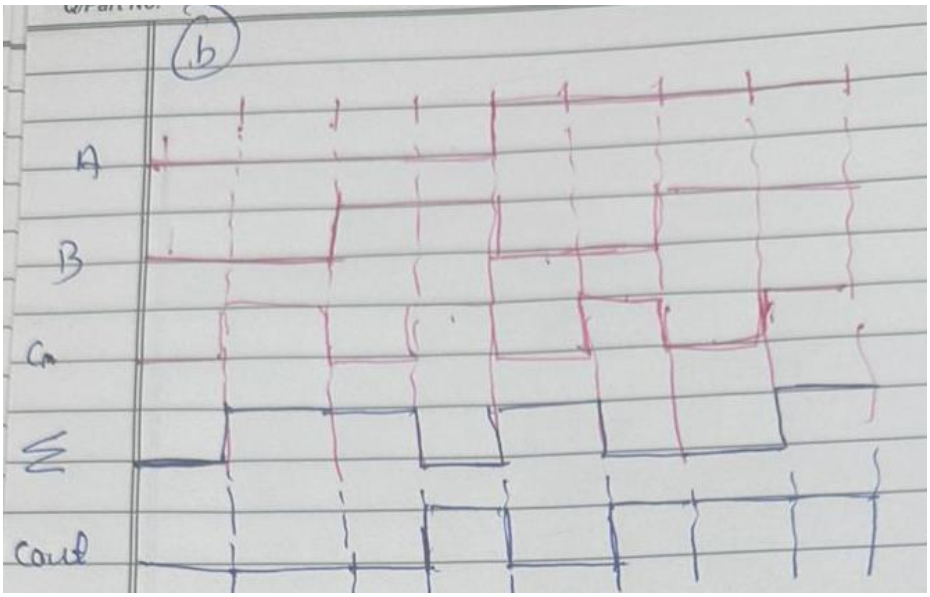
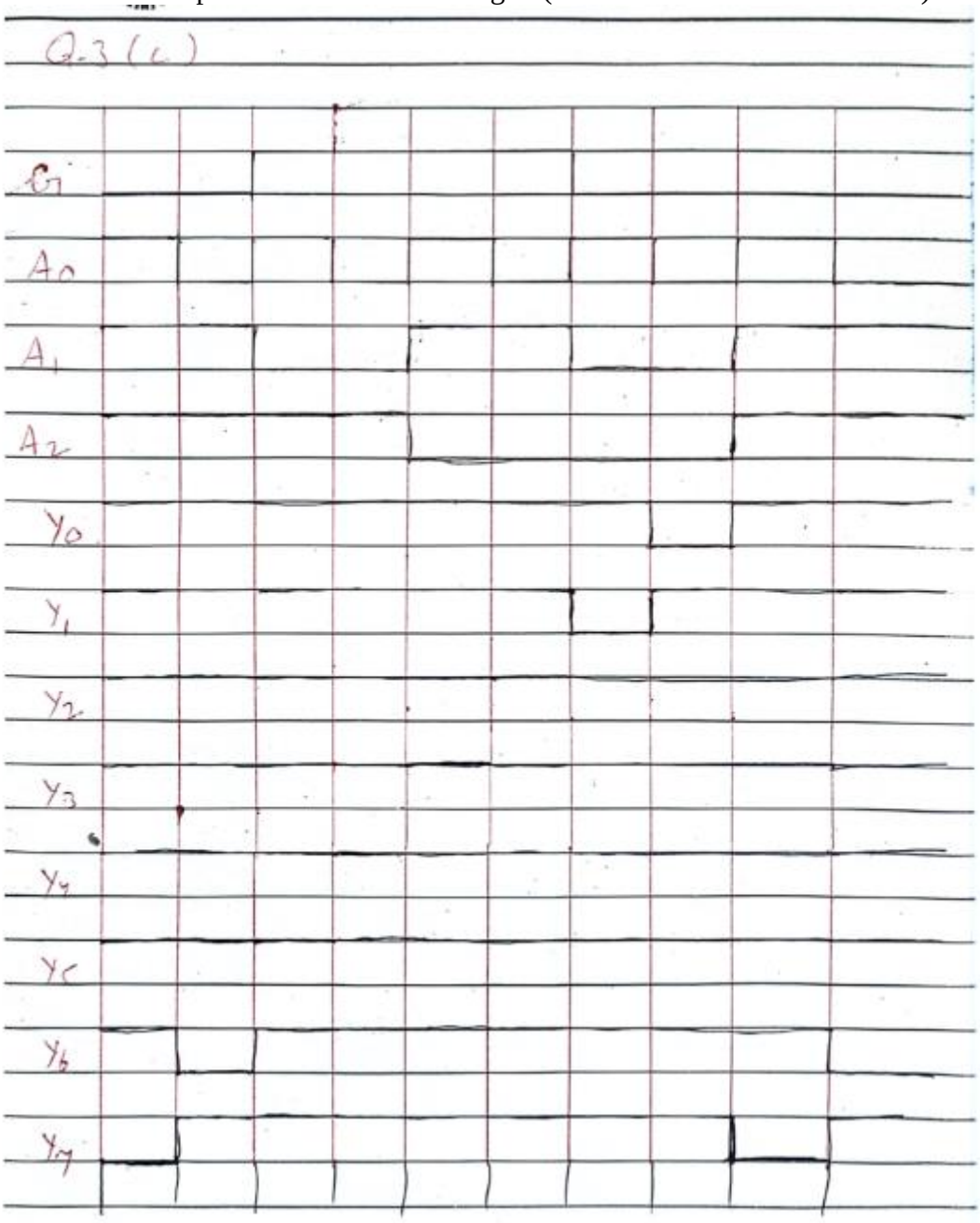


Fig-1



(c) Determine the output (Y0-Y7) waveform for the De-multiplexer shown in Fig -2 for the data select lines and enable input lines are shown in Fig 3. (**Consider G2A and G2B Low**) [4]



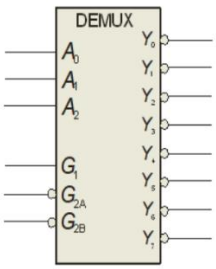
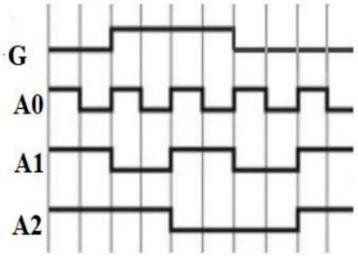


Fig-2



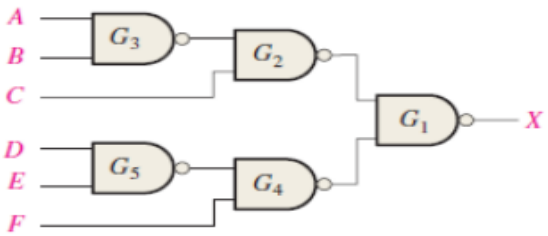
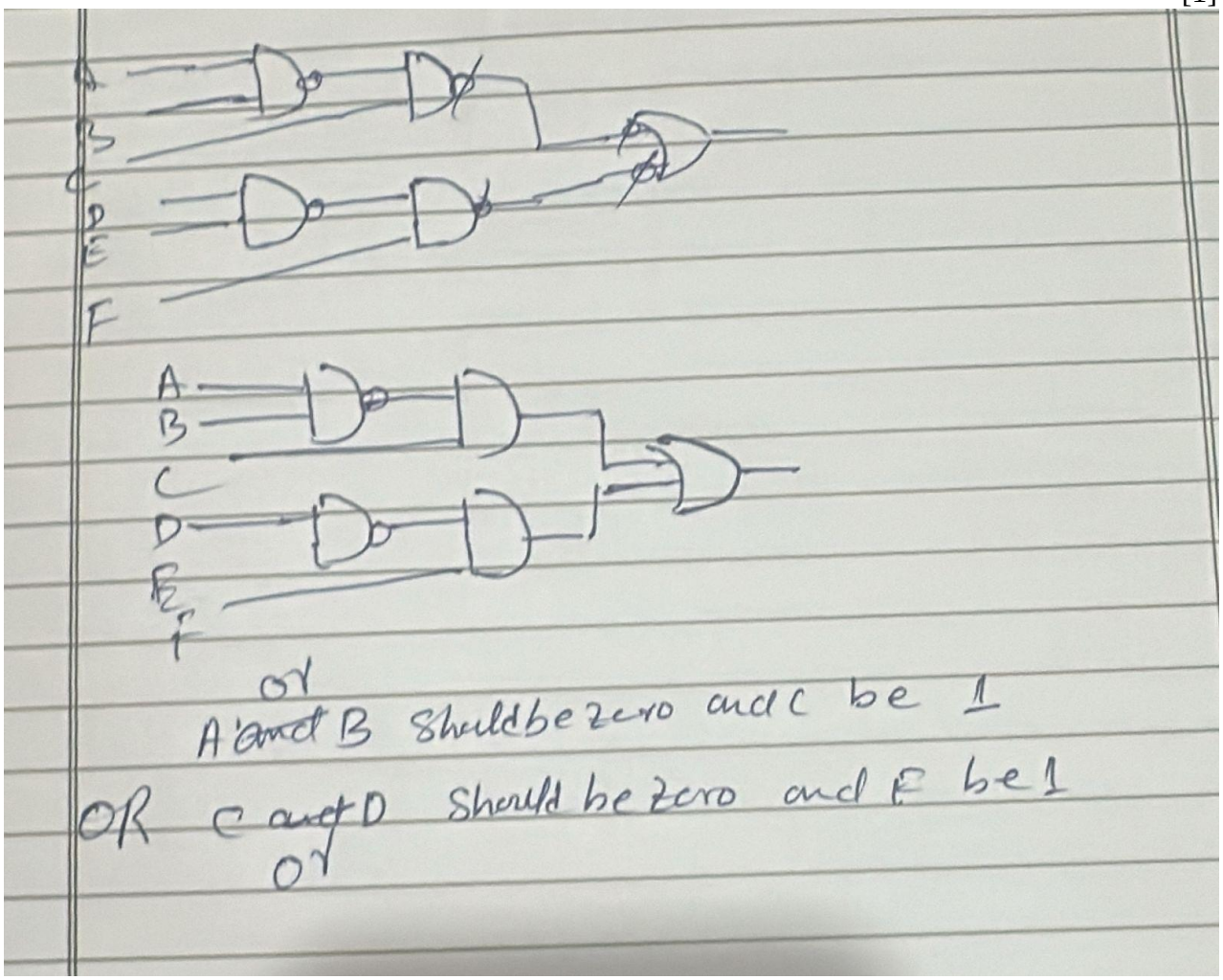


Fig-3

(d) The circuit Fig-3 is supposed to be a simple digital combination lock whose output will generate an active–LOW signal for only one combination of inputs. Modify the circuit diagram for active HIGH output. Also, determine the input conditions needed to cause the output to go to its active state. [1]



CLO # 4 Analyze Sequential Circuits to utilize in different applications. [3 marks]

Q4:(a)Two edge-triggered J-K flip-flops are shown in Fig-4 below. If the inputs are as shown, draw the Q output of each flip-flop relative to the clock, and explain the difference between the two. The flip-flops are initially RESET. [2]

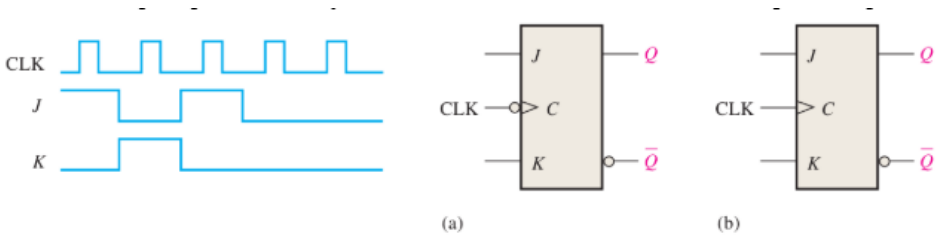


Fig-4

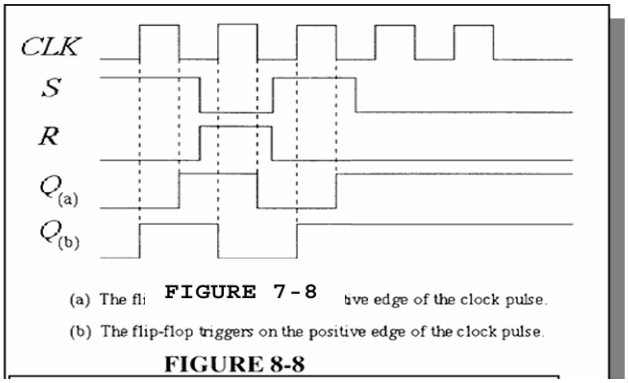


FIGURE 7-8

FIGURE 8-8

(b) For a gated D latch, the waveforms shown in Fig-5 below are observed on its inputs. Draw the timing diagram showing the output waveform you would expect to see at Q if the latch is initially RESET. [1]

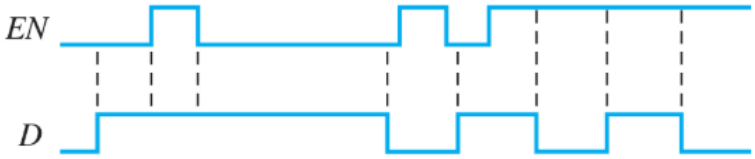


Fig-5

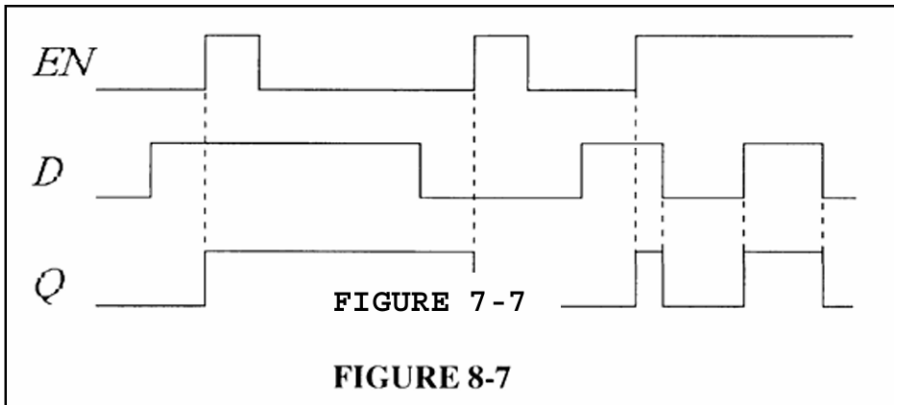
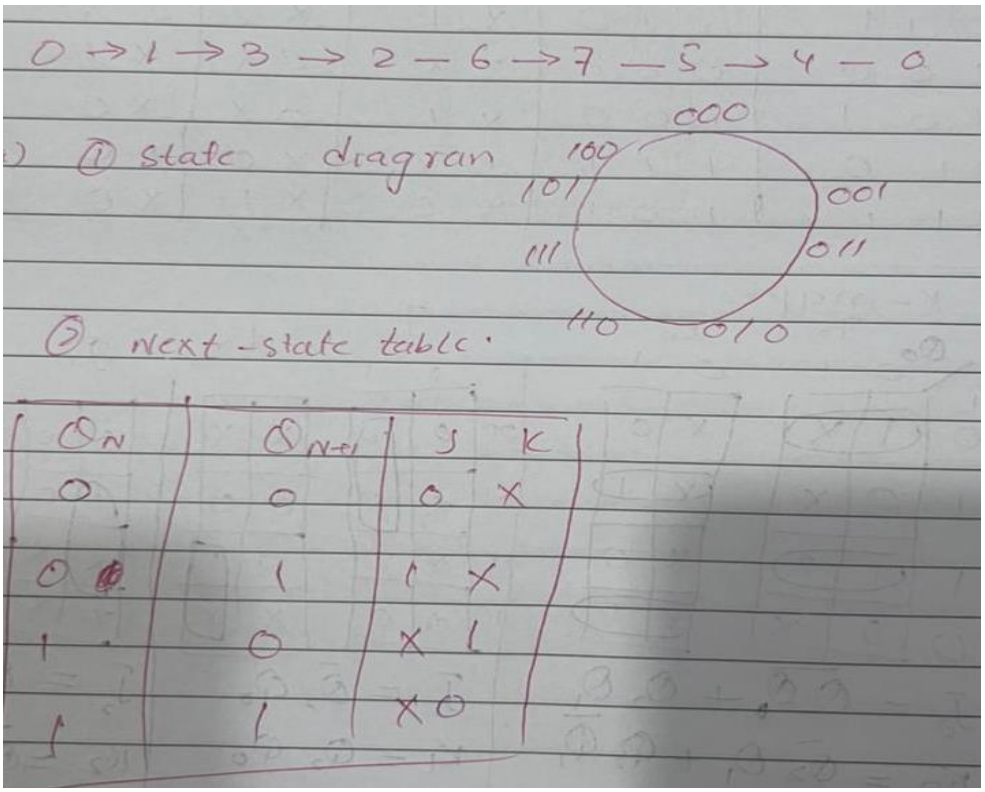


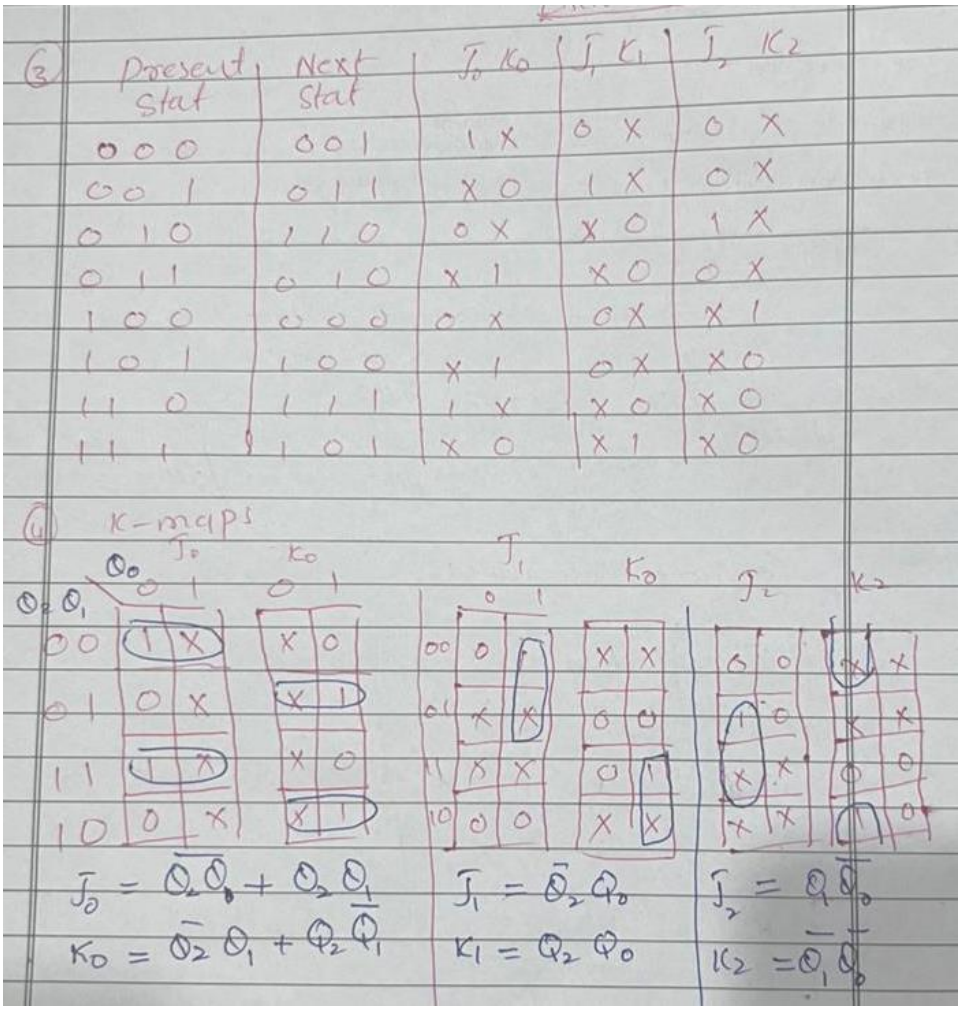
FIGURE 7-7

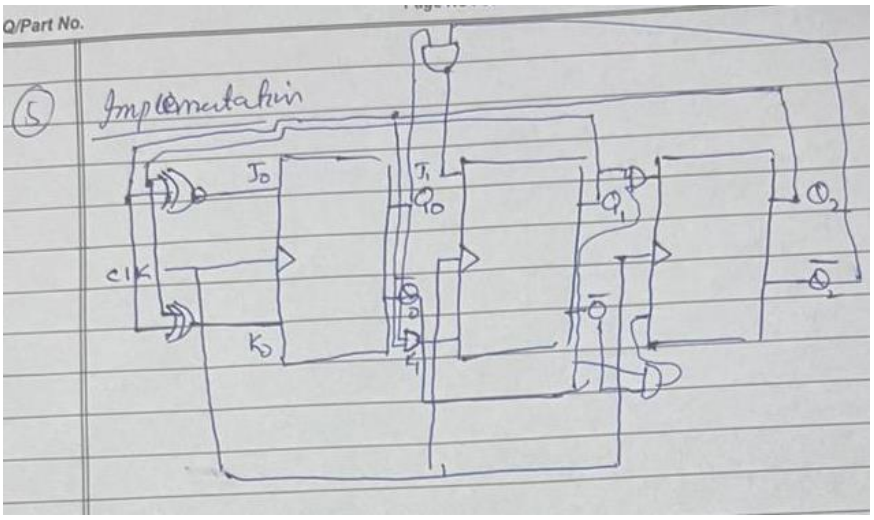
FIGURE 8-7

CLO # 4 Analyze Sequential Circuits to utilize in different applications. [14 marks]

Q5. (a) Using JK flip flop design a synchronous counter that counts the sequence (0-1-3-2-6-7-5-4) [6]


0 → 1 → 3 → 2 → 6 → 7 → 5 → 4 → 0
① state diagram
000
100
101
001
111
011
110
010
② next-state table:
Q_N | Q_{N+1} | J | K
0 | 0 | 0 | X
0 | 1 | 1 | X
1 | 0 | X | 1
1 | 1 | X | 0

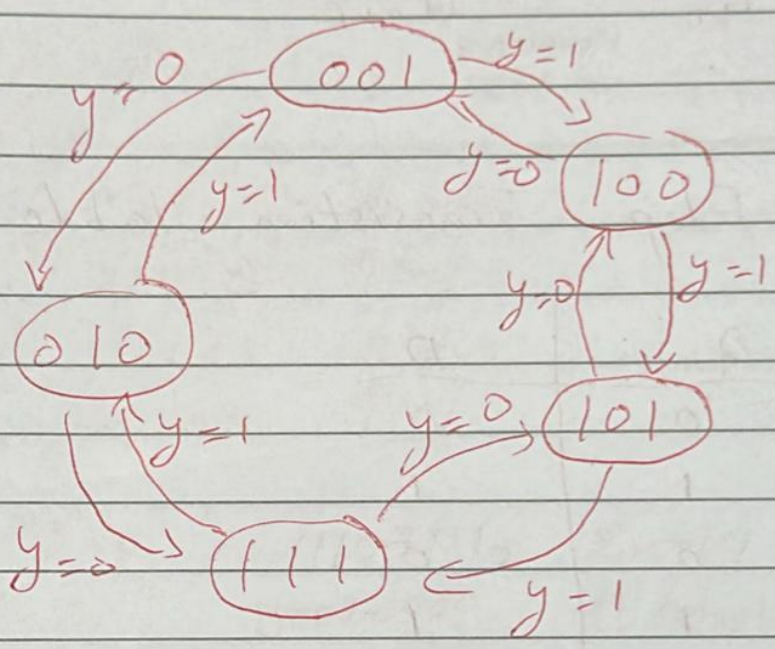




(b) Design a UP/DOWN counter using D flip-flops to produce the following sequence (1-4-5-7-2). [4]

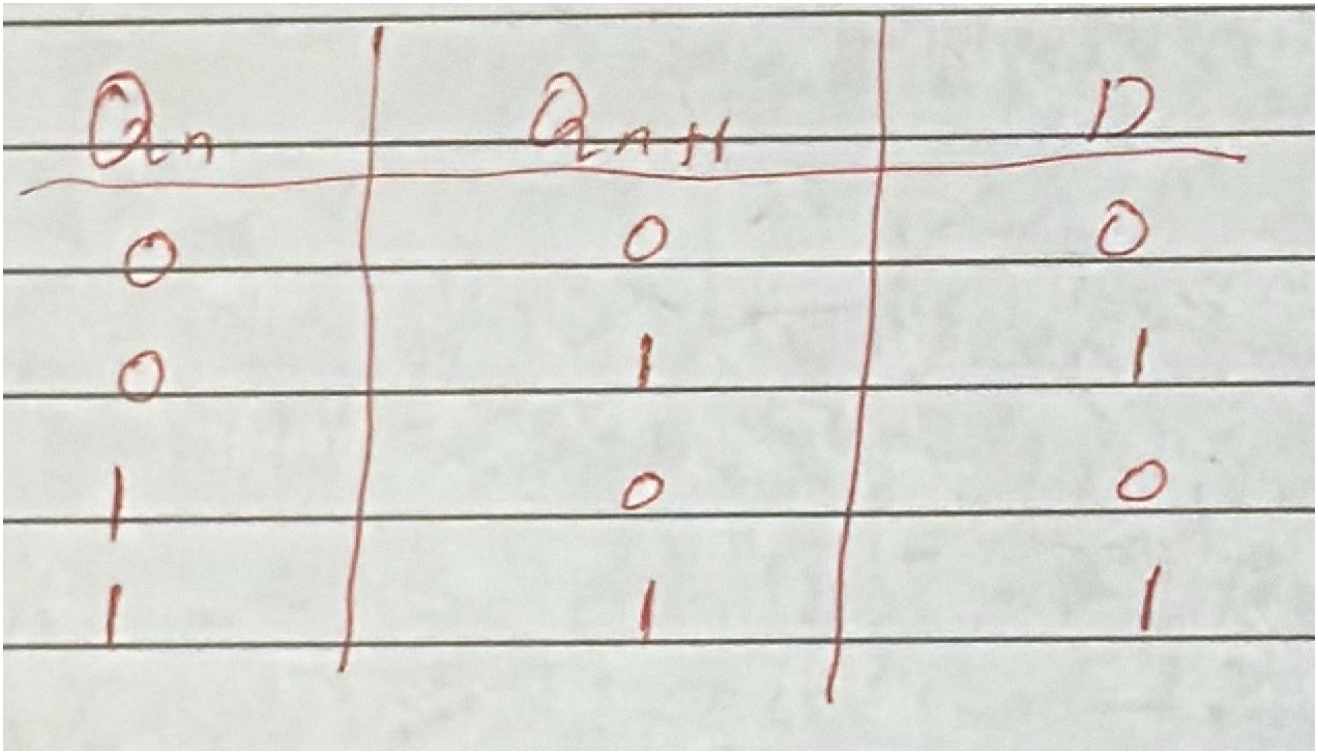
(b)

State diagram:-

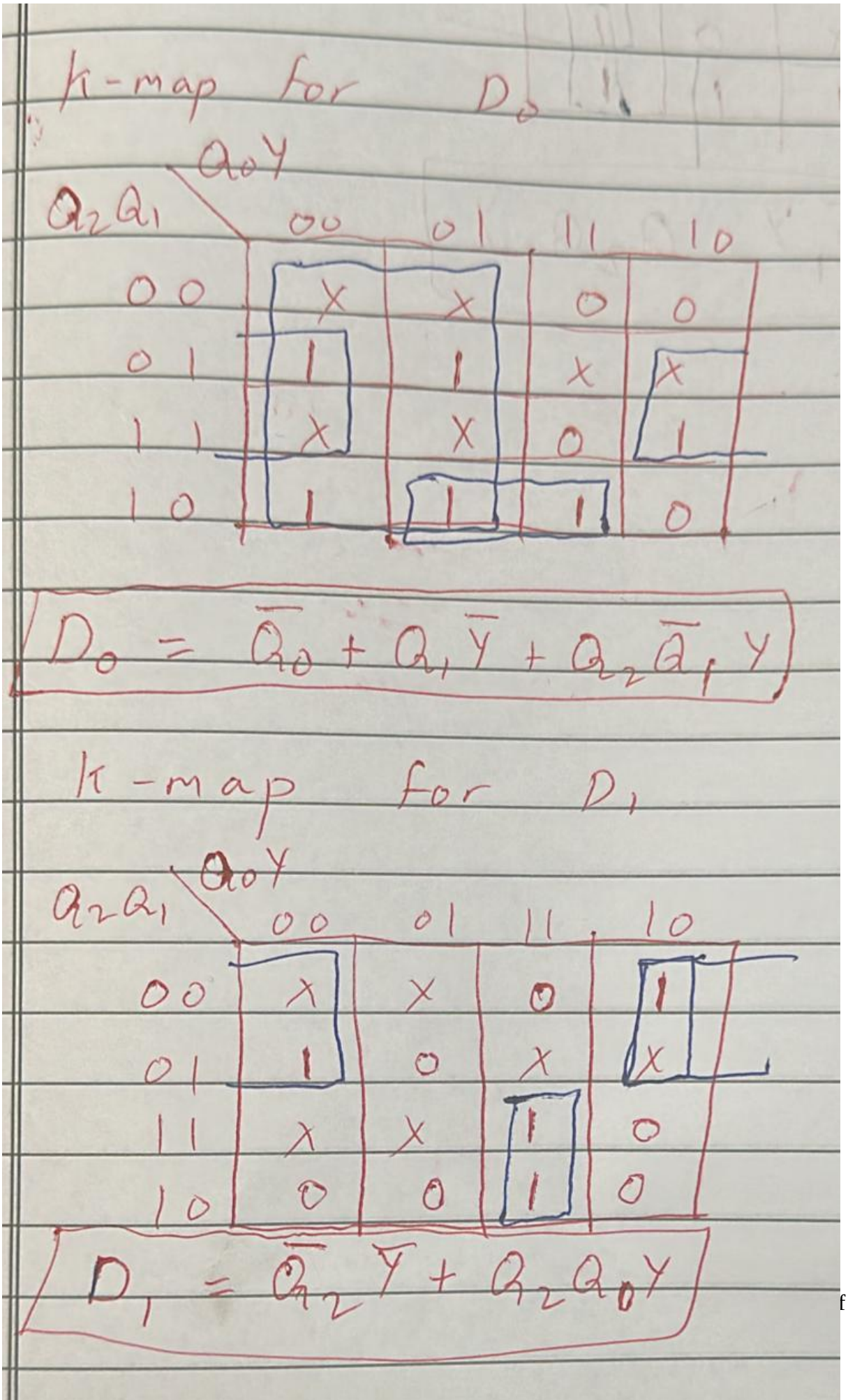


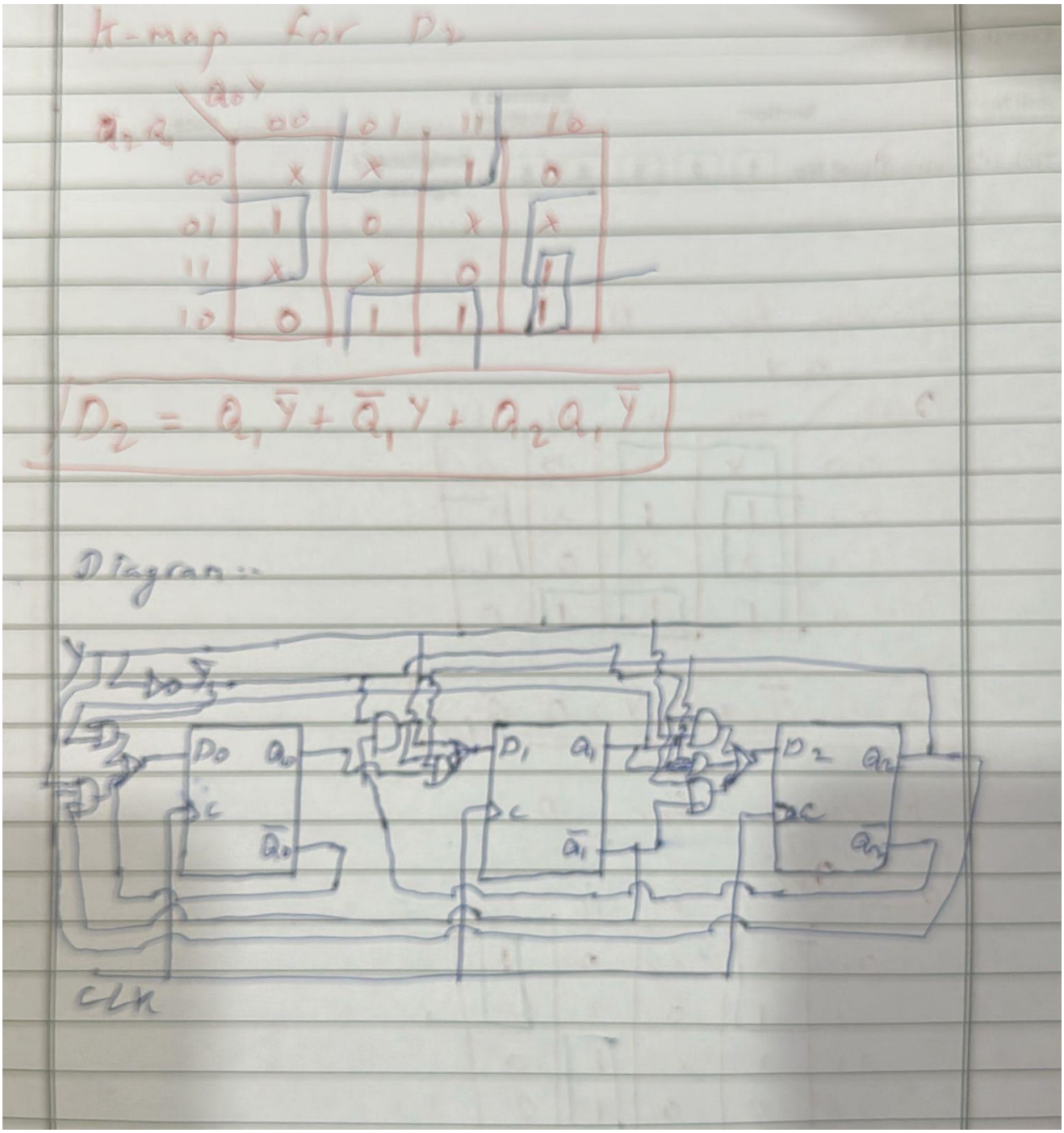
State Table

Present state			Next state					
			$Y=1$			$Y=0$		
Q_2	Q_1	Q_0	Q_2	Q_1	Q_0	Q_2	Q_1	Q_0
0	0	1	1	0	0	0	1	0
1	0	0	1	0	1	0	0	1
1	0	1	1	1	1	1	0	0
1	1	1	0	1	0	1	0	1
0	1	0	0	0	1	1	1	1

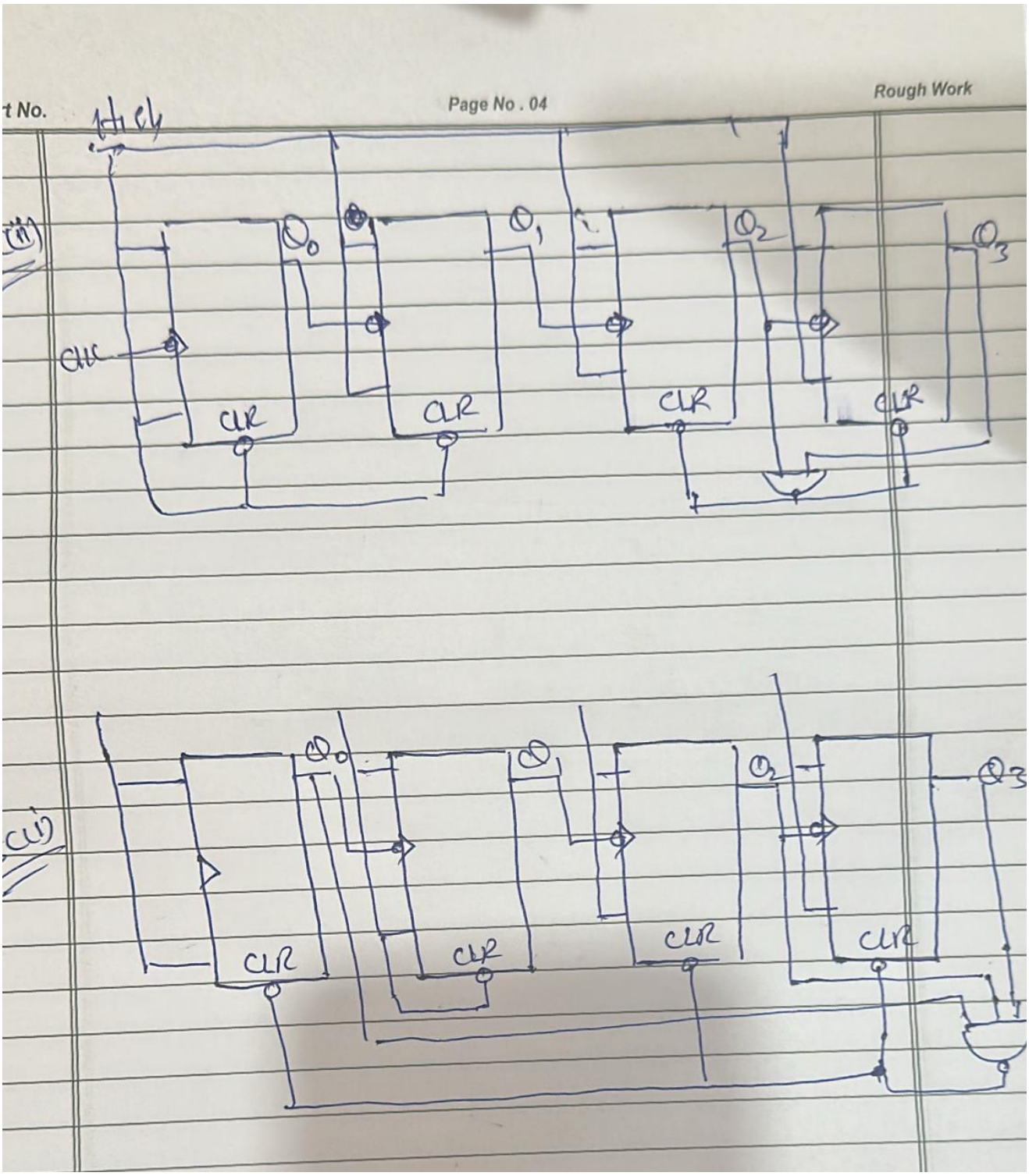


Q_n	Q_{n+1}	D
0	0	0
0	1	1
1	0	0
1	1	1


k-map for D_0
Q_0Y
Q_2Q_1
00 01 11 10
00 X X 0 0
01 1 1 X X
11 X X 0 1
10 1 1 1 0
$D_0 = \bar{Q}_0 + Q_1\bar{Y} + Q_2\bar{Q}_1Y$
k-map for D_1
Q_0Y
Q_2Q_1
00 01 11 10
00 X X 0 1
01 1 0 X X
11 X X 1 0
10 0 0 1 0
$D_1 = \bar{Q}_2\bar{Y} + Q_2Q_0Y$



(c) Show how to connect a 4-bit asynchronous counter for the moduli (i) 13 (ii) 12. [2]



(d) For the ripple counter shown in Fig-6 below, show the complete timing diagram for eight clock pulses, showing the clock, Q0, and Q1 waveforms. [2]

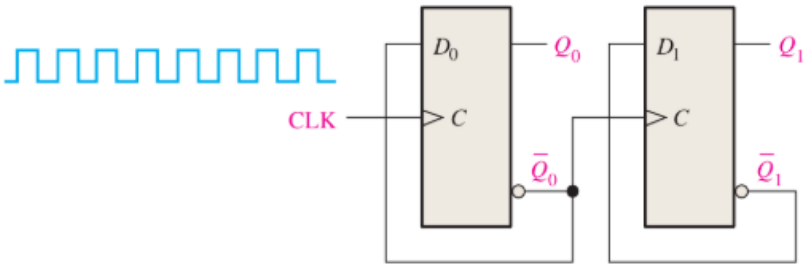
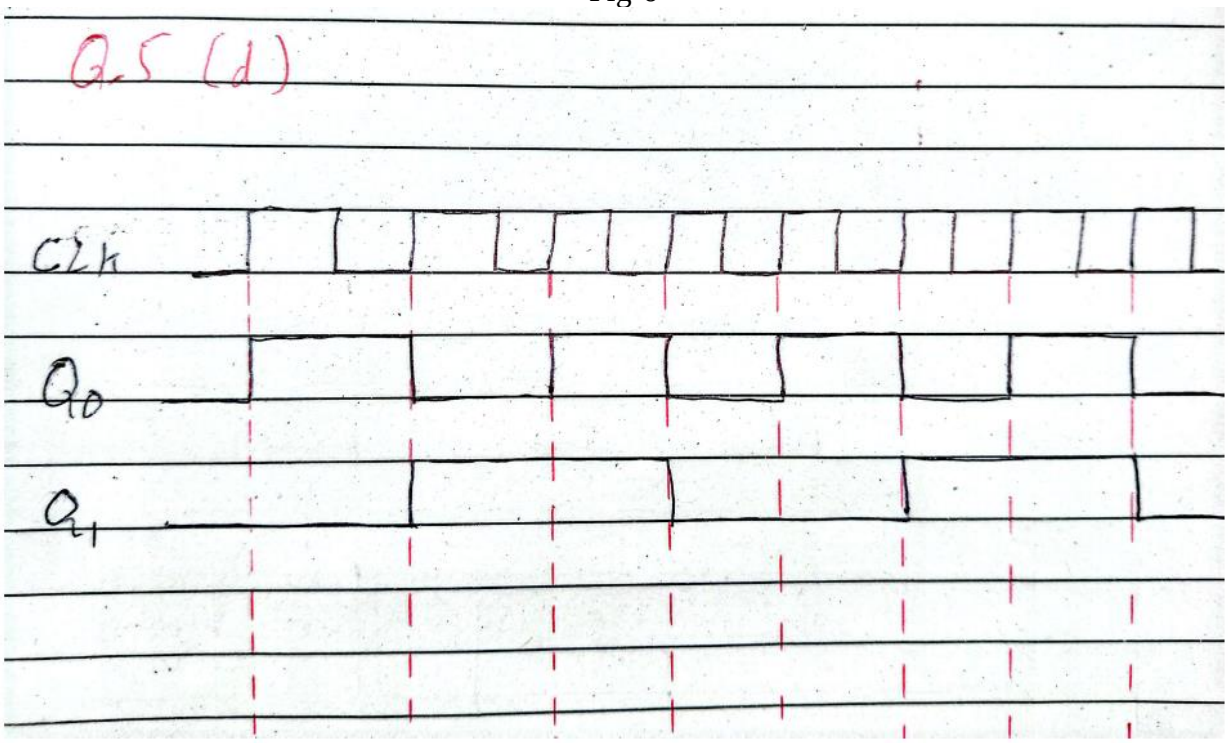
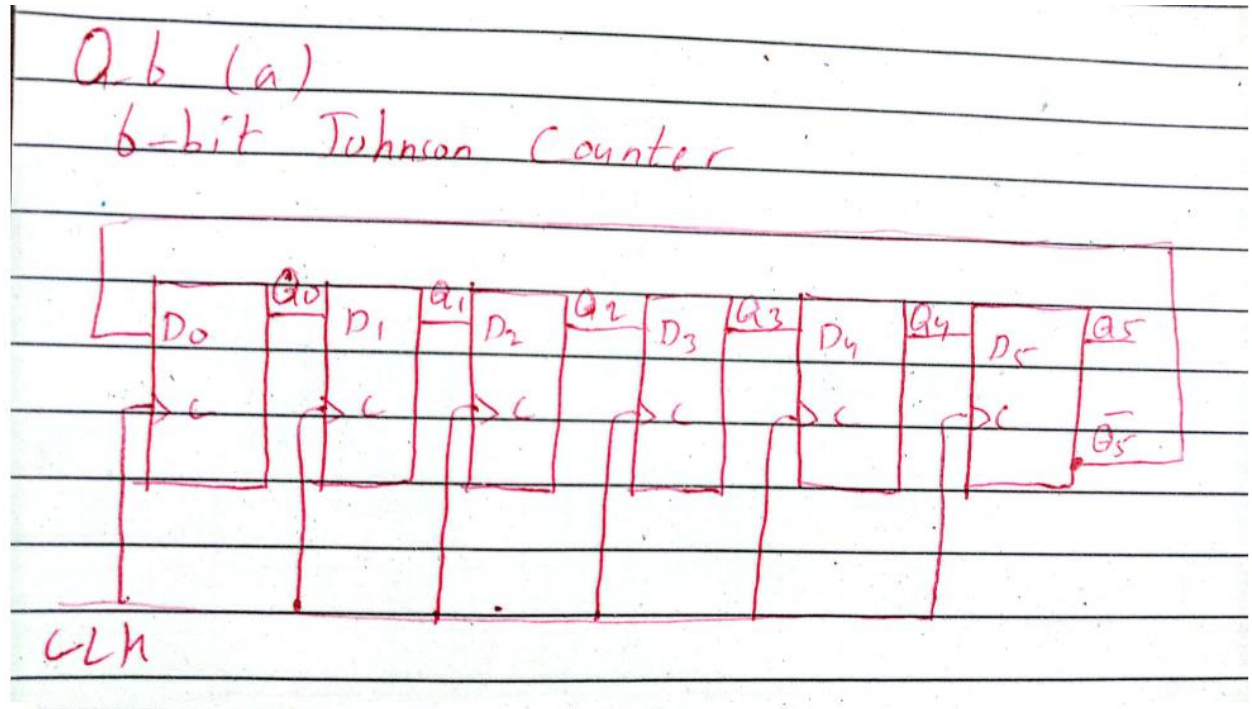


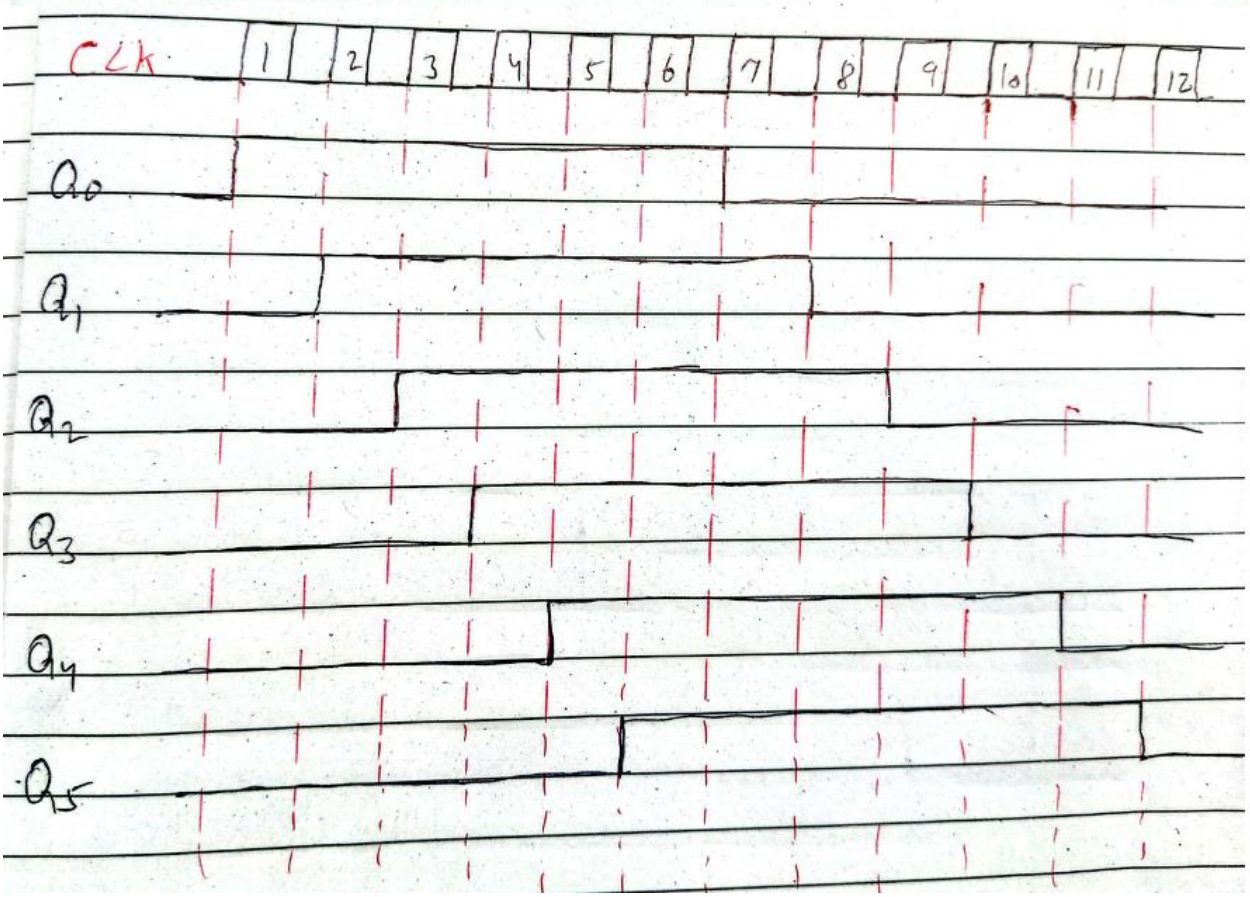
Fig-6



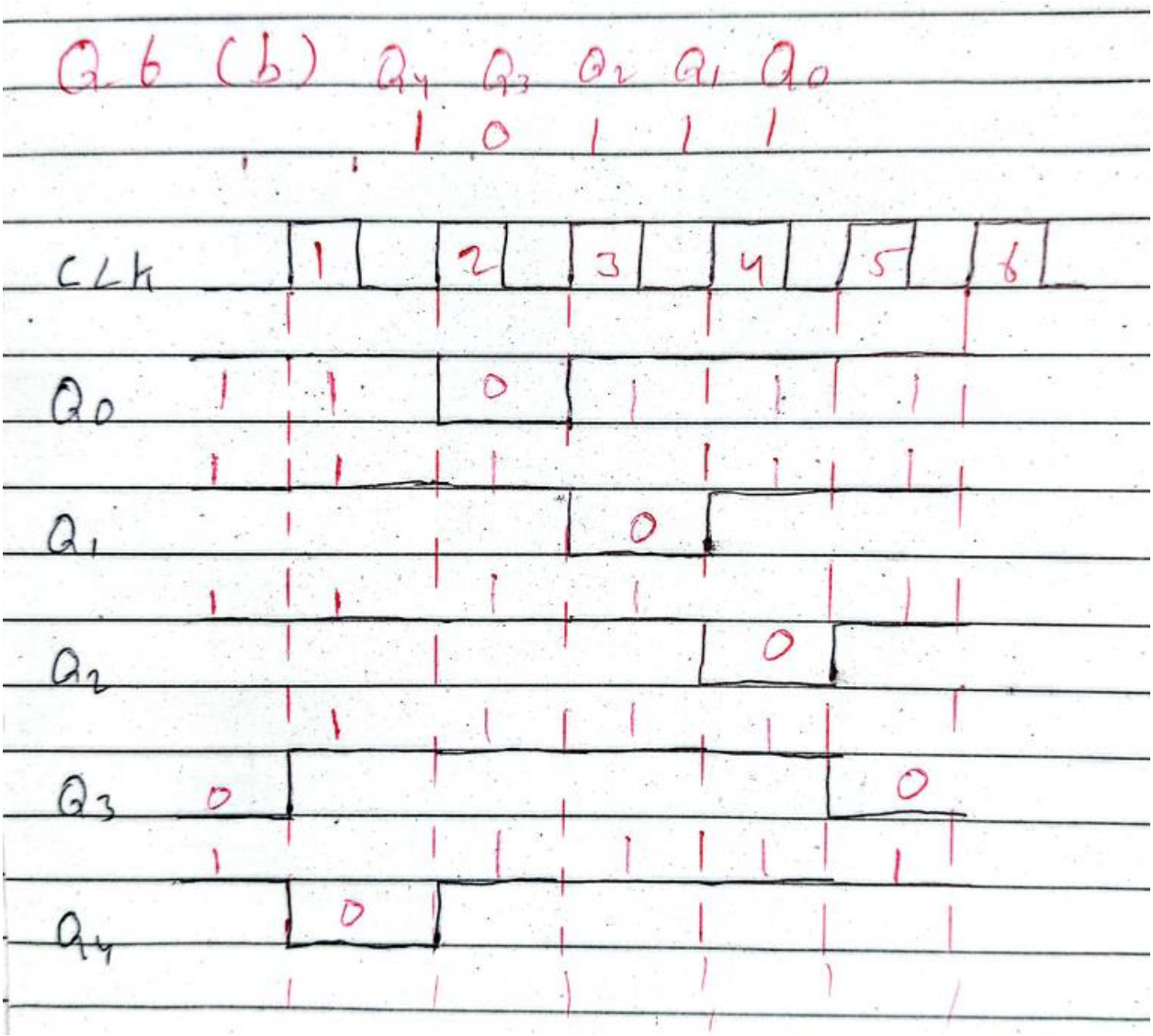
CLO # 4 Analyze Sequential Circuits to utilize in different applications. [8 marks]

Q6: (a) Draw 6- bit Johnson Counter and the Timing Diagram [Initially all input are RESET] [3]





Q6(b) If a 5 bit ring counter has initially state 10111, determine the waveform of each Q output. [2]



(c) Draw the states of the 5-bit register in Fig-7, for the specified data input (10111_2) and clock waveforms. Assume that register is initially cleared. [3]

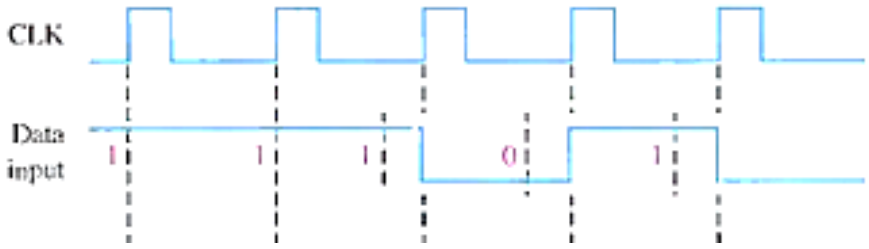
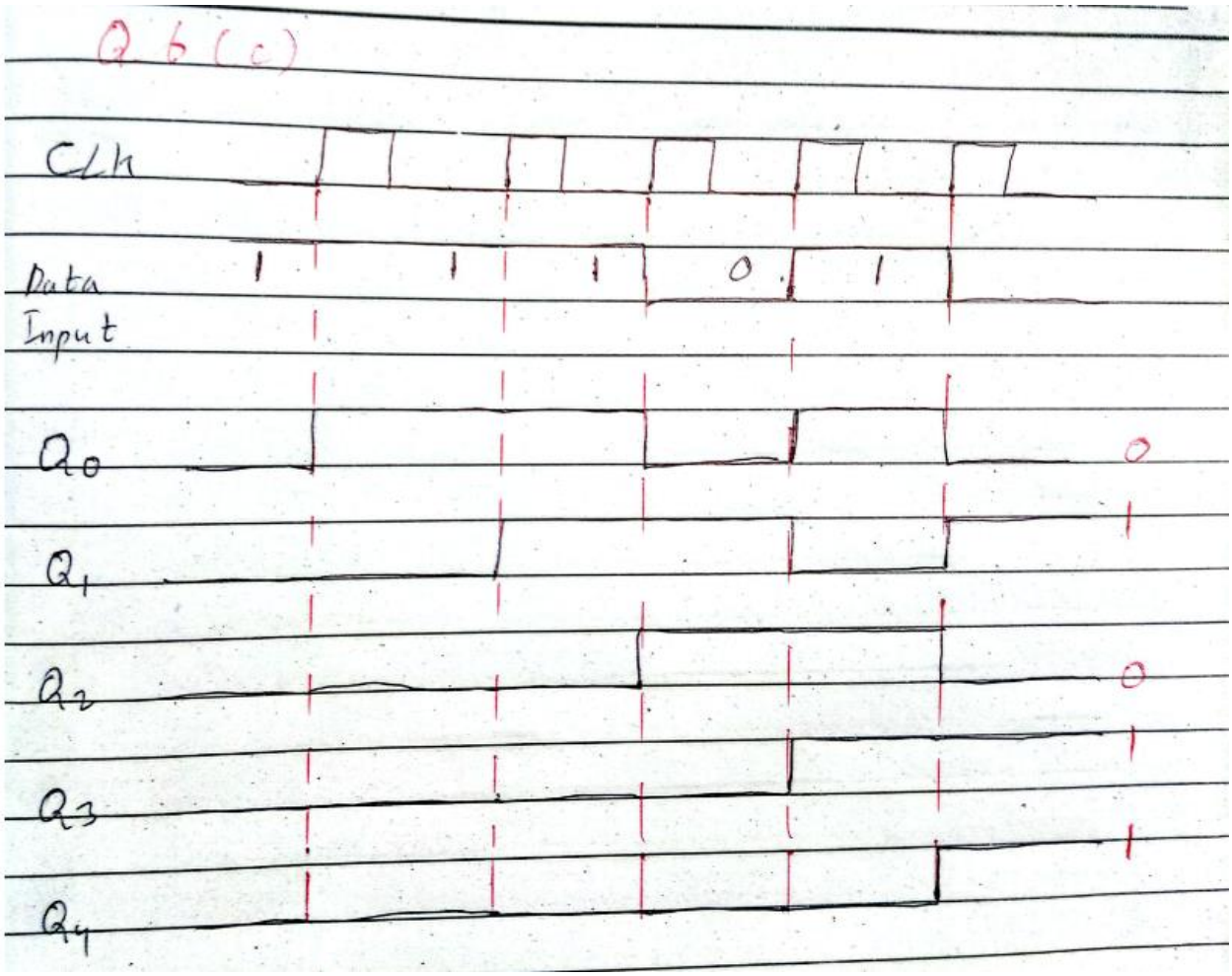


Fig-7



GOOD LUCK