YASH RAJ OJHA

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Education

Indraprastha Institute of Information Technology, Delhi (IIIT-D) Delhi

Bachelor of Technology, Electronics & Communication Engineering *2021 – 2025*

- **Relevant Coursework:** Digital Circuits, Circuit Theory & Devices, Integrated Electronics, CMOS, **VLSI Design Flow (Prof. Sneh Saurabh), Digital VLSI Design (Prof. Anuj Grover)**, Computer Architecture.

Technical Skills

Languages and Methodologies: C, C++, Verilog, System Verilog, Python.

VLSI Flow & Skills: Physical Design, Static Timing Analysis (STA), Clock Tree Synthesis (CTS), Design For Testability (DFT), Place & Routing (PnR), Digital Design, Debugging, Breadboard Prototyping, ASIC and RTL to GDSII Generation Flow.

Tools and Technologies: Cadence Virtuoso and Innovus, Xilinx Vivado, Keysight DSO & ADS, LTSpice, Eaglecad, Tinkercad, Digital Multimeter, Wave Generator, Linux, MATLAB, FPGA, Git (GitHub), Ubuntu, VS Code.

Work Experience

Incubation Center & Institute Innovation Council – Strategist Intern Jan 2025 – May 2025

Guide – Prof. Pankaj Vajpayee (Director & CEO, IIITD-IC & IIC)

- Evaluated 10+ startup proposals, including several in embedded systems and electronics hardware, producing technical feedback reports and steering 3 ECE-focused projects to EiR (Entrepreneur in Residence) approvals.
- Planned and executed 5+ technical entrepreneurship events for founders and incubators, fostering 40% higher engagement using data-driven strategies tailored to the ECE and tech community.
- Collaborated with the Dean to develop pitch templates and review workflows for technology product startups, improving funding approval turnaround by 20%.

Cognitive Sciences Lab, IIIT Delhi – Undergraduate Researcher Jan 2024 – May 2024

Guide – Prof. Sonia Baloni Ray

- Engineered 4+ real-time signal processing algorithms in Python, boosting data throughput by 25% on EEG data..
- Built automated Python pipelines for quantitative analysis, cutting error-checking time by 15%.
- Collaborated with a 5-member research team to validate datasets and optimize algorithm accuracy.
- Utilized MATLAB Profiler to identify performance bottlenecks, reducing algorithm runtime by 10% through targeted optimizations.

Projects

Network on Chip Simulator: RTL to GDS Flow Jan 2025 – Apr 2025

- Architected a 2×2 NoC simulator in Verilog and executed the complete RTL-to-GDSII VLSI design flow.
- Performed RTL coding, simulation, synthesis, STA, and formal verification using Cadence Genus and Conformal, ensuring functional and timing closure.
- Validated NoC layout by resolving 15+ DRC/CTS issues during Innovus-based placement and routing, improving reliability and minimizing congestion.

3X3 NOC ROUTER Jul 2024 – Dec 2024

- Constructed a cycle-accurate simulator for a 3×3 NoC router mesh supporting XY/YX adaptive routing.
- Enhanced packet transfer efficiency by 12% through optimized flit-based routing and conducted latency and throughput analysis under PVA/PVS traffic patterns.

Two-Stage BJT Audio Amplifier Design Jan 2023 – Apr 2023

- Engineered and simulated a two-stage analog amplifier using LTSpice, achieving 40 dB fixed gain in stage 1 and variable gain in stage 2 to drive an 8 Ω/1W speaker.
- Optimized transistor biasing and small-signal parameters for a flat 20 Hz–20 kHz audio response.
- Validated performance by implementing RC filters with -40 dB/decade roll-off and testing on a breadboard using oscilloscope measurements.

Scholarships, Research & Leadership

Cadence Scholarship Program by Cadence Design Systems: CSP Scholar (awarded to top 1% ECE students.)
Undergraduate Researcher, Cognitive Sciences Lab, IIIT Delhi: Led EEG-based neuro-visual emotion analysis, processing 150+ data samples.
Centre for Intelligent Product Design: Mentored 10+ product teams, guiding prototypes from concept to MVP.
Entrepreneurship Cell, IIIT Delhi: Core Team Lead, organized 80+ events and mentored 15+ campus startups.
Student Mentorship Program, IIIT Delhi: Mentor,Mentored 30+ first-year students on academics and career planning.