

Bluetooth

- ① It does not have full form full form
- ② Its range is upto 10m Range
- ③ Its bandwidth is low Bandwidth
- ④ It is less secure than wifi Secure
- ⑤ It needs Adaptor Power Device
- ⑥ It consumes less power power consumption than wifi

Property

Bluetooth

~48 GHz

wifi

2.4 GHz

16

ch-1

- what is CPU Organisation
- General Register based CPU Organisation
- Stack based CPU Organization - Push - Pop
- INSTRUCTION formats [three, Two, One, Zero, Cisc, Risc]
- Difference between [CISC & RISC]
- Addressing Mode [10 Types]
 - Immediate Mode
 - Register Mode
 - Register Indirect Mode
 - Auto Increment / Decrement Mode
 - Direct Addressing Mode
 - Indirect Addressing Mode
 - Relative Addressing Mode
 - Displacement Addressing Mode
 - Base Register Addressing Mode
 - Stack Addressing Mode

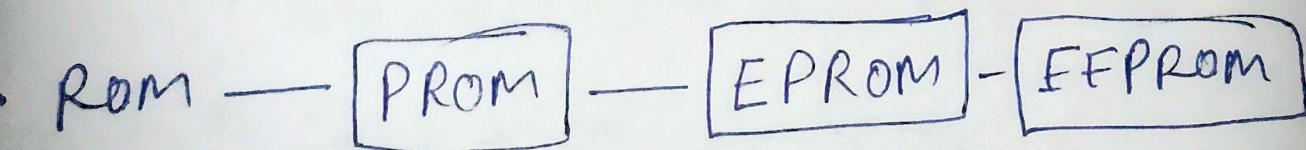
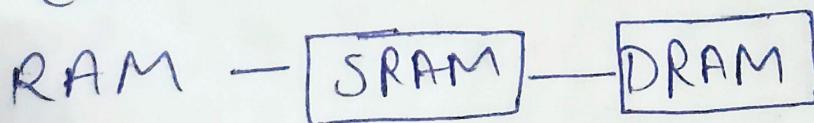
- Instruction Cycle
- CPU Design
- Hardwired Control Unit
- Micro-programmed Control Unit
- Type of Micro-programmed Control Unit
- Difference between Hardwired & Micro-programmed Control Unit

Ch-2

- Introduction of Memory
- Volatile & Non-Volatile Memory
- Memory Request?
- what is Memory HIERARCHY
- Memory Hierarchy Design type
 - External / Secondary Memory
 - Internal / Primary Memory

① Auxiliary Memory \rightarrow Difference
• Main Memory

② What is Cache Memory Explain
• Memory Accessing Mode
• Characteristics of Memory HIERARCHY



RAM Integrated Circuit chips

Typical Ram chip (Diagram)

A Difference between SRAM & DRAM

- Difference between RAM & ROM
- Memory Addressing MAP ? Define
- Explain MMU

BRIE • MAGNETIC Disks | characteristics

- MAGNETIC TAP → Difference

• Define Associative Memory

C Application of Cache memory :-

- Type of Cache ① Primary Cache
② Secondary Cache

• What is Virtual Memory

Ch-3

- Introduction of Arithmetic Operations
- Read About Number System
- Base Conversion for Number Conversion
 - Decimal to Binary
 - Binary to Decimal
 - Decimal to Octal
 - Octal to Decimal
 - Hexadecimal to Binary

One's Complement & two's Complement

Binary Adder (+)

what is Half & Full Adder

Ch- 4

- Define BIOS ?
- what bios do ?
- what is (CMOS) do ?
- Define • ~~████████~~ Interrupt handlers
 - Device Driver
 - (SCSI)

Input /output Commands , Instruction
Difference between - Isolated I/O &
Memory Mapped I/O

Explain Direct Memory Access

① 8085 Micro Processor - Introduction

② 8086 Micro processor - Introduction

③ 8085 - Introduction

- Addressing Mode

① Immediate Addressing Mode

② Register Addressing Mode

③ Direct Addressing Mode

④ Register Indirect Addressing Mode

⑤ Implied Addressing Mode

- Instruction Cycle in 8085 Microprocessor

- • Fetch Cycle

- • Decode Instruction

- • Reading Effective Address

- • Execution Cycle

- Architecture of 8085 Micro-processor

- Operation of 8085 Microprocessor

- Flag Register

- Control & Timing Unit

- Register Array

- Special purpose Register

- Program Counter

- Stack Point in 8085

- Increment or Decrement Register
- Address-Buffer & Address-Data Bus
- Address Bus and Data Bus
- Timing & Control Unit

- PIN DIAGRAM OF 8085

- Its Connection

- Brief about 8086 Micro-processor
- Feature of 8086
- PIN DIAGRAM of 8086 Micro-processor

* Difference between 8085 & 8086

- Introduction of Multiprocessor

- Type
- ① shared Memory Multiprocessor,
 - ② distributed Memory Multiprocessor,

- Type
- ① Symmetric Multiprocessor
 - ② Asymmetric Multiprocessor

- Advantage of Multiprocessor

- Application of Multi-processor

- Basic character of multiprocessor

- what is Parallel processing

- Define pipe line

- Define Flynn classification

- ① (SISD)
- ② (SIMD)
- ③ (MISD)
- ④ (MIMD)

- Difference between Series and parallel processing

- Type of parallelism

- ① Bit-level parallelism

- ② Instruction-level parallelism

- ③ Task parallelism

- Application of parallel computing

- Limitations of It

- Pipeling Processing — Type
 - ① Arithmetic pipeline
 - ② Instruction Pipeline
- INTERCONNECTION NETWORK
 - Characteristics :-
 - 1 Time-shared Common bus
 - 2 Multiport Memory
 - 3 Crossbar Switch
 - 4 Multistage Switching Network
 - 5 HyperCube System
 - Multi Computer
- * Difference between Multiprocessor and Multi Computer

IMPORTANT

QUESTION

^ To Night

CISC

RISC

SRAM

DRAM

RAM

ROM

Magnetic Tape

Magnetic Disc

Isolated I/O

Memory Mapped

8085

8086

MicroProgrammed

Hard wired

8085 pin Diagram -

Difference between CISC & RISC

CISC

- ① It has a Microprocessor Unit
- ② The instruction set has various different instruction
Can be used for complex operation
- ③ only Single Register Set
- ④ Limited addressing Mode
- ⑤ A Small number of fixed-length instruction
- ⑥ Varying Format (16-64 bit)
- ⑦ Request for a minimum amount of RAM
- ⑧ Application:-
Such as Desktop, Computer & Laptop

RISC

- It has a hard-wired unit of programming
- The instruction set is Less, instructions used for primitive Operation (Simple)
- Multiple Register Sets are present
- Compound addressing Mode
- A Large Number of instruction
- fixed (32 bit) Format
- Request More RAM
- Application:-
Mobile phones
Tablets

Difference between RAM & ROM

RAM

Random Access Memory

① Temporary Storage

② Store in MBs

③ Volatile

④ Used in Normal Operation

⑤ Writing data is Faster

ROM

Read Only Memory

Permanent Memory

Store in GBs

Non-Volatile

Used in start-up process of Computer

Writing data is Slow

Difference between SRAM & DRAM.

SRAM

B Stands: Static Random Access Memory

② Require a Recharge Every few milliseconds to maintain its data

③ InExpensive

④ Slower than DRAM

⑤ Can store many bit per chip

⑥ Use less power

⑦ Generate Less Heat

⑧ Use for Main Memory

DRAM

Stands: Dynamic Random Access Memory

Hold its Contents as long as power is available

Expensive

Faster than SRAM

Can not store many bit per chip

Use more power

Generate more Heat

Use for Cache.

Difference between Magnetic Disk & TAPE

MAGNETIC DISK

- ① Expensive
- ② Reliability is more
- ③ Access time is less
- ④ Data transfer rate is more
- ⑤ Use for Secondary Storage
- ⑥ Less Portable

MAGNETIC TAPE

- Less Expensive
- Reliability is less
- Access time is more
- Data transfer rate is less
- Use for backup
- More Portable

Difference between Isolet I/O & Memory Mapped

Isoleted I/O

- ① Isoleted I/O use Separate memory Space
- ② Limited instruction Can be used
- ③ The address for Isoleted I/O device are called PORT

Memory I/O

Memory Mapped I/O uses memory from the Main Memory

Any instruction which reference to memory can be used

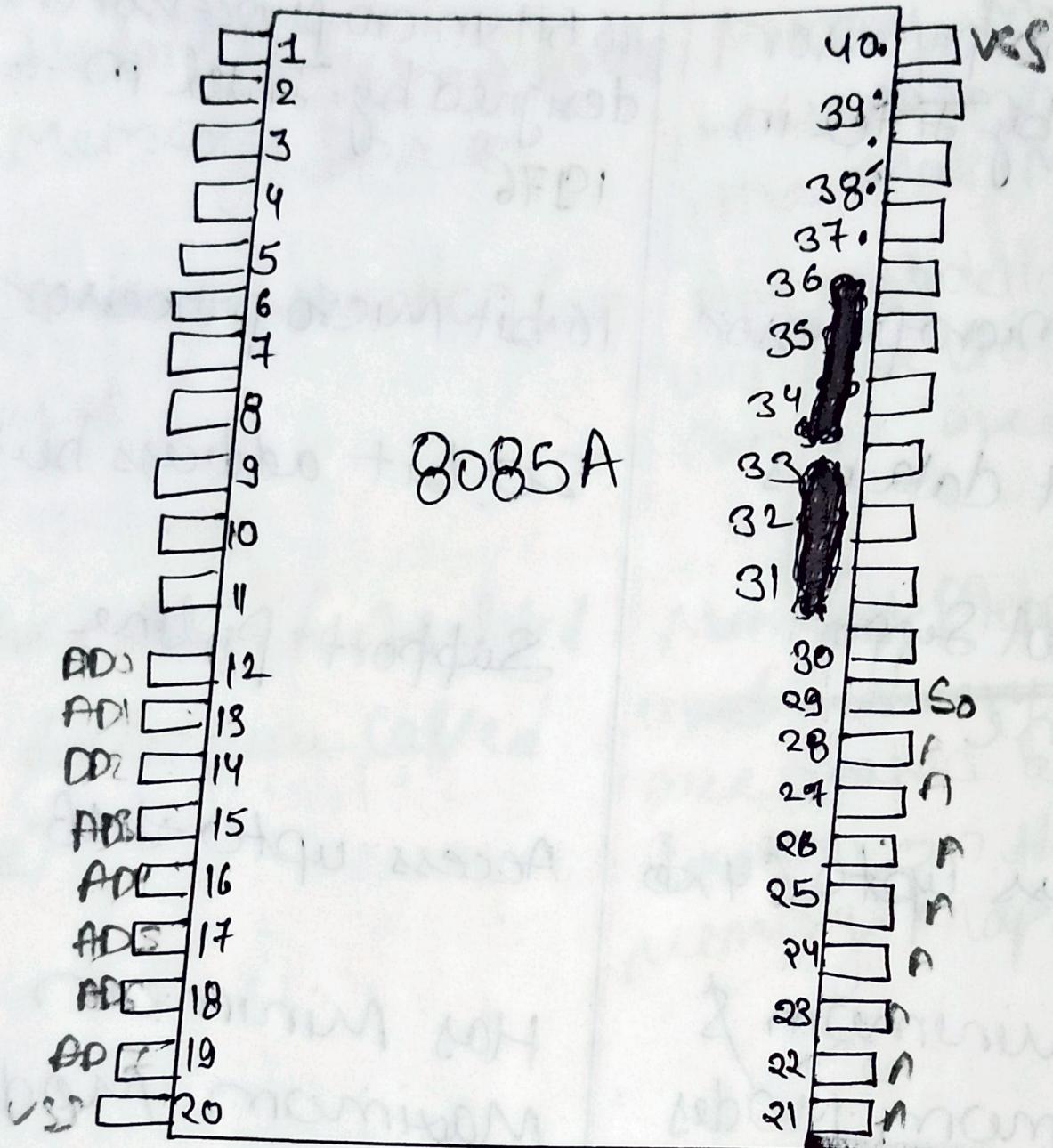
Memory Mapped I/O

~~used memory of device~~ are treated as memory Location on the memory Map.

Difference between 8085 & 8086

8085	8086
8 bit Micro-processor produce by Intel in 1976	16 bit micro-processor chip designed by Intel in 1976
② 8 bit Micro-processor	16 bit Micro-processor
③ 16 bit data bus	20 bit address bus
④ Does not Support Pipeline	Support Pipeline
⑤ Access upto 64 kB	Access upto 1 MB
⑥ No minimum & maximum Modes	Has minimum & maximum Mode
⑦ Cost Effective	Expensive

Design PIN Diagram of 8085



Difference between Hardwired Control Unit & Microprogrammed Control Unit

HARDWIRED Control Unit

① It is a Circuitry Approach

② RISC Style instruction

③ Modification required
change in Hardware

④ Implementation of hard-wired required a Cost

⑤ No Control Memory
is Required

⑥ Fast Execution

Microprogrammed

This Control unit implemented
by programming

CISC style Instruction

To modify it Only
Required change in
Code

Implementation in
Micro-programmed is NOT
Costly

Control memory is
Required

Comparatively slow

CPU organisation

A Central processing Unit is the electronic circuitry within a computer that carries out the instructions of a computer program by performing the basic arithmetic and logical operations specified by the instructions.

CPU its self have following 3 Component

- ① Memory Unit
- ② Control Unit
- ③ Arithmetic Logical Unit

Memory Unit

This Unit can store data & intermediate result
This Unit supplies information required later

It is also known as
Internal Storage main memory Primary storage
Random Access Memory

functions of the Memory Unit

- It stores data and instruction.
- It stores the Data & instruction in the memory
- It stores intermediate results of processing
- It stores the final result of processing before these results

Control Unit

this unit controls ~~all~~ operation of all the computer but it does not control the data part it just carries out functions:-

- ① It is responsible of controlling & Instruction among ~~the~~ units ~~of~~
- ② It manages & coordinates all the units of computer
- ③ It obtains the instructions from the memory direct ~~from~~ ^{operation of} Computer
- ④ It communicates with Input/Output devices for transfer of data into the storage

f. It does not process or store data

ALU

this Unit consist of 2 ~~sets~~

① Arithmetic Section

② Logic Section

Arithmetic Section

function of Arithmetic Section is to perform
Arithmetic Section like Addition, Subtraction,

Logic Section :-

used to perform Logical Section such as
Comparing, Selecting or Merging of data

CHAM



when we are Using Multiple general purpose
Resistor instead of Single Accumulator
Resistor in the CPU organisation this type
of organisation is known as general
Resistor based CPU organisation

In this type of org. the Comp. uses 2 or
3 address field in the instruction
format

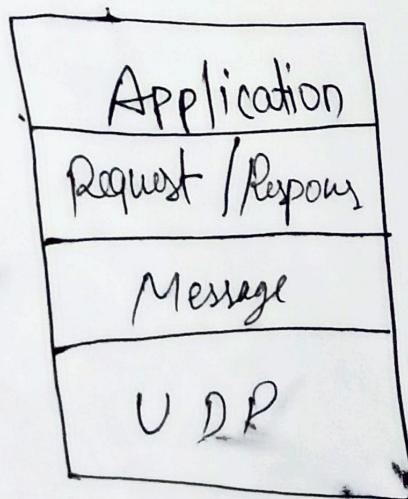
Each Address fields may specify a general
~~Resistor~~ or memory ~~specify~~ a
if many CPU Resistor are ~~not~~ available for
Every use & Intermediate Results we can
avoid memory References much of time

the ~~mostly~~ increasing program ~~activation~~
Activation Speed & Reducing Program Size
Ex. MULR, R₁, R₂

COAP

1. It is a IoT protocol
2. It is designed to allow Single & Small devices to join the IoT from to low bandwidth Restricted Network
3. the protocol is design for M2M (Machine2Machine) & IoT application such as Smart Energy & building Automation.
4. It is an application Layer protocol follows the Request & Response Pattern/Model
5. COAP runs over UDP Protocol (User Data -> Port)
6. It uses Less Resources than HTTP
7. In Coap Client Can use GET, PUT, DELETE Methods during Request

COAP Layers



mostly it is divided into 2 layers:-

1. Upper Layer (Request & Response)

It concerns Comm. Method & deal with
Request Response Method

2. Lower Layer (Message)

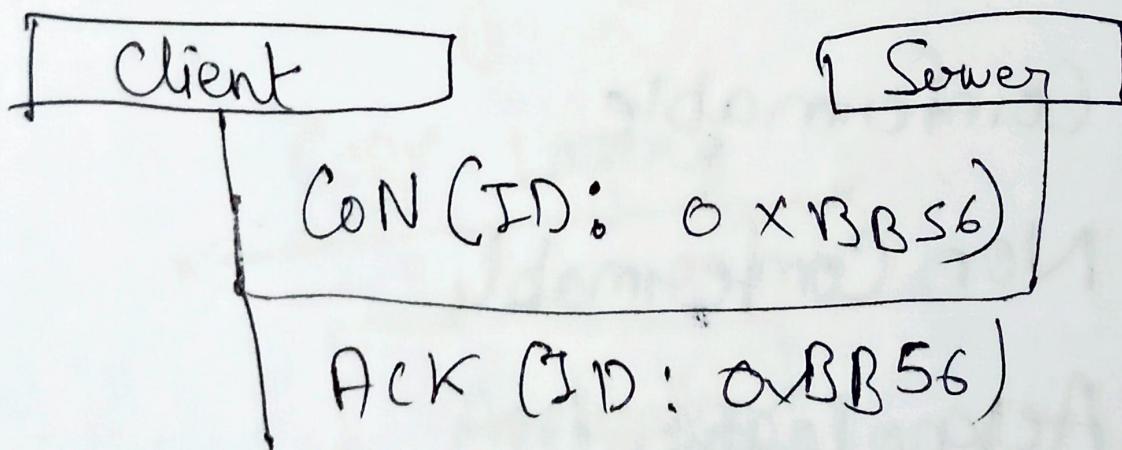
It has been designed to deal with UDP &
Asynchronous

Message type:-

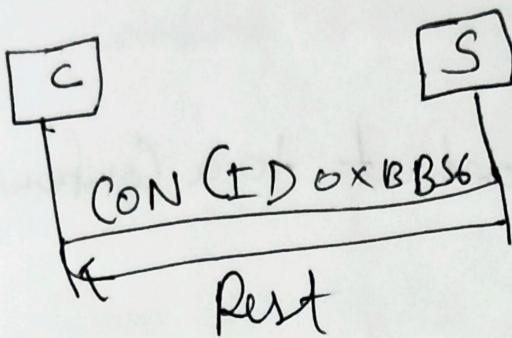
- ① Conformable
- ② Non Conformable
- ③ Acknowledgment
- ④ Reset

Conformable \rightarrow (CON), (Reliable)

- ① Either a positive Acknowledgment or
Either a Negative Acknowledgment
- ② In Case acknowledgement is not Received.
Retransmission are made until all
Attempts are Exceeded
- ③ the Acknowledgment Mess. Contain
the same ID of the Conferable
Message (CON)



If the Server has troubles in Managing the Incoming Request, it can send back a Test Message in Status of Acknowledgment Method



Non Conformable C

A Non Conformable Request is used for Non Reliable Transmission. These are messages that don't require acknowledgment by the Server.

Messages do not contain Critical Information that must be delivered to the Server.

~~like~~ Fx - Request for a Sensor ~~data~~

message made in a periodic basis

Even if ~~one~~ 1 value is miss, there is not much impact

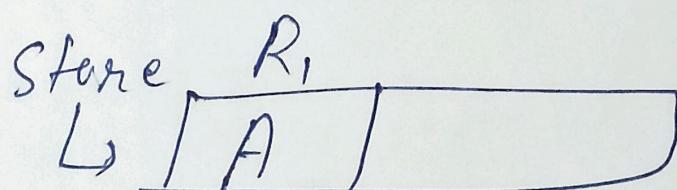
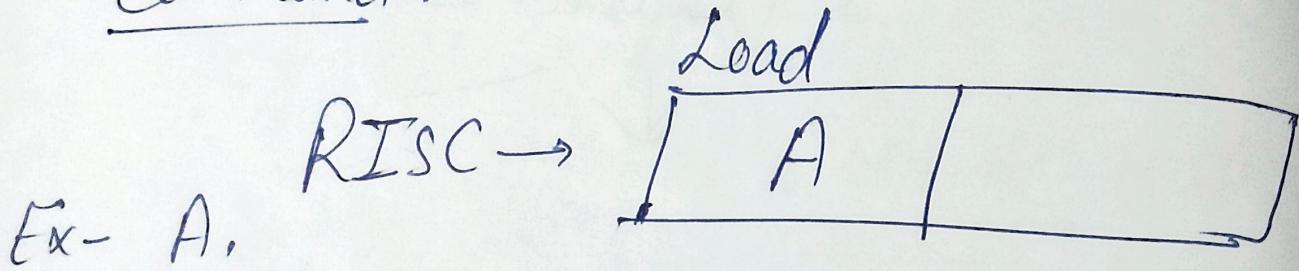
Even if this message is unreliable, they have a unique ID

RISC - Reduced Instruction Set Computer.

Different command used for different operations.

For Example:-

- for loading any data we use the load Command.
- for storing any data we use-Store Command.



CISC

Complex Instruction Set Computer

Ex → Mul A

~~Load~~ → A, R,
~~Store~~ → ~~A, R,~~

RISC

It is hardwired unit of program.

Multiple register set are present.

Execution time is very less.

Code expansion may create problem.

Decoding of instruction is simple.

fixed (32 bit) format

CISC

It is microprogramming unit.

Single register set is present.

Execution time is very high.

Code expansion is not a problem.

Decoding of instruction is complex.

Varying format (16-64 bit)

(A) ~~twinkles~~

CAHM

Addressing MODE:

- Immediate Mode —
- Register Mode
- Register Indirect Mode
- Auto Increment / Decrement Mode
- Direct Addressing Mode
- Indirect addressing Mode
- Displacement Addressing Mode
- Relative Addressing Mode
- Base Register Addressing Mode
- Stack Addressing Mode

RISC

It is a hardwired programming unit

Code execution is very fast

Multiple set of register are present.

~~Decoder~~ Decoding creates a problem

ed (32 bit) format

CISC

It is a micro-programming unit

Code execution is very slow

Single set of register is present.

Decoding is not a problem.

~~Variable~~ Variable (16-64 bit) format.

Shallow copy

CRAHM

A designer of a Computer System must calculate the amount of memory required for the particular application & Assign it to RAM or ROM

② The interconnection b/w memory & processor is than established for knowledge of the size of memory needed & the type of RAM & ROM Available

③ The addressing of memory can be established by means of a table that has specified the memory address assigned to each chip

④ The table called a Memory address Map in pictorial representation of a ~~fix~~ assign addressing space each chip in the system

③ To demonstrate with a particular example
that a computer system need 512 byte of RAM
& 512 bytes of ROM

The RAM & ROM chip to be used are
specified in figure

CS whatsapp 2 Dec.

Resistor Resistor Reference Architecture

In this org. ALU operation are perform only on a resistor data so operant are required in the resistor after manipulation Result is also placed in Resistor

Here 3 address instruction format is compatible instruction format

Stack Based CPU Org. →
The Computer which use Stack based CPU org. are based on a data structure

Stack is a list of Data word
Stack is a list of Data ~~word~~ word

it uses Last in First Out Access method which is most popular Access

method in most of CPU in this R Resistor we to store the address of top most element of Stack

Advantages of general based CPU

CPU Efficiency increase as the
as large No. of Resistor use less memory.
Space is used to store the program
because of the instruction are used
in compact way.

Dis. Adv. of general based CPU

Care should be taken to avoid unnecessary
uses of Resistors thus Compiler need to
be more intelligent in this aspect

~~Cost~~

Large No. of Resistor is used thus Extra
Cost is required in this organisation.

(Types of general Resistor based CPU)

① Resistor Memory ~~base~~ Reference Architec.

② In this Org. source 1 is always required
a Resistor Source 2 can be present Either
in Resistor or in Memory