

1. Description

1.1. Project

Project Name	Final_project
Board Name	custom
Generated with:	STM32CubeMX 6.13.0
Date	01/14/2025

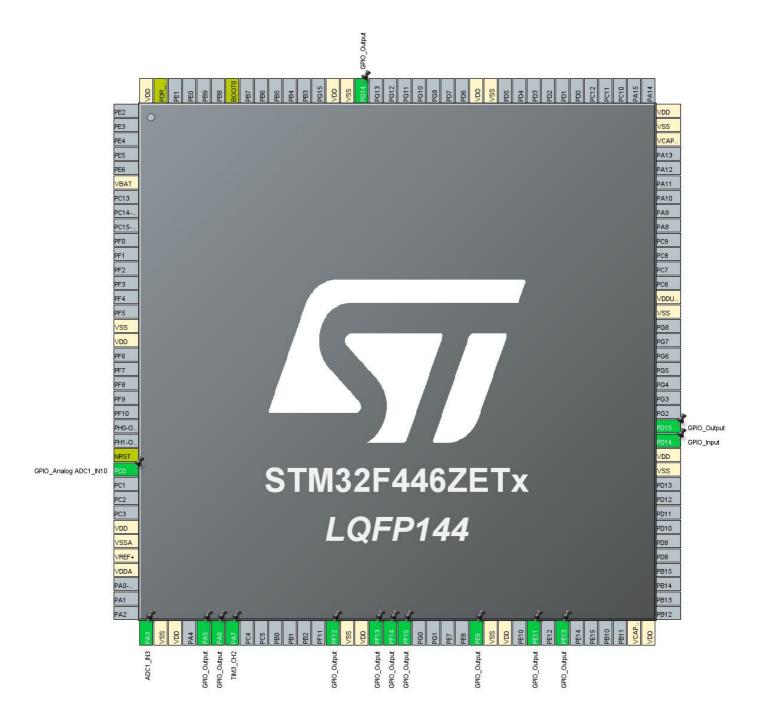
1.2. MCU

MCU Series	STM32F4
MCU Line	STM32F446
MCU name	STM32F446ZETx
MCU Package	LQFP144
MCU Pin number	144

1.3. Core(s) information

Core(s)	Arm Cortex-M4

2. Pinout Configuration



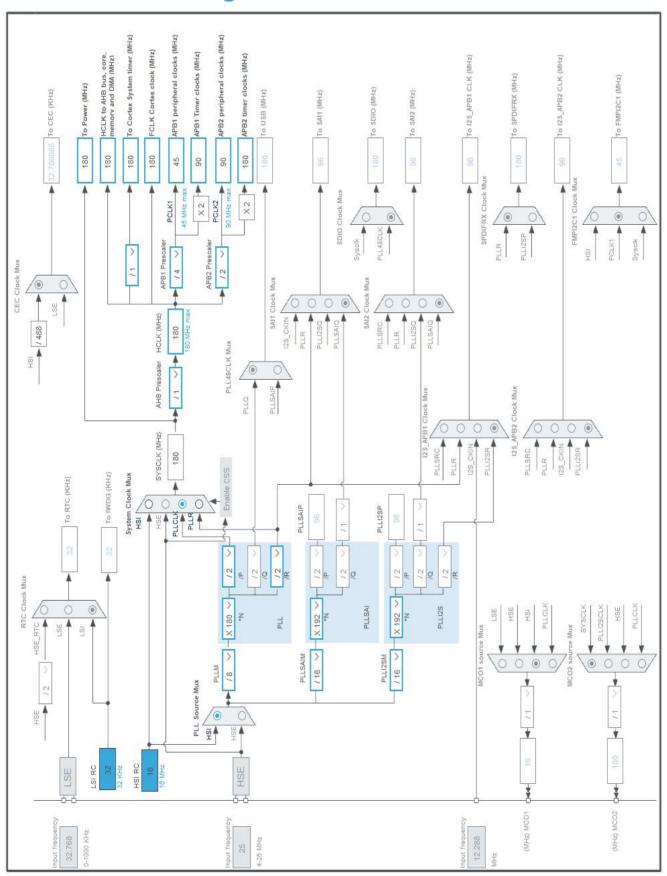
3. Pins Configuration

Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
6	VBAT	Power		
16	VSS	Power		
17	VDD	Power		
25	NRST	Reset		
26	PC0	I/O	GPIO_Analog, ADC1_IN10	
30	VDD	Power		
31	VSSA	Power		
32	VREF+	Power		
33	VDDA	Power		
37	PA3	I/O	ADC1_IN3	
38	VSS	Power		
39	VDD	Power		
41	PA5 *	I/O	GPIO_Output	
42	PA6 *	I/O	GPIO_Output	
43	PA7	I/O	TIM3_CH2	
50	PF12 *	I/O	GPIO_Output	
51	VSS	Power		
52	VDD	Power		
53	PF13 *	I/O	GPIO_Output	
54	PF14 *	I/O	GPIO_Output	
55	PF15 *	I/O	GPIO_Output	
60	PE9 *	I/O	GPIO_Output	
61	VSS	Power		
62	VDD	Power		
64	PE11 *	I/O	GPIO_Output	
66	PE13 *	I/O	GPIO_Output	
71	VCAP_1	Power		
72	VDD	Power		
83	VSS	Power		
84	VDD	Power		
85	PD14 *	I/O	GPIO_Input	
86	PD15 *	I/O	GPIO_Output	
94	VSS	Power		
95	VDDUSB	Power		
106	VCAP_2	Power		
107	VSS	Power		

Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
108	VDD	Power		
120	VSS	Power		
121	VDD	Power		
129	PG14 *	I/O	GPIO_Output	
130	VSS	Power		
131	VDD	Power		
138	BOOT0	Boot		
143	PDR_ON	Reset		
144	VDD	Power		

^{*} The pin is affected with an I/O function

4. Clock Tree Configuration



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1. Power Consumption Calculator report

1.1. Microcontroller Selection

Series	STM32F4
Line	STM32F446
MCU	STM32F446ZETx
Datasheet	DS10693_Rev6

1.2. Parameter Selection

Temperature	25
Vdd	3.3

1.3. Battery Selection

Battery	Li-SOCL2(A3400)
Capacity	3400.0 mAh
Self Discharge	0.08 %/month
Nominal Voltage	3.6 V
Max Cont Current	100.0 mA
Max Pulse Current	200.0 mA
Cells in series	1
Cells in parallel	1

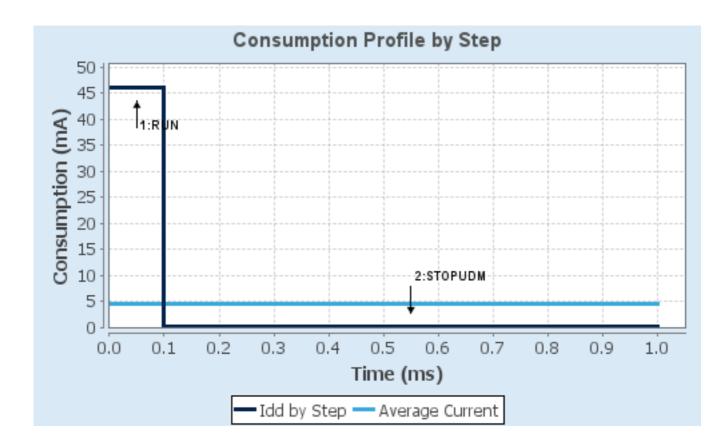
1.4. Sequence

Step	Step1	Step2
Mode	RUN	STOP UDM (Under Drive)
Vdd	3.3	3.3
Voltage Source	Battery	Battery
Range	Scale1-High	No Scale
Fetch Type	RAM/FLASH/REGON/ART/P REFETCH	n/a
CPU Frequency	180 MHz	0 Hz
Clock Configuration	HSE PLL	Regulator LP Flash-PwrDwn
Clock Source Frequency	4 MHz	0 Hz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	46 mA	55 μA
Duration	0.1 ms	0.9 ms
DMIPS	225.0	0.0
Ta Max	99.99	104.99
Category	In DS Table	In DS Table

1.5. Results

Sequence Time	1 ms	Average Current	4.65 mA
Battery Life	1 month	Average DMIPS	225.0 DMIPS

1.6. Chart



2. Software Project

2.1. Project Settings

Name	Value
Project Name	Final_project
Project Folder	C:\Users\yasin\STM32CubeIDE\workspace_1.17.0\Final_project
Toolchain / IDE	STM32CubeIDE
Firmware Package Name and Version	STM32Cube FW_F4 V1.28.1
Application Structure	Advanced
Generate Under Root	Yes
Do not generate the main()	No
Minimum Heap Size	0x200
Minimum Stack Size	0x400

2.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No
Enable Full Assert	No

2.3. Advanced Settings - Generated Function Calls

Rank	Function Name	Peripheral Instance Name
1	SystemClock_Config	RCC
2	MX_GPIO_Init	GPIO
3	MX_ADC1_Init	ADC1
4	MX_TIM3_Init	TIM3

3. Peripherals and Middlewares Configuration

3.1. ADC1 mode: IN3 mode: IN10

3.1.1. Parameter Settings:

ADCs_Common_Settings:

Mode Independent mode

ADC_Settings:

Clock Prescaler PCLK2 divided by 4

Resolution 12 bits (15 ADC Clock cycles)

Data Alignment

Scan Conversion Mode

Continuous Conversion Mode

Disabled

Discontinuous Conversion Mode

Disabled

DMA Continuous Requests

Disabled

End Of Conversion Selection EOC flag at the end of single channel conversion

ADC_Regular_ConversionMode:

Number Of Conversion 1

External Trigger Conversion Source Regular Conversion launched by software

External Trigger Conversion Edge None
Rank 1

Channel 3
Sampling Time 3 Cycles

ADC_Injected_ConversionMode:

Number Of Conversions 0

WatchDog:

Enable Analog WatchDog Mode false

3.2. RCC

3.2.1. Parameter Settings:

System Parameters:

VDD voltage (V) 3.3
Instruction Cache Enabled
Prefetch Buffer Enabled
Data Cache Enabled

Flash Latency(WS) 5 WS (6 CPU cycle)

RCC Parameters:

HSI Calibration Value 16

TIM Prescaler Selection Disabled
HSE Startup Timout Value (ms) 100
LSE Startup Timout Value (ms) 5000

Power Parameters:

Power Regulator Voltage Scale Power Regulator Voltage Scale 1

Power Over Drive Enabled

3.3. SYS

Timebase Source: SysTick

3.4. TIM3

Clock Source: Internal Clock
Channel2: PWM Generation CH2

3.4.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value) 180-1 *

Counter Mode Up

Counter Period (AutoReload Register - 16 bits value) 10000-1 *
Internal Clock Division (CKD) No Division
auto-reload preload Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit) Disable (Trigger input effect not delayed)

Trigger Event Selection Reset (UG bit from TIMx_EGR)

PWM Generation Channel 2:

Mode PWM mode 1

Pulse (16 bits value) 0

Output compare preload Enable

Fast Mode Disable

CH Polarity High

^{*} User modified value

4. System Configuration

4.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PC0	ADC1_IN10	Analog mode	No pull-up and no pull-down	n/a	
	PA3	ADC1_IN3	Analog mode	No pull-up and no pull-down	n/a	
TIM3	PA7	TIM3_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
GPIO	PC0	GPIO_Analog	Analog mode	No pull-up and no pull-down	n/a	
	PA5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PA6	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PF12	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PF13	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PF14	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PF15	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PE9	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PE11	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PE13	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PD14	GPIO_Input	Input mode	Pull-up *	n/a	
	PD15	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PG14	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	

4.2. DMA configuration

nothing configured in DMA service

4.3. NVIC configuration

4.3.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority	
Non maskable interrupt	true	0	0	
Hard fault interrupt	true	0	0	
Memory management fault	true	0	0	
Pre-fetch fault, memory access fault	true	0	0	
Undefined instruction or illegal state	true	0	0	
System service call via SWI instruction	true	0	0	
Debug monitor	true	0	0	
Pendable request for system service	true	0	0	
System tick timer	true	15	0	
PVD interrupt through EXTI line 16	unused			
Flash global interrupt	unused			
RCC global interrupt	unused			
ADC1, ADC2 and ADC3 interrupts	unused			
TIM3 global interrupt		unused		
FPU global interrupt	unused			

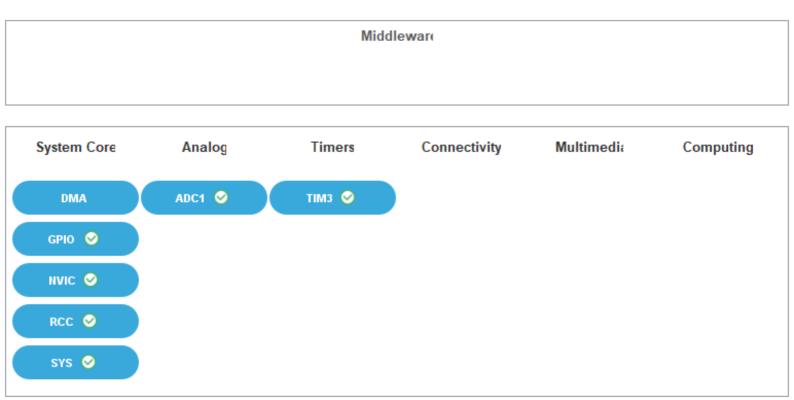
4.3.2. NVIC Code generation

Enabled interrupt Table	Select for init	Generate IRQ handler	Call HAL handler
	sequence ordering	nanulei	
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
Memory management fault	false	true	false
Pre-fetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false
System service call via SWI instruction	false	true	false
Debug monitor	false	true	false
Pendable request for system service	false	true	false
System tick timer	false	true	true

* User modified value

5. System Views

- 5.1. Category view
- 5.1.1. Current



6. Docs & Resources

Type Link

BSDL files https://www.st.com/resource/en/bsdl_model/stm32f446_bsdl.zip https://www.st.com/resource/en/ibis_model/stm32f446_ibis.zip

System View https://www.st.com/resource/en/svd/stm32f4-svd.zip

Description

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