Department of Computer Science & Engineering

Course No : **CSE 2106**
Course Title : **Digital Logic Design Sessional**

Experiment No : 08
Experiment Name : a) Design a 4 bit CLA (Carry Look Ahead) Adder Circuit
b) Design a Magnitude Comparator for 1-bit
c) Design an 8 to 3 Line Priority Encoder where priority is $I_0 > I_1 > I_2 > I_3 > I_4 > I_5 > I_6 > I_7$

Date of Submission : 05-02-22

Submitted to : **Zarin Tasnim Shejuti & Tamanna Tabassum**

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Experiment: Design a 4 bit CLA (Carrey Look Ahead) adder circuit

Objective: The carrey look ahead adder calculates one or more carrey bits before sum which reduces the wait time to calculate the result of the largere value bits of adder. So, ripple carrey adder is less efficient than CLA. The main objective is to design a 4-bit CLA adder circuit.

Truth Table: [For 1 bit Carrey Look Ahead Adder]

Input			Output	
C_{in}	A	B	C_{out}	Sum (S)
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

Function Evaluation using k-map:

Sum, $S = \Sigma(1,2,4,7)$

C_{in} \ AB	$\bar{A}\bar{B}$	$\bar{A}B$	AB	$A\bar{B}$
$\bar{C}_{in}$		[1]		[1]
C_{in}	[1]		[1]	

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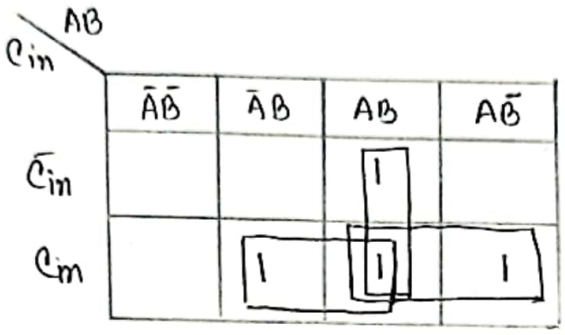
$S = \bar{A}\bar{B}C_{in} + \bar{A}B\bar{C}_{in} + A\bar{B}\bar{C}_{in} + ABC_{in}$

$= \bar{A}(\bar{B}C_{in} + B\bar{C}_{in}) + A(\bar{B}\bar{C}_{in} + BC_{in})$ [Distribution Law]

$= \bar{A}(B \oplus C_{in}) + A(\overline{B \oplus C_{in}})$ [definition of XOR, XNOR]

$= A \oplus B \oplus C_{in}$ [Definition of XOR]

$C_{out} = \Sigma(3,5,6,7)$



$C_{out} = BC_{in} + AC_{in} + AB$

$= C_{in}(B+A) + AB$ [Distribution Law]

$= C_{in}(B+A) \cdot 1 + AB$ [Identity Law]

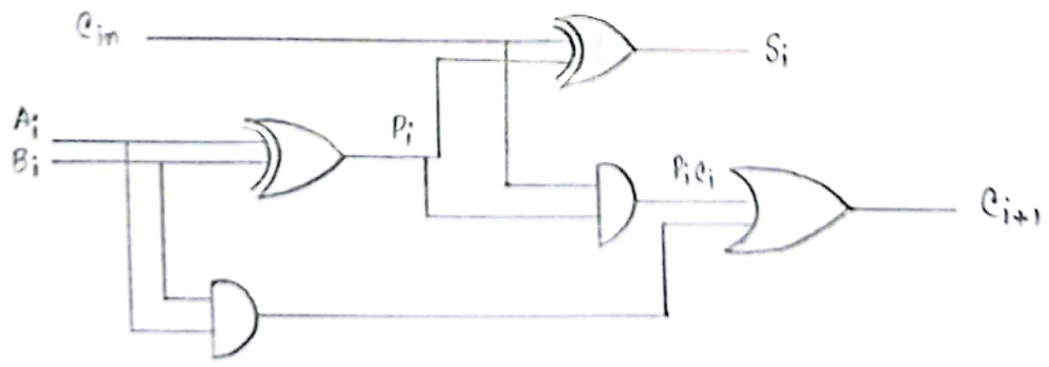
$= C_{in}(B+A)(B+\bar{B}) + AB$ [Complement Law]

$= C_{in}(A\bar{B} + \bar{A}B) + AB$ [Distribution Law]

$= AB + C_{in}(A \oplus B)$

Now, $S = A \oplus B \oplus C_{in}$

$C_{out} = AB + C_{in}(A \oplus B)$



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Here, $P_i = A_i \oplus B_i$ $\quad G_i = A_i B_i$

$S_i = P_i \oplus C_i$ $\quad C_{i+1} = G_i + P_i C_i$

For 1st bit:

$P_1 = A_1 \oplus B_1$

$G_1 = A_1 B_1$

$C_1 = 0$

$S_1 = P_1 \oplus C_1 = P_1 \; [\because C_1 = 0] = A_1 \oplus B_1$

For 2nd bit:

$P_2 = A_2 \oplus B_2$

$G_2 = A_2 B_2$

$C_2 = G_1 + P_1 C_1 = A_1 B_1 + (A_1 \oplus B_1) \cdot A_1 B_1$ [From 1st bit]

$S_3 = P_2 \oplus C_2 = (A_2 \oplus B_2) \oplus (A_1 B_1)$

For 3rd bit:

$P_3 = A_3 \oplus B_3$

$G_3 = A_3 B_3$

$C_3 = G_2 + P_2 C_2 = A_2 B_2 + (A_2 \oplus B_2) \cdot A_1 B_1$ [From 2nd bit]

$S_3 = P_3 \oplus C_3 = (A_3 \oplus B_3) \oplus [A_2 B_2 + (A_2 \oplus B_2) \cdot A_1 B_1]$

For 4th bit:

$P_4 = A_4 \oplus B_4$

$G_4 = A_4 B_4$

$C_4 = G_3 + P_3 C_3 = A_3 B_3 + (A_3 \oplus B_3) [A_2 B_2 + (A_2 \oplus B_2) \cdot A_1 B_1]$

[From 3rd bit]

$S_4 = P_4 \oplus C_4$

$= (A_4 \oplus B_4) \oplus [A_3 B_3 + (A_3 \oplus B_3) \{ A_2 B_2 + (A_2 \oplus B_2) \cdot A_1 B_1 \}]$

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Truth Table: [For 4 bit Carry Look Ahead Adder]

Input								Output				
A_3	A_2	A_1	A_0	B_3	B_2	B_1	B_0	C_{out}	S_3	S_2	S_1	S_0
0	0	1	1	0	0	0	1	0	0	1	0	0
0	1	0	1	0	0	1	1	0	1	0	0	0
0	1	1	0	1	0	0	1	0	1	1	1	1
1	0	1	1	0	1	0	1	1	0	0	0	0
1	1	0	0	1	1	0	0	1	1	0	0	0

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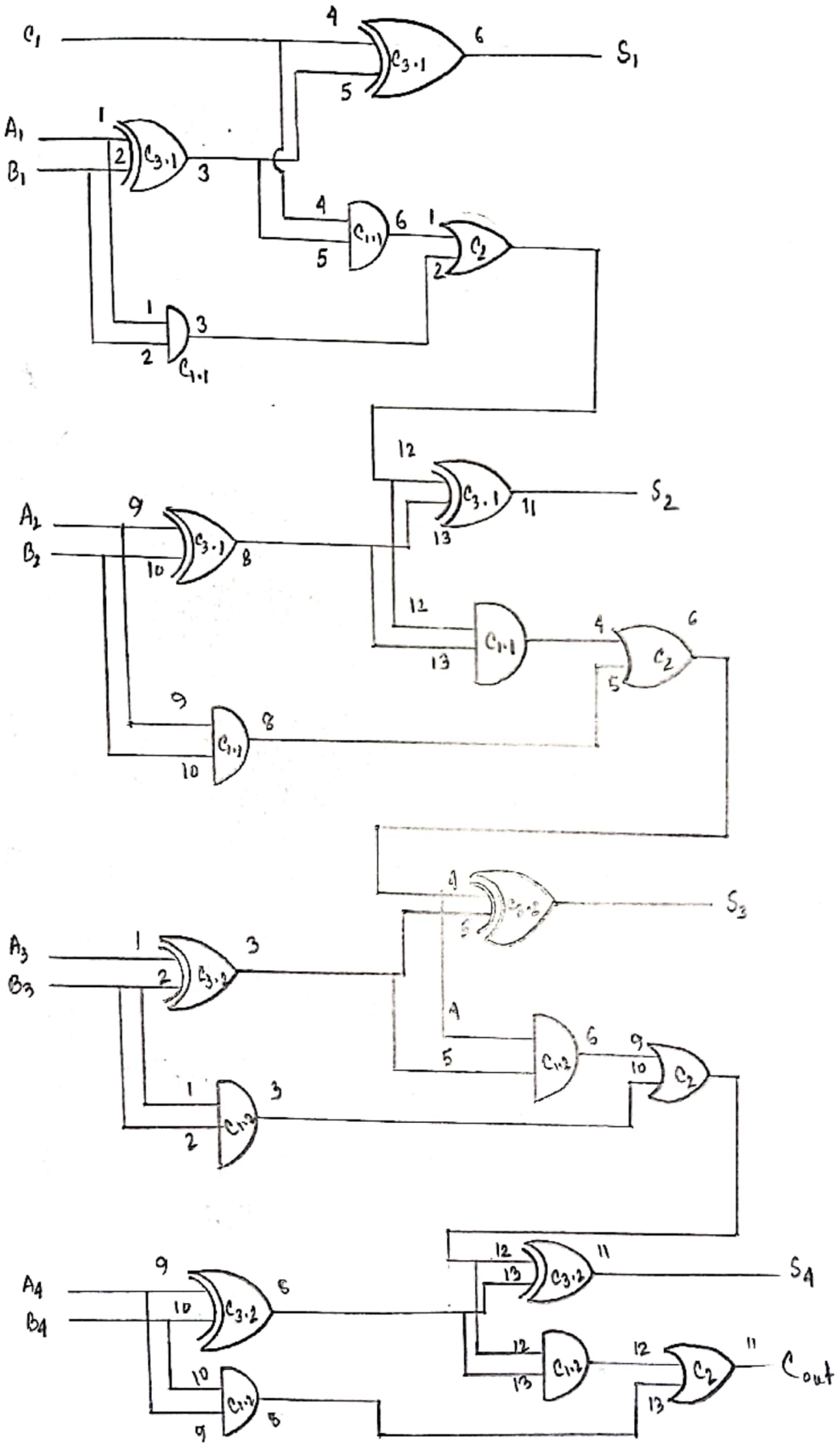
Circuit Diagram:



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IC Requirements:

1) $C_1 \rightarrow$ 74LS08 (AND Gate) $\rightarrow$ 2 pieces
2) $C_2 \rightarrow$ 74LS32 (OR Gate) $\rightarrow$ 1 piece
3) $C_3 \rightarrow$ 74LS86 (XOR Gate) $\rightarrow$ 2 pieces

Conclusion: We have learnt through this experiment how to design a 4 bit CLA Adder Circuit which reduces the time and efficiently do addition without adding the previous elements.

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Experiment Name: Design a Magnitude Comparator for 4 bit.

Objective: A magnitude comparator is a combinational circuit that compares two digit or binary number in order to find out whether one binary number is equal or less or greater than other binary number. The main objective of this experiment is to design a magnitude comparator for 4 bit to check whether two inputs are $A>B$, $A=B$ or $A<B$.

Truth Table: (For 1 bit Magnitude Comparator)

Input		Output		
A	B	$F_1 (A>B)$	$F_2 (A=B)$	$F_3 (A<B)$
0	0	0	1	0
0	1	0	0	1
1	0	1	0	0
1	1	0	1	0

For, 1 bit: we write, $F_1 = A_1 \bar{B}_1$ when $A>B$

$F_2 = \bar{A}_1 \bar{B}_1 + A_1 B_1 = \overline{A_1 \oplus B_1}$ when $A=B$

$F_3 = \bar{A}_1 B_1$ when $A<B$

For 2 bit: $A = A_2 A_1$; $B = B_2 B_1$

$(A>B) \Rightarrow (A_2 > B_2) + (A_2 = B_2) \cdot (A_1 > B_1)$

$\Rightarrow A_2 \bar{B}_2 + \overline{A_2 \oplus B_2} \; (A_1 \bar{B}_1)$

$(A=B) \Rightarrow (A_2 = B_2)\,(A_1 = B_1) \Rightarrow \overline{A_2 \oplus B_2} \cdot \overline{A_1 \oplus B_1}$

$(A<B) \Rightarrow (A_2 < B_2) + (A_2 = B_2)\,(A_1 < B_1)$

$\Rightarrow \bar{A}_2 \cdot B_2 + \overline{A_2 \oplus B_2} \; (\bar{A}_1 \cdot B_1)$

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Truth Table: (For 4 bit Magnitude Comparator)

Input								Output		
A_4	A_3	A_2	A_1	B_4	B_3	B_2	B_1	A>B	A=B	A<B
1	0	0	0	0	1	0	0	1	0	0
1	1	0	0	1	1	0	0	0	1	0
1	0	0	1	1	0	1	1	0	0	1
0	1	0	1	0	0	0	1	1	0	0

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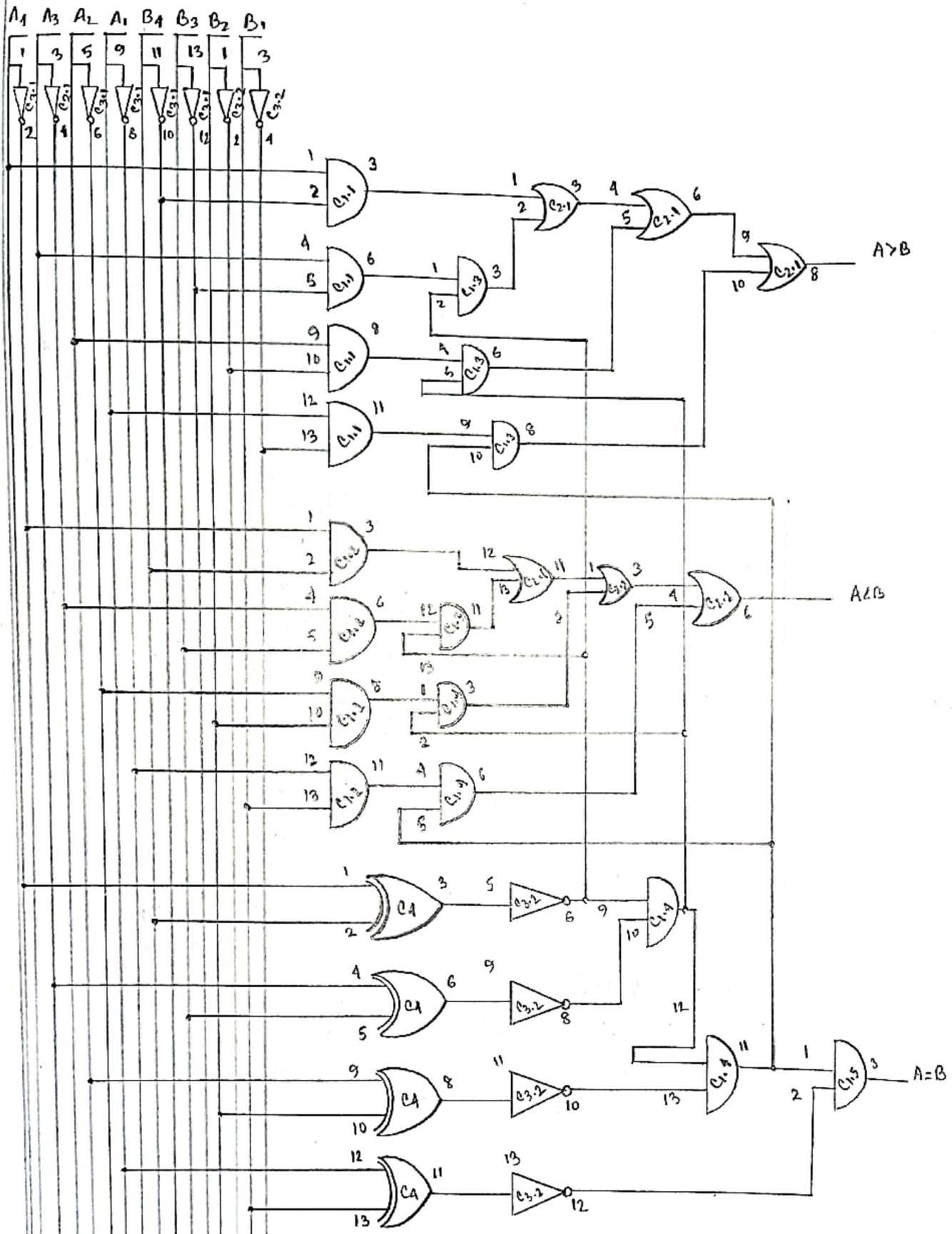
Circuit Diagram:



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IC Requirements:

1. C_1 → 74LS08 (AND Gate) - 5 pieces
2. C_2 → 74LS32 (OR Gate) - 2 pieces
3. C_3 → 74LS04 (NOT Gate) - 2 pieces
4. C_4 → 74LS86 (XOR Gate) - 1 piece

Conclusion: Through this experiment, we have successfully designed a magnitude comparator using basic gates such as AND, OR, NOT and X-OR for 4 bits.

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Experiment: Design a 8 to 3 line Priority Encoder where the priority is $I_0 > I_1 > I_2 > I_3 > I_4 > I_5 > I_6 > I_7$

Objective: A priority encoder is an encoder circuit that includes the priority encoder is such that if two or more inputs are equal to 1 at the same time, the input having the highest priority will take preference. Here, we have to design a 8 to 3 line priority encoder.

Truth Table:

Input								Output		
I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7	F_0	F_1	F_2
0	0	0	0	0	0	0	1	1	1	1
0	0	0	0	0	0	1	x	1	1	0
0	0	0	0	0	1	x	x	1	0	1
0	0	0	0	1	x	x	x	1	0	0
0	0	0	1	x	x	x	x	0	1	1
0	0	1	x	x	x	x	x	0	1	0
0	1	x	x	x	x	x	x	0	0	1
1	x	x	x	x	x	x	x	0	0	0

Here, $F_0 = \bar{I}_0\bar{I}_1\bar{I}_2\bar{I}_3\bar{I}_4\bar{I}_5\bar{I}_6 I_7 + \bar{I}_0\bar{I}_1\bar{I}_2\bar{I}_3\bar{I}_4\bar{I}_5 I_6 + \bar{I}_0\bar{I}_1\bar{I}_2\bar{I}_3\bar{I}_4\bar{I}_5 + \bar{I}_0\bar{I}_1\bar{I}_2\bar{I}_3 I_4$

$= (\bar{I}_0\bar{I}_1\bar{I}_2\bar{I}_3)(\bar{I}_4\bar{I}_5\bar{I}_6 I_7 + \bar{I}_4\bar{I}_5 I_6 + \bar{I}_4 I_5 + I_4)$ [Distributive Law]

$= (\bar{I}_0\bar{I}_1\bar{I}_2\bar{I}_3)\{\bar{I}_4\bar{I}_5(\bar{I}_6 I_7 + I_6) + \bar{I}_4 I_5 + I_4\}$ [Distributive Law]

$= (\bar{I}_0\bar{I}_1\bar{I}_2\bar{I}_3)\{\bar{I}_4\bar{I}_5(I_6 + I_7) + I_4 + I_5\}$ [Absorption Law]

$= (\bar{I}_0\bar{I}_1\bar{I}_2\bar{I}_3)(\bar{I}_4\bar{I}_5 I_6 + \bar{I}_4\bar{I}_5 I_7 + I_4 + I_5)$ [Distributive Law]

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$= (\bar{I}_0 \bar{I}_1 \bar{I}_2 \bar{I}_3)\{(\bar{I}_5 + I_5)(I_5 + \bar{I}_4 I_6) + (\bar{I}_4 + I_4)(I_4 + \bar{I}_5 I_7)\}$ [Distributive Law]

$= (\bar{I}_0 \bar{I}_1 \bar{I}_2 \bar{I}_3)(I_5 + \bar{I}_4 I_6 + I_4 + \bar{I}_5 I_7)$ [Complement Law]

$= (\bar{I}_0 \bar{I}_1 \bar{I}_2 \bar{I}_3)\{(I_5 + \bar{I}_5 I_7) + (I_4 + \bar{I}_4 I_6)\}$ [Commutative Law]

$= (\bar{I}_0 \bar{I}_1 \bar{I}_2 \bar{I}_3)(I_4 + I_5 + I_6 + I_7)$ [Absorption Law]

$\therefore F_0 = (\bar{I}_0 \bar{I}_1 \bar{I}_2 \bar{I}_3)(I_4 + I_5 + I_6 + I_7)$

$F_1 = \bar{I}_0 \bar{I}_1 \bar{I}_2 \bar{I}_3 \bar{I}_4 \bar{I}_5 \bar{I}_6 I_7 + \bar{I}_0 \bar{I}_1 \bar{I}_2 \bar{I}_3 \bar{I}_4 \bar{I}_5 I_6 + \bar{I}_0 \bar{I}_1 \bar{I}_2 I_3 + \bar{I}_0 \bar{I}_1 I_2$

$= \bar{I}_0 \bar{I}_1 (\bar{I}_2 \bar{I}_3 \bar{I}_4 \bar{I}_5 \bar{I}_6 I_7 + \bar{I}_2 \bar{I}_3 \bar{I}_4 \bar{I}_5 I_6 + \bar{I}_2 I_3 + I_2)$ [Distributive Law]

$= \bar{I}_0 \bar{I}_1 \{\bar{I}_2 \bar{I}_3 \bar{I}_4 \bar{I}_5 (\bar{I}_6 I_7 + I_6) + \bar{I}_2 I_3 + I_2\}$ [Distributive Law]

$= \bar{I}_0 \bar{I}_1 \{\bar{I}_2 \bar{I}_3 \bar{I}_4 \bar{I}_5 (I_6 + I_7) + I_2 + I_3$ [Absorption Law]

$= \bar{I}_0 \bar{I}_1 (\bar{I}_2 \bar{I}_3 \bar{I}_4 \bar{I}_5 I_6 + \bar{I}_2 \bar{I}_3 \bar{I}_4 \bar{I}_5 I_7 + I_2 + I_3)$ [Distributive Law]

$= \bar{I}_0 \bar{I}_1 [(\bar{I}_2 + I_2)(I_2 + \bar{I}_3 \bar{I}_4 \bar{I}_5 I_6) + (\bar{I}_3 + I_3)(I_3 + \bar{I}_2 \bar{I}_4 \bar{I}_5 I_7)]$ [Distributive Law]

$= \bar{I}_0 I_1 [I_2 + \bar{I}_3 \bar{I}_4 \bar{I}_5 I_6 + I_3 + \bar{I}_2 \bar{I}_4 \bar{I}_5 I_7]$ [Complement Law]

$= \bar{I}_0 \bar{I}_1 [I_3 + I_2 + \bar{I}_4 \bar{I}_5 (I_6 + I_7)]$ [Distributive Law]

$F_1 = \bar{I}_0 \bar{I}_1 [I_2 + I_3 + \bar{I}_4 \bar{I}_5 (I_6 + I_7)]$

$F_2 = \bar{I}_0 \bar{I}_1 \bar{I}_2 \bar{I}_3 \bar{I}_4 \bar{I}_5 \bar{I}_6 I_7 + \bar{I}_0 \bar{I}_1 \bar{I}_2 \bar{I}_3 \bar{I}_4 I_5 + \bar{I}_0 \bar{I}_1 \bar{I}_2 I_3 + \bar{I}_0 I_1$

$= \bar{I}_0 (\bar{I}_1 \bar{I}_2 \bar{I}_3 \bar{I}_4 \bar{I}_5 \bar{I}_6 I_7 + \bar{I}_1 \bar{I}_2 \bar{I}_3 \bar{I}_4 I_5 + \bar{I}_1 \bar{I}_2 I_3 + I_1)$

$= \bar{I}_0 \{\bar{I}_1 \bar{I}_2 \bar{I}_3 \bar{I}_4 (\bar{I}_5 \bar{I}_6 I_7 + I_5) + (\bar{I}_1 + I_1)(I_1 + \bar{I}_2 I_3)\}$ [Distributive Law]

$= \bar{I}_0 \{\bar{I}_1 \bar{I}_2 \bar{I}_3 \bar{I}_4 (I_5 + \bar{I}_6 I_7) + I_1 + \bar{I}_2 I_3\}$ [Complement Law]

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$= \bar{I}_0 \{ \bar{I}_1 \bar{I}_2 \bar{I}_3 \bar{I}_4 I_5 + \bar{I}_1 \bar{I}_2 \bar{I}_3 \bar{I}_4 \bar{I}_6 I_7 + I_1 + \bar{I}_2 \}$ [Distribution Law]

$= \bar{I}_0 (I_1 + \bar{I}_2 \bar{I}_3 \bar{I}_4 I_5 + \bar{I}_2 \bar{I}_3 \bar{I}_4 I_6 I_7 + \bar{I}_2 I_3)$ [Absorption Law]

$= \bar{I}_0 [I_1 + \bar{I}_2 (\bar{I}_3 \bar{I}_4 I_5 + \bar{I}_3 \bar{I}_4 \bar{I}_6 I_7 + I_3)]$ [Distribution Law]

$= \bar{I}_0 [I_1 + \bar{I}_2 (I_3 + \bar{I}_4 I_5 + \bar{I}_4 \bar{I}_6 I_7)]$ [Absorption Law]

$= \bar{I}_0 [I_1 + \bar{I}_2 \{ I_3 + \bar{I}_4 (I_5 + \bar{I}_6 I_7) \}]$ [Distribution Law]

$F_2 = \bar{I}_0 [I_1 + \bar{I}_2 \{ I_3 + \bar{I}_4 (I_5 + \bar{I}_6 I_7) \}]$

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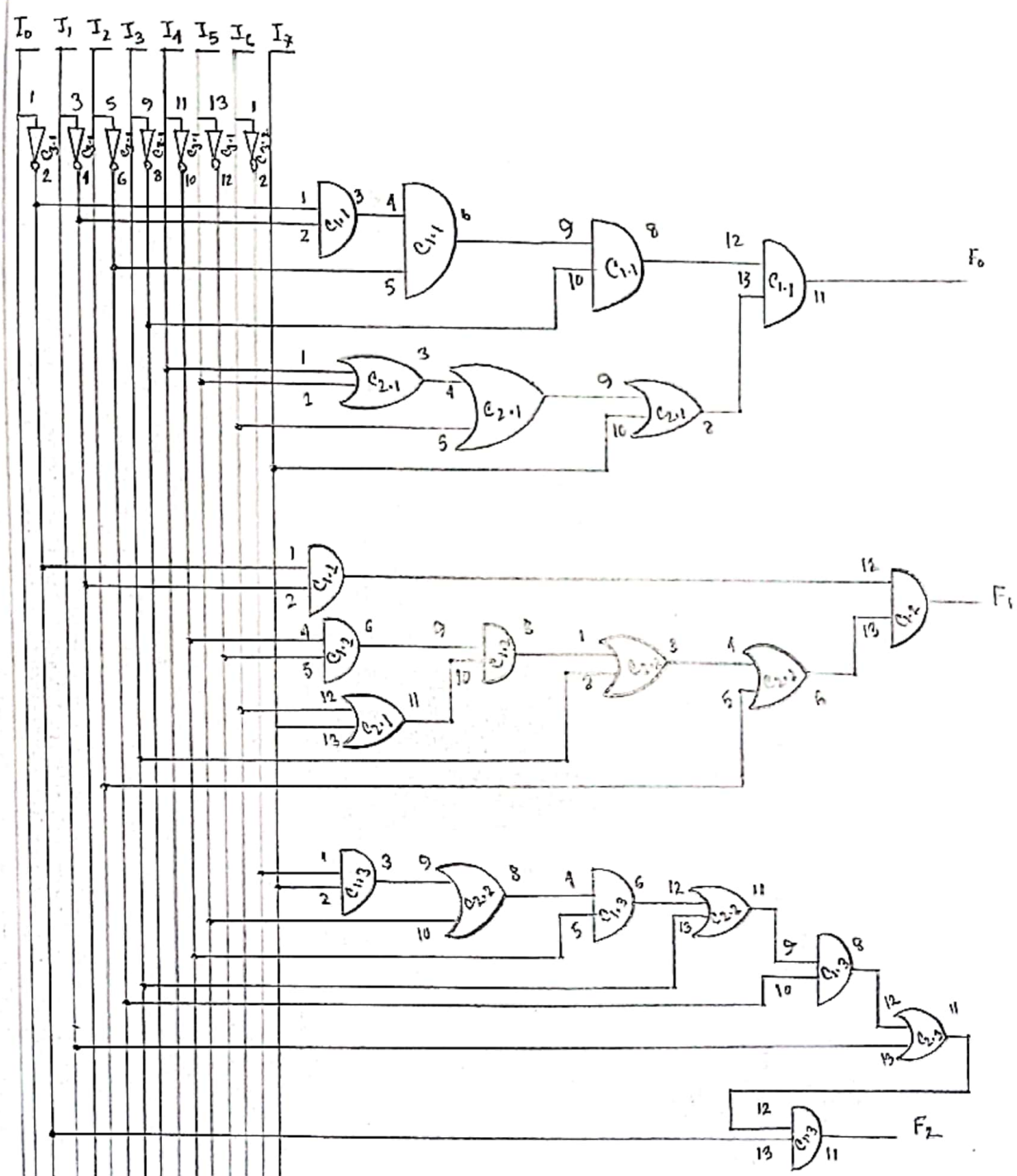
Circuit Diagram:



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IC Requirements:

1. C_1 → 74LS08 (AND Gate) → 3 pieces
2. C_2 → 74LS32 (OR Gate) → 3 pieces
3. C_3 → 74LS04 (NOT Gate) → 2 pieces

Conclusion: We have designed a 8 to 3 line priority encoder where the priority is $I_0 > I_1 > I_2 > I_3 > I_4 > I_5 > I_6 > I_7$. I_0 has the most priority and I_7 has least priority. From truth table we have gained F_0, F_1, F_2 expressions and by using logic gates we have implemented those expression properly and got proper output.