Department of Computer Science & Engineering

Course No	**: CSE 2106**
Course Title	**: Digital Logic Design Sessional**
Experiment No	: 09
Experiment Name	: (a) Implement the following boolean function using (i) 1 to 8 Line De-Multiplexer / 3 to 8 Line Decoder (IC-74138) (ii) 1 to 16 Line De-Multiplexer / 4 to 16 Line Decoder (IC-74154) $F(A,B,C,D) = \Sigma(1,3,4,8,12,14)$ (b) Implement the following boolean function using (i) An 8 to 1 Line Multiplexer (IC-74151) (ii) An 4 to 1 Line Multiplexer (IC-74153) $F(A,B,C,D) = \Sigma(1,3,4,8,12,14)$
Date of Submission	: 12-02-22
Submitted to	**: Zarin Tasnim Shejuti & Tamanna Tabassum**

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Experiment Name: Implement the following boolean function using
(i) 1 to 8 Line Demultiplexer / 3 to 8 line Decoder (IC-74138)
(ii) 1 to 16 Line De-multiplexer / 4 to 16 line Decoder (IC-74154) $F(A,B,C,D) = \Sigma(1,3,4,8,12,14)$

Objective: De multiplexer also known as Decoder. It is a combinational Logic circuit that receives the information on a signal input line and transfer the same information are of 'n' possible outlines. It consist of 1 input line, 'n' outputlines and 'm' selector lines. In this 'm' selector lines are required to produce 2^m possible output lines ($2^m = n$). 1 to 8 line demultiplexer, it requires a selector lines to control 8 output lines ($2^3 = 8$). The demultiplexer is called 3 to 8 line decoder. The main objective of this experiment is to implement this above function using 3 to 8 Line decoder and 4 to 16 - line Decoder.

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Truth Table :

Input				Output
A	B	C	D	F
0	0	0	0	0
0	0	0	1	1
0	0	1	0	0
0	0	1	1	1
0	1	0	0	1
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	1
1	0	0	1	0
1	0	1	0	0
1	0	1	1	0
1	1	0	0	1
1	1	0	1	0
1	1	1	0	1
1	1	1	1	0

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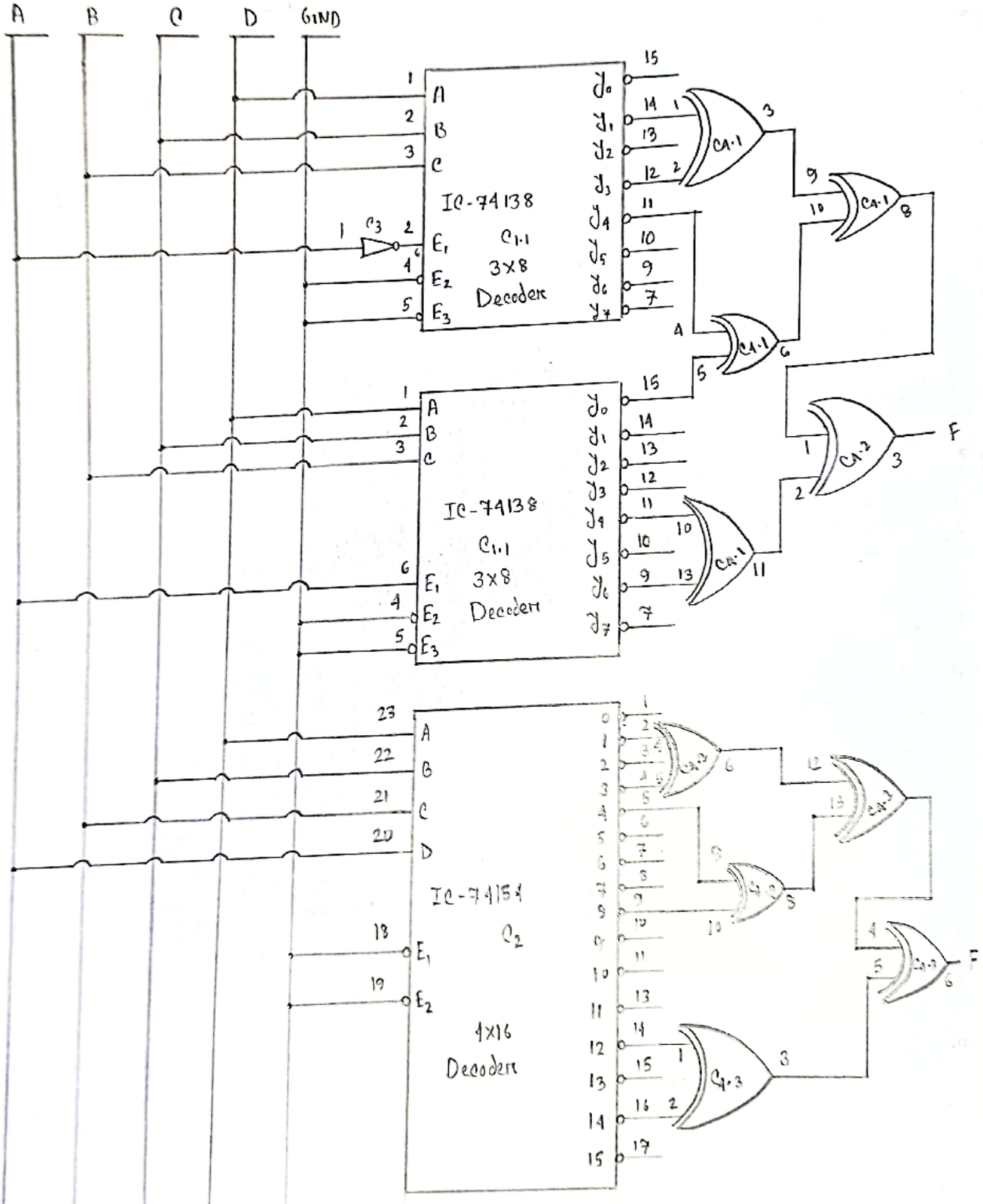
Circuit Diagram:

i) 3 to 8 Line Decoder

ii) 4 to 16 Line Decoder



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IC Requirements:

1. C_1 → IC - 74138 (3 to 8 Line Decoder) - 2 pieces
2. C_2 → IC - 74154 (4 to 16 Line Decoder) - 1 piece
3. C_3 → IC - 74LS04 (NOT Gate) - 1 piece
4. C_4 → IC - 74LS86 (XOR Gate) - 4 pieces

Conclusion: In this experiment we successfully have implemented the given function using both 3-8 Line Decoder and 4- to 16 Line Decoder.

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Experiment Name: Implement the following boolean function using
(i) An 8 to 1 Line Multiplexer (IC-74151)
(ii) An 4 to 8 Line Multiplexer (IC-74153)

$F(A,B,C,D) = \Sigma(1,3,4,8,12,14)$

Objective: A multiplexer is a device that selects between several analog or digital input signals and towards it to a single output line. The objective is to implement the given function using 8 to 1 line and 4 to 1 Line Multiplexer. Implementation table have to be used for this implementation.

Truth Table:

Input				Output
A	B	C	D	F
0	0	0	0	0
0	0	0	1	1
0	0	1	0	0
0	0	1	1	1
0	1	0	0	1
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	1
1	0	0	1	0
1	0	1	0	0
1	0	1	1	0
1	1	0	0	1
1	1	0	1	0
1	1	1	0	1
1	1	1	1	0

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Implementation Table:

For 8 x 1 MUX:

$$F(A,B,C,D) = \Sigma(1,3,4,8,12,14)$$

selector $8 = 2^3$ (B, C, D)

MUX Input Line	I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7
$\bar{A}$	0	(1)	2	(3)	(4)	5	6	7
A	(8)	9	10	11	(12)	13	(14)	15
Input values	A	$\bar{A}$	0	$\bar{A}$	1	0	A	0

For 4 x 1 MUX:

$$F(A,B,C,D) = \Sigma(1,3,4,8,12,14)$$

Selector, $4 = 2^2$ (C, D)

MUX Input Line	I_0	I_1	I_2	I_3
$\bar{A}\bar{B}$	0	(1)	2	(3)
$\bar{A}B$	(4)	5	6	7
$A\bar{B}$	(8)	9	10	11
AB	(12)	13	(14)	15
Input Value	✱	$\bar{A}\bar{B} = \overline{A+B}$	AB	$\bar{A}\bar{B} = \overline{A+B}$

Here, ✱ $\rightarrow$ $\bar{A}B + A\bar{B} + AB$

$= \bar{A}B + A(\bar{B}+B)$ [Distributive Law]

$= \bar{A}B + A \cdot 1$ [Complement Law]

$= \bar{A}B + A$

$= (\bar{A}+A)(B+A)$ [Distributive Law]

$= (A+B)$ [Complement Law]

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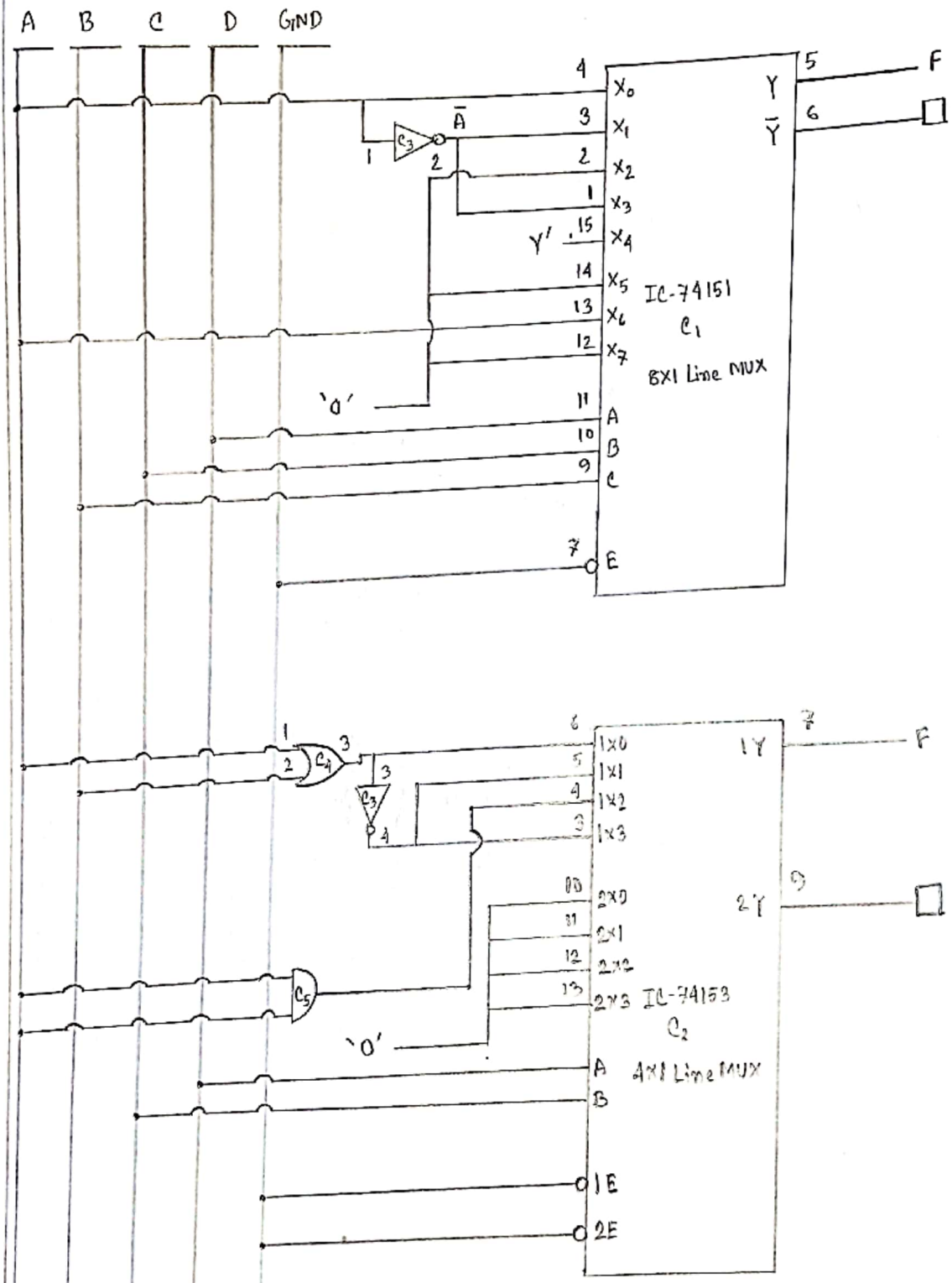
Circuit Diagram:



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IC Requirements:

1. C_1 → IC - 74151 (8 to 1 Line MUX) - 1 piece
2. C_2 → IC - 74153 (4 to 1 Line MUX) - 1 piece
3. C_3 → IC - 74LS04 (NOT Gate) - 1 piece
4. C_4 → IC - 74LS32 (OR Gate) - 1 piece
5. C_5 → IC - 74LS08 (AND Gate) - 1 piece

Conclusion: We have implemented two type of MUX. We have implemented 8×1 Line multiplexer and 4×1 Line multiplexer with the help of implementation table. We have maintained carefulness while working with these mux and every input pin is implemented correctly and thus the proper output is received.