Department of Computer Science & Engineering

Course No : **CSE 2106**
Course Title : **Digital Logic Design Sessional**

Experiment No : 10
Experiment Name : (a) Design a switch controlled Binary random up-down counter using J-k Flip-Flop for following sequence.
If s=0 down, $3 \leftarrow 0 \leftarrow 5 \leftarrow 2 \leftarrow 1$
If s=1 up, $3 \rightarrow 0 \rightarrow 5 \rightarrow 2 \rightarrow 1$
(b) Design a 4 bit Synchronous down counter using TFF
(a) Design a BCD Ripple Up Counter using D Flip-Flop
Date of Submission : 26-02-22

Submitted to : **Zarin Tasnim Shejuti & Tamanna Tabassum**

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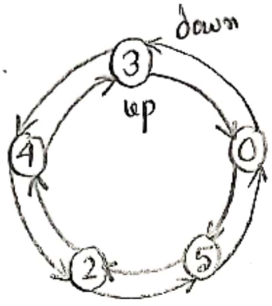
Experiment Name: (a) Design a Switch Controlled Binary Random Up-down Counter Using J-K Flip-Flop for the following Sequence:

If S=0, Down : 3 ← 0 ← 5 ← 2 ← 1

If S=1, Up : 3 → 0 → 5 → 2 → 1

Objective: In this experiment, we are going to design a switch controlled binary random up-down Counter using J-K flip-flop. If the Switch, S=0 it will work as down counter otherwise, if the switch S=1 it will work as a up counter.

State Diagram:



State Table:

Switch	Present State	Next State
0(down)	3	1
	0	3
	5	0
	2	5
	1	2
1(up)	3	0
	0	5
	5	2
	2	4
	4	3

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Number of flip-flop: In the sequence, the maximum value is 5, so the number of flip-flops = $\lceil \log_2 5 \rceil = 3$

Excitation Table:

Decimal	Switch	Present State			Next State			JK FF's input					
		Q_3	Q_2	Q_1	Q_3'	Q_2'	Q_1'	J_3	K_3	J_2	K_2	J_1	K_1
3	0	0	1	1	1	0	0	1	X	X	1	X	1
0	0	0	0	0	0	1	1	0	X	1	X	1	X
5	0	1	0	1	0	0	0	X	1	0	X	X	1
2	0	0	1	0	1	0	1	1	X	X	1	1	X
4	0	1	0	0	0	1	0	X	1	1	X	0	X
11	1	0	1	1	0	0	0	0	X	X	1	X	1
8	1	0	0	0	1	0	1	1	X	0	X	1	X
13	1	1	0	1	0	1	0	X	1	1	X	X	1
10	1	0	1	0	1	0	0	1	X	X	1	0	X
12	1	1	0	0	0	1	1	X	1	1	X	1	X

Function Simplification using k-map:

Here, Common don't care, $d = \Sigma(1,6,7,9,14,15)$

$J_3 = \Sigma(3,2,8,10)$

$d = \Sigma(1,4,5,6,7,9,12,13,14,15)$

$K_3 = \Sigma(4,5,12,13)$

$d = \Sigma(1,2,3,6,7,8,9,10,11,14,15)$

SQ_3 \ Q_2Q_1	$\bar{Q}_2\bar{Q}_1$	$\bar{Q}_2Q_1$	Q_2Q_1	$Q_2\bar{Q}_1$
$\bar{S}\bar{Q}_3$		X	1	1
$\bar{S}Q_3$	X	X	X	X
$S Q_3$	X	X	X	X
$S\bar{Q}_3$	1	X		1

$J_3 = \bar{S}Q_2 + S\bar{Q}_1$

SQ_3 \ Q_2Q_1	$\bar{Q}_2\bar{Q}_1$	$\bar{Q}_2Q_1$	Q_2Q_1	$Q_2\bar{Q}_1$
$\bar{S}\bar{Q}_3$	X	X	X	X
$\bar{S}Q_3$	1	1	X	X
$S Q_3$	1	1	X	X
$S\bar{Q}_3$	X	X	X	X

$K_3 = 1$

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$J_2 = \Sigma(0,4,12,13)$

$d = \Sigma(1,2,3,7,9,6,10,11,14,15)$

SQ_3 \ Q_2Q_1	$\bar{Q}_2\bar{Q}_1$	$\bar{Q}_2Q_1$	Q_2Q_1	$Q_2\bar{Q}_1$
$\bar{S}\bar{Q}_3$	1	X	X	X
$\bar{S}Q_3$	1		X	X
SQ_3	1	1	X	X
$S\bar{Q}_3$		X	X	X

$J_2 = SQ_3 + \bar{S}\bar{Q}_1$

$K_2 = \Sigma(2,3,10,11)$

$d = \Sigma(0,1,4,5,6,7,8,9,12,13,14,15)$

SQ_3 \ Q_2Q_1	$\bar{Q}_2\bar{Q}_1$	$\bar{Q}_2Q_1$	Q_2Q_1	$Q_2\bar{Q}_1$
$\bar{S}\bar{Q}_3$	X	X	1	1
$\bar{S}Q_3$	X	X	X	X
SQ_3	X	X	X	X
$S\bar{Q}_3$	X	X	1	1

$K_2 = 1$

$J_1 = \Sigma(0,2,8,12)$

$d = \Sigma(1,3,5,6,7,9,11,13,14,15)$

SQ_3 \ Q_2Q_1	$\bar{Q}_2\bar{Q}_1$	$\bar{Q}_2Q_1$	Q_2Q_1	$Q_2\bar{Q}_1$
$\bar{S}\bar{Q}_3$	1	X	X	1
$\bar{S}Q_3$		X	X	X
SQ_3	1	X	X	X
$S\bar{Q}_3$	1	X	X	

$J_1 = \bar{S}\bar{Q}_3 + S\bar{Q}_2$

$K_1 = \Sigma(3,5,11,13)$

$d = \Sigma(0,1,2,4,6,7,8,9,10,12,14,15)$

SQ_3 \ Q_2Q_1	$\bar{Q}_2\bar{Q}_1$	$\bar{Q}_2Q_1$	Q_2Q_1	$Q_2\bar{Q}_1$
$\bar{S}\bar{Q}_3$	X	X	1	X
$\bar{S}Q_3$	X	1	X	X
SQ_3	X	1	X	X
$S\bar{Q}_3$	X	X	1	X

$K_1 = 1$

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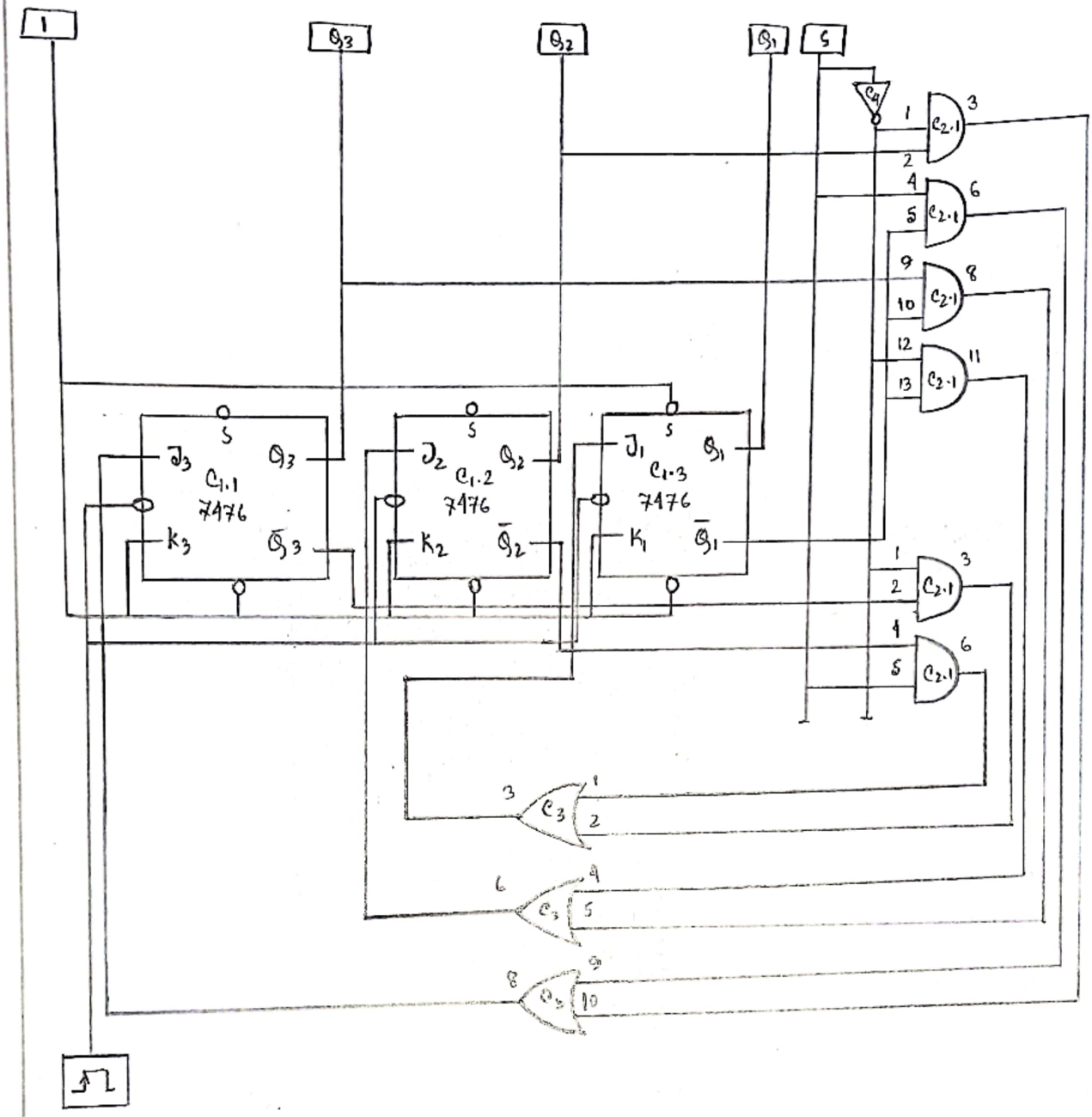
Circuit Diagram:



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IC Requirements:

1. JK flip-flop (7476 → C_1) - 3 pieces
2. AND (74LS08 → C_2) - 2 pieces
3. OR (74LS32 → C_3) - 1 piece
4. NOT (74LS04 → C_4) - 1 piece

Conclusion: From this experiment, we have constructed a switch controlled binary random up-down counted using JK flip-flop. When the switch is turned off it works as down counter and when the switch is on it works as up counter.

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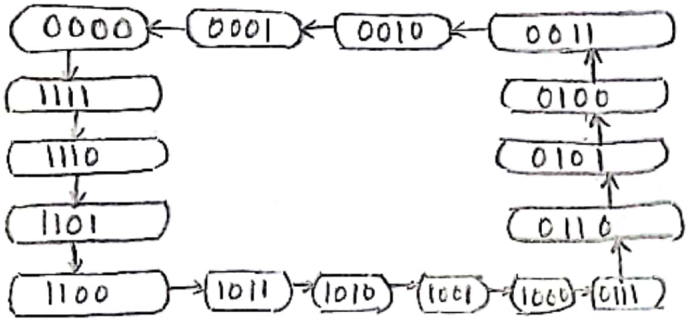
Experiment Name: (b) Design a 4 bit Synchronus Down-Counter using T Flip-Flop.

Objective: Here, we are going to construct a circuit for 4 bit Synchronus Down Counter using T Flip-Flop. JK Flip-Flop can work as a T Flip-Flop if we input the same value in J & K. Here both the values of J and K can either be zero or one. By using this method, we can construct a JK flip-flop IC into a T Flip-Flop IC.

State Diagram:



State Table:

Present State	Next State
0	15
1	0
2	1
3	2
4	3
5	4
6	5
7	6
8	7
9	8
10	9
11	10
12	11
13	12
14	13
	14

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Number of Flip-Flop:

Highest Number = 15

Number of Flip-Flop = $\lceil \log_2 15 \rceil = 4$

Excitation Table:

Decimal	Present State				Next State				Flip Flop Input			
	Q_4'	Q_3'	Q_2'	Q_1'	Q_4	Q_3	Q_2	Q_1	T_4	T_3	T_2	T_1
0	0	0	0	0	1	1	1	1	1	1	1	1
1	0	0	0	1	0	0	0	0	0	0	0	1
2	0	0	1	0	0	0	0	1	0	0	1	1
3	0	0	1	1	0	0	1	0	0	0	0	1
4	0	1	0	0	0	0	1	1	0	1	1	1
5	0	1	0	1	0	1	0	0	0	0	0	1
6	0	1	1	0	0	1	0	1	0	0	1	1
7	0	1	1	1	0	1	1	0	0	0	0	1
8	1	0	0	0	0	1	1	1	1	1	1	1
9	1	0	0	1	1	0	0	0	0	0	0	1
10	1	0	1	0	1	0	0	1	0	0	1	1
11	1	0	1	1	1	0	1	0	0	0	0	1
12	1	1	0	0	1	0	1	1	0	1	1	1
13	1	1	0	1	1	1	0	0	0	0	0	1
14	1	1	1	0	1	1	0	1	0	0	1	1
15	1	1	1	1	1	1	1	0	0	0	0	1

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Function Simplification using k-map:

$T_1 = \Sigma(0,8)$

Q_1Q_3 \ Q_2Q_1	$\bar{Q}_2\bar{Q}_1$	$\bar{Q}_2Q_1$	Q_2Q_1	$Q_2\bar{Q}_1$
$\bar{Q}_1\bar{Q}_3$	1			
$\bar{Q}_1Q_3$				
Q_1Q_3				
$Q_1\bar{Q}_3$	1			

$T_1 = \bar{Q}_3\bar{Q}_2\bar{Q}_1$

$T_3 = \Sigma(0,4,8,12)$

Q_1Q_3 \ Q_2Q_1	$\bar{Q}_2\bar{Q}_1$	$\bar{Q}_2Q_1$	Q_2Q_1	$Q_2\bar{Q}_1$
$\bar{Q}_1\bar{Q}_3$	1			
$\bar{Q}_1Q_3$	1			
Q_1Q_3	1			
$Q_1\bar{Q}_3$	1			

$T_3 = \bar{Q}_2\bar{Q}_1$

$T_2 = \Sigma(0,2,4,6,8,10,12,14)$

Q_1Q_3 \ Q_2Q_1	$\bar{Q}_2\bar{Q}_1$	$\bar{Q}_2Q_1$	Q_2Q_1	$Q_2\bar{Q}_1$
$\bar{Q}_1\bar{Q}_3$	1			1
$\bar{Q}_1Q_3$	1			1
Q_1Q_3	1			1
$Q_1\bar{Q}_3$	1			1

$T_2 = \bar{Q}_1$

$T_1 = \Sigma(0,1,2,3,4,5,6,7,8,9,10,11,12,13,14,15)$

Q_1Q_3 \ Q_2Q_1	$\bar{Q}_2\bar{Q}_1$	$\bar{Q}_2Q_1$	Q_2Q_1	$Q_2\bar{Q}_1$
$\bar{Q}_1\bar{Q}_3$	1	1	1	1
$\bar{Q}_1Q_3$	1	1	1	1
Q_1Q_3	1	1	1	1
$Q_1\bar{Q}_3$	1	1	1	1

$T_1 = 1$

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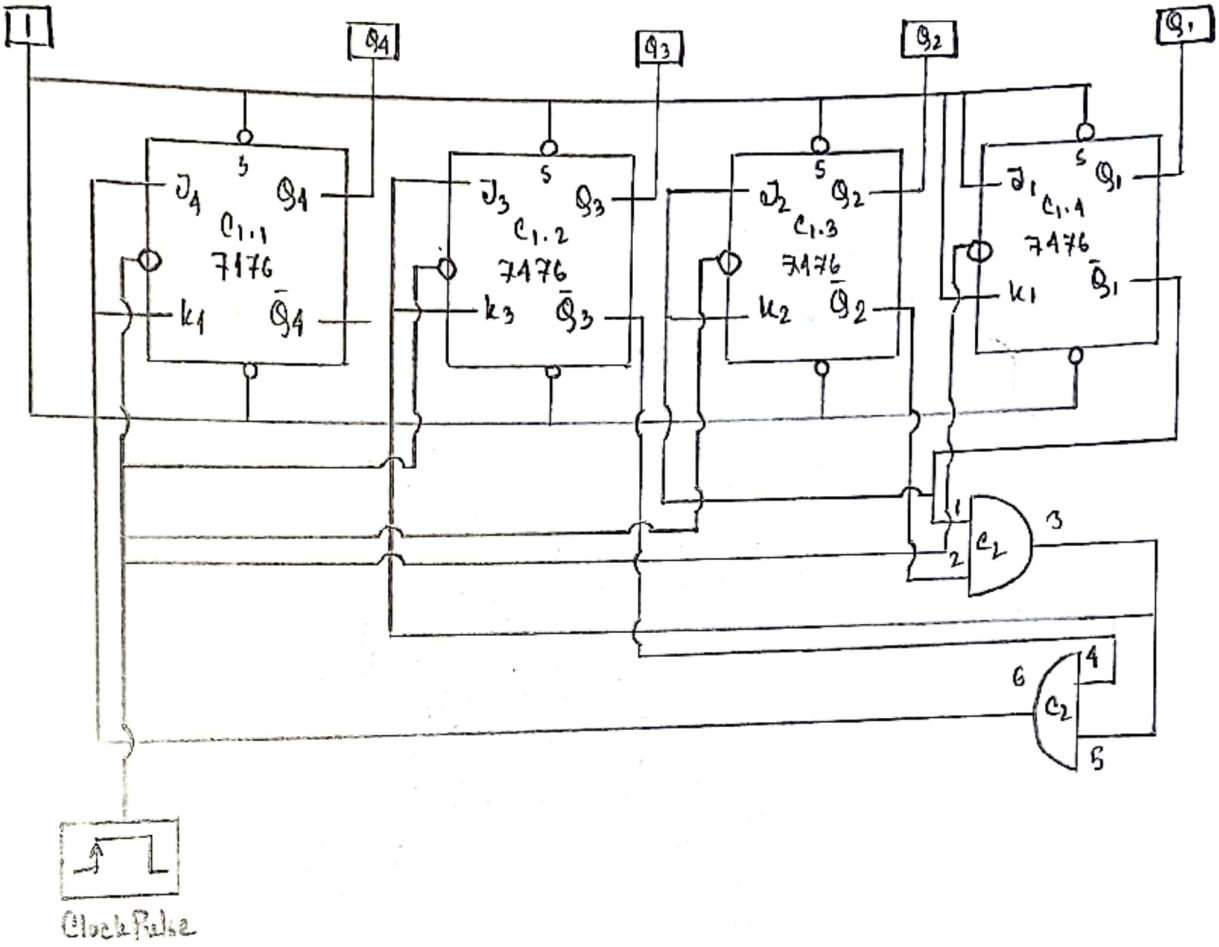
Circuit Diagram:



IC Requirement:

1. JKFF (7476) → 4 pieces
2. C_2 → AND Gate (74LS08) → 1 piece

Conclusion: In this experiment, we have constructed a circuit for 4 bit Synchronous down counter using T flip-flop. Synchronous means its clock pulse never depends on the output values. We need to input position level clock value and thus the four JK flip-flop works at a same time for this experiment.

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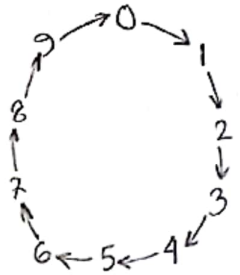
Experiment Name: (c) Design a BCD Ripple up counter using D flip-flop.

Objective: Our objective is to design a BCD Ripple up counter using a D flip-flop. This counter is designed to count ten digits, (0 - 9). It counts for every new clock input.

State Diagram:



State Table:

Present State	Next State
0	1
1	2
2	3
3	4
4	5
5	6
6	7
7	8
8	9
9	0

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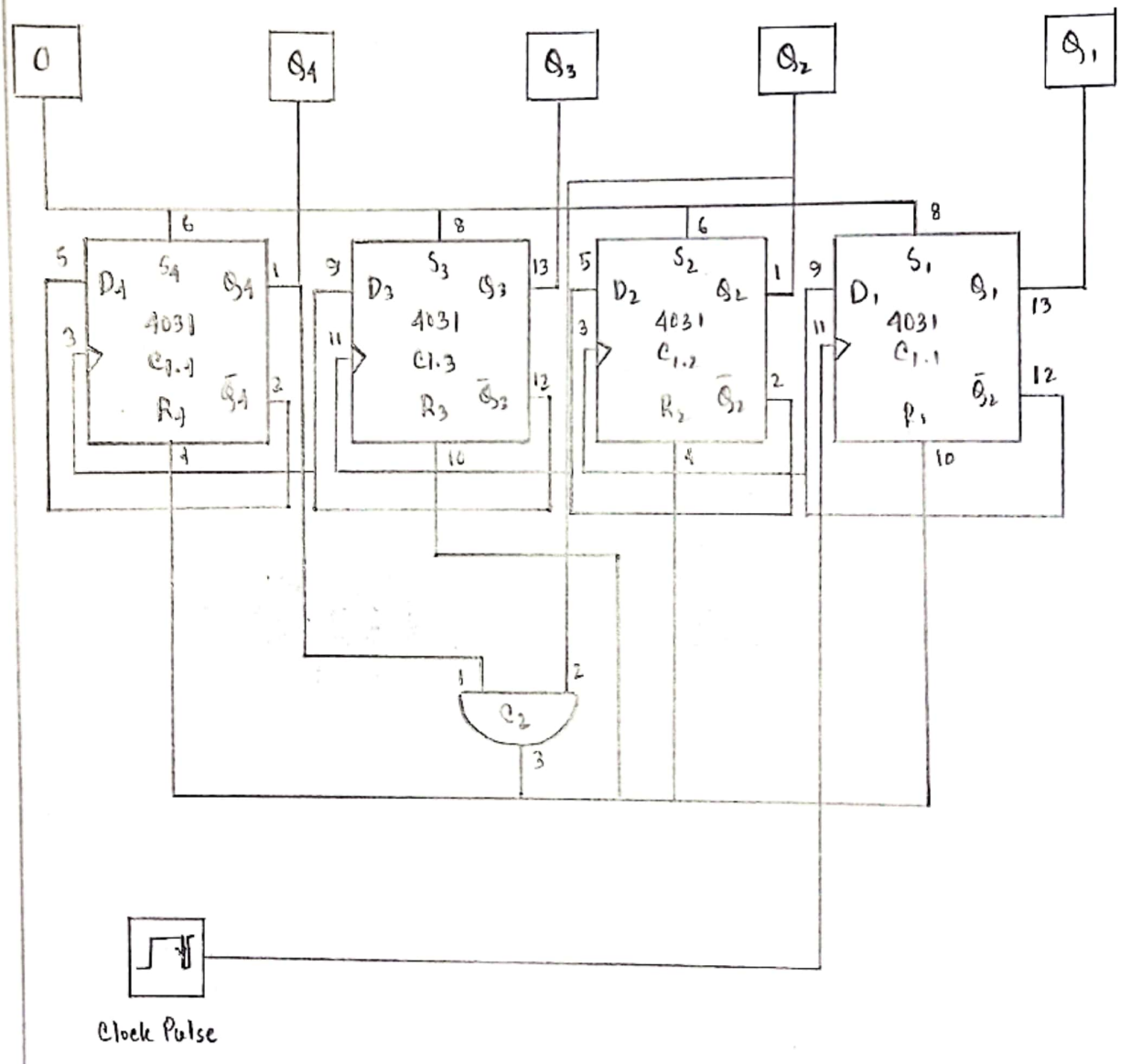
Number of flip-flop: In the sequence, the maximum value is 9. So, the number of flip-flop = $\lceil \log_2 9 \rceil = 4$

D-flip flop Excitation Table:

Q_n	Q_{n+1}	D
0	0	0
0	1	1
1	0	0
1	1	1

Circuit Diagram:



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IC Requirements:

1. C_1 → 4013 (D-Flip Flop) - 4 pieces
2. C_2 → 74LS08 (AND Gate) - 1 piece

Conclusion: We have constructed a BCD ripple up counter using D-flipflop. Here, the connection were given properly and required output was found.