

### Department of Computer Science & Engineering

Course No

: CSE 2106

Course Title

: Digital Logic Design Sessional

Experiment No

: 06

**Experiment Name** 

: a) Design a combinational logic circuit to convert the code Excess-1 to 2421 code

b) Design a combinational circuit which will show active

segment for 0,1,2,3,5,7,8,9 (decimal)

e) Design a combinational circuit to convert 5-bit BeD to binary equivalent: 17.01.22

Date of Submission

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: A

Experiment Name: Design a combinational logic circuit which will show the active segment for 0,1,2,3,5,7,8,9 (decimal)

Objective: A seven segment display device is capable to display both alphabets and decimal digit. In this experiment, a combinational circuit is needed to be designed for the decimal digit of 235 789. Here don't cares are (4,6,10,11,12,13,14,15)

### Truth Table:

Decimal		$I_{np}$	ut				0	utput			
Value	Α	В	C	D	a	Ь	e	9	2	£.	g
0	0	0	0	0	1	1	1	1	1	1	0
1	Ö	0	0	1	0	1	1	0	0	0	0
2	0	0	1	0	1	1	0	1	1	0	1
3	O	0	١	1	1	1	1	1	0	0	1
4	0	1	0	0	×	×	×	X	*	X	X
5	O	i	0	1	1	D	1	1	0	1	i
6	0	I	ı	0	X	X	×	X	×	×	X
7	O	1	ŀ	1	1	1	1	0	٥	D	6
8	1	0	0	0	1	)	١	ī	1	1	1
9	1	0	0	1	1	1	1	1	Ď	ı	1
16	I	0	t	0	X	X	×	×	X	*	X
l)	1	0	l	1	X	X	X	×	×	×	×
12	, 1	l	0	0	×	X	X	*	X	X	X
13	1	١	O	1	X	X	×	X	×	×	×
14	1	1	l <sub>i</sub>	O	X	X	X	×	*	×	×
15	I	1	1	1	X	X	×	×	*	X	×

Forca:  $\alpha = \Sigma(0,2,3,5,7,8,9)$   $\partial = \Sigma(4,6,10,11,12,13,14,15)$ 

k-map:

ABCD	ĒŌ	ČD	CD	cō
ĀĞ	1	٥	T	TT
ØĀ	X	١	١	X
AB	×	Х	×	X
ΑĒ	1	1	×	×

Using k-map, the simplified expression is a=A+B+C+D

For b: b= \(\Sigma(1,2,3,7,8,9)\) \(\partial = \Sigma(4,6,10,11,12,13,14,15)\)

k-map:

·				,
ABCD	ŌŌ	ēО	CD	σ <u>p</u>
ĀÃ	1	1		
ĀB	X	0	١	X
AB	X	Х	×	X
AĒ	1	١	×	×

The simplified expression is, b= B+C

For e: e = \(\Sigma(0,1,3,5,\frac{1}{2},8,9)\) \(\partial = \Sigma(4,6,10,11,12,13,14,15)\)

k-map:

AB	ēõ	ēD	CD	٥Đ,
ĀĒ	1	1	١	0
ĀB	Х	6	1	×
ВA	X	X	X	X
AĒ	1	1	X	×

The simplified expression is, c = c + D

For d: d= \( \int (0,2,3,5,8,9) \) D = \( \Sigma(4.6,10,11,12,13,14,15) \)

A	ep s	ēō	-	ē٥		CO	СŌ	
A	ē	,		0	,	ı	ι	
Ī	B	×		١		0	×	
F	મછ	×		×		X	X	1
	76	1		1		×	×	
_		_					_	

The simplified expression is, d=A+D+Bc+Bc=A+D+(BBc)

Force: e = Σ(0,2,8) D = Σ(4,6,10,11,12,13,14,15)

ABCD	сī	ĒD.	GD	cō
āĀ	1	0	0	1
ĀB	Х	0	D	×
AB	X	X	X	X
AB	1	D	Х	X

The simplified expression is , e = D

For  $f: f = \Sigma(0,5,8,9)$   $D = \Sigma(4,6,10,11,12,13,14,15)$ 

ABUD	ēō	ēD	GD	āg
ĀĒ	1	0	٥	0
ĀB	×		0	X
AB	×	×	X	メ
ΒĒΑ		1	×	×

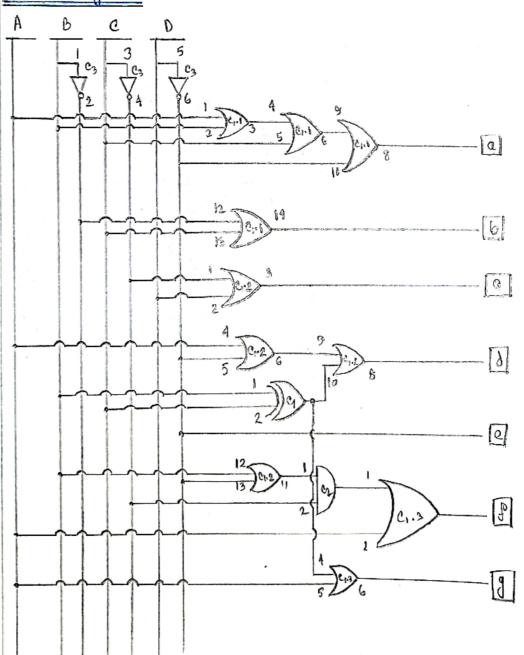
The simplified exprassion is,  $f = A + B\bar{C} + \bar{C}\bar{D} = A + \bar{C}(B + \bar{D})$ [Distribution Law]

Forc 9: 9 = \(\Sigma(2,3,5,8,9)\) D = \(\Sigma(4,6,10,11,13,12,14,15)\)

AB	ēō	ēD	CD	cō
ĀĒ	0	0	1	١
ÃB	X	I	0	X
AB	X	x	X	*
AG	1	1	X	X

The simplified exprassion g= A+BC+BE = A+(BAC)

### Circuit Diagram:



### Il Requirements:

1.C1 -> 74LS32 (OR Grate) - 3 pieces

2.C2 -> 74LSO8 (AND Grate) - 1 piece

3. C3 > 74LSO4 (NOT Grate) - 1 piece

1. CA → 71LS86 (x-OR Grate) - 1 piece

Conclusion: In this experiment, we have excepted a seven segment display derice. We also designed a combinational circuit which shows the active segments for 0,1,2,3,5,7,8,9. With k-map we have got the simplified expression and circuit diagrams are drawn accordingly.

Experiment Name: Design a combinational logic circuit to convert the code Excess - 4 to 2,4,2,1 code

Objective: 2.4,2,1 code is a complementary binary-coded decimal (BCD) code · Excess-4 codes are unweighted codes which are obtained by adding 4 to each decimal digit. In this experiment we are going to convert Excess-4 to 2421 rode. Using k-map, we will get the simplified expression.

### Truth Table:

Decimal		Inpu	+		Out	12 4	,2,1 co	Ja )
Value	A	B	C	D		-	1	
0	0	+			w	ス	J	2
1	-	0	0	0	X	X	×	<b>×</b>
	0	0	O	1	×	×	X	×
2	0	0	}	0	X	X	×	×
3	0	0	1	1	X	X	×	*
4	0	1	0	0	0	0	0	0
5	0	J	0	1	0	0	0	1
6	O	1	1	0	0	0	1	6
7	0	1	l	1	0	D	1	1
8	ı	0	Ö	D	0	1	0	0
9	1	0	D	I	0	1	0	1
lo	1	0	1	0	0	1	1	0
11	}	0	1	1	б	. 1	1	}
12	ì	1	0	0	1	1	1	0
13	3	1	Ď	I	1	1	1	1
14	1	1	J	0	Х	×	X	×
15	1	1	ı	1	×	×	×	*

## Function Simplification:

For w: W = \(\Sigma(12,13)\) d = \(\Sigma(0,1,2,3,14,15)\)

k-map:

	,		
ēĎ	ēD	СD	сō
X	×	×	×
1	1	×	×
			X X X

The simplified expression is, w = AB

k-map:

	_	,		
AB	٥Ď	g D	GD	СĎ
ĀB	X	×	×	*
ĀВ				
AB	1	١	Х	X
ΑĒ	1	ı	1	ı

The simplified expression is, x = A

For y: y = \( \( \xi, \xi, \10, 11, 12, 13 \) \( \delta = \S(0, 1, 2, 3, 14, 15 \)

k-map:

AB CD	ēĎ	ē٥	cD	сō
ÂĒ	×	X	×	X
ĀΒ			١	1
AB	1	1	×	×
ĀĀ			1	1

The simplified expression is, y = AB+e

k-map:

AB	ēĎ	ēр	co	e ō
ÂĒ	X	×	×	×
ÃВ		1	1	
AB		1	X	
AÃ		1	t	

The simplified expression is, 2 = D

Circuit Diagram: W = AB X = A Y = AB + C Z = D Z = D Z = D Z = D Z = D Z = D Z = D Z = D Z = D Z = D Z = D Z = D

#### IC Requirements:

Conclusion: In this experiment, we have designed a combinational logic circuit to convert Excess-4 to 2421 code. With truth table and k-map we got the minimized expression and we implemented the expression with proper IC requirements.

Experiment Name: Design a combinational logic circuit to convert the 5-bit BCD to Binary Equivalent

Objective: Bed is a class of binary encoding of decimal number. The binarcy number is a number express in the binarcy numerical system or base - 2 numerical system which prepresents numeric values using two different symbols typically 0 and 1. The objective is to design a combinational logic circuit to convert the 5 bit Bed to binarcy equivalent.

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Truth	Table:

muth lak	ole;									
Decimal		Inpu	+ (Be	Output (Binarcy)						
Value	A	B	C	D	E	F <sub>5</sub>	F4	F <sub>3</sub>	F <sub>2</sub>	Fi
0	0	0	0	0	0	0	0	0	0	10
1 .	0	0	0	0	1	10	0		0	+-
2	0	0	0	1	0	0	0	0	1	0
3	0	0	0	1	1	0	0			1
4	0	0	1	0	0	10	0	0	0	0
5	0	0	1	0	1	10	-		0	1
6	0	0	1	1	0	0	0	Mary laws for the second section 1		0
7	0	0	1		1	0	0	1		1
8	.0	1	0	0	0	0	ì	1	1	0
9	0	1	0	0	1	0	Andrew or commenters in the	0.	0	
lo	0	1	0		D	-	2	0	X	X
11	0	ASSESSED AND ADDRESS OF THE PARTY OF THE PAR	0	PERCENT AND A STATE OF THE PARCE OF THE PARC	matter principle of the property	×	×	×	and the second second second	- Commence of the Commence of
12	0	1	1		1	×	×	Х	×	*
13	0	1	1.	0	0	X	X	Х	×	×
14	0	1	1	1	1	X	Х	X	X	×
15	0	-		The second of the second of the second	0	Х	Х	Х	X	X
		-	1			X	X	×	×	×
16	1	0	D	0	0	0	1	ð	Salah Sa	0
17	1	0	0	0	1	0	1	0	1	1
18	1	0	0		b	0	i	1	b	0
19	1	0	0		1	0	1	1	0	1
2.0	1	0	1	0	0	0	1	Ţ	1	D
21	1	0	1	0	l	0	1	1	١	1
22	)	0	1	, Ł	6	1	O	0	Ů	6
23	ľ	0	1	I	1	1	b	0	Ď	1
24	1	1	O	0	Ó	1	D	0	1	Ô
25	1	1	0	٥		3	U	0	1	1
26	1	1	0	-	Q	X	χ	X	X	×
27	1	1	0	1	I	X	X	×	×	×
28	1	1	1	б	0	×	×	Χ	X	X
29	1	!	1	0	l 6	×	X	*	×	Х
3 o 31	1	1	1	L L		×	×	X	X	×

# Function Simplification:

For  $F_5 = \Sigma(22,23,24,25)$   $\delta = \Sigma(10,11,12,13,14,15,26,27,28,29,30,31)$ 

CUE								
AB	ODE	<u>GDE</u>	CDE	COE	CDE	CDE	CDE	CŌĒ
ĀĒ								
ĀB			. v					×
				×	×	×	×	
AB	1	١	×	Х	×	×	×	×
AĒ					1	1		
				1				

The simplified expression is F5 = AB+ACD = A(B+CD)[Distributive Law]

Fore F4 = \(\Sigma(8,9,16,17,18,19,20,21)\) d=\(\Sigma(10,11,12,13,14,15,26,27,28,29,30,31)\)

1	-							and the second second second second
AB CDE	ĒŌĒ	ÜĒ	ರ್ಷ	<u> Ĉ</u> DĒ	<u>edē</u>	ODE	യ്ട	CŌĒ
ĀĀ								
ĀB	1	ì	×	×	×	Х	×	×
AB			X	×	×	×	Х	X
Аб	I	1	1	1			ì	1

The simplified expression is F4= AB+ABC+ABD = AB+AB(c+D)

Forc F3: \(\Sigma(4,5,6,7,18,19,20,21)\) \(\delta = \Sigma(10,11,12,13,14,15,26,27,28,29,30,31)\)

AB	CDĒ	€0E	CDE	CDĒ	COĒ	CDE	ଲୁହ	CDE	
ÂÐ		~			1	1	1		]
ĀB			X	×	X	Х	Х	Х	
AB			X	X	Х	X	×	×	
AG			1	1		and the second	1	1	

The simplified expression is F3 = AOD+ AC+CD

2 A C D + C ( A + D ) [ Distributive Law]

For F2: F2 = \(\Sigma(2,3,6,7,16,17,20,21,24,25)\) \(\delta = \Sigma(10,11,12,13,14,15,26,27,28,29,30,31)\)

200								
AB CDE	CDE	₫ŌE.	ODE	CDE	CDĒ	CDE	CDE	eĎĒ
ĀĒ			I	i	1	1		
ÃB			X	×	×	X		
AB	1	1	×	×	×	*	X	×
AĒ	1	1					1	<u> </u>

The simplified expression is, F2 = AD + AD = ADD

For F1: F1 = \(\Sigma(1,3,5,7,9,17,19,21,23,25)\)

d= Σ(10,11,12,13,14,15,26,27,28,29,30,31)

AB	CDE	- CÔE	<u>ē</u> DE	<b>E</b> DĒ	ωĒ	CDE	CŌE	ŒĒ
ĀĒ		1	ı			1	1	
ÃB		١	Х	×	×	×	Х	X
AB		١	Х	×	×	×	*	×
AĞ		1	1			1	1	un approximate conservation of the last

The Simplified expression is Fi=E

### Circuit Diagram:

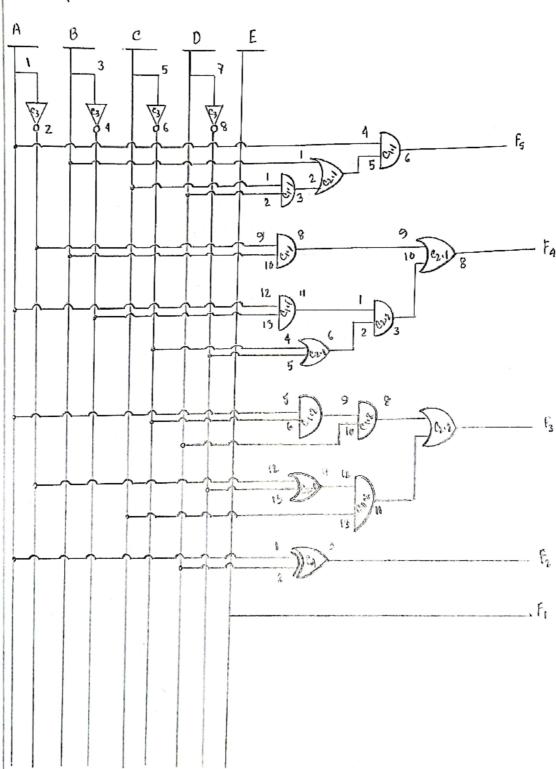
F5 = A (B+CD)

F4 = AB + AB ( c + D)

f3 = ACD+ Q (A+D)

F2 = A +D

 $F_1 = E$ 



### Ic Requirements:

- 1) C1 74 LSO8 (AND Grate) 2 pieces
- 2) C2 741532 (OR Grate) -2 pieces
- 3) (3 74L504 (NOT Grate) 1 piece
- 4) C4 74LS86 (XOA Grate) 1 piece

Conclusion: In the experiment, we have designed combinational logic circuit to convert 5 bit BeD to Binary Equivalent. Here 10 to 15 and 26 to 31 are don't carce. We have implemented the circuit with proper IC connections.