

Department of Computer Science & Engineering

CourseNo : CSE2106

Course Title : Digital Logic Design Sessional

Experiment No : 05

Experiment Name a)Design a switch(s) controlled Even/Odd parity checker circuit for 4 bit data if S=0 then Even parity if S=1 then Odd parity
 b)Design a Excess-4 to BCD Converter Circuit
 c)Design a switch(s) controlled 4 bit Binary to Gray & Gray to Binary code conversion circuit

circuit if S=0 then Gray to Binary Code if S=1 then Binary to Gray Code

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Section : A Experiment Name: Design a switch(s) controlled even/odd Parcity. Checker circuit for 4-bit Data. It s=0, then Even parcity.

If s=1 then odd parcity.

Objective: To make a number of 1's either old on even, a extrea bit is included with a binary message which is called pareity bit. The necesiver checks even/old pareity as a nesult of the calculation of the number of 1's in the message bit. If the number is even, F gets the value 1 & if the number is old, the F gets 0. At old pareity, F gets 1 when the number of 1's is old and 0 when the number of 1's is old and 0 when the number of 1's is even. Our objective is to check a switch controlled even/old pareity circuit for 4 bit.

Truth Table:

	Input	ß	C	D	Output F					
5	A 0	0	0	0	1					
0	0	0	0	ı	0					
0	0	0	1	6	0					
0	0	0	1	-	1					
0	0	1	O	0	0					
0	0		0	I	1					
0	0			0						
0	0	I	1	1	0					
0	1	0	O	D	Ó					
0	1	0	6	1	1					
0	1	0	1	0	١					
0	1	0		1	0					
0	1	and the state of t	0	0	1					
0			Ô		0					
0	1		Autorius mais martinosauro recurrente se o ribbera	0	0					
0	The T	person conditions with the Miles 74, in		1						
1	0	0	O	O						
1	O	0	٥	1	1					
1	0	0	1	ð	l					
1	0	0	1		G and a second contract of the second contrac					
1	0	t	0	٥	1					
1	0	1	0		٥					
1	0	1	f	O	0					
1	Ó	ŀ	1							
1		0	0	0	1					
1	1	O	0	1	0					
ľ		Ó	1	O	0					
}	1	0	1	1	1					
1	1	1	0	0	6					
1	ı	1	0	1						
23 F	!	<u>\</u>	1	0	0					

Herce F, = \(\Sigma(0,3,5,6,9,10,12,15,17,18,20,23,24,27,29,30)\)

K-map:

=						1		T	0 - 5
	SABED	ВēБ	Бèр	всD	BCD.	Beō	Bed	BED	BEŌ
		-		757		N			
	ŝĀ			l UI_		<u> </u>			+-1
	2.0		П		1		(I)		Ш
	ŝA				<u> </u>				
		ГП		Ī					
	SA	Ш							177
1			111				Π	1	
	SÃ						_		
- 1									

F= SABCD + SABCD

= SAB (cō+cD)+SAB(cD+cō)+SAB(cD+cō)+SAB(cD+cō)
+ SAB(cō+cō)+SAB(cō+cō)+SAB(cD+cō)

[Distributive Law]

= SAB(COD) + SAB(COD)

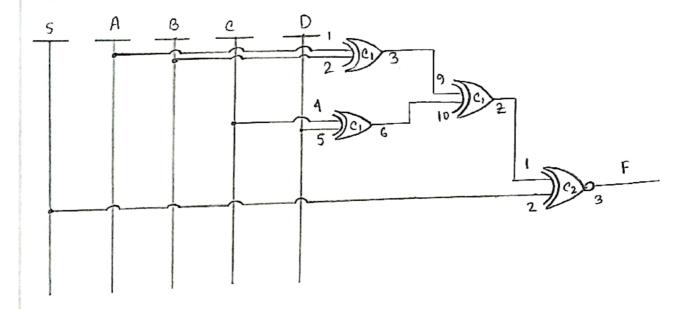
=\$ (ABB)(CBD)+\$(ABB)(CBD)+\$(ABB)(CBD)+\$(ABB)(Distributive)

= 3 ((ABB) & (CDD)) + S((ABB) & (CDD)) [Definition of X-OR, X-NOR]

= 5 0 ((A 0B) 0 (COD)) [Definition of X-NOR]

Using k-map the simplified expression is, F = S + ((A + B) + (C + D))

Circuit Diagram:



IC Requirements:

- 1. C1 741586 (x- OR Grate) 1 piece
- 2. (2 7415266 (x-NOR Grate) 1 piece

Conclusion: In this experiment, we have learnt that it is a 4-bit switch controlled odd and even parcity and we can check fore both odd and even parcity. From the truth table and the k-map we have obtained the simplified expression which we implemented in the circuit with proper IC nequirements.

Experciment Name: Design a excess - 4 to BeD converter circuit Objective: Beo is the abbreibiation of Binarry Coded Decimal and Excess-4 codes are unweighted codes which are obtained by adding 1 to each decimal digit and can be reprosented by binarcy reprosentation. In this experciment, we are going to design a circuit of Excess-4 to BCD and using k-map to obtain simplified expression.

Treuth Table:

						Be	-D	
Decimal		Excess		T 5	w	×	K	2
Value	A	В	C	D		-	X	×
٥	0	0	0	Ó	X	×		
	0	0	D	1	X	X	X	×
2	0	0	1	0	×	X	X	×
3	0	0		l	×	×	X	×
4	0	1	0	0	0	٥	٥	٥
5	0	1	0	-	0	0	0	1
6	0	1	And the second s	0	Ö	0	1	0
7	0	1	[T.	0	0	l.	. 1
8	1	0	0	0	0	l	0	Ö
9	1	0	O	t	0	1	O	l
<u>}</u> 0		0		0	Ö	ſ	١	b
11	1	0	1	ı	0	and the second s	1	1
12	1	1	0	D	1	O	0	0
13	1	1	Ó	1	1	Ø	0	l
14	1	1		0	X	×	×	×
15	1	1	1	1	×	×	×	X

Function Evaluation:

For $\omega = \Sigma(12,13)$ $\delta = \Sigma(0,1,2,3,14,15)$

k-map:

ABCD	ēō	ēD	CD	cō
ĀĒ	×	×	×	X
ĀB				
AB	1	1	×	×
AĒ				

Using k-map, the simplified function is w = ABFor x, $x = \sum (8,9,10,11) d = \sum (0,1,2,3,14,15)$

k-map:

AB CD	ēō	ćD	CD	c <u>o</u>
ĀĒ	×	X	×	×
ĀВ				
AB			×	×
AĞ	I	١	1	\

Using k-map, the simplified function is $x = \tilde{B}$ For y, $y = \Sigma(6, \chi, 10, 11)$ $d = \Sigma(0, 1, 2, 3, 14, 15)$

h-map:

AB	ēĎ	ēО	cD	cō
ĀB	×	×	×	×
ĀB			1	1
AB			X	×
ВÃ			1	1

Using k-map, the simplified function is y = c

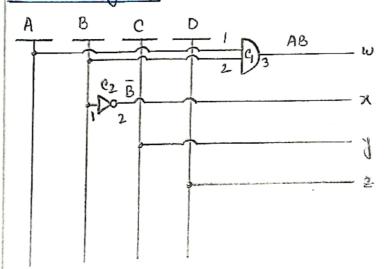
For
$$2, 2 = \sum (5,7,9,11,13)$$
 $\delta = \sum (0,1,2,3,14,15)$

k-map:

AGCD	ĕĎ	čρ	CO	حة
ĀĒ	×	×	×	*
Āß		1	ı	
AB		1	×	×
AĒ		1	1	

Using k-map the simplified function is, 2 = D

Cincuit Diagram:



IC Requirements:

- i) c, → 74LSO8 (AND Grate) 1 piece
- ii) c2-> 74 LSO 4 (NOT Grate) 1 piece

Conclusion: In this experiment, we have learned the convertion of Excess-4 to BCD where (0-3) and (14-15) were don't cares. From the truth table and k-map we have got the minimized expression and implemented it on the circuit with proper IC requirements.

Experciment Name: Design a switch controlled 4-bit bimary to Greay and Greay to bimarcy code conversion circuit.

If s=0 then Ginay to Binary Code
If s=1 then Binary to Gircay Code

Objective: Binarcy code is a group of binarcy bits which are used to storce, nepresent and transmit data is called binarcy code. On the other hand, Guray code is a non-weighted code. The successive greay code differe in one bit positions. The objective is to design a switch controlled binarcy to Greay and Greay to binarcy convertere.

Trouth Table:

Heach					0.1)				
		Input				Outpu	and the same of th	1 2	
5	A	B	C	D	ω	*	<u></u> <u> </u>	0	
0	0	0	0	0	0	0	0		
0	0	0	0	1	Ô	0	0	1	
0	0	0	1	0	0	0	(0	
0	0	0		l	0	0	1		
0	0	1	0	0	0	1	b	0	
0	0	1	0	1	0	1	0		
0	0	1	1	0	0	1	1	0	
0	0	1	1	1	0	. 1	ţ		
0	1	0	0	0	1	0	0	6	
0	1	0	0	1	t	0	0		
0	-	0	i	٥	1	0	l	0	
	1	0	1		1	0	1		
0		1	0	0	1)	0	0	
0	1	1	0		1	1	0		
				0	1	1	1	6	
0	1	1	1	1	1	1	1		
0	1	1	0	0	Ô	D	0	٥	
1	Ů	0	The second secon	Ĭ	O	0	0	1	
1	0	0	0		0	0	1	ľ	
1	0	0	1	0	0	0	1	O	
1	0	0		0	O	1	01	0	
1	0	1	0	1	0	1	1		
1	0		1	0	6	1	0	(
1	0			1	0		0	O	
1	0	1	1	O		OI.	0	0	
1	1	0	0		1		0		
1	1	0	0	J	1	1	1		
-		0		0	1		1	0	
1	1	1	0	0	1	0	.,	0	
-			0	1	1	0	1	1	
1	1	1		0	1	0	0		
-,-	1	1	1	1		0	0	0	
			'	'	1	· ·		V	

Herce, w= \(\Sigma(8,9,10,11,12,13,14,15,24,25,26,27,28,29,30,31)\)

k-map:

-							T	T	1
	SA BCD	5 ē ō	Бcр	BeD	Beō	BCD	BCD	BED	BCD
	ŠĀ	0	0	0	O	0	٥	0	0
	54					1	1	1	1
	ŠΑ	, 1	1	(1	'			
			1	1	1	1	1	1	
	SA	L'	<u> </u>						0
	• -		^	0	0	0	0	0	
	SĀ	U	0						

Using k-map, simplified expression is, w= A

Herce, x = \(\Sigma(4,5,6,7,8,9,10,11,20,21,22,23,24,25,26,27)\)

٠														
	SABED	BeD	BCD	BCD	ট্রত	Beō	BCD	BCD	BCD					
	šĀ	0	0	0	0	1	١	l	1					
		,					^	^						
	ŠΑ	1	1	t	1 1	D	U	U						
			-		1	0	0	0	0					
	SA	1	,	1		U	Ü							
				Manager Manager and Control of the			-							
	CA	٥	0	0	0	1	1	ţ	'					
	077	_						Section of America de America of						

Using k-map, the simplified expression is, 2 = AB + AB = ABB

Herce, y = \(\Sigm(2,3,4,5,8,9,14,15,18,19,20,21,26,27,28,29)\)

			T				050	2-2
SABCD	BeD	1	i	Ben	BCD	Ren	BCD	BCD
ĪĀ	0	0	1	1	0	0	1	
SA.	1	1	0	0	3	1	٥	٥
AZ	0	6	1	1	0	0	1	I
SFI						0		
SÃ	0	0	1		U	J	4	-,

J= ABC+SBC+SABC+ABC +SBC +SABC

= SABC + SABC + SBC + SBC + ABC + ABC [Commutative Law]

```
=$A(BC+BC)+S(BC+BC)+Ā(BC+BC)[Distributive Law]
=$A(BBC)+S(BBC)+Ā(BBC)[Definition of X-OR and X-NOR]
=$A(BBC)+(S+Ā)(BBC)[Distributive Law]
=$A(BBC)+($S+Ā)(BBC)[Double Negation]
=$A(BBC)+$\tilde{s}-\tilde{A}(BBC)[De Morgan's Law]
=$A(BBC)+$\tilde{s}-\tilde{A}(BBC)[Double Negation]
=$A(BBC)+$\tilde{s}-\tilde{A}(BBC)[Double Negation]
=$A(BBC)+$\tilde{s}-\tilde{A}(BBC)[Double Negation]
=$A(BBC)+$\tilde{s}-\tilde{A}(BBC)[Double Negation]
=$ABBC[Using k-map]
Now, 2 = \tilde{S}(1,2,4,7,8,11,13,14,17,18,21,22,25,26,29,30)
```

BOD	BED	ēēd	Bed	Ēcō	Beō	BCD	BED	B <u>c</u> p
ŠĀ	0	1	0		D		D	1
šΑ		0		0	[1]	0	economic Survivament Instrumental	O
SA	0	1	0	1		0		0
25			0		1	0	1	0
SA	0		The second secon				of the set of the second secon	

Z= SED+ SCD+ ABED+ABCD + ABED+ABCD + SABCD+ SABCD+

```
= (S + \overline{AB} + AB)(C \oplus D) + \overline{S}(\overline{AB} + A\overline{B})(\overline{C} \oplus \overline{D}) [Distributive Law]

= (S + \overline{A} \oplus B)(C \oplus D) + \overline{S}(A \oplus B)(C \oplus D) [Definition of x-or and]

= (S + \overline{A} \oplus B)(C \oplus D) + \overline{S}(A \oplus B)(\overline{C} \oplus D) [Complement Law]

= \overline{S} \cdot (\overline{A} \oplus \overline{B})(C \oplus D) + \overline{S}(A \oplus B)(\overline{C} \oplus D) [De-Moregan's Law]

= \overline{S} \cdot (\overline{A} \oplus B)(C \oplus D) + \overline{S}(A \oplus B)(\overline{C} \oplus D) [Double Negation]

= \overline{S} \cdot (\overline{A} \oplus B)(C \oplus D) [Definition of x-or]

2 = \overline{S}(A \oplus B) \oplus (C \oplus D) [Definition of x-or]
```

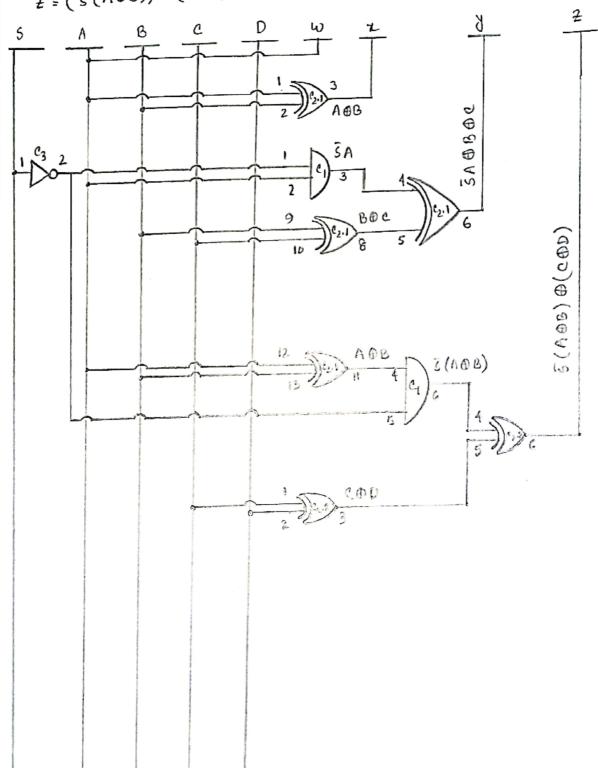
Cincuit Diagram:

 $\omega = A$

X = ABB

J=(\$A) BBBC

2 = (5(ABB)) +(C+D)



IC Requirements:

- 1. C1 -> 74LSO8 (AND Grate) 1 piece
- 2. C2 74LS86 (XOR Grate) -2 pieces
- 3. C3 -> 74LSO4 (NOT Grate) 1 piece

Conclusion: From the experiment, we have learent that it is a 4-bit switch controlled Binarcy to Gray and Gray to Binarcy code converter. if s = 0, then (0-15) will be converted into gray to binarcy, when s = 1 then (16-31) will be converted into binarcy to gray. And implemented the minimized expressions in the circuit.