Department of Computer Science & Engineering

Course No : **CSE 2106**
Course Title : **Digital Logic Design Sessional**

Experiment No : 07
Experiment Name : a. Design a Switch Controlled 4-Bit Adder/Subtractor Circuit (using Adder IC).
If S=0 it performs subtraction (only A>B)
If S=1 it performs addition
b. Design a BCD Adder Circuit
c. Design a BCD Subtractor Circuit (for both A>B and A<B)

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Experiment Name: Design a switch controlled 4 bit Adder/Substractor Circuit

If S=0 perform substraction (only A>B)

If S=1 perform addition

Objective: The operation of adding two binary numbers is one of the fundamental tasks performed by a digital computer. In 0+0=0, 0+1=1, 1+0=1 these operations each binary operation gives one bit sum, either 0 or 1 But fourth operation gives two bits. Lower significant and higher signification bit are accordingly bit and carry bit. The objective of this experiment is to design switch controlled 4-bit Adder/Subtractor circuit using adder IC.

Truth Table:

There are 2 binary number of 4 bit as input with a carry bit and switch as input also. So there would be too many combination. To avoid difficulties, there is shown some combinations. If the switch is 0, substraction will be performed and when switch is 1, addition will be performed.

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Switch	Input									Output				
	C_{in}	A_3	A_2	A_1	A_0	B_3	B_2	B_1	B_0	C_{out}	S_3	S_2	S_1	S_0
0	1	0	1	0	1	0	1	0	0	1	0	0	0	1
0	1	0	1	1	0	0	1	0	0	1	0	0	1	0
0	1	0	1	1	1	0	0	1	1	1	0	1	0	0
0	1	1	0	0	0	0	0	1	0	1	0	1	1	0
0	1	1	0	0	1	0	0	1	1	1	0	1	1	0

When $S = 0$, Substraction $(A > B)$ is performed

Switch	Input									Output				
	C_{in}	A_3	A_2	A_1	A_0	B_3	B_2	B_1	B_0	C_{out}	S_3	S_2	S_1	S_0
1	0	1	0	0	1	0	0	1	1	0	1	1	0	0
1	0	1	0	0	0	0	0	1	0	0	1	0	1	0
1	0	0	1	1	1	0	0	1	1	0	1	0	1	0
1	0	0	1	1	0	0	1	0	0	0	1	0	1	0
1	0	0	1	0	1	0	1	0	0	0	1	0	0	1

When $S = 1$ addition is performed

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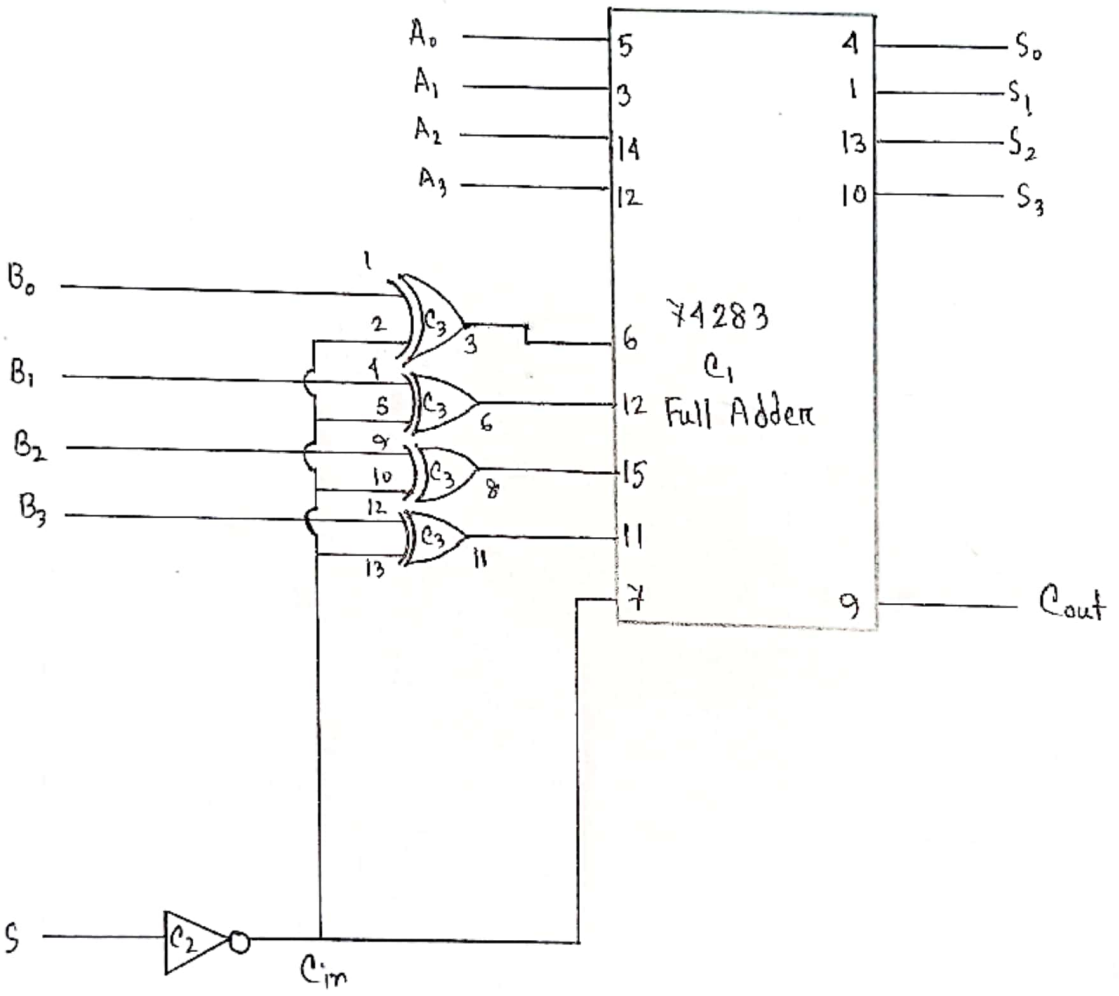
Circuit Diagram:



Here we have to perform Adder/Substraction Circuit. When Switch, S = 0 Substraction is performed only for the condition A > B

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Now, for example we take two inputs including 4 bit each,

A = 5 B = 4

A_3	A_2	A_1	A_0		B_3	B_2	B_1	B_0
0	1	0	1		0	1	0	0

In Substraction to get accurate output we have to change the input of using XOR gate and compliment of switch bit, $S' = (0)' = 1$ it also act as carry bit, $C_{in} = S' = 1$

$B_3 \oplus C_{in} = 0 \oplus 1 = 1$

$B_2 \oplus C_{in} = 1 \oplus 1 = 0$

$B_1 \oplus C_{in} = 0 \oplus 1 = 1$

$B_0 \oplus C_{in} = 0 \oplus 1 = 1$

New input of B is 1011

Here Substraction is performed By A+B+ C_{in} expression

$A_0 + B_0 + C_{in} = 1 + 1 + 1 = 1$ Carry 1

$A_1 + B_1 + C_{in} = 0 + 1 + 1 = 0$ Carry 1

$A_2 + B_2 + C_{in} = 1 + 0 + 1 = 0$ Carry 1

$A_3 + B_3 + C_{in} = 0 + 1 + 1 = 0$ Carry 1

Hence, the prefercable output of Substraction is got, which is 0001 and Carryout is 1

Now, when switch, S = 1 addition is performed

A=5 B=4

A_3	A_2	A_1	A_0		B_3	B_2	B_1	B_0
0	1	0	1		0	1	0	0

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In addition, to get proper output, we have to change the input of B using XOR gate and compliment of switch bit $S' = (1)' = 0$, it also act as Carrey in bit, $C_{in} = S'$

$B_3 \oplus C_{in} = 0 \oplus 0 = 0$

$B_2 \oplus C_{in} = 1 \oplus 0 = 1$

$B_1 \oplus C_{in} = 0 \oplus 0 = 0$

$B_0 \oplus C_{in} = 0 \oplus 0 = 0$

The new input of B will remain same as 0100

Now addition is performed like,

$A_0 + B_0 + C_{in} = 1 + 0 + 0 = 1$ Carrey 0

$A_1 + B_1 + C_{in} = 0 + 0 + 0 = 0$ Carrey 0

$A_2 + B_2 + C_{in} = 1 + 1 + 0 = 0$ Carrey 1

$A_3 + B_3 + C_{in} = 0 + 0 + 1 = 1$ Carrey 0

Thus, the desirable output of addition is got, 1001 and carrey out is zero (0).

IC Requirements :

1. C_1 - 74283 (Full Adder) - 1 piece
2. C_2 - 74LS04 (NOT Gate) - 1 piece
3. C_3 - 74LS86 (XOR Gate) - 1 piece

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Conclusion: In this experiment, we have designed a switch controlled 4 bit adder / substractor circuit. In order to implement this circuit we have used 4-bit Full adder and XOR and NOT gate each.

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Experiment Name: Design a BCD Adder Circuit

Objective: BCD stands for Binary Coded Decimal. Suppose we have two 4 bit numbers A and B along with the carry. The maximum value of output will be 19 (i.e 9+9+1 = 19). In this experiment, we have to derive output equations for designing a BCD Adder Circuits and implement the output in the circuit.

Truth Table: Even though many different combination of two 4 bits number can be taken but their binary sum will always be in between 0 to 19. So, the truth table are going to take the binary sum (0 to 19) as input.

Decimal Value	Binary Sum					BCD Sum				
	C'	S_3'	S_2'	S_1'	S_0'	C	S_3	S_2	S_1	S_0
0	0	0	0	0	0	0	0	0	0	0
1	0	0	0	0	1	0	0	0	0	1
2	0	0	0	1	0	0	0	0	1	0
3	0	0	0	1	1	0	0	0	1	1
4	0	0	1	0	0	0	0	1	0	0
5	0	0	1	0	1	0	0	1	0	1
6	0	0	1	1	0	0	0	1	1	0
7	0	0	1	1	1	0	0	1	1	1
8	0	1	0	0	0	0	1	0	0	0
9	0	1	0	0	1	0	1	0	0	1
10	0	1	0	1	0	1	0	0	0	0
11	0	1	0	1	1	1	0	0	0	1
12	0	1	1	0	0	1	0	0	1	0
13	0	1	1	0	1	1	0	0	1	1
14	0	1	1	1	0	1	0	1	0	0
15	0	1	1	1	1	1	0	1	0	1
16	1	0	0	0	0	1	0	1	1	0
17	1	0	0	0	1	1	0	1	1	1
18	1	0	0	1	0	1	1	0	0	0
19	1	0	0	1	1	1	1	0	0	1

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k-map:

Binary uncorrected sum input $\Sigma(10\text{-}19)$ for $\Sigma(10\text{-}15)$ the k-map.

$S_3'S_2'$ \ $S_1'S_0'$	$\bar{S}_1'\bar{S}_0$	$\bar{S}_1'S_0'$	$S_1'S_0'$	$S_1'\bar{S}_0'$
$\bar{S}_3'\bar{S}_2'$				
$\bar{S}_3'S_2'$				
$S_3'S_2'$	1	1	1	1 → $S_3'S_2'$
$S_3'\bar{S}_2$			1	1 → $S_3'S_1'$

$$\text{Sum} = S_3'S_2' + S_3'S_1' = S_3(S_2' + S_1') \quad \ldots\ldots (1)$$

If we add the carry with eqn (1) we get,

$$C' + S_3'(S_1' + S_2') \quad [\text{As } C' \text{ contains the input of } \Sigma 16\text{-}19]$$

the function is $F = C' + S_3'(S_1' + S_2')$

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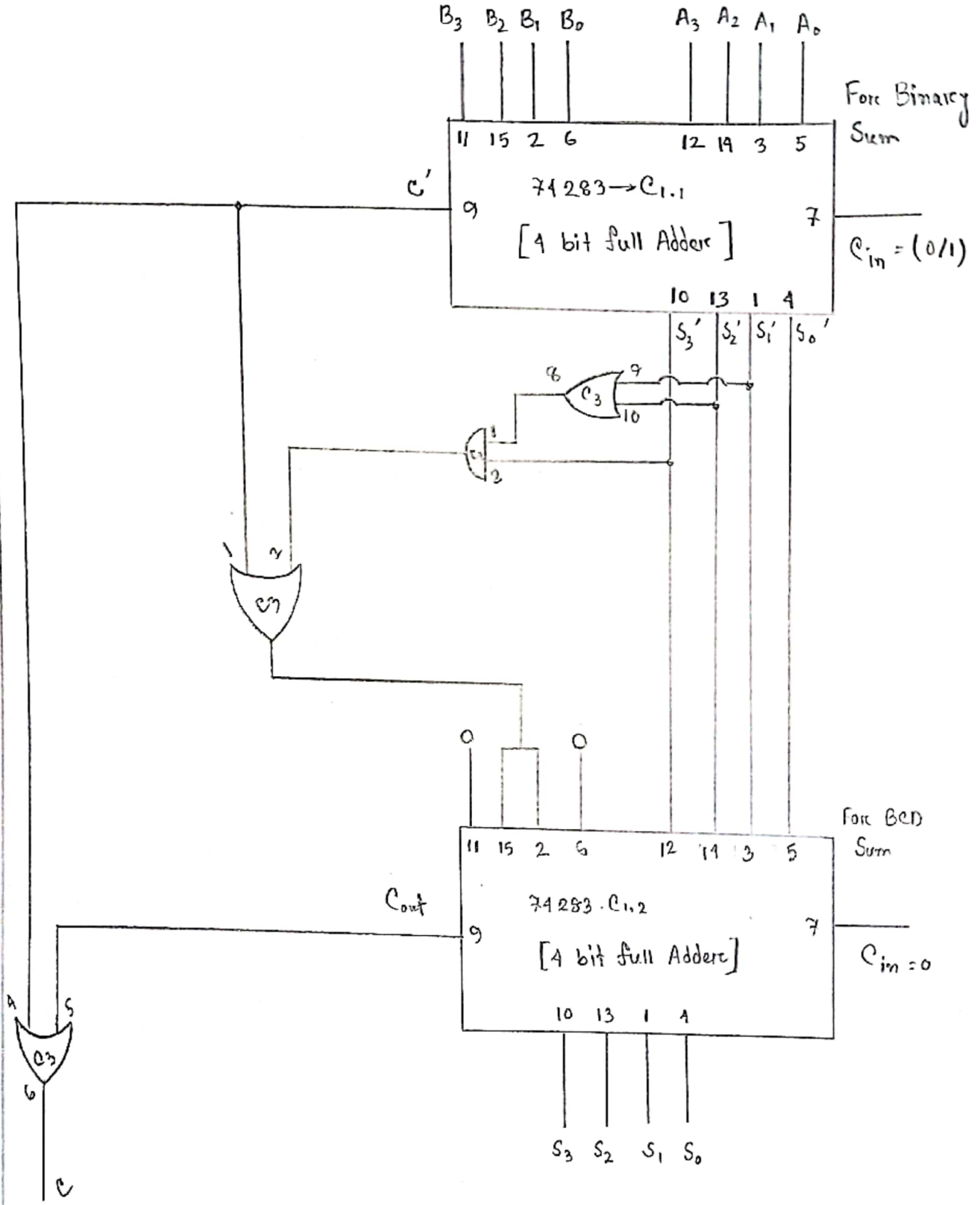
Circuit Diagram:



BCD Adder (using two 4 bit full Adders)

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Here we have to find BCD sum from the given Binary Sum. Since the input digit not exceeds 9, the output sum cannot be generated than 9+9+1 = 19. The 1 in sum being on input carry. When the binary sum is equal to or less than 1001, the corresponding BCD is identical and no conversion is necessary when the binary sum is generated more than 1001, the addition of binary 6 (0110) converts it into corrected BCD representation and also produces on output carry as required.

For Binary Sum not exceeding 9:

Sum = 9 ; A = 5 , B = 4

A_3	A_2	A_1	A_0		B_3	B_2	B_1	B_0		C_{in}
0	1	0	1		0	1	0	0		0

$A_0 + B_0 + C_{in} = 1 + 0 + 0 = 1$ Carry = 0

$A_1 + B_1 + C_{in} = 0 + 0 + 0 = 0$ Carry = 0

$A_2 + B_2 + C_{in} = 1 + 1 + 0 = 0$ Carry = 1

$A_3 + B_3 + C_{in} = 0 + 0 + 1 = 1$ Carry = 0

$C_{out} = 0$

Binary Sum = 1001

C_{out}	S_3'	S_2'	S_1'	S_0'
0	1	0	0	1

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We know, $F = C_{out} + S_3'(S_2' + S_1')$

$= 0 + 1\ (0+0)$

$= 0 + 1.0$

$= 0+0$

$= 0$

As F is 0; The input B portion of second adder becomes (0000) and the input A is as same as the output of first adder (1001)

A_3	A_2	A_1	A_0	B_3	B_2	B_1	B_0
1	0	0	1	0	0	0	0

$A_0 + B_0 + C_{in} = 1 + 0 + 0 = 1$ Carry = 0

$A_1 + B_1 + C_{in} = 0 + 0 + 0 = 0$ Carry = 0

$A_2 + B_2 + C_{in} = 0 + 0 + 0 = 0$ Carry = 0

$A_3 + B_3 + C_{in} = 1 + 0 + 0 = 1$ Carry = 0

C_{out}

∴ BCD sum = 1001

We get, Cout of Second Adder is 0

OR ing the Cout of first and second adder,

$0+0 = 0$

The final output is

Cout	S_3	S_2	S_1	S_0
0	1	0	0	1

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For Binary Sum Exceeding 9:

Sum = 10

A_3	A_2	A_1	A_0		B_3	B_2	B_1	B_0	C_{in}
0	1	0	1		0	1	0	1	0

$A_0 + B_0 + C_{in} = 1 + 1 + 0 = 0$ Carry = 1

$A_1 + B_1 + C_{in} = 0 + 0 + 1 = 1$ Carry = 0

$A_2 + B_2 + C_{in} = 1 + 1 + 0 = 0$ Carry = 1

$A_3 + B_3 + C_{in} = 0 + 0 + 1 = 1$ Carry = 0

$C_{out} = 0$

∴ BCD sum is 1001

We get, Cout of Second Adder is 0

ORing the Cout of first and second adder,

$0 + 0 = 0$

The final output is

C_{out}	S_3	S_2	S_1	S_0
0	1	0	0	1

For Binary Sum Exceeding 9:

Sum = 10

A_3	A_2	A_1	A_0		B_3	B_2	B_1	B_0	C_{in}
0	1	0	1		0	1	0	1	0

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$A_0 + B_0 + C_{in} = 1+1+0 = 0$ Carry = 1
$A_1 + B_1 + C_{in} = 0+0+1 = 1$ Carry = 0
$A_2 + B_2 + C_{in} = 1+1+0 = 0$ Carry = 1
$A_3 + B_3 + C_{in} = 0+0+1 = 1$ Carry = 0 → C_{out}

Binary Sum = 1010

Now,

S_3'	S_2'	S_1'	S_0'	C_{out}
1	0	1	0	0

We know,

S_3'	S_2'	S_1'	S_0'	C_{out}
1	0	1	0	0

We know, $F = S_3'(S_2' + S_1') + C_{out}$

$= 1(0+1)+0$

$= 1.1+0$

$= 1+0$

$= 1$

As the F is 1;

The input B of the second adder become (0 1 1 0) the input of A portion is as same as the output of 1st adder (1010)

A_3	A_2	A_1	A_0	B_3	B_2	B_1	B_0	C_{in}
1	0	1	0	0	1	1	0	0

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$A_0 + B_0 + C_{in} = 0 + 0 + 0 = 0$ Carrey = 0

$A_1 + B_1 + C_{in} = 1 + 1 + 0 = 0$ Carrey = 1

$A_2 + B_2 + C_{in} = 0 + 1 + 1 = 0$ Carrey = 1

$A_3 + B_3 + C_{in} = 1 + 0 + 1 = 0$ Carrey = 1 → C_{out}

BCD Sum

$\therefore$ BCD Sum = 0 0 0 0

We get, the C_{out} of 2nd adder is 1.

ORing the C_{out} of 1st and 2nd Adder 0+1 = 1

The final output is

C_{out}	S_3	S_2	S_1	S_0	
1	0	0	0	0	[16 in decimal]

IC Requirements:

1. C_1 → 74283 (4 bit full adder) - 2 piece
2. C_2 → 74LS08 (AND Gate) - 1 piece
3. C_3 → 74LS32 (OR Gate) - 1 piece

Conclusion: In this experiment, we designed a BCD adder circuit using two Full Adder IC and the help of AND gate, OR gate. Here, we needed two full adder IC as there are same bit difference in $\Sigma(10\text{-}19)$. Experiments are done with proper IC connection.

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Experiment Name: Design a BCD Substractor Circuit (For both A>B and A<B)

Objective: We have to construct a BCD substractor circuit. Here, the two input range must be 0-9. When the sign bit is '0', it means the result is positive and the result is negative when the bit is '1'. We will implement BCD substractor using full adder and basic gates NOT and XOR for both the condition A>B; B>A

Truth Table:

As input A and B are 4 bit numbers, so while doing subtraction there could be 10*10 = 100 possible combination in the input part. It will be very difficult to show their outputs. So to avoid this problem, few combinations are shown in the truth table. The Subtraction will be performed using 2's compliment. So, Cin will always be 1 high Cin's represent the carry input in first adder.

When A>B

Input									Output				
C_{in}'	A_3	A_2	A_1	A_0	B_3	B_2	B_1	B_0	C_{out}	D_3	D_2	D_1	D_0
1	0	1	0	0	0	0	0	1	0	0	0	1	1
1	0	0	1	0	0	0	0	0	0	0	0	1	0
1	0	1	1	0	0	1	0	1	0	0	0	0	1
1	1	0	0	1	1	0	0	0	0	0	0	0	1

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When B>A

Input									Output				
C_{in}	A_3	A_2	A_1	A_0	B_3	B_2	B_1	B_0	C_{out}	D_3	D_2	D_1	D_0
1	0	0	1	0	0	0	1	1	0	0	0	0	1
1	0	1	0	0	0	1	1	0	0	0	0	1	0
1	0	1	1	0	0	0	0	0	0	0	0	1	0
1	0	0	1	1	1	0	0	1	0	0	1	1	0

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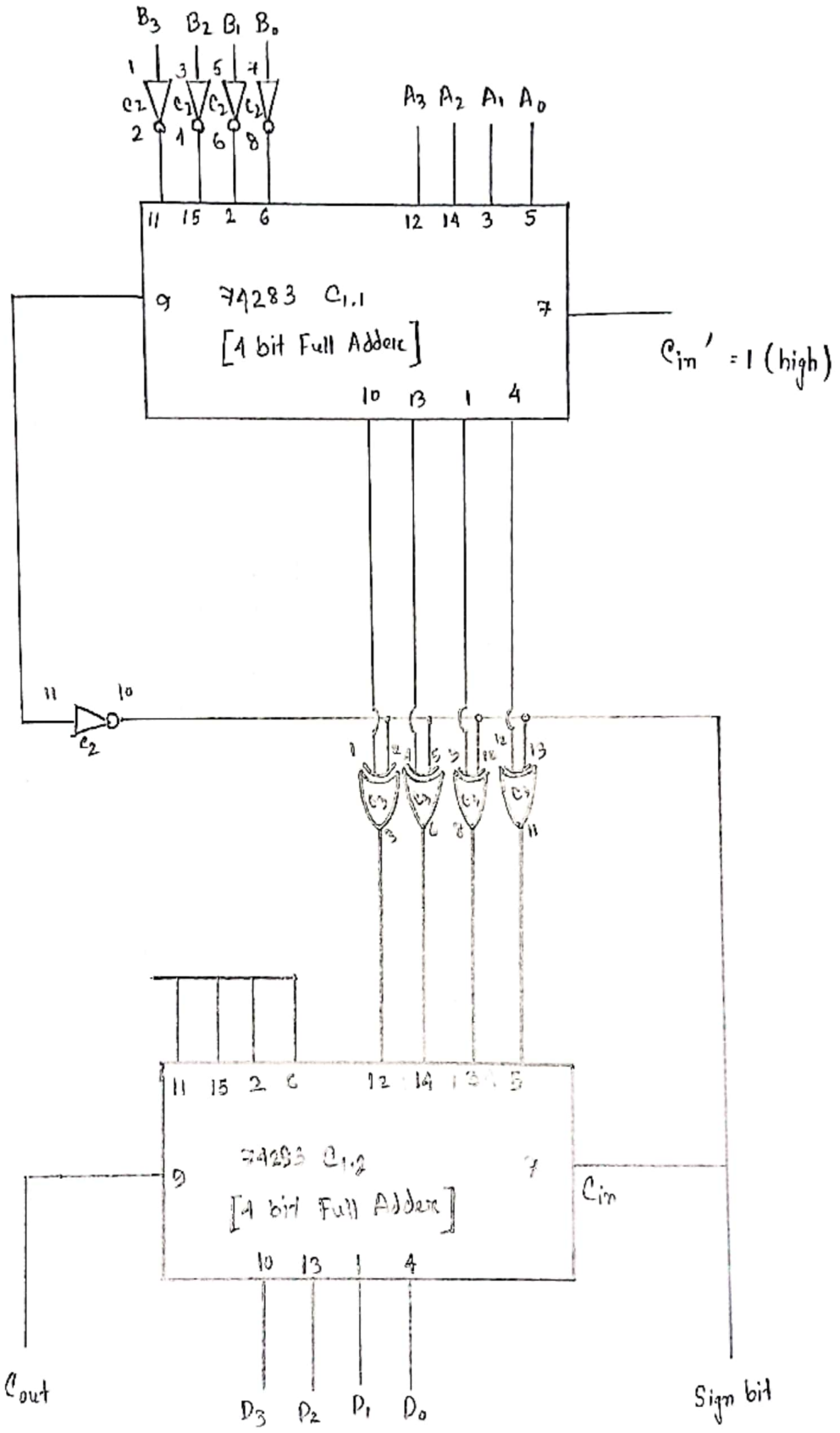
Circuit Diagram:



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Two get BCD Substraction for both conditions we have to use two 4 bit full adder circuit and input range must be 0-9. For A > B, suppose here two inputs A = 4 B = 1 when we do substraction in first adder circuit we followed $A + \bar{B} + C_{in}'$ expression where C_{in}' always be 1.

A_3	A_2	A_1	A_0		B_3	B_2	B_1	B_0
0	1	0	0		0	0	0	1

$A_0 + \bar{B}_0 + C_{in}' = 0 + 0 + 1 = 1$ Carrey = 0

$A_1 + \bar{B}_1 + C_{in}' = 0 + 1 + 0 = 0$ Carrey = 0

$A_2 + \bar{B}_2 + C_{in}' = 1 + 1 + 0 = 0$ Carrey = 1

$A_3 + \bar{B}_3 + C_{in}' = 0 + 1 + 1 = 0$ Carrey = 1

Hence the result of first adder is $S_3\ S_2\ S_1\ S_0$ = 0 0 1 1 and C_{out}' is 1.

To gain propere output and corrceat sign bit we have to take each output from the first adder into the XOR gate with compliment of Cout for each bit respectively. Then the output of XOR gates acts as input of 2nd adder and another input will be zero (0) and here carrey in will be same as $(C_{out}') = (1)' = 0$

So, the final result will be same as output of first adder with sign bit $= (C_{out}')' = 0$ which represent positive result.

The final output

D_3	D_2	D_1	D_0
0	0	1	1

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For B>A, two inputs are A = 2 B = 3
while doing substraction in first adder circuit, we will follow $A+\bar{B}+C_{in}'$ expression where C_{in}' always be high

A_3	A_2	A_1	A_0		B_3	B_2	B_1	B_0
0	0	1	0		0	0	1	1

$A_0+\bar{B}_0+C_{in}' = 0+0+1 = 1$ Carrry = 0
$A_1+\bar{B}_1+C_{in}' = 1+0+0 = 1$ Carrry = 0
$A_2+\bar{B}_2+C_{in}' = 0+1+0 = 1$ Carrry = 0
$A_3+\bar{B}_3+C_{in}' = 0+1+0 = 1$ Carrry = 0

So, the result of first adder is $S_3\ S_2\ S_1\ S_0$ = 1 1 1 1 and $(C_{out}') = 0$
To gain proper result and correct sign bit, we have to take each output from first adder into XOR Gate with compliment of C_{out}' for each bit respectively. Then the output of XOR gates acts as input of 2nd adder and another input will be zero(0). Here, carrry in and sign bit will be same as $(C_{out}')' = (0)' = 1$

Now,

$S_0' = S_0 \oplus (C_{out}')' = 1 \oplus 1 = 0$
$S_1' = S_1 \oplus (C_{out}')' = 1 \oplus 1 = 0$
$S_2' = S_2 \oplus (C_{out}')' = 1 \oplus 1 = 0$
$S_3' = S_3 \oplus (C_{out}')' = 1 \oplus 1 = 0$

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Then in 2nd adder,

$S_0' + 0 + C_{in} = 0+0+1 = 1$ Carry = 0

$S_1' + 0 + C_{in} = 0+0+0 = 0$ Carry = 0

$S_2' + 0 + C_{in} = 0+0+0 = 0$ Carry = 0

$S_3' + 0 + C_{in} = 0+0+0 = 0$ Carry = 0

Here the desirable result is $D_3\ D_2\ D_1\ D_0$ = 0 0 0 1 with negative sign bit 1 and carry out, C_{out} is 0.

Sign	C_{out}	D_3	D_2	D_1	D_0
1	0	0	0	0	1

IC Requirements:

1. C_1 - 74283 (4 bit Full Adder) - 2 piece
2. C_2 - 74LS04 (NOT Gate) - 1 piece
3. C_3 - 74LS86 (XOR Gate) - 1 piece

Conclusion: In this experiment we have designed a BCD circuit for substraction. Here we learnt how to build a BCD substractor and how to handle the sign bit.