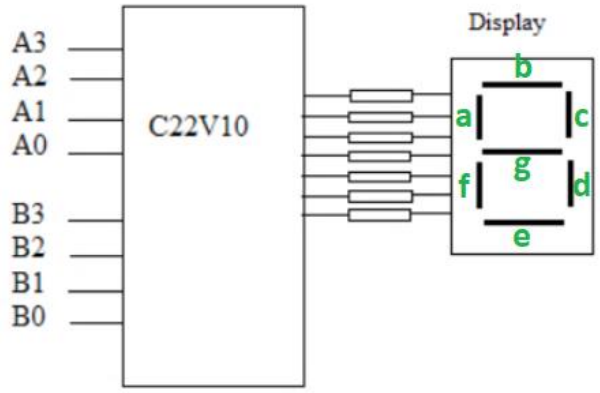
Yasir Riyadh Jabbar KTH/2020

LAB 3 Grundkursnivå



Om A=B skall displayen visa  e,g

Om A<B skall displayen visa  e,f,g

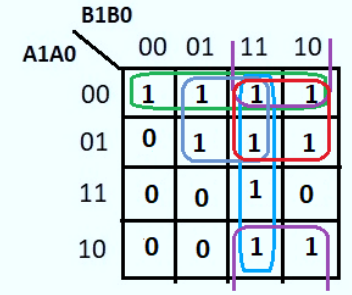
Om A>B skall displayen visa  d,e,g

G1: Kombinatorisk VHDL

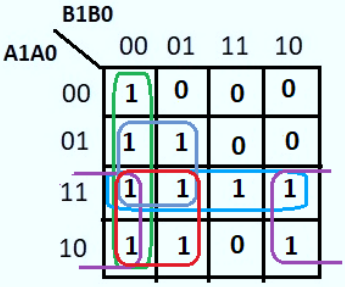
- En där A och B är tvåbitars binära tal A=(A1,A0) och B=(B1,B0). Utsignalerna ska här skrivas med Booleska uttryck (ta fram dem mha Karnaugh-diagram)

A1	A0	B1	B0	a	b	c	d	e	f	g
0	0	0	0	1	1	1	1	0	1	0
0	0	0	1	1	1	1	1	0	0	0
0	0	1	0	1	1	1	1	0	0	0
0	0	1	1	1	1	1	1	0	0	0
0	1	0	0	1	1	1	0	0	1	0
0	1	0	1	1	1	1	1	0	0	0
0	1	1	0	1	1	1	1	0	0	0
0	1	1	1	1	1	1	1	0	0	0
1	0	0	0	1	1	1	0	0	1	0
1	0	0	1	1	1	1	1	0	0	0
1	0	1	0	1	1	1	1	0	0	0
1	0	1	1	1	1	1	1	0	0	0
1	1	0	0	1	1	1	1	0	1	0
1	1	0	1	1	1	1	1	0	0	0
1	1	1	0	1	1	1	1	0	0	0
1	1	1	1	1	1	1	1	0	0	0

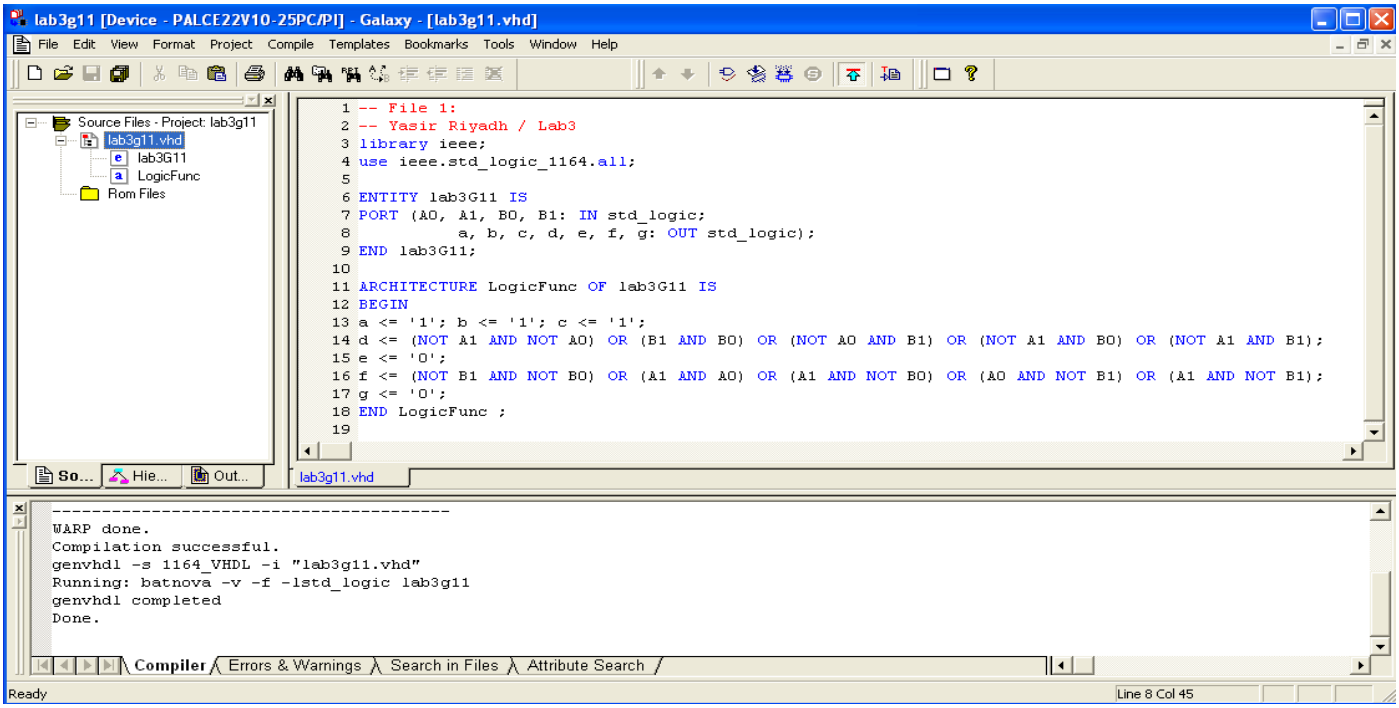
a=1 b=1 c=1 e=0 g=0

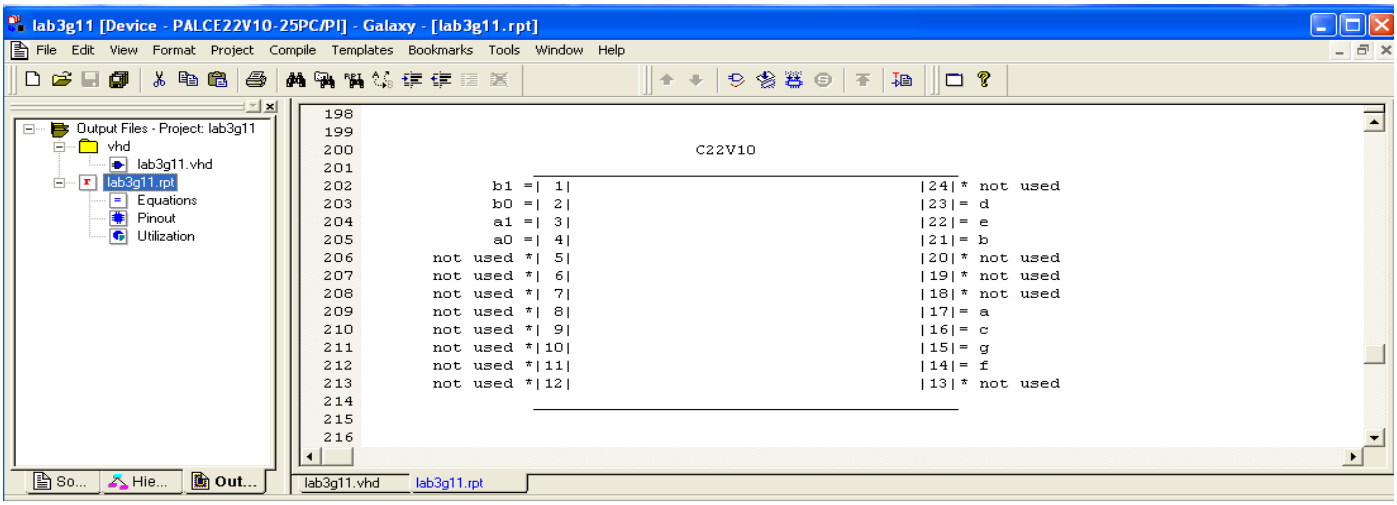


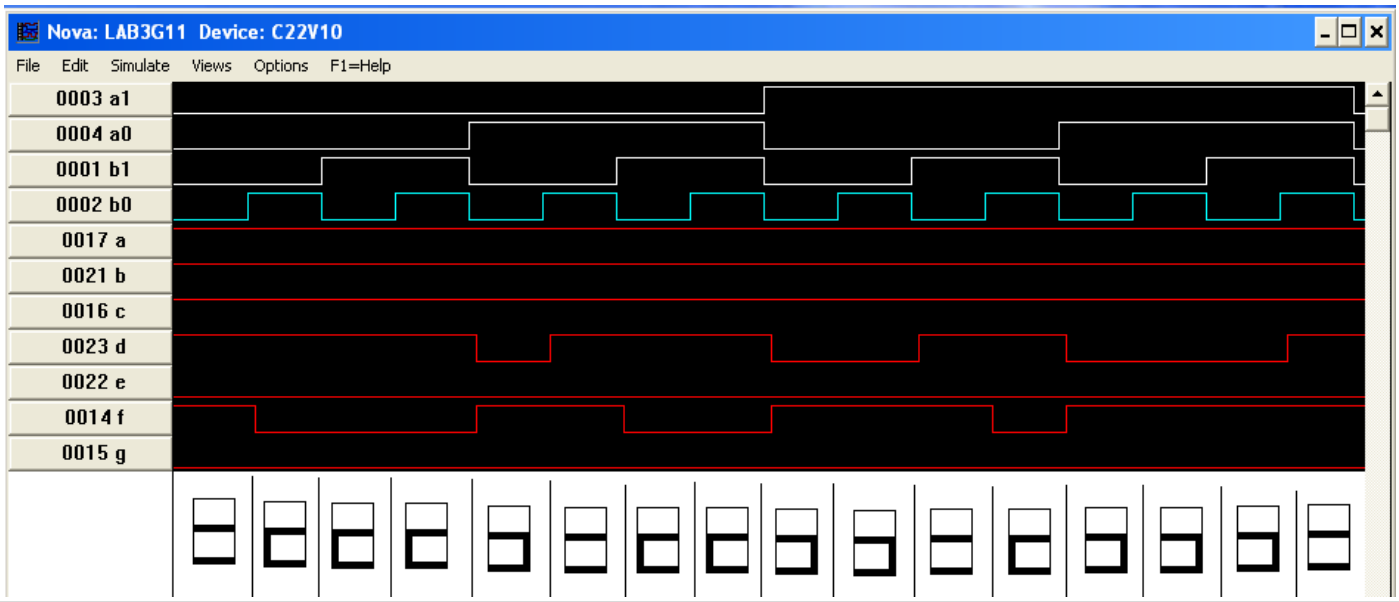
$d = \overline{A1}\,\overline{A0} + B1\,\overline{B0} + A0\,\overline{B1} + \overline{A1}\,B0 + A1\,\overline{B1}$



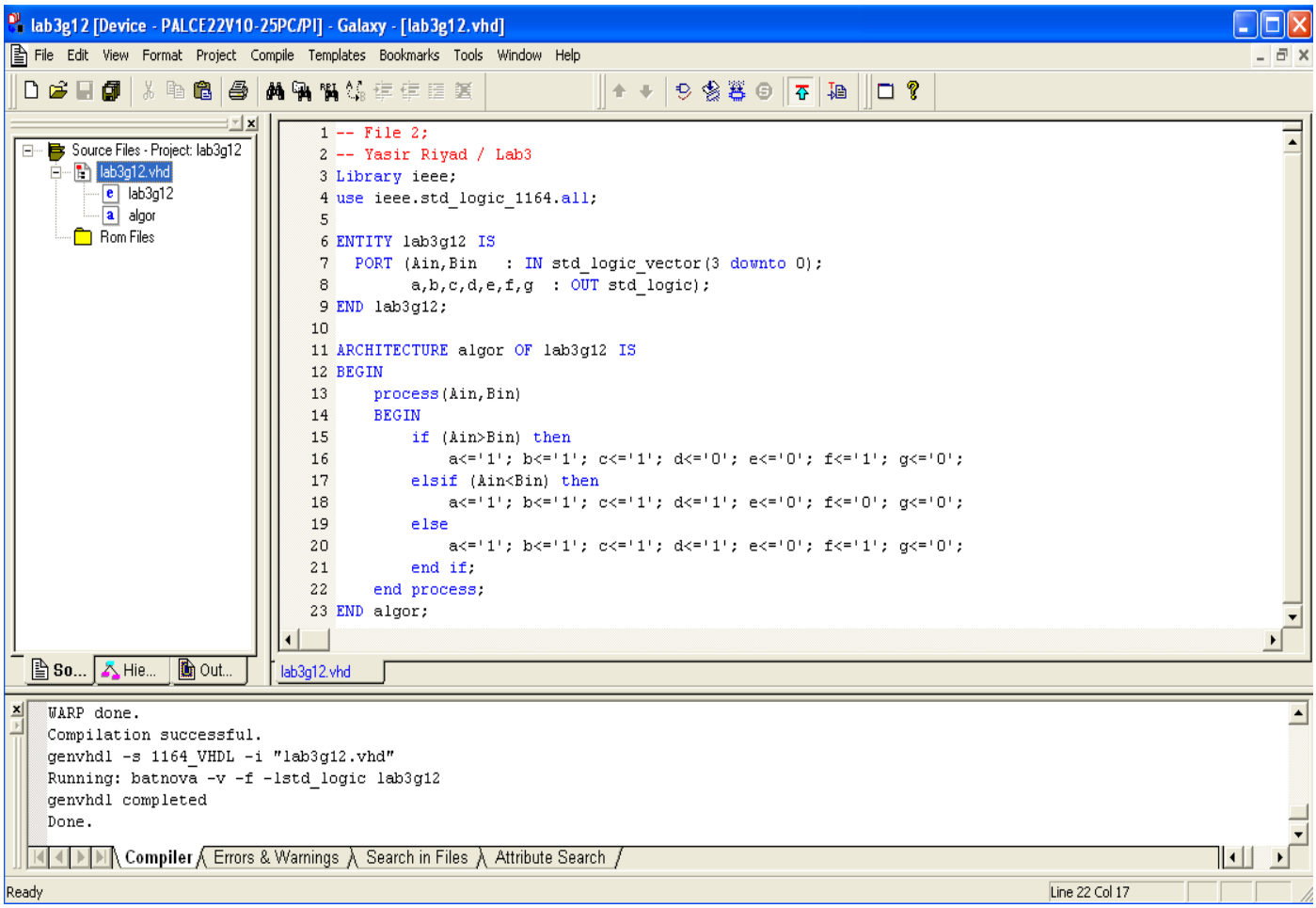
$f = \overline{B1}\,\overline{B0} + A1\,A0 + A1\,\overline{B0} + A0\,\overline{B1} + A1\,\overline{B1}$

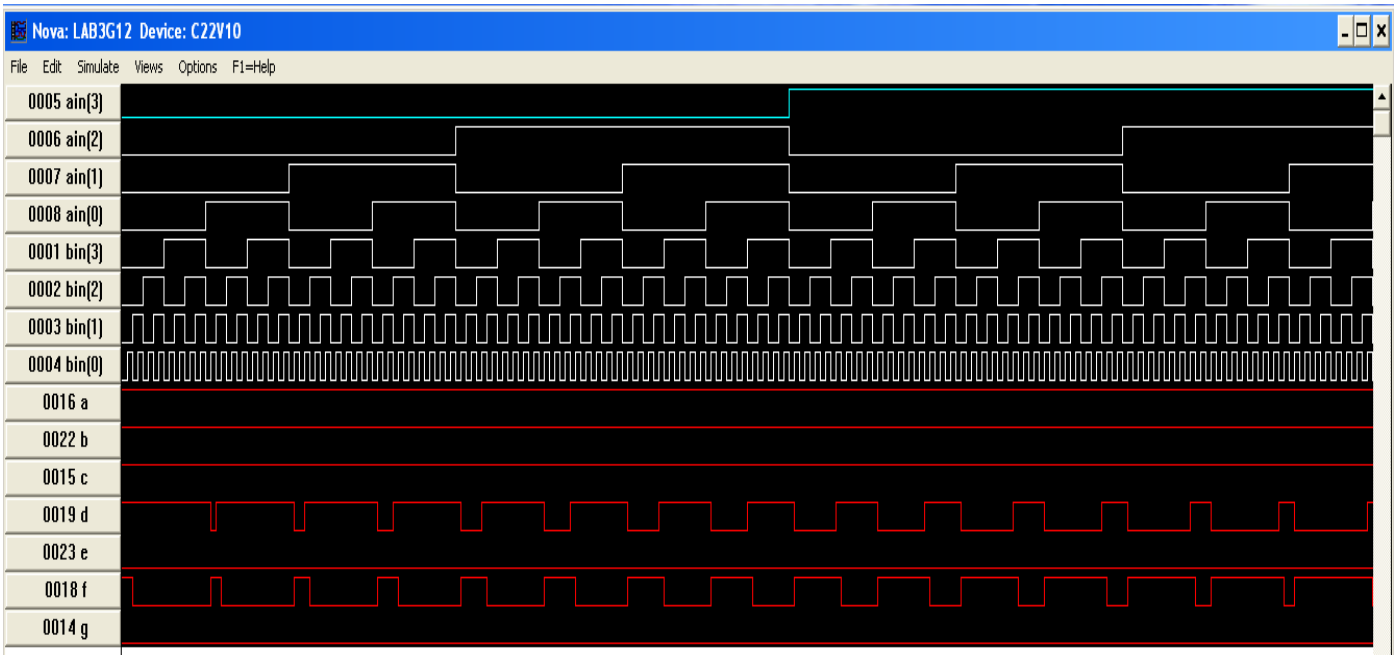

lab3g11 [Device - PALCE22V10-25PC/PI] - Galaxy - [lab3g11.vhd]
File Edit View Format Project Compile Templates Bookmarks Tools Window Help
Source Files - Project: lab3g11
lab3g11.vhd
lab3G11
LogicFunc
Rom Files
1 -- File 1:
2 -- Yasir Riyadh / Lab3
3 library ieee;
4 use ieee.std_logic_1164.all;
5
6 ENTITY lab3G11 IS
7 PORT (A0, A1, B0, B1: IN std_logic;
8 a, b, c, d, e, f, g: OUT std_logic);
9 END lab3G11;
10
11 ARCHITECTURE LogicFunc OF lab3G11 IS
12 BEGIN
13 a <= '1'; b <= '1'; c <= '1';
14 d <= (NOT A1 AND NOT A0) OR (B1 AND B0) OR (NOT A0 AND B1) OR (NOT A1 AND B0) OR (NOT A1 AND B1);
15 e <= '0';
16 f <= (NOT B1 AND NOT B0) OR (A1 AND A0) OR (A1 AND NOT B0) OR (A0 AND NOT B1) OR (A1 AND NOT B1);
17 g <= '0';
18 END LogicFunc ;
19
lab3g11.vhd
WARP done.
Compilation successful.
genvhdl -s 1164_VHDL -i "lab3g11.vhd"
Running: batnova -v -f -lstd_logic lab3g11
genvhdl completed
Done.
Compiler Errors & Warnings Search in Files Attribute Search
Ready
Line 8 Col 45


lab3g11 [Device - PALCE22V10-25PC/PI] - Galaxy - [lab3g11.rpt]
File Edit View Format Project Compile Templates Bookmarks Tools Window Help
Output Files - Project: lab3g11
vhd
lab3g11.vhd
lab3g11.rpt
Equations
Pinout
Utilization
C22V10
b1 =| 1| |24|* not used
b0 =| 2| |23|= d
a1 =| 3| |22|= e
a0 =| 4| |21|= b
not used *| 5| |20|* not used
not used *| 6| |19|* not used
not used *| 7| |18|* not used
not used *| 8| |17|= a
not used *| 9| |16|= c
not used *|10| |15|= g
not used *|11| |14|= f
not used *|12| |13|* not used
lab3g11.vhd
lab3g11.rpt


Nova: LAB3G11 Device: C22V10
File Edit Simulate Views Options F1=Help
0003 a1
0004 a0
0001 b1
0002 b0
0017 a
0021 b
0016 c
0023 d
0022 e
0014 f
0015 g

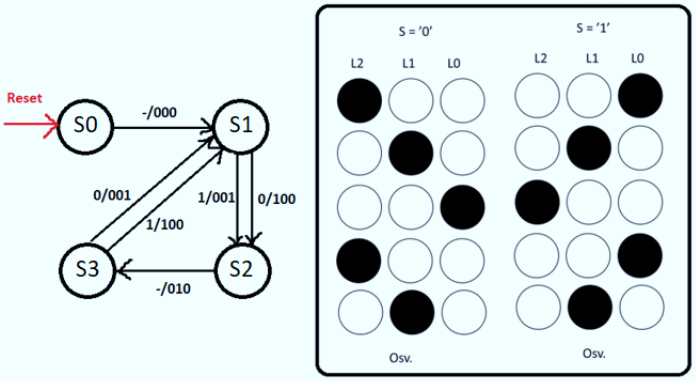
- En där A och B är fyrabitars binära tal A=(A3,A2,A1,A0) och B=(B3,B2,B1,B0). Utsignalerna ska här skrivas med villkorssatser (IF, CASE eller motsvarande).





G2: Sekventiell VHDL:

Skriv en VHDL-fil som realiserar samma tillståndsmaskin som du byggde i lab 2 (alltså den med det ”rullande” ljuset).



lab3g2 [Device - PALCE22V10-25PC/PI] - Galaxy - [lab3g2.vhd]

File Edit View Format Project Compile Templates Bookmarks Tools Window Help

Source Files - Project: lab3g2
lab3g2.vhd
rullande
FSM
Rom Files

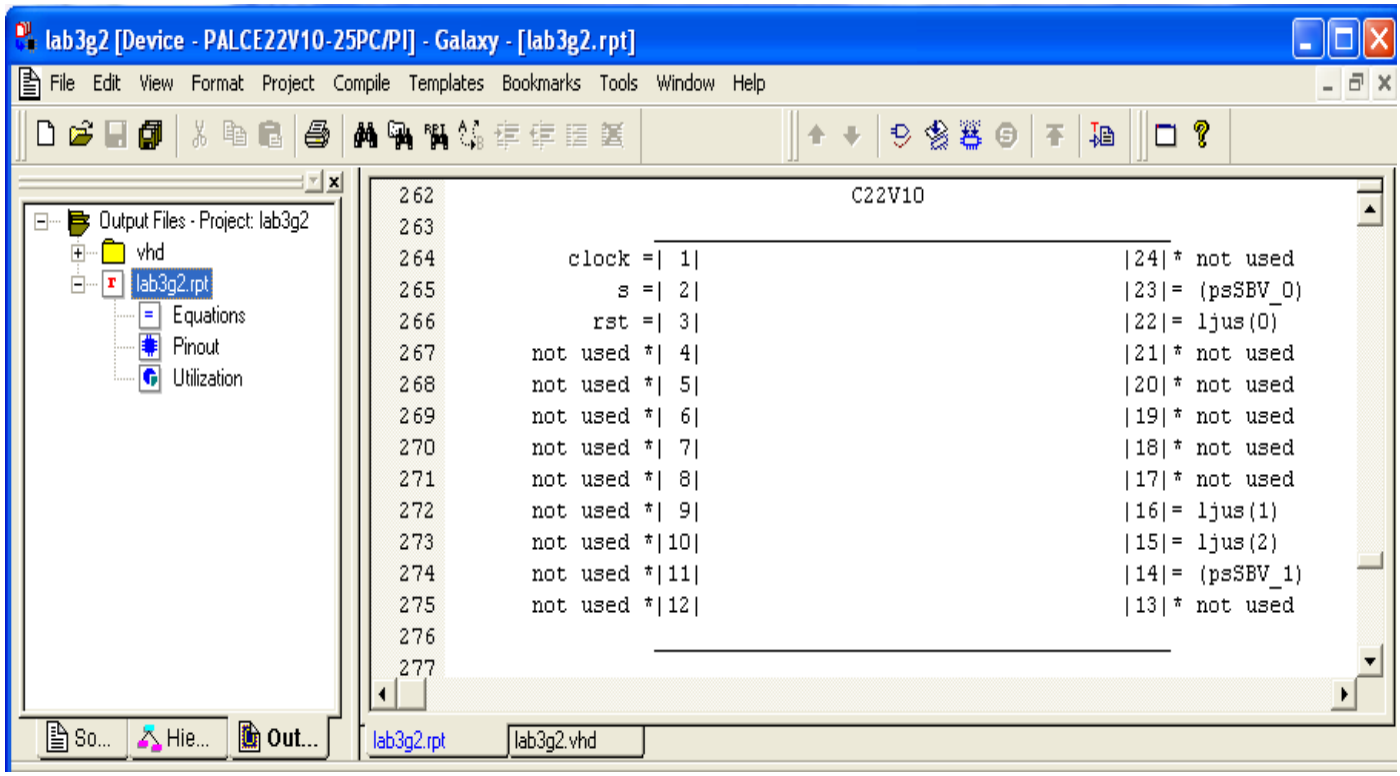
```
1 -- File 3
2 -- Yasir Riyadh / Lab3
3 LIBRARY ieee ;
4 USE ieee.std_logic_1164.all ;
5 ENTITY rullande IS
6   PORT (Clock, Rst, S: IN std_logic;
7         Ljus: OUT std_logic_vector (2 DOWNTO 0));
8 END rullande;
9 ARCHITECTURE FSM OF rullande IS
10  TYPE Statetype IS (S0, S1, S2, S3);
11  SIGNAL PS, NS: Statetype;
12 BEGIN
13  PROCESS (Clock, Rst)
14  BEGIN
15    IF (Rst = '1') THEN   PS <= S0;
16    ELSIF (Clock = '1' AND Clock'EVENT) THEN  PS <= NS;
17    END IF;
18  END PROCESS;
19  PROCESS (PS, S)
20  BEGIN
21    NS <= S0;
22    CASE PS IS
23      WHEN S0 => NS <= S1; Ljus <= "000";
24      WHEN S1 => IF (S = '1') THEN  NS <= S2; Ljus <= "001";
25             ELSE NS <= S2; Ljus <= "100";
26             END IF;
27      WHEN S2 => IF (S = '1') THEN  NS <= S3; Ljus <= "010";
28             ELSE NS <= S3; Ljus <= "010";
29             END IF;
30      WHEN S3 => IF (S = '1') THEN  NS <= S1; Ljus <= "100";
31             ELSE NS <= S1; Ljus <= "001";
32             END IF;
33      END CASE;
34  END PROCESS;
35 END FSM;
```

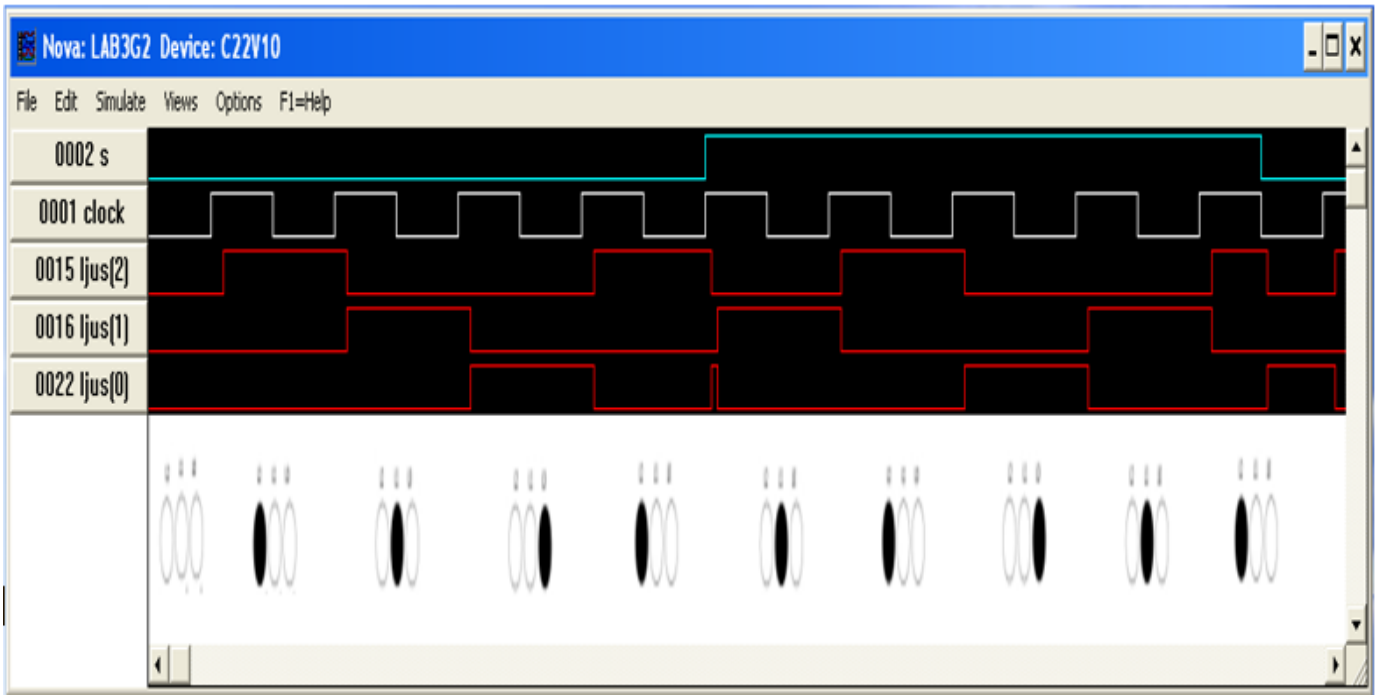
So... Hie... Out... lab3g2.vhd

```
WARP done.
Compilation successful.
genvhdl -s 1164_VHDL -i "lab3g2.vhd"
Running: batnova -v -f -lstd_logic lab3g2
genvhdl completed
```

Compiler | Errors & Warnings | Search in Files | Attribute Search

Ready Line 38 Col 1


lab3g2 [Device - PALCE22V10-25PC/PI] - Galaxy - [lab3g2.rpt]
File Edit View Format Project Compile Templates Bookmarks Tools Window Help
Output Files - Project: lab3g2
vhd
lab3g2.rpt
Equations
Pinout
Utilization
So... Hie... Out...
C22V10
clock =| 1| |24|* not used
s =| 2| |23|= (psSBV_0)
rst =| 3| |22|= ljus(0)
not used *| 4| |21|* not used
not used *| 5| |20|* not used
not used *| 6| |19|* not used
not used *| 7| |18|* not used
not used *| 8| |17|* not used
not used *| 9| |16|= ljus(1)
not used *|10| |15|= ljus(2)
not used *|11| |14|= (psSBV_1)
not used *|12| |13|* not used
lab3g2.rpt
lab3g2.vhd


Nova: LAB3G2 Device: C22V10
File Edit Simulate Views Options F1=Help
0002 s
0001 clock
0015 ljus(2)
0016 ljus(1)
0022 ljus(0)