Department of Electronic & Telecommunication Engineering

University of Moratuwa



**EN2111 - Electronic Circuit Design**

# UART Implementation in FPGA

Group 09

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# Introduction

This report is about setting up a UART transceiver and receiver on the DE0-Nano FPGA board. There are three main parts which are the simulation timing diagram, the test benches that go with it, and the RTL codes. UART is a way for devices to talk to each other without needing a clock signal. It uses start and stop bits to show where data begins and ends. The RTL code explains in detail how the UART module handles data packets, acting as a model for the module's working. The test benches are carefully made to check that the module works well in different situations. Also, the timing diagram from the simulation helps us see when data is sent and received, guiding us on how to make communication better. Once the FPGA is set up with this, the Tx and Rx pins allow devices to talk to each other smoothly.

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# **RTL code for UART**

## Baud Rate CodeA screenshot of a computer program Description automatically generated

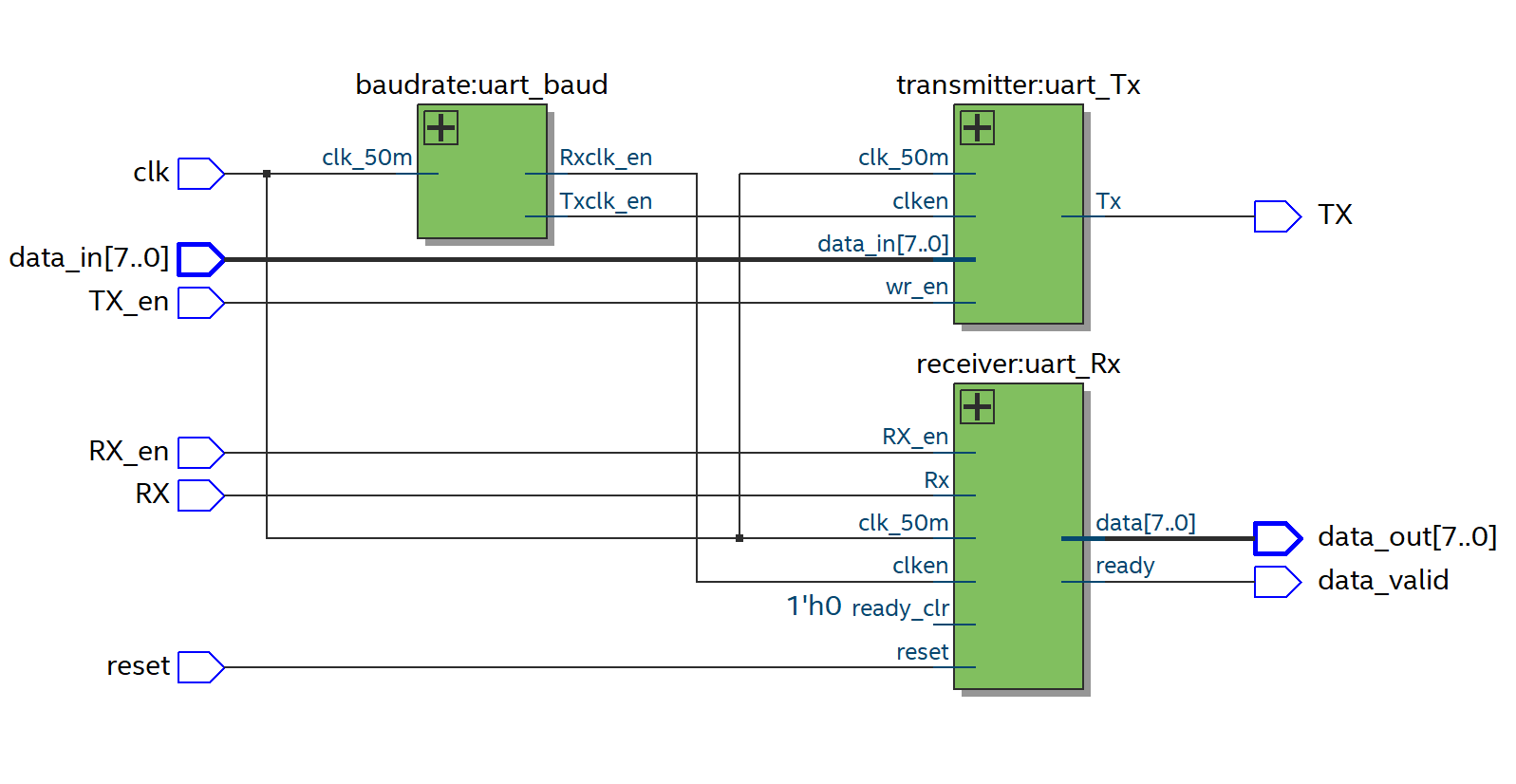
## Transmitter CodeA screenshot of a computer program Description automatically generated

## Receiver Code

## A screenshot of a computer Description automatically generated

## UART Code

## A screenshot of a computer Description automatically generated



# **Testbenches**

## Baud Rate Tb

A screenshot of a computer

Description automatically generated



## Transmitter Tb

## A screenshot of a computer program Description automatically generated

A green lines on a black background

Description automatically generated

## Receiver Tb

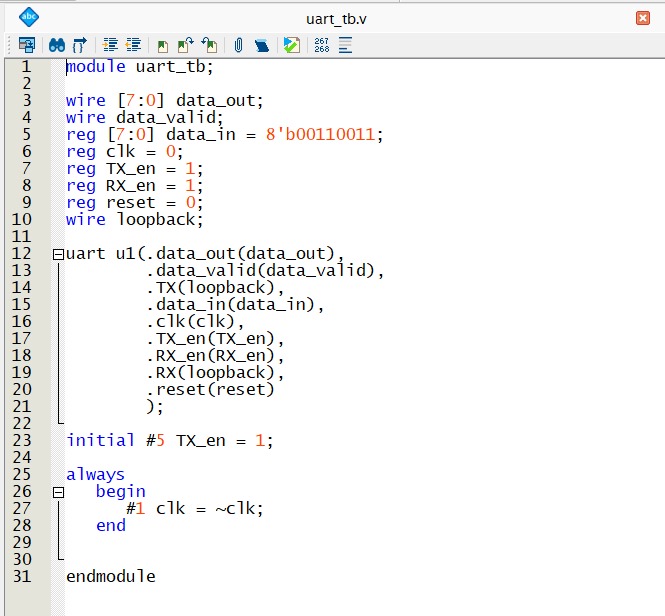
A screenshot of a computer program

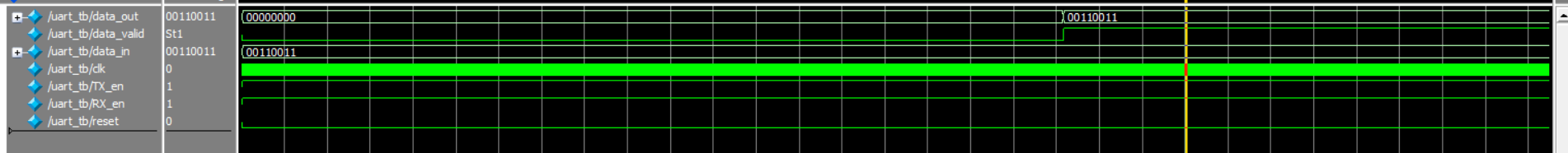
Description automatically generated

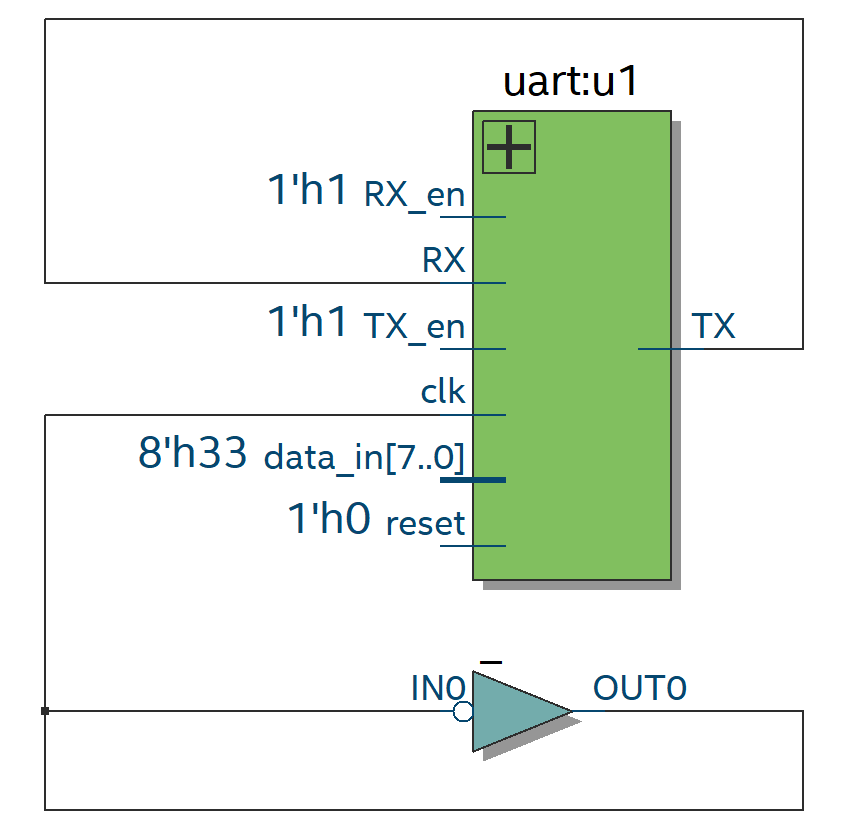
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Description automatically generated

## UART Tb







# **Timing Analysis**

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