DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING
IMPERIAL COLLEGE LONDON

EE3 – 14
POWER ELECTRONICS
COURSEWORK 1 REPORT
SYSTEM ANALYSIS, SIMULATION AND DESIGN

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TABLE OF CONTENTS

1. INTRODUCTION

The aim of this report is to discuss and analyse the design and simulation of a Buck switch mode power supply. Ideal and real simulations will be examined with regards to the desired operational specifications (see Appendix A) and techniques to improve efficiency will be explored. Finally, close loops designs will be studied and implemented.

2. CONVERTER DESIGN

2.1 BASIC CONVERTER DESIGN

2.1.1 COMPONENT VALUES

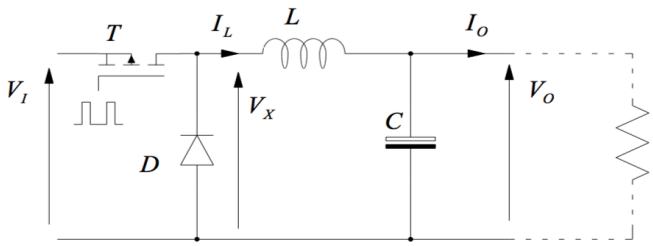


Figure 1: Simple Buck Converter Design

A – Inductor sizing

The minimum inductor value is found considering the following extremities:

$$L_{min} = \frac{V_{in_{min}} - V_{out}}{\Delta I(on)} \frac{\delta_{max}}{f_{swtich_{max}}} = \frac{22-3.3}{0.25} \frac{0.15}{250\times10^3} = 44.88\ \mu H$$

where $\delta_{max} = \frac{V_{out}}{V_{in_{min}}} = \frac{3.3}{22} = 15\%$ and $\Delta I(on)_{max} = 5\%(I_{out_{max}}) = \frac{5(5)}{100} = 0.25\ A$

B – Inductor current

i. If the peak inductor current is larger than the rated saturation current, efficiency reduces as the inductance will roll off, resulting in less energy being stored in the inductor and an increased current ripple [1]. The worst case peak current is calculated at the maximum output power:

$$I_{L_{peak}} = I_{O_{max}} + \frac{1}{2}\Delta I_L = I_{O_{max}} + \frac{1}{2}\Delta I(on) = 5 + \frac{1}{2}(0.25) = 5.125\ A$$

ii. The RMS inductor current is the average current through the inductor, a key factor in defining the I^2R conduction losses. The worst case RMS current is:

$$I_{L_{RMS}} = \sqrt{I_{out}^2 + \frac{\Delta I_L^2}{12}} = \sqrt{5^2 + \frac{(0.25)^2}{12}} \approx 5.00\ A$$

C – Capacitor sizing

i. The corner frequency of the LC filter is selected to be at least one order of magnitude smaller than the minimum switching frequency: $f_{LC} = 0.1 f_{switch_{min}} = 0.1(150\times10^3) = 15\ kHz$. This is to avoid high gain at the switching frequency, which would lead to undesirable sub-cycle oscillations in the control system. The minimum capacitance is therefore:

$$C_{min} = \frac{1}{(2\pi f_{LC})^2 L} = \frac{1}{\left(2\pi(15\times10^3)\right)^2(44.88\times10^{-6})} \approx 2.51\mu F$$

ii. The output voltage ripple given by the capacitor is:

$$\Delta V_{C_{min}} = \frac{\Delta I(on)}{8 f_{switch_{min}} C_{min}} = \frac{0.25}{(8)(150\times10^3)(2.51\times10^{-6})} \approx 83\ mV$$

Using the maximum output ripple, the minimum acceptable capacitance is:

$$C_{min} = \frac{\Delta I(on)}{8 f_{switch_{min}} \Delta V_{max}} = \frac{0.25}{(8)(150\times10^3)(100\times10^{-3})} \approx 2.08\mu F$$

D – Switch selection

The peak current that could potentially run through the switch current was previously calculated as $I_{max} = 5.125A$. However, in order to compensate for transients, a choice of $I_{switch_{max}} \geq 7A$ is preferable.

Finally, the voltage blocking capability is found by considering the maximum input voltage and the diode voltage drop. Choosing $V_{in_{max}} = 26V$ and $V_{AK} = 1.0V$, the MOSFET will require $V_{block} = 27V$. Again, due to transients, a choice of $V_{block} \geq 35V$ is preferable.

2.2 Static and Dynamic Converter Model

Diode Voltage Drop

Previous calculations have so far assumed a negligible voltage drop across the diode. However, in reality, this voltage drop will affect both output voltage and efficiency. The expressions for the ripple currents, assuming a $V_{AK} \neq 0$ are:

$$\Delta I(on) = \frac{V_{in} - V_{out}}{L} t_{on} \quad \Delta I(diode) = \frac{-V_{AK} - V_{out}}{L} t_{diode}$$

Setting $\Delta I(on) + \Delta I(diode) = 0$ now yields a duty cycle of:

$$\delta_{AK \neq 0} = \frac{V_{out} + V_{AK}}{V_{in}} \left(1 + \frac{V_{AK}}{V_{in}}\right)^{-1}$$

Converter Transfer Function

It is useful to derive a s-domain plant model of the converter, especially for the design of control techniques explored in Section 7 (refer to Appendix B.1 for the full derivation).

$$\frac{V_{out}(s)}{\delta(s)} = \frac{V_{in}}{1 + s\frac{L}{R} + s^2 LC}$$

Note that this transfer function does not take into account parasitic components of the circuit (see Section 5).

3. Simulation of Ideal Converter in Open Loop

3.1 Simulations

To simulate an ideal Buck SMPS, the circuit in *Figure 2* was designed. The simulations were run using ideal components under the following assumptions:

- Negligible $V_{DS_{on}}$ and parasitic impedances
- Operation at maximum output current and output ripple current, i.e. $\Delta I(on) = 0.25\ A$
- Operation at rated input and output voltages, $V_{in} = 24\ V$ and $V_{out} = 3.3\ V$
- Almost ideal square wave at the switch driver output – the switch's R_{on} had been set to 0.1 $\mu\Omega$ and R_{off} to 1 $G\Omega$ and the rise and fall times of the switch driver had been set to 0.1 ns

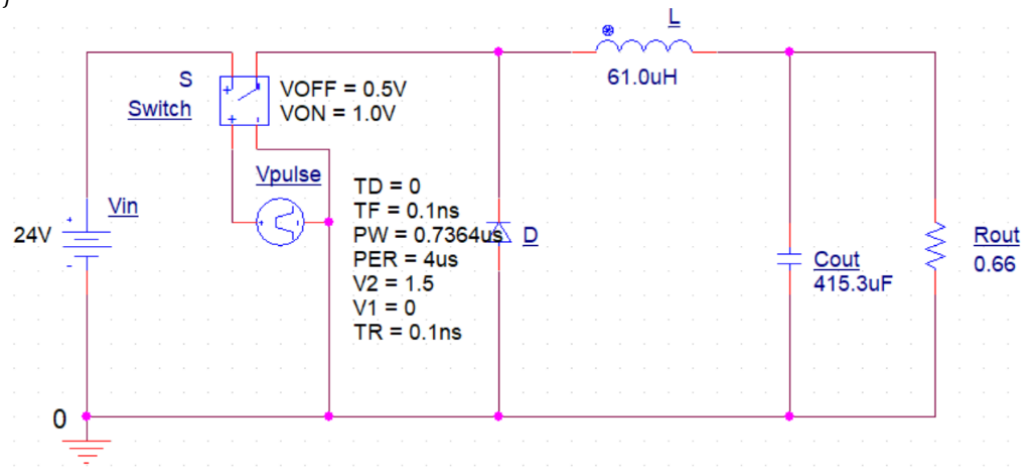


Figure 2: Ideal Buck Implementation in PSpice

In reality, the majority of the output voltage ripple is due to the ESR of the capacitor and hence it is vital to keep it as small as possible. This can be achieved by choosing the largest capacitor possible, which corresponds to the maximum switching frequency of 250 kHz (see Appendix C). Although a high frequency additionally has the benefit of a small inductor, it also results in an increase in switching losses. Nevertheless, these losses are considered insignificant for now as an ideal switch is being used.

It is important to note that the voltage drop across the diode contributes to a significant reduction in output voltage (replacing the diode with a synchronous rectifier will correct this and will be explored in Section 6). For now, in order to achieve the ideal $V_{out} = 3.3\ V$, an appropriate duty cycle was selected to compensate for the diode voltage drop. Using the measured forward diode drop of $V_{AK} \approx 1.37\ V$, the duty cycle is hence-forth:

$$\delta = \frac{V_{out} + V_{AK}}{V_{in}} \left(1 + \frac{V_{AK}}{V_{in}}\right)^{-1} = \frac{3.3 + 1.37}{24} \left(1 + \frac{1.37}{24}\right)^{-1} = 0.1841$$

3.1.1 EFFICIENCY

In order to reliably measure efficiency, only steady-state values have been considered. *Figure 3* illustrates how the efficiency varies with input voltage and load, calculated as $\eta = \frac{P_{out}}{P_{in}} = \frac{P_{in} - P_{loss}}{P_{in}}$.

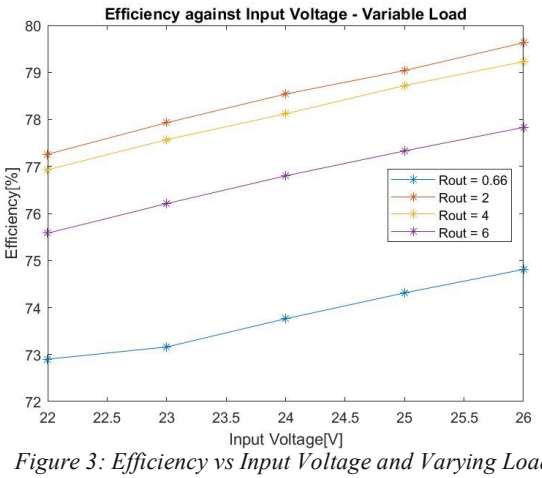


Figure 3: Efficiency vs Input Voltage and Varying Load

Overall, the efficiency of the converter is lower than the minimum required of 90%. This is mainly due to the significant voltage drop across the diode. Considering the output voltage of 3.3 V, a 1.37 V drop across the diode is a considerable loss of approximately 42%. However, as the input voltage and thus the output voltage increases, efficiency will rise as this lossy diode drop becomes less and less significant.

However, it is interesting to note that the efficiency initially increases quickly with the load and then begins to slowly drop. This is because there is a trade-off with an improving diode drop to output voltage ratio and worsening parasitic losses that follow an increase in output voltage. The optimum operating point lies at $R_{out} = 2\ \Omega$.

3.1.2 START-UP BEHAVIOUR

In order to investigate the start-up behaviour of the converter, the capacitor and inductor are set to begin in a discharged state. *Figure 4* illustrates the voltage across the capacitor at turn on.

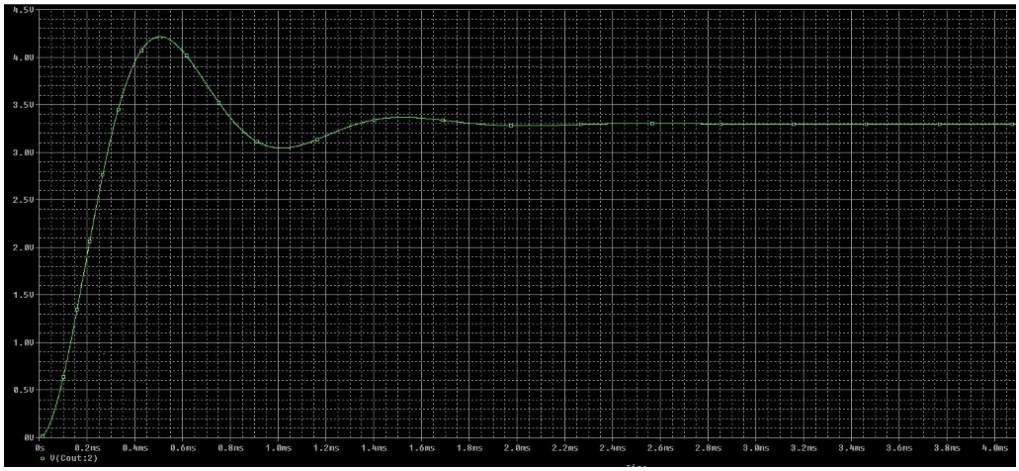


Figure 4: Capacitor Voltage During Start-Up

An overshoot of $\frac{4.2139-3.3}{3.3} \times 100 = 27.69\%$ occurs, which is much higher than desired (a compensator will be explored in Section 7 to reduce this). The system was then investigated and found to have two poles at $-1.82 \pm 6.01\ krads/s$ and a damping factor of $\zeta = 0.2898$, confirming it is underdamped. The rise and settling time measured are $294\mu s$ and $1.26\ ms$ respectively. Furthermore, the average oscillation frequency was calculated as $947.07\ Hz$.

The following measurements do not coincide perfectly with the values predicted by the transfer function (see Appendix B.2). This is because MATLAB does not take into account the resistances of the switch, rise/fall times of the pulse, etc. and thus they are not directly comparable.

3.1.3 CHANGE IN LOAD

No Load

In a no load situation, there is no path for the capacitor to release its accumulated charge during the 'off' state. Consequently, the voltage across the capacitor increases asymptotically towards the input voltage as shown in *Figure 5*; the circuit thus loses its functionality as a power converter. Furthermore, the system was found to have two poles on the imaginary axis, verifying this system is marginally stable (see Appendix D).

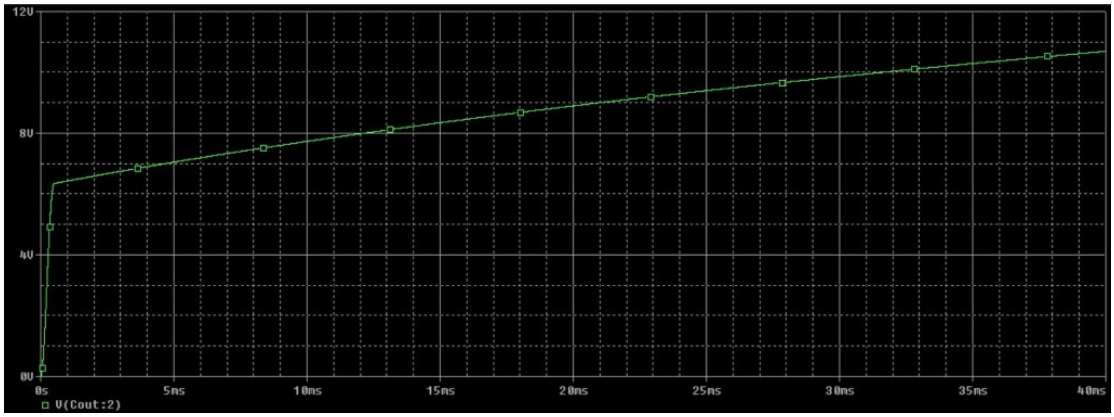


Figure 5: 0% Load

Further investigation revealed that the converter will eventually conduct in discontinuous mode. *Figure 6* displays the behaviour of the inductor current as the capacitor's voltage increases towards the input voltage. At first, the 'on' state inductor current begins to increase at a high rate as $V_{out} = 0\,V$. During the first few cycles, the 'off' state voltage difference across the inductor is small, resulting in a slow discharge. Overall, the average inductor current rises with every cycle. However, as the output voltage rises, there comes a turning point where the average inductor current begins to decrease. Eventually, the inductor current will go to zero during the 'off' state and the inductor enters discontinuous conduction (*Figure 7)*. After an infinite amount of time, I_L would remain at 0 A and $V_{out} = V_{in}$.

Figure 6: 0% Load

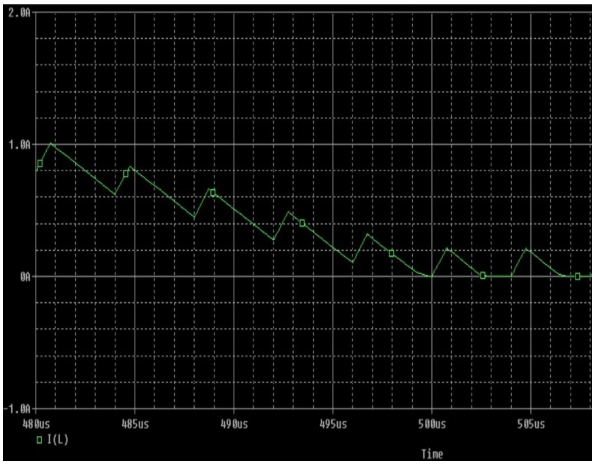


Figure 7: Zoomed in Inductor Current

Switching between Load Extremes

An output load of 0.66Ω results in the maximum output current of $5A$. *Figure 8* illustrates what happens to the output voltage and inductor current when the load switches between this value and no load. When the latter occurs, the output voltage will start shooting up to match the input voltage as described earlier. When the load is re-connected, the output voltage shoots back down and settles around $3.3V$. Oscillations occur when switching from no load to load due to resonance between the inductor and diode capacitance.

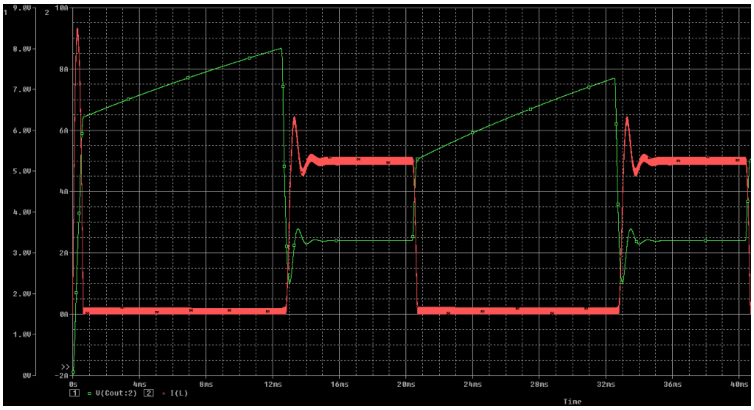


Figure 8: Load Switching

4. REAL COMPONENT CHOICES

Real components introduce new sources of power losses not yet considered. For instance, the inductor and capacitor will have equivalent series inductance, R_{ESL} (negligible), and resistance, R_{ESR}, that will introduce I^2R losses along with additional noise and voltage ripple. Moreover, potentially significant switching losses may occur in the real MOSFET, along with conduction losses. These switching losses are proportional to the rise and fall times of the currents and voltages during switching (see Appendix E). They can be significant at high frequencies, however, a higher frequency allows for smaller reactive components and thus lower parasitic resistances.

Considering this trade-off, a switching frequency of $f_{switch} = 225\,kHz$ has been chosen resulting in an inductance of $L = 68\,\mu H$. To avoid high gain at the switching frequency, the corner frequency of the low-pass output filter is set to $1kHz$ by selecting an output capacitance of $374\,\mu F$. This ensures an early roll off and a tiny gain at $225\,kHz$, avoiding any switching noise being passed into the closed-loop system. This choice has the additional benefit of a larger capacitance, which is better equipped to stabilise the output voltage.

Inductor *- 1468373C, Murata Power Solutions*

The following inductor has been chosen due to its inductance value of $68\,\mu H \pm 10\%$ and low resistance of $0.025\,\Omega$. It additionally has a suitable maximum DC current rating of $7.3\,A$. Furthermore, its closed-loop core will minimise the amount of escaping magnetic flux, which may significantly affect the tracks in the PCB.

Capacitors *– Electrolytic: Panasonic EEHZK1V331P (*$330\,\mu F \pm 20\%$*) and Ceramic: Murata Power Solutions GRM21BR61E226ME44L* $(22\,\mu F \pm 20\%)$

To minimise the output voltage ripple, the output capacitance must have a low ESR. Instead of using one capacitor with the desired value of $374\,\mu F$, a parallel combination of an electrolytic capacitor and ceramic capacitors will be implemented in order to reduce the overall parasitic resistance. The electrolytic capacitor has an ESR of $20\,m\Omega$ however, the ceramic capacitors' ESR are undefined and will be experimentally measured.

Diode *– STMicroelectronics, STPS10L25D*

This diode is used during synchronous rectification, in parallel with the low-side MOSFET. The diode needs to be fast-switching and have a very low forward voltage drop. A Schottky diode is preferred as it is composed of a metal-semiconductor junction and therefore has very low stored charge, resulting in fast switching. The selected Schottky diode has a rated voltage drop of $\approx 350\,mV$.

MOSFET *- IPP048N04NGXKSA1, Infineon*

The chosen N-channel MOSFET has very fast turn-on ($13ns$) and turn-off ($19ns$) times, limiting the switching losses throughout operation. Additionally, it has a low on-state resistance of $4.8\,m\Omega$. As calculated in Section 2.1.1, the MOSFET will need to sustain a $V_{DS} \approx 27\,V$ and a $I_{L_{peak}} \approx 5.125\,A$. The selected MOSFET can support a $V_{DS} = 40\,V$ and $I_D = 70\,A$. The V_{DS} rating is considered suitably low as the higher the rating, the larger the separation between the drain and source, ultimately leading to a larger on-state resistance and conduction loss. This large current rating may be an issue as the device will have a high gate capacitance, potentially resulting in high AC gate currents. However, this is commonly solved with a passive gate resistor and will be explored in Section 5.

MOSFETs in the DPAK or SOT-223 configuration have also been considered as they offer a lower capacitance and current rating. The SOT-223 BSP603S2LHUMA1 OptiMOS by Infineon could be used in case the primary device fails to respect the specifications.

Gate Driver *- TPS2830,* ***Texas Instruments***

A good gate driver should add and remove charge from the gate with minimal loss and at high speeds; therefore, the main requirements are a low supply current and low rise/fall times. The selected gate driver is of CMOS technology which is better capable to achieve a low supply current over TTL. Furthermore, the gate driver has support for synchronous rectification in which it can drive both high-side and low-side MOSFETS while preventing shoot-through currents from the input side to ground during switching.

5. Simulations and Analysis with Real Components

5.1 Simulations

The converter simulation circuit is now transformed using the real components as shown in *Figure 9*.

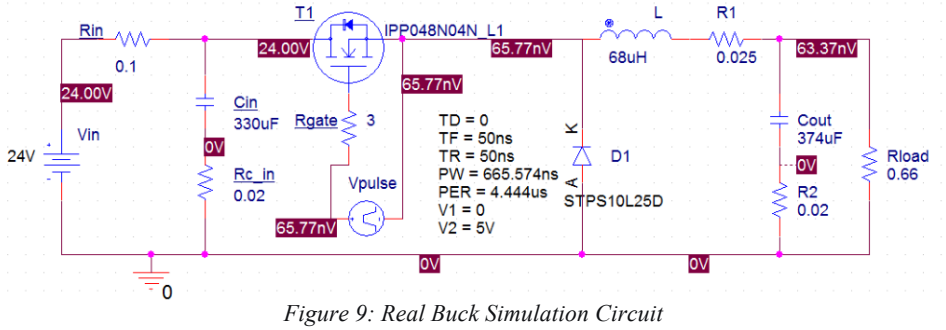


Figure 9: Real Buck Simulation Circuit

The model of the real MOSFET was imported into PSpice and the ESR values of the capacitors and inductor were added. As the datasheets of the ceramic capacitors do not provide a constant ESR value, the worst case ESR is considered, corresponding to the electrolytic capacitor of 0.02 Ω.

The transfer function of the SMPS, now including parasitic resistances, is:

$$\frac{V_{out}(s)}{\delta(s)} = V_{in}\frac{1+sCr_c}{1+\frac{r_L}{Rout}+S(\frac{L}{R}+Cr_c+C\left(1+\frac{r_C}{R_{out}}\right)r_L)+s^2LC\left(1+\frac{r_C}{R_{out}}\right)}$$

In order to meet the input ripple current specification, a low-pass RC filter is placed at the input. The corner frequency is set to 5 kHz using an electrolytic capacitance of 330μF and a resistance of 0.1 Ω (in reality this will be the resistance of the wire).

During the rise and fall times of the gate driver output, the capacitive impedance of the gate will be extremely low due to high frequency components present in the rising/falling signal. This could cause high AC gate current, reducing efficiency. The losses associated with this current increase with an increasing V_{GS}. On the other hand, the conduction losses are directly proportional to the on-state resistance of the transistor which, in the triode region, is approximately given by,

$$R_{DS}(on) = \frac{1}{\mu_n C_{ox}\frac{W}{L}(V_{GS}-V_{TH})}$$

However, this illustrates that conduction losses decrease with an increasing V_{GS}. From experimental data, it was found that switching losses are much more significant than the conduction losses. Therefore, operation at the minimum V_{GS}, observed to be 5 V, is preferred to minimise switching losses.

To simulate the gate driver, the V_{pulse} Capture part was used with the according rise and fall times of the real gate driver. The highest frequency component of the gate driver output can be roughly calculated as $\frac{1}{t_r}$, where t_r is the rise time of the gate pulse (typically 50 ns for the chosen driver). In the worst-case scenario, the highest gate capacitance $C_{in} = 3.3\ nF$ is considered. Therefore,

$$Z_{g_{switch}} = \left|\frac{1}{j\omega C}\right| \approx 2.41\ \Omega$$

To limit the AC gate current during switching to below 1 A, a 3 Ω passive gate resistor is used.

Finally, due to the introduction of the Schottky diode, the new duty-cycle corresponding to the newly measured voltage drop of 0.3459 V is:

$$\delta = \frac{V_{out}+V_{AK}}{V_{in}}\left(1+\frac{V_{AK}}{V_{in}}\right)^{-1} = \frac{3.3+0.3459}{24}\left(1+\frac{0.3459}{24}\right)^{-1} = 0.1498$$

However, the transfer function shows that the DC gain has been reduced by a factor of $1+\frac{r_L}{R_{out}} = 1.0379$. Consequently, the average output voltage is expected to lie below $\frac{3.3}{1.0379} \approx 3.18\ V$. After simulation, the correct duty cycle was found to be 0.15975.

5.1.1 Efficiency

The efficiency has increased compared to the ideal simulation. This is due to the use of the new Schottky diode which has a smaller voltage drop and contributes to a lower 10.48% voltage loss and is due to the diode drop, switching losses and I^2R dissipations. Furthermore, it is believed that the switching losses of the chosen MOSFET are the significant factor. This will be analysed further in Section 6.1.3. The pattern with increasing load and input voltage are the same in Section 3.1.1.

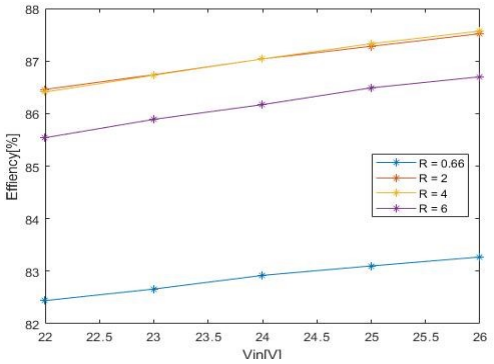
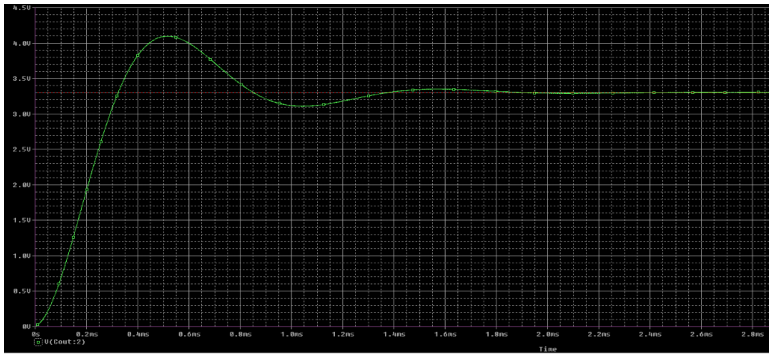


Figure 10: Efficiency vs Input Voltage and Load

5.1.2 Start- Up Behaviour



As shown in *Figure 11,* the start-up behaviour is very similar to the ideal, with the following measurements:

Overshoot, %	24.22
Rise Time, s	303.2867μ
Settling Time, s	$1.276\ m$
Oscillation Frequency, Hz	$1003.3\ Hz$

Table 1: Start-Up Measurements

5.1.3 Change in Load

No Load

Assuming the output capacitor starts in a discharged state, the power converter will enter discontinuous operation and the output voltage will saturate to the input voltage as discussed in Section 3.1.3. However, the use of the real MOSFET has changed the behaviour of the circuit. The body diode of the MOSFET now gives a path for negative current to flow, undermining efficiency as energy is pulled from the output capacitor.

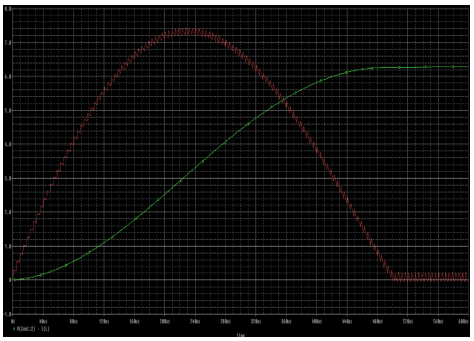


Figure 11: 0% Load

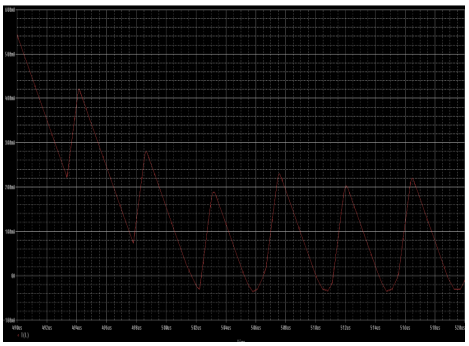


Figure 12: 0% Load Zoomed In

Switching between Load Extremes

Figure 13 illustrates switching between no load and 0.66 Ω, which gives the maximum output current. This result replicate the simulation for the ideal Buck in Section 3.1.3.

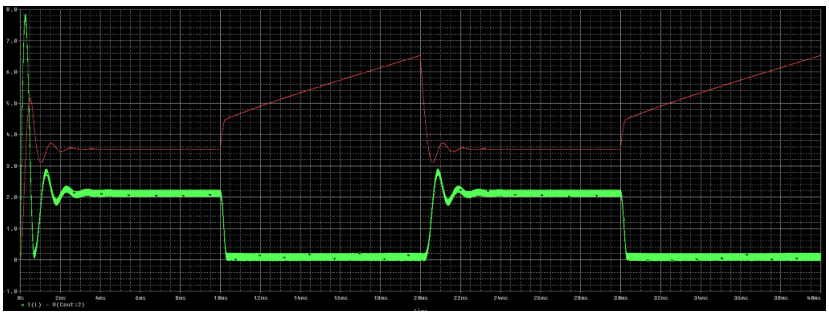


Figure 13: Load Switching

6. SYNCHRONOUS RECTIFICATION

6.1 SIMULATIONS

As mentioned earlier, the converter's efficiency may be improved using synchronous rectification. As shown in *Figure 14,* the diode has been replaced with a MOSFET, or also known as a "sync" FET.

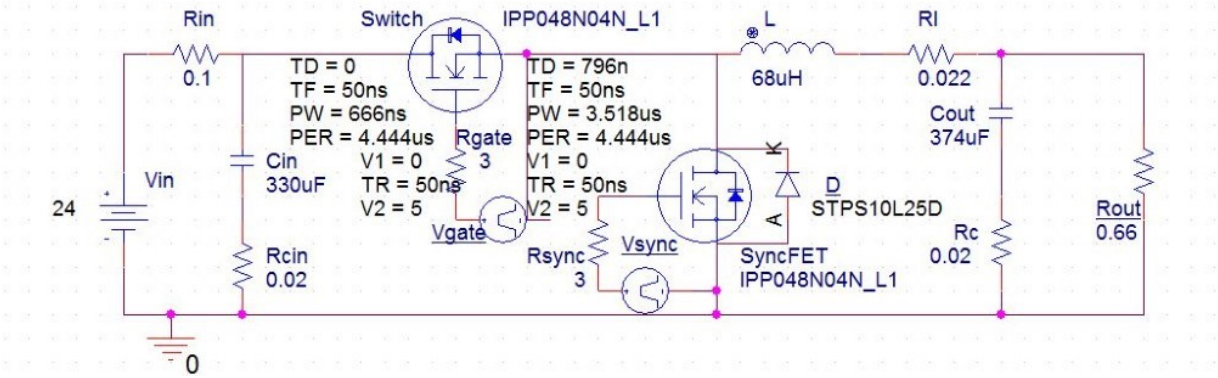


Figure 14: Buck Design with Synchronous Rectification

The sync FET has a lower voltage drop compared to the diode during the on-state, thus increasing the overall efficiency of the converter. However, the new transistor will introduce a further inefficiency via the dead-time delay. Dead-time is needed to avoid shoot-through, which occurs when both MOSFETs are on at the same time, resulting in short circuiting the input power rail and producing sharp current spikes. Although both transistors are off during the dead-time, the current through the inductor will still be able to flow and does so through the parasitic body diode of the sync FET, which is lossy. To reduce losses in the body diode, an external diode has been added in parallel to the sync FET. Efficiency will be improved as the diode goes into conduction at lower voltages compared to the lossy body diode, ensuring the body diode never conducts.

The selected gate driver can drive both high-side and low-side MOSFETs and additionally implements dead time control. However, as the full simulation of this device is particularly time consuming, the low-side driver is simulated with a pulse generator, whose output is inverted with respect to the high-side pulses. Furthermore, a dead-time of $50ns$ has been implemented.

Now that the diode voltage drop has been removed, a new duty cycle is found to achieve the correct output voltage. This has been experimentally measured as $\delta = 14.985\%$.

6.1.1 CONTINUOUS MODE

Figure 15 illustrates the behaviour of the system at maximum output current. The system converges to the desired steady-state output voltage after a brief oscillation, as expected.

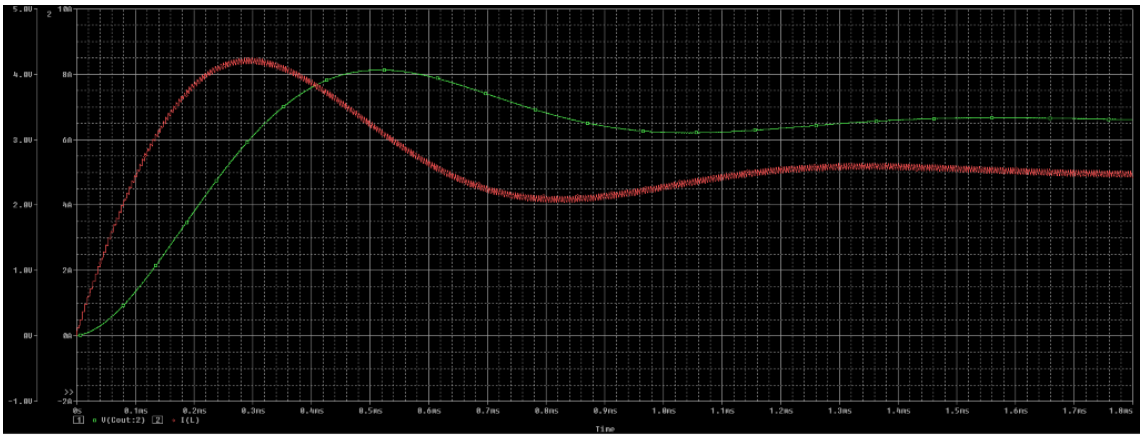


Figure 15: Continuous Conduction

6.1.3 Discontinuous Mode

As shown in *Figure 16,* the converter as it stands will never enter discontinuous conduction as the sync FET is able to conduct in both directions. However, when the current reverses the sync FET will pull current from the output, discharging the capacitor and decreasing the output voltage. This loss in output energy will have to be replaced in the next half cycle, resulting in more power dissipation through the capacitors ESR. This can be avoided by allowing discontinuous conduction operation by either simply disabling the sync FET or using pulse frequency modulation. Operating in discontinuous conduction is beneficial as it avoids the switching and reverse current conduction losses that occur when the inductor current drops below zero [3].

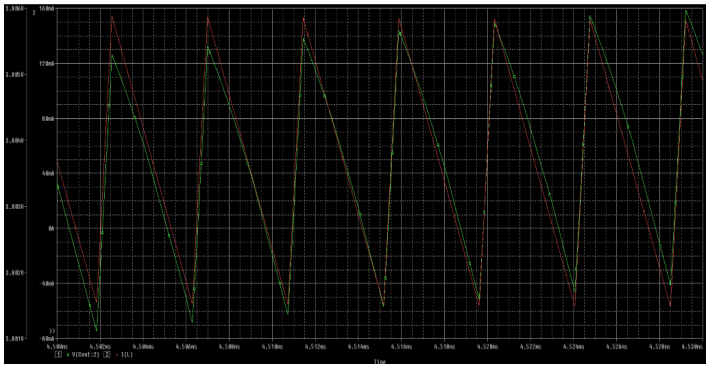


Figure 16: Discontinuous Conduction

6.1.2 Efficiency

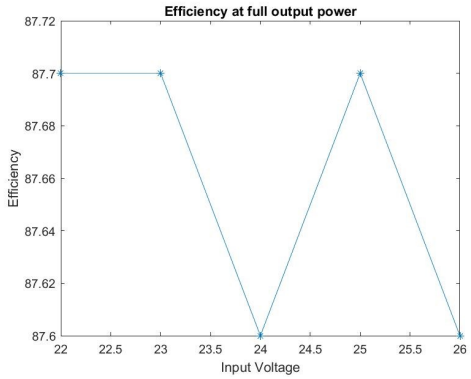


Figure 17: Efficiency vs Input Voltage

The voltage drop across the sync FET and diode is now insignificant, therefore the efficiency will slightly vary with input voltage, as shown in *Figure 17*.

Note that the efficiency still lies below the minimum 90%. This is believed to be due to capacitive current spikes stemming from parasitic capacitances and inductances at the output of the MOSFETs and is shown in *Figure 18.* The phenomenon can cause premature MOSFET activation, resulting in short, but large, current spikes between the two devices. This current has been measured to be approximately 2 *A* during switching, significantly increasing the power losses. The phenomenon was not predicted and hence may require a change in transistor in practice (see Section 4 for considered options).

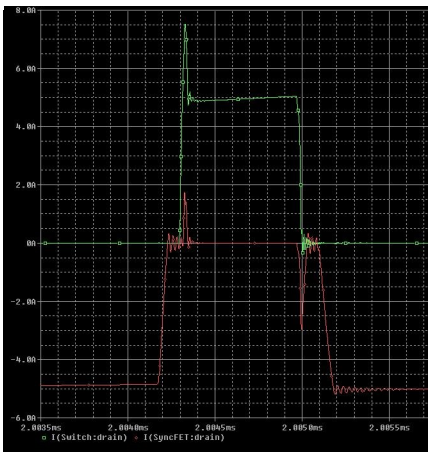


Figure 18: Current Spikes

7. Closed-Loop System

7.1 Compensator Transfer Function Design

Up to now, the configuration designed is realistically undesirable as the output voltage is directly affected by changes in the input voltage and the load. A control system is therefore required to automatically adjust the duty cycle depending on the error between the observed output voltage and the ideal value. This is achieved by closing the loop and introducing a feedback gain *H(s)* and a compensator *C(s).* The design will be based on the following requirements:

- Regulate a fixed output voltage of 3.3 V, regardless of varying input voltage and load
- Reduce any overshoot at turn-on
- Low gain at the switching frequency to avoid amplifying and propagating switching noise

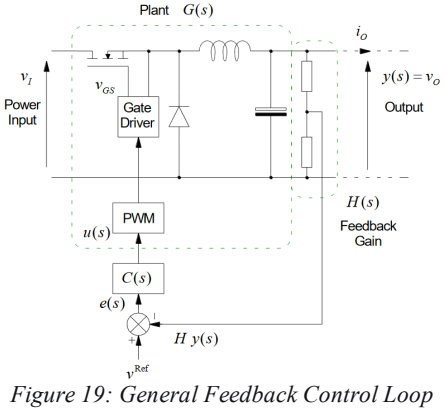


Figure 19: General Feedback Control Loop

The Buck design so far is modelled as the forward plant and is defined with the transfer function stated in Section 5. To observe the stabilising effects of a compensator, the load has been set as $R_{out} = 10\,\Omega$. In this open-loop condition, an overshoot of 50% is observed in addition to a large steady-state error.
A chosen feedback factor $H \approx 0.6061$ results in the controller's input reference to be $V_{ref} = 2\,V$. The following *Figures 20* and *21* respectively show the open loop bode plot and the root locus of the current converter.

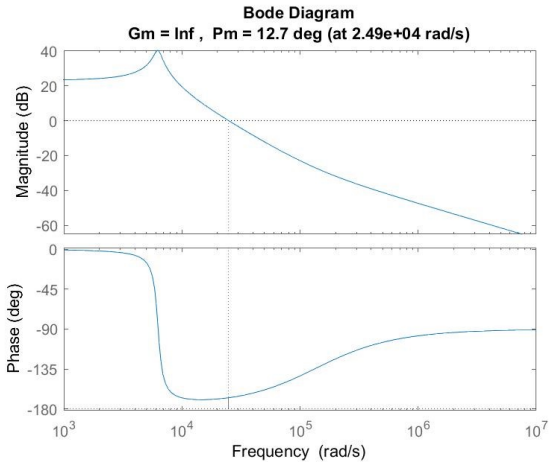


Figure 20: Open Loop Bode Plot

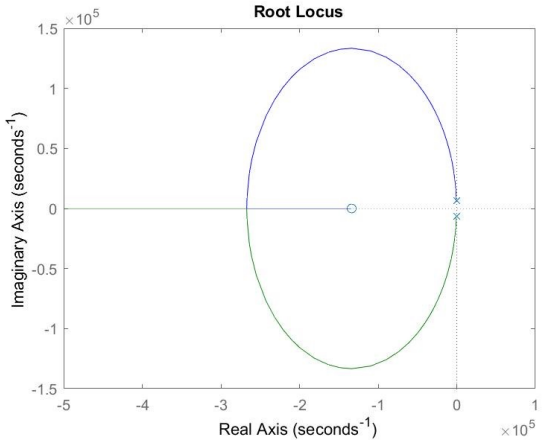


Figure 21: Root Locus Plot

The system is found to have a phase margin of 12.7^0, much lower than desired. Therefore, the compensators contemplated are:

- *Proportional Compensator:* satisfies the low steady-state error but a high gain destabilises the closed-loop
- *Lag Compensator:* introduces a stabilising gain reduction for frequencies above ω_p and a destabilising phase margin between ω_o and ω_p.

$$C_{lag}(s) = K\frac{1+\frac{s}{\omega_o}}{1+\frac{s}{\omega_p}}, \qquad \omega_o > \omega_p$$

- *Lead Compensator:* introduces a destabilising gain increase for frequencies above $\omega_p$and a stabilising positive phase between ω_p and ω_o.

$$C_{lag}(s) = K\frac{1+\frac{s}{\omega_o}}{1+\frac{s}{\omega_p}} \qquad \omega_o < \omega_p$$

The most suitable compensator for the system has been chosen to be the lead compensator, with proportional gain, which is to be followed by a PI controller, which is a special form of lag compensation with the following transfer function.

$$C(s) = K_p\frac{s+\frac{K_i}{K_p}}{s}$$

The lead compensator is necessary to increase the phase margin. The open-loop transfer function contains an unwanted zero at $134\ krads/s$ which is too close to the switching frequency and could cause instability. To mitigate the effects of this zero, the pole of the lead compensator has been designed to match it. However, an extra zero is also added and has been placed at $500\ rad/s$. Although this in turn creates a destabilising gain at a low frequency, the following PI controller will counteract this increasing gain.

$$C_{lead}(s) = K\frac{1+500}{1+134000}$$

To select the optimal values for the PI controller, the MATLAB tool *PID Tuner* has been used. Considering the trade-off between transient robustness and speed, the values selected are $K_p = 50$ and $K_i = 71816$. This places a pole at the origin and a zero at $2393\ rad/s$. To achieve an acceptable overshoot, a proportional gain block has been added with a gain of $K = 0.8$.

The following *Figure 22* shows the bode plot of the compensated closed-loop system.

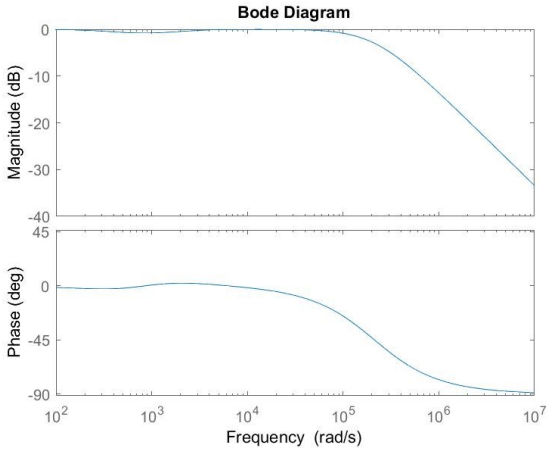


Figure 22: Compensated System Bode Plot

The gain and phase margins are well above the critical stable values and therefore the close-loop system is stable.

7.2 Closed Loop Pspice Model

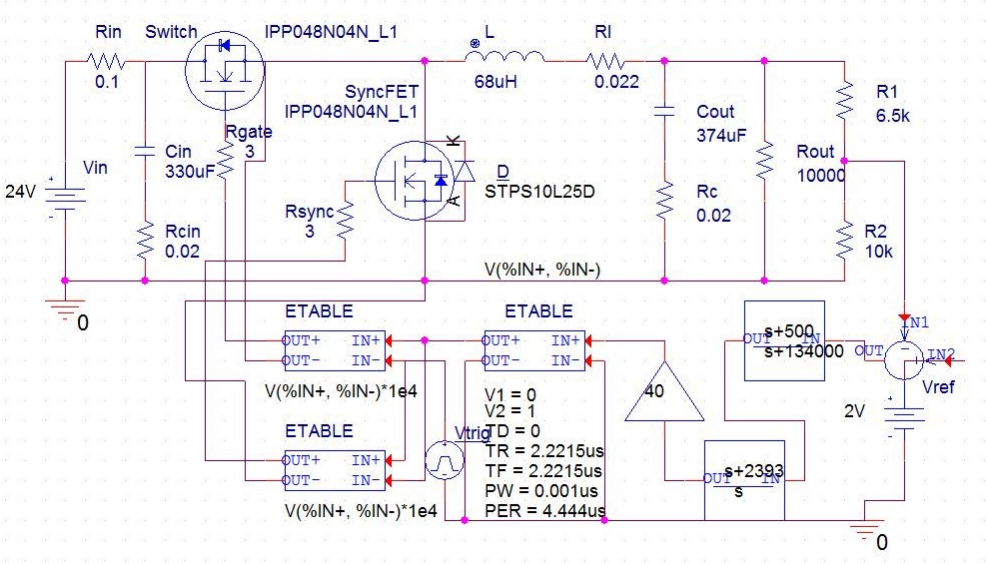


Figure 23: Closed-Loop Design

The PWM circuit compares the error voltage to the output of a triangular wave generator to obtain a square wave signal of variable duty cycle. This is then fed into the gate driver to drive both the high-side and low-side MOSFETs. The triangular wave generator, implemented with a V_{pulse} module in the simulations, will be built using an op-amp square wave generator and an integrator, as shown in *Figure*. The frequency of oscillation is set by the variable input resistor and capacitor and is expressed as $f = \frac{1}{2.1976RC}$. The resistor R_7 in parallel with the feedback capacitor is needed to avoid a saturated output. The comparison between the triangular wave generator and the error signal will be made by a comparator chip instead of a conventional op-amp. Comparators are preferred as they have a much higher slew-rate and an output voltage very close to the supply.

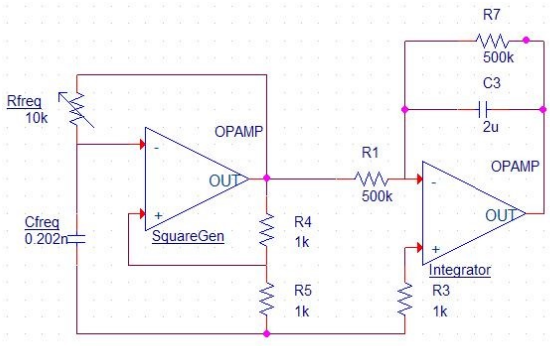


Figure 24: PWM Hardware Implementation

To test the stabilising effect of the compensator, the output load is switched from $R_{out} = 10\ k\Omega$ to $R_{out} = 0.66$ and back at intervals of $4\ ms$ using a switch producing the results displayed in *Figure 25*.

Figure 25:Compensator Response to Load Switches

The compensator senses the change in output voltage, adjusts the duty cycle of the square wave driving the MOSFETs and brings the output voltage back to the rate value. As shown above, the output voltage stabilises after an average settling window of $1\ ms$.

The following *Figure 26* illustrates the systems step response at full output power.

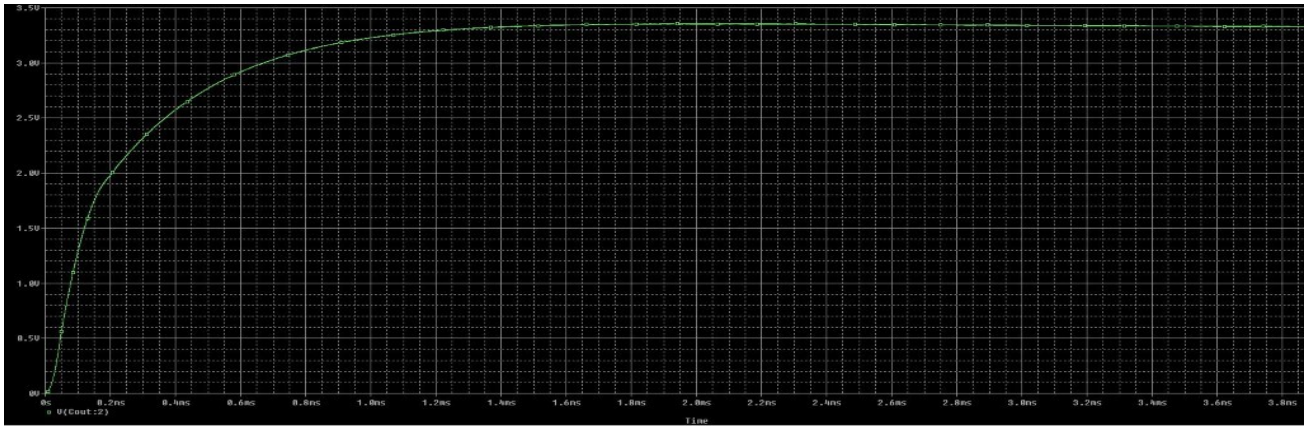


Figure 8: Step Response

8. CONCLUSION

Based on the simulation results and the considerations made in the previous sections, the proposed designed of the Buck SMPS meets all the design specifications except the rated efficiency. In practice, the efficiency is likely to be lower than the predicted value of 87.7% due to the energy consumed by the loop circuitry and the resistance of the PCB tracks. The future design steps include the considerations of techniques to reduce switching losses, and those due to the capacitive current spike phenomenon. If this requires a change of MOSFET, the back-up device will be considered along with other options. Furthermore, analysis of the thermal behaviour of the circuit will be carried out and a choice of a suitable heat sink will be made.

9. APPENDICES

APPENDIX A – CONVERTER SPECIFICATIONS

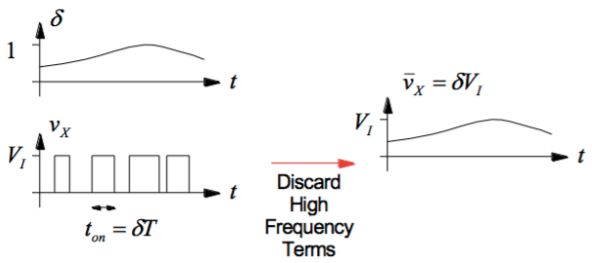
Desired Operational Specifications

Input Voltage	$24\ V(\pm 2\ V)$
Output Voltage	$3.3\ V$ (± 100 mV ripple)
Maximum Output Current	$5\ A$, continuous, resistive loads only
Inductor Ripple Current	Max 5% (peak to peak) at max output power
System Input Ripple Current	$< 100\ mA$ peak to peak
System Frequency	$150\ kHz < f < 250\ kHz$
Efficiency	$> 90\%$ at full load
Maximum Inductor Volume	$10\ cm^3$

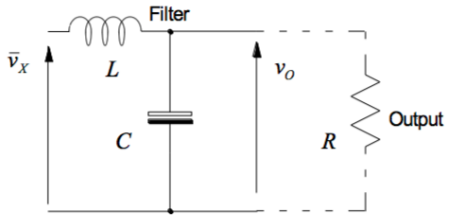
APPENDIX B – TRANSFER FUNCTION

B.1 - DERIVATION

Assuming a constant input voltage, the converter can be considered to have an input voltage of a pulse train with pulses of amplitude V_{in} and a duty cycle δ. $\bar{V}_x$ is the voltage at the output side of the transistor and therefore switches between V_{in} and $-V_{AK}$. Since $-V_{AK}$ does not affect the frequency response of the converter, it can be safely neglected. Therefore, the average voltage over a cycle can be represented as,



$$\bar{V}_x = \frac{t_{on}}{T} V_{in} + \frac{t_{off}}{T}(-V_{AK}) = \frac{t_{on}}{T} V_{in} + \frac{t_{off}}{T}(0) = \delta V_{in}.$$



The output of the converter can be viewed as a simple low-pass filter with a cut-off frequency that only permits DC to pass. Assuming a simple resistive load at the output, the transfer function is found as $\frac{V_{out}(s)}{\bar{V}_x(s)}$.

$$\frac{V_{out}(s)}{\bar{V}_x(s)} = \frac{\frac{1}{sC} // R}{(\frac{1}{sC} // R) + sL} = \frac{1}{1 + s\frac{L}{R} + s^2 LC}$$

B.2 - PREDICTIONS

The transfer function predicts the following parameters:

Overshoot	38.5069%
Rise Time	208.6 µs
Settling Time	2.2 ms
Oscillation Frequency	999.4 Hz.

```
>> L = 61*10^-6;
>> C = 415.3*10^-6;
>> Vin = 24;
>> R = 0.66;
>> buck = tf(Vin, [L*C, L/R, 1]);
>> stepinfo(buck)

ans =

  struct with fields:

        RiseTime: 2.0860e-04
    SettlingTime: 0.0022
     SettlingMin: 20.4404
     SettlingMax: 33.2417
       Overshoot: 38.5069
      Undershoot: 0
            Peak: 33.2417
        PeakTime: 5.3015e-04
```

```
>> syms zeta wn;
>> eq1 = -zeta*wn == -1.82e+03;
>> eq2 = wn*sqrt(zeta^2 - 1) == 6.01e+03i;
>> solution = solve([eq1 eq2]);
>> double(solution.zeta)

ans =

    0.2898

>> double(solution.wn)

ans =

   6.2795e+03
```

APPENDIX C – VALUES W.R.T FREQUENCY SWEEP

f_{switch} [kHz]	L [μH]	C [μF]	Δv_C[μV]
150	101.6	249.3	835.7
175	87.1	290.8	614.1
200	76.2	332.4	470.1
225	67.7	374.2	371.2
250	61.0	415.3	301.0

APPENDIX D – IDEAL NO LOAD SIMULATION

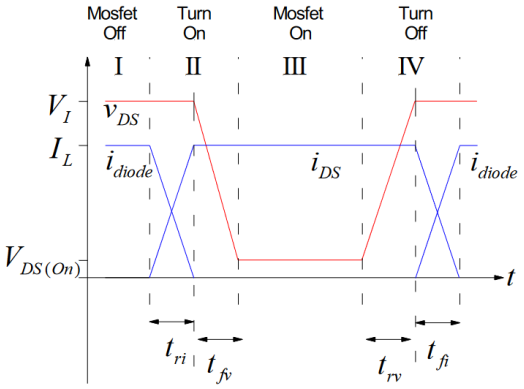
```
>> buck = tf(Vin, [L*C, 0, 1]);
>> damp(buck);

        Pole              Damping       Frequency
                                      (rad/seconds)

  0.00e+00 + 6.28e+03i     0.00e+00       6.28e+03
  0.00e+00 - 6.28e+03i     0.00e+00       6.28e+03
```

APPENDIX E – SWITCHING LOSSES

Switching losses can be analysed using the following equations:



$$E_{cond} = V_{DS} I_L t_{on} = I_{DS}^2 R_{DS}(on) t_{on}$$

$$E_{sw_{on}} = \frac{1}{2} V_I I_L (t_{ri} + t_{fv})$$

$$E_{sw_{off}} = \frac{1}{2} V_I I_L (t_{rv} + t_{fi})$$

$$P_{avg} = \frac{1}{T} (E_{cond} + E_{sw_{on}} + E_{sw_{off}})$$

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