2nd national RISC-V student contest 2021-2022

Sponsored by Thales, the GDR SOC² and the CNFM

Power optimisation of the CV32A6 RISC-V soft-core

You are students and like new challenges.
You are interested in electronics and computer architectures and want to participate in the design of a renowned OpenHW processor core.
Then join this contest and win up to € 5,000!

Context

Thales is a world leader for mission critical information systems for the security, defense, space, aerospace and ground transportation domains. It employs 81,000 people in 68 countries. Following the success of the 1st national RISC-V student contest (2020-2021), Thales Research & Technology France, together with the GDR SOC² and the CNFM, are proud to announce the co-organization of the 2nd edition of the contest (2021-2022). This new contest will focus on the **power optimisation** of the CV32A6 RISC-V soft-core.

RISC-V is a recent open ISA that is gaining every day more attraction. From this ISA, ETH Zürich has designed a mid-range open-source application core named **ARIANE**. It has the capacity to execute rich operating systems and integrates an MMU function and several privilege levels. In 2019, the **OpenHW Group** was created with the ambition to design industrial-grade RISC-V processors. It has integrated the ARIANE core as its new 64-bit application core under the name CV64A6. Thales engineers have created a more compact 32-bit version from the original design, named **CV32A6**. CV32A6 and CV64A6 share the same source code and are together referred to as CVA6.

ARIANE was primarily designed for ASIC targets, i.e. ICs that are synthesized over standard cells. Although the ARIANE source code can be compiled to FPGA matrices, e.g. for prototyping, further optimizations and smart architectural evolutions need to be brought to the design to increase its power efficiency on FPGA targets. That is the focus of this student contest targeting French universities and engineering schools.

Targeted participants

You are a team of 1 to 4 students:

- 1 to 4 **Master 2 students** (or equivalent: final year in engineering schools)[1]
- Registered in a **French engineering school or university**
- Coached by one or several **supervisors** (teachers, assistant professors, professors)
- A PhD student can additionally provide some coaching.

You have the following skills or will get them:

- Digital electronics
- HDL languages
- Digital simulation
- Computing architecture
- Embedded programming
- FPGA design and tools
- Power consumption optimization

The broad timeline of the contest should make it a good fit for your last-year university/school project. You can start a few months after the official kick-off date or submit results weeks or months before the deadline, e.g. before you start an internship.

Description of the contest

Inputs

Thales will prepare a kit composed of:

- A testbench to simulate the **CV32A6**;
- The parameters of the **CV32A6** core to consider;
- Scripts for synthesis and power estimations of the baseline core;
- A BSP;
- A reference design to run the **CV32A6** core on an FPGA development board
- A CNN application to run on the processor core.

The kit will be obtained from a Thales GitHub repository. The repository address will be communicated through the Discord platform (see next section).

You will get support from your university/school and coaching from your supervisor. The organizers (Thales, GDR SOC², CNFM) will remain in contact with the teams and the supervisors.

Communication and support

Supervisors, together with the university/school staff, will provide level 1 support to the team. Level 2 support may only be exercised if the issue cannot be solved at level 1.

A Discord place will be created by the organizers to:

- Communicate announcements and practical information;
- Allow level 2 support;
- Host forums and discussions open to all participants.

The Discord place will log messages so that teams, which will start later, can recover past information. No mailing list will be maintained; all messages will go through Discord after the team is registered. The invitations to the Discord place will be sent when the registration is accepted.

[1] Although the contest does not primarily target M1 students, they are also accepted.

The French language will be used on Discord and during the interim event. Results can be reported in French or English.

Prerequisites

Most parts of CVA6 are written in **SystemVerilog**, a language widely adopted by the industry. You will have to use this language. Students who have followed a VHDL curriculum can for instance follow the Mentor online course (30 days free[2]) to learn SystemVerilog fundamentals or other resources.

The **FPGA development board** selected for this context is the Digilent Zybo Z7-20. The list of necessary material is:

Reference	URL	List price	Remark
Zybo Z7-20	https://store.digilentinc.com/zybo-z7-zynq-7000-arm-fpga-soc-development-board/	$299.00	Zybo Z7-10 is too small for CVA6.
Pmod USBUART	https://store.digilentinc.com/pmod-usbuart-usb-to-uart-interface/	$9.99	Used for the console output
JTAG-HS2 Programming Cable	https://store.digilentinc.com/jtag-hs2-programming-cable/	$59.00	
Connectors	https://store.digilentinc.com/pmod-cable-kit-2x6-pin-and-2x6-pin-to-dual-6-pin-pmod-splitter-cable/	$5.99	At least a 6-pin connector Pmod is necessary; other references may offer it.

The complete set can be ordered by the supervisors from CNFM (contact: fpga@cnfm.fr).

The **Mentor Questa** digital simulator will be needed and supported by Thales. Questa licenses can be obtained through CNFM. As the Questa licence tokens are hosted on a CNFM server, you will likely need support from your IT (e.g. configure a firewall, communicate IP address with CNFM…).

Xilinx Vivado will be used for the synthesis, place & route and for power optimizations. Participants can use evaluation licenses or the Xilinx University Program (XUP).

The kit prepared by Thales will run on Linux.

CAD tools are available in schools/universities through CNFM. For any information, supervisors can get in touch with cao@cnfm.fr.

From last year experience, you should anticipate the provisioning of CAD licences, IT infrastructure and FPGA board to avoid unnecessary delays. The list of CAD tools and the FPGA board are unchanged w.r.t. the previous edition, so that schools/universities having participated last year may have the pre-requisite for this contest.

Work to perform and constraints

Your goal is to increase the **power efficiency** of the CV32A6 core, measured as the energy (Joule) used when running an iteration of the CNN application. The energy will be estimated thanks to the Xilinx Vivado Power Estimator. The guidelines to measure the energy will include the main memory in addition to the memory caches.

Your creativity should prevail as long as these constraints are fulfilled:

- The energy you estimate for the original design is consistent with the estimation performed by the organizer (i.e. we have the same references).
- You do not increase the size of the FPGA design beyond 10%.
- You do not alter the source code of the CNN application
- You do not decrease the application performance (e.g. measured in frames per second).
- You keep the same pipeline depth.
- You do not remove features from the core (MMU, CSR, floating-point operations…).
- Only the CAD tools cited in this document can be used.
- The CNN application can correctly be executed on the modified processor on the FPGA board.

[2] Registration with your university email address.

Outputs

You shall provide:

- A 6-page report presented as a scientific paper, in French or English, with illustrations[3]
- A 10-minute recorded video, that will be presented during the defense session (and during the prize ceremony for the winning teams), in French or English
- A link to your new source code and results uploaded on GitHub (under Apache 2.0 or Solderpad 2.0 licenses)
- The reports from the CAD tools that justify the results presented in the report.

During the course of the contest, the organizers will provide additional instructions with a standardized way to estimate and present results, according to the defined criteria.

Contributions to the OpenHW Group

Thales may promote some of the student open-source contributions to the OpenHW Group. The OpenHW Group criteria for accepting contributions may differ from those used in this contest.

Prizes and jury's criteria

To be eligible for the final selection, your solution must simulate correctly, work on the FPGA board, provide the correct results and fulfill the constraints listed above.

The jury will then **rank the results based on the energy efficiency improvement (performance per watt)** of the solutions compared to the original design delivered in the kit.

Thales will award **€ 5,000** to the winning team and **€ 2,000** to the second best team (both prizes will be shared among the team members).

The winning teams will present their video at an event organized by Thales and/or the GDR SOC². In addition to the prize, they will get a diploma.

Registration

Teams may register anytime between **2021-09-27** and **2022-01-31** and run the contest at their own pace. They will recover past information from the Discord server.

Teams from a same university/school will register separately and can start at different dates.

Teams may deliver their results at any time before the end of the contest (**2021-04-22**). For instance, they can deliver their results in February if students start their internships in March.

To register, the supervisor will send an email to Jérôme Quévremont, Sébastien Pillement and Pascal Benoît (addresses below) with the following details:

- Name of the university/school
- Name of the team[4]
- Supervisor: Name, position (e.g. assistant professor), email address
- For each student: Name, option/major/"filière", email address

The organizers will then check whether the registration is valid and send Discord invitations to the students and the supervisors.

A few additional rules:

- Individual candidates and teams without a supervisor are not accepted.

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[3] An IEEE template is recommended: https://www.ieee.org/conferences/publishing/templates.html.

[4] It is important if several teams from a same university/school register. If only one team registers, it can have the name of its university/school. The team name will be printed on the winners' diploma.

- There may be several teams from a given university/school. A team may include students from different options/majors/"filières".
- A student may not be in more than one team.
- A supervisor may supervise several teams and ensure no co-operation between these teams on their technical solutions. Joint teaching/learning (e.g. SystemVerilog, ISA, architecture courses) is of course accepted and encouraged.
- The supervisor may be replaced during the project.
- Once the team is registered, the list of students shall not change (except under exceptional circumstances, with the organizers' agreement).
- The organizers will consider specific requests (if a situation is not clearly defined in the rules) while maintaining the fairness with other teams.

Abbreviations

ASIC	Application-Specific Integrated Circuit
BSP	Board Support Package
CAD	Computer-Aided Design
CNN	Convolutional Neural Network
FPGA	Field-Programmable Gate Array
HDL	Hardware Description Language
IC	Integrated Circuit
ISA	Instruction Set Architecture
OS	Operating System
RISC	Reduction Instruction Set Computer
M1/M2	Master 1 / Master 2
MMU	Memory Management Unit
TBA	To be announced
XUP	Xilinx University Program

Planning

	Thales	GDR SOC²	CNFM	Teams and universities/schools
September 27th, 2021	Launch the contest			Start registering teams (until 2021-01-31)
Until October 29th, 2021				The teams and their supervisors can anticipate the contest: gaining knowledge on SystemVerilog, computing architectures, RISC-V, CV32A6, power optimization techniques… No support from the organizers during that time
November 2nd , 2021	Deliver the kit as a GitHub repo.			The teams can start later than this date.
November-April	Level 2 support (fix bugs in the kits…)			Run the project. Supervisors provide level 1 support to the student team.
January 18th, 2022 13h-15h	Organize online event: teams' introduction, guidelines to prepare submission, Q&A…			Participate to the event
April 22nd, 2022				**Deadline to submit results (reports, source code…)**. The teams can submit results sooner.
Between May 9th and 13th, 2022	Organize the defense session as online meeting(s)			Attend the defense session: recorded video (10') + live Q&A (5')
June 2022 (TBA)	Final event: prize announcement, presentation by the winning teams			

Contacts

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