milestone1

PC LD AR LD AC LD DR LD TR LD IR LD

x1 x1 x1 x1 x1 x1

WRITE READ

x1 x1

reg
(3b)

128B RAM

A   D

D

str sel ld clr

MUX

AR
ctr
(7b)

0
16 7
extend

0 16
17
extend

AR CLR x1 AR INC x1

ctr
(7b)

0 7
16
extend

7 16
extend

PC CLR x1 PC INC x1

AC

AC
ctr
(16b)

AC CLR x1 AC INC x1

DR

DR
ctr
(16b)

DR CLR x1 DR INC x1

c in
+
c out

TR
ctr
(16b)

TR CLR x1 TR INC x1

AC^DR

E
Q

D en0

IR
ctr
(16b)

IR CLR x1 IR INC x1

BUS

c in
+
c out

MUX

c in
×
c out

c in
×
c out

MUX

ctr
(4b)