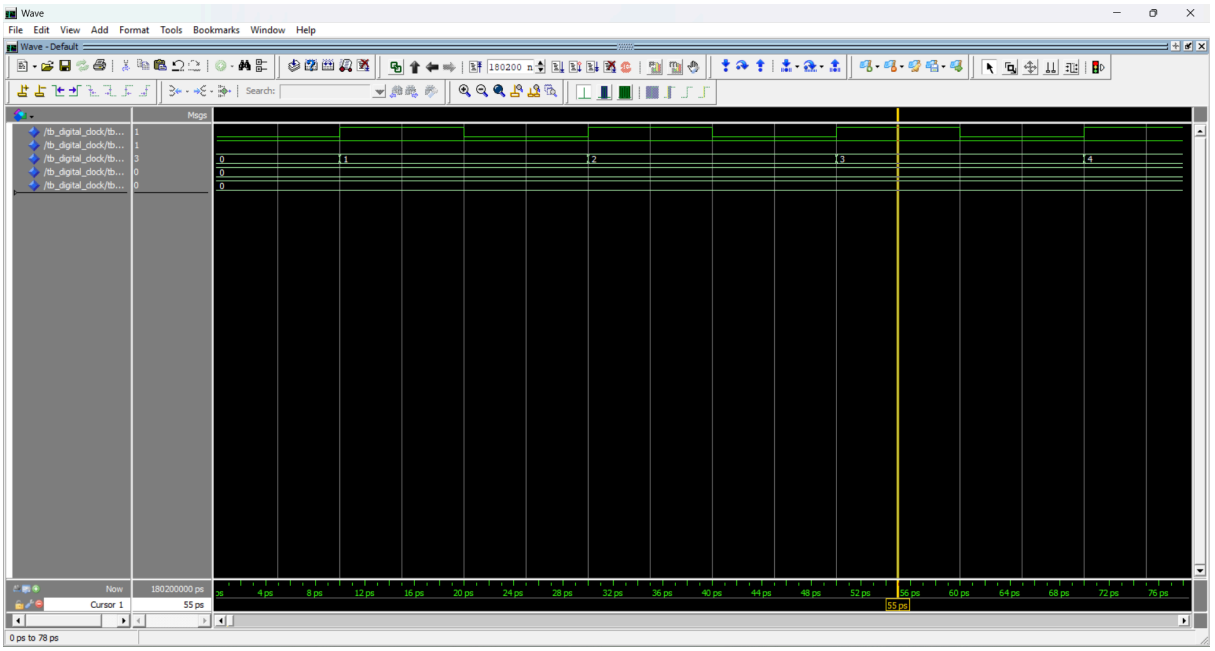
# DSD project team 33

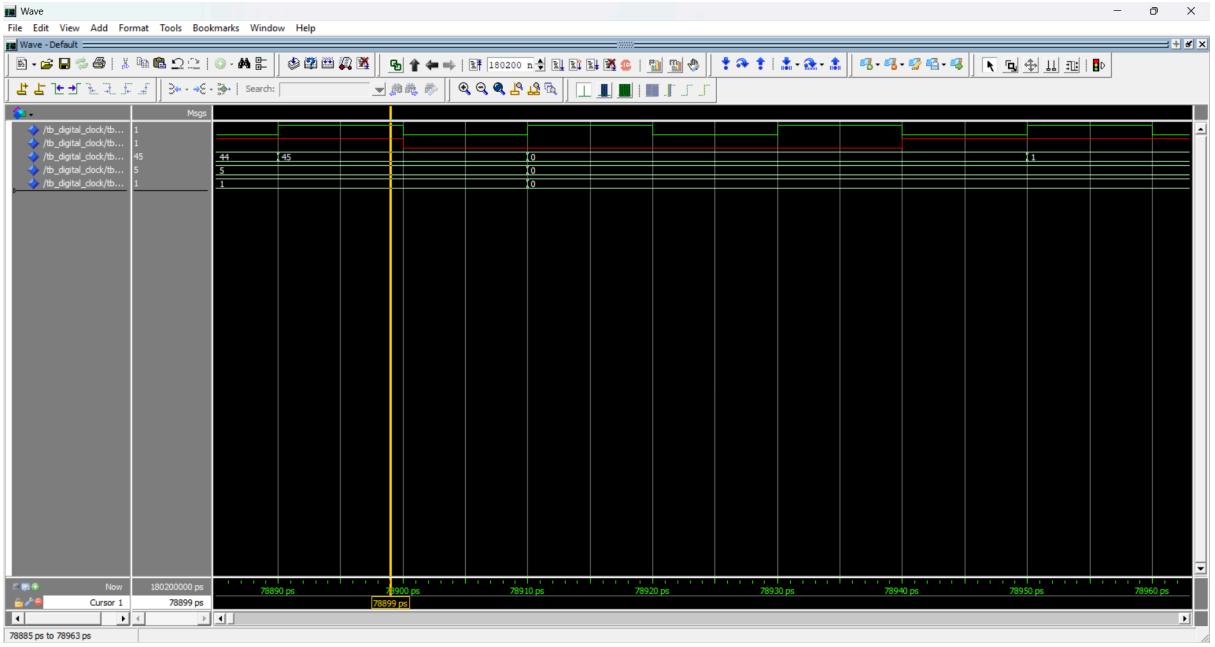



$period = 20ps = 1/50GHz$

## requirement#7:

**You must apply the reset at least once in the testbench, and in the next clock cycle, the clock should continue normally.**

1.before reset




## 2.after reset