2-Day Workshop Plan

VLSI

Day	Time	Activity
Day 1	10:00 AM - 10:45 AM	Introduction to VLSI: What is VLSI? Applications of VLSI, Evolution of VLSI technology, Importance in modern electronics
Day 1	10:45 AM - 11:30 AM	Overview of VLSI Design Flow: System design, Logic design, Circuit design, Layout design, Fabrication
Day 1	11:30 AM - 11:45 AM	Break (15 minutes)
Day 1	11:45 AM - 1:00 PM	CMOS Technology Basics: CMOS inverter, CMOS logic gates, Transistor-level design, Electrical properties of CMOS
Day 1	1:00 PM - 2:00 PM	Lunch Break (1 hour)
Day 1	2:00 PM - 2:45 PM	Logic Design in VLSI: Boolean algebra, Logic gates, Minimization techniques (K-map, Quine-McCluskey method)
Day 1	2:45 PM - 4:00 PM	Hands-On: Implementing Basic Logic Circuits: Designing and simulating simple logic circuits using VLSI design tools
Day 1	4:00 PM - 4:15 PM	Break (15 minutes)
Day 1	4:15 PM - 5:00 PM	Q&A and Day 1 Wrap-Up: Recap of concepts, Discuss tools for VLSI design, Introduction to Day 2

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2-Day Workshop Plan

VLSI

Day	Time	Activity
Day 2	10:00 AM - 10:45 AM	Advanced VLSI Topics: VLSI fabrication process, MOSFET sizing, Parasitic capacitance and resistance, Power dissipation, and performance
Day 2	10:45 AM - 11:30 AM	Timing Analysis and Synchronization: Setup and hold times, Clocking strategies, Timing diagrams, Metastability
Day 2	11:30 AM - 11:45 AM	Break (15 minutes)
Day 2	11:45 AM - 1:00 PM	VLSI Design Tools and CAD: Overview of industry-standard tools (Cadence, Synopsys), Toolchain for synthesis, simulation, and layout
Day 2	1:00 PM - 2:00 PM	Lunch Break (1 hour)
Day 2	2:00 PM - 2:45 PM	Hands-On: Using VLSI Tools for Layout Design: Implementing a layout for a small circuit using CAD tools, DRC and LVS checks
Day 2	2:45 PM - 4:00 PM	Hands-On: Verifying the Design: Running simulations (timing, power), Analyzing results, Troubleshooting design issues
Day 2	4:00 PM - 4:15 PM	Break (15 minutes)
Day 2	4:15 PM - 5:00 PM	Q&A and Final Wrap-Up: Discussion of VLSI design challenges, Certification distribution, Closing remarks

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