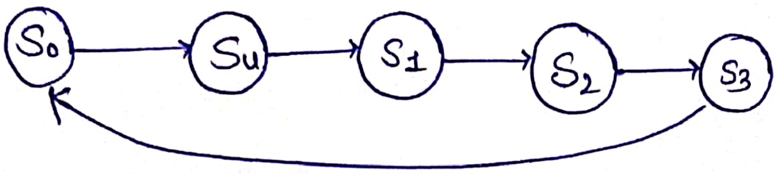
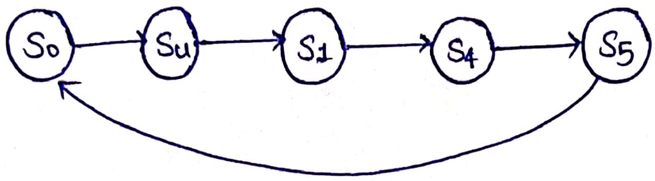
- **Instruction State Flow Diagram:**

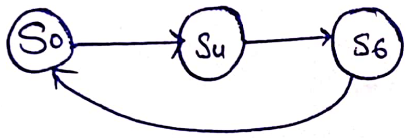
1. **ADD/SUB/MUL/ORA/AND/IMP:**



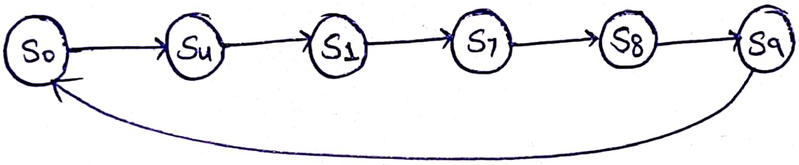
2. **ADI:**



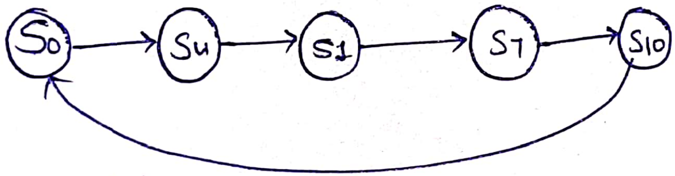
3. **LHI/LLI:**



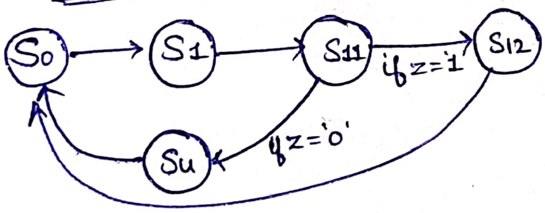
4. **LW:**



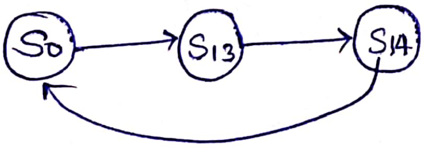
5. **SW:**



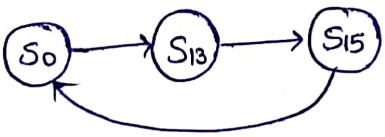
6. **BEQ:**



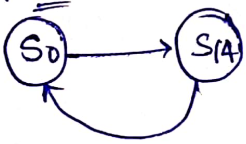
7. **JAL:**



8. **JLR:**



9. **J:**



Dataflow and Control

S0: PC → Mem_address   Mem_read
mem_data → IR   IR-en

Su: PC → ALU_A   ADD(ALU)
+2 → ALU_B
ALU_C → PC   PC_en

S1: IR_{9-11} → RF_A1
IR_{6-8} → RF_A2
RF_D1 → T1   T1-en
RF_D2 → T2   T2-en

- Register file is always readable no enable for read! enable required while writing.

S2: T1 → ALU_A   OPERATION(ALU)
T2 → ALU_B
ALU_C → T3   T3-en
IR_{12-14} → ALU sel

- here OPERATION can be ADD/SUB/MUL/IMP/OR/AND

S3: IR_{3-5} → RF_A3
T3 → RF_D3   RF_en

S4: T1 → ALU_A
IR_{0-5} → SE6 → ALU_B   ADD(ALU)
ALU_C → T3   T3_en

- SE6 is for sign extension of 6bit imm. to 16-bit.

S5: IR_{6-8} → RF_A3
T3 → RF_D3   Af-en

S6: IR_{12} → concat_sel
IR_{9-11} → RF_A3
IR_{0-7} → concat_in   RF_en
concat_out → RF_D3

S_7:

T_2 → ALU_A

IR_{0-5} → SE6 → ALU_B — ADD (ALU)

ALU_C → T3 — T3_en

S_8:

T_3 → Mem_address — Mem_read

mem_data → T_3 — T_3_en

S_9:

T_3 → RF_D3

IR_{9-11} → RF_A3 — RF_en

S_{10}:

T_3 → Mem_address — Mem_write

T_1 → mem_data

S_{11}:

T_1 → ALU_A — SUB(ALU)

T_2 → ALU_B

Z → M1_sel

- M1_sel is the selection line for a MUX which occurs in BEQ split.
- Z is the zero flag, it is 1 if A-B = 0.

S_{12}:

PC → ALU_A — ADD(ALU)

IR_{5-0} → SE6 → 1s → ALU_B

ALU_C → PC — PC-en

- 1s is a left shift operator to multiply imm. with 2.

S_{13}:

IR_{9-11} → RF_A3

PC → RF_D3 — RF-en

S_{14}:

PC → ALU_A

IR_{0-8} → SE9 → 1s → ALU_B

ALU_C → PC

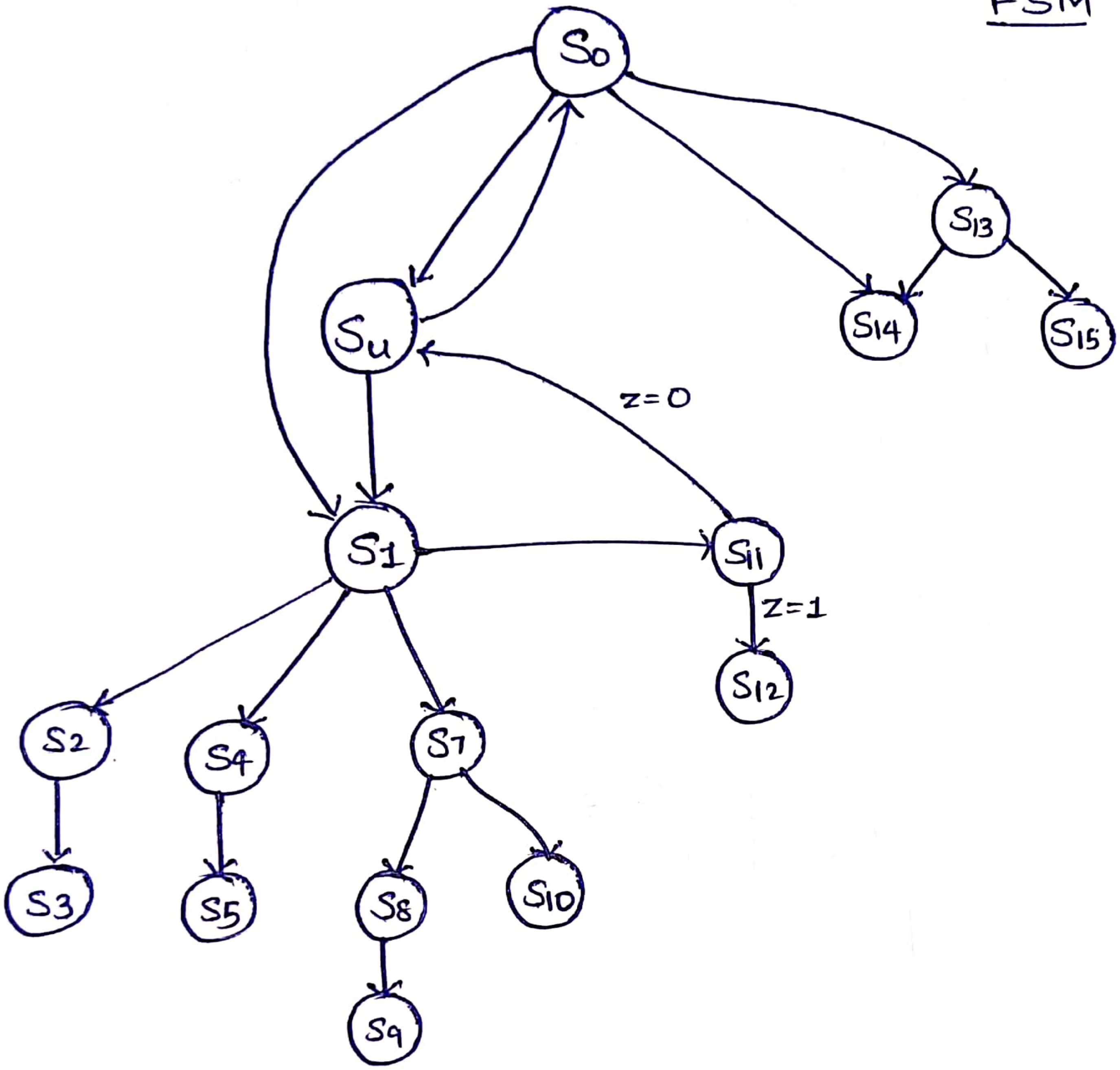
- SE9 is signextender for 9 bit imm. to 16 bits.

S_{15}:

IR_{6-8} → RF_A2 — PC-en

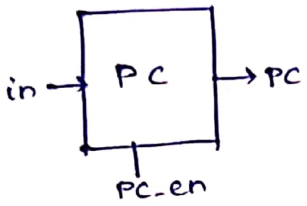
RF_D2 → PC

FSM

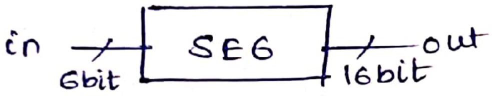


Components

1. Program counter (P.C) : contains the next instruction's pointer. Has an enable pin 'pc-en', PC can be updated only when 'pc-en' is active.

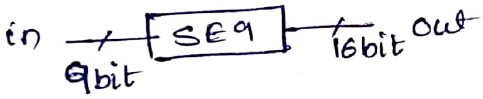


2. SE6 :

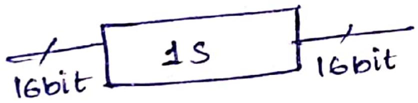


say input is 010000 , output is 0000 0000 0001 0000.

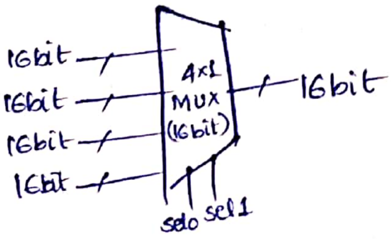
3. SE9 :



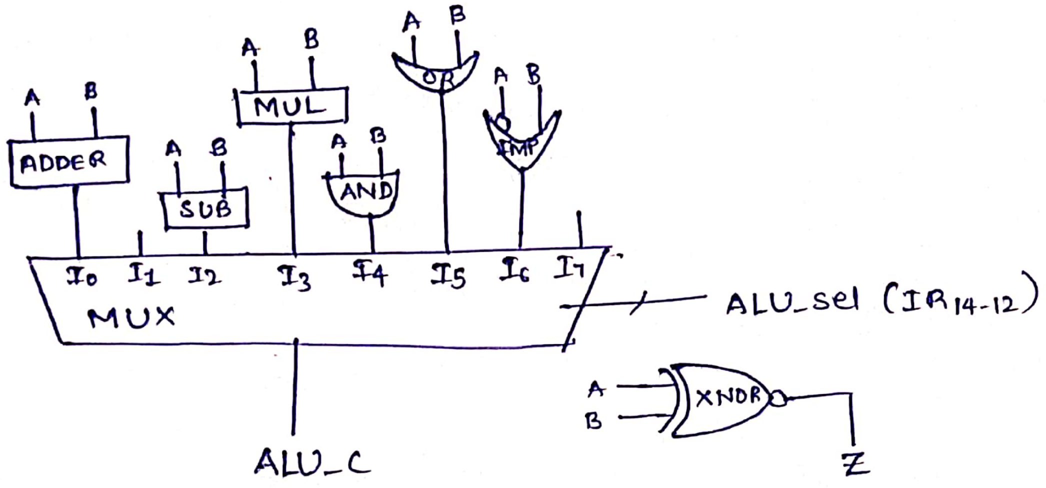
4. 1s : Left shifts the 16bit number to multiply by 2.



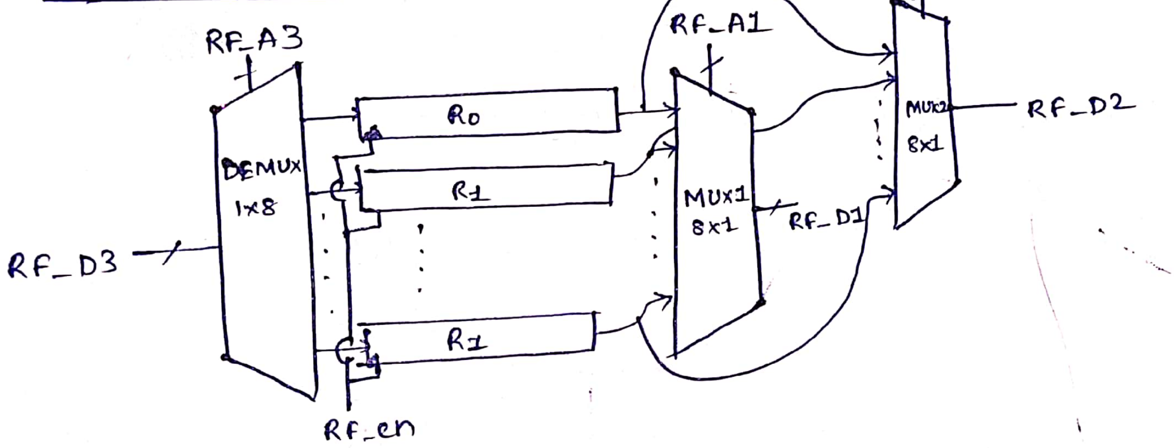
5. Multiple Multiplexers of different orders are going to be used. like a 16bit 4x1 MUX.



6. ALU : This performs ADD,SUM,MUL, AND, ORA, IMP and it has a (Z) zero flag.



7. Register File : (RF)



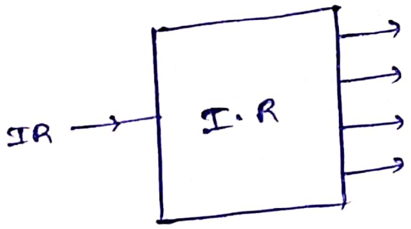
8. FSM : Shown in the diagram.

S0 is the reset state.

S1 → updates PC by adding 2.

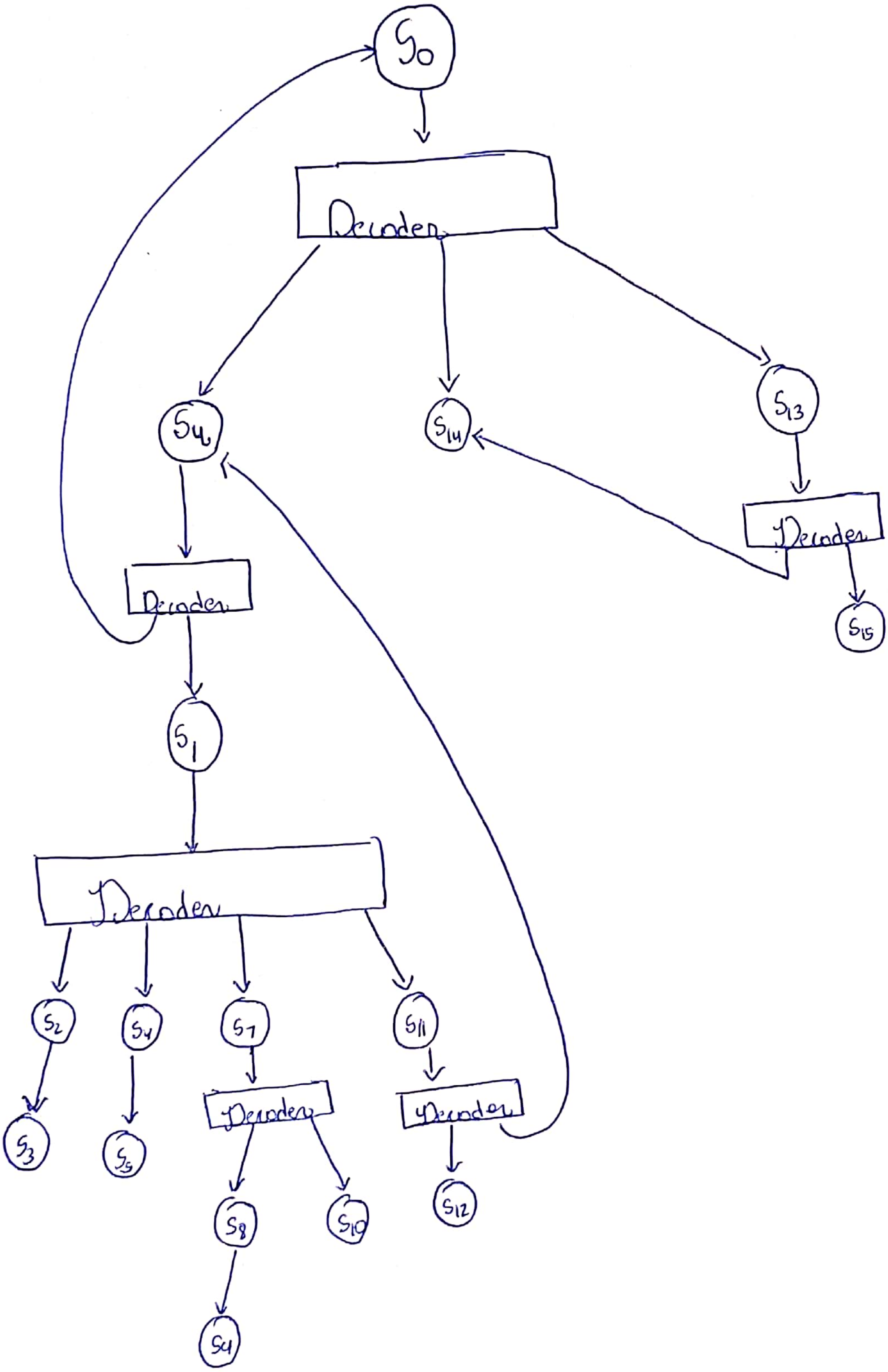
9. Datapath:
Combines all units like ALU, MUXs, RF, PC, IR etc.

10. IR :



Different combinations of the output vectors with diffent dimensions

FSM



S0
Decoder
S4
S14
S13
Decoder
S15
Decoder
S1
Decoder
S2
S4
S7
S11
S3
S5
Decoder
Decoder
S8
S10
S12
S9