EE 671: VLSI DESIGN

Assignment 2: Layout with Magic and LVS Check for CMOS Inverter

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Under the guidance of
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1 Introduction

This assignment focuses on the layout and simulation of CMOS inverters using the **Magic** along with **NGSPICE**. Both the Inverters of strength 1 (INVX1) and strength 2 (INVX2) are laid out in Magic and parasitic extraction (PEX) files have been generated to model parasitics. Also **Netgen** is used for LVS check. Finally, transient analysis is performed to compare rise time, fall time and propagation delays against results from Assignment-01.

2 Circuit Diagram

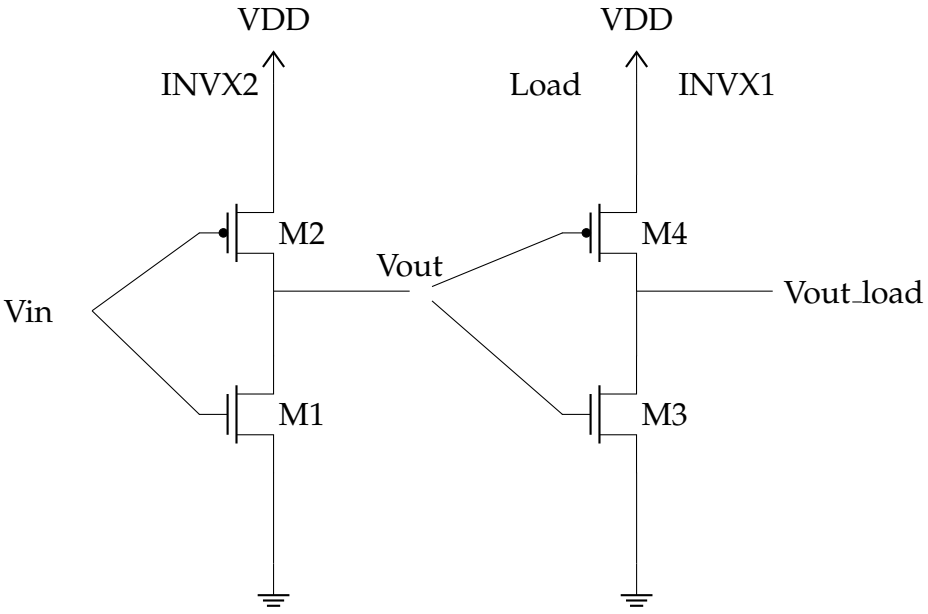


Figure 1: CMOS Inverter Circuit: INVX2 driving INVX1 as load

All files related to this assignment and `Assignment-01` are maintained in this GitHub repository: Yaswanth2747/VLSI-Design.

3 INVX1 Results

3.1 Design Parameters

Table 1: INVX1 Design Parameters

Parameter	Value
PMOS Width (μm)	1.31
PMOS Length (μm)	0.15
NMOS Width (μm)	0.42
NMOS Length (μm)	0.15

3.2 Timing Results

Table 2: Timing Results for INVX1

Parameter	Assignment-02 (PEX)	Assignment-01 (Ideal)
Rise time t_r (ps)	35.35	29.37
Fall time t_f (ps)	32.89	29.43
t_{pHL} (ps)	23.91	23.06
t_{pLH} (ps)	20.19	19.36

3.3 Screenshots for INVX1

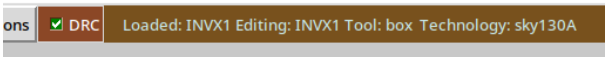


Figure 2: INVX1 DRC

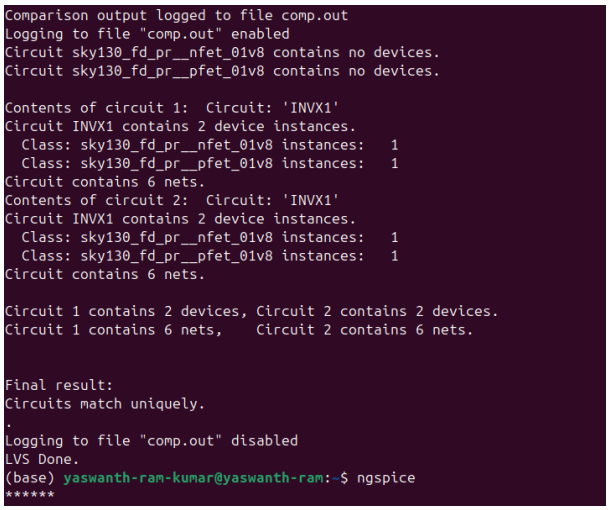


Figure 3: INVX1 LVS

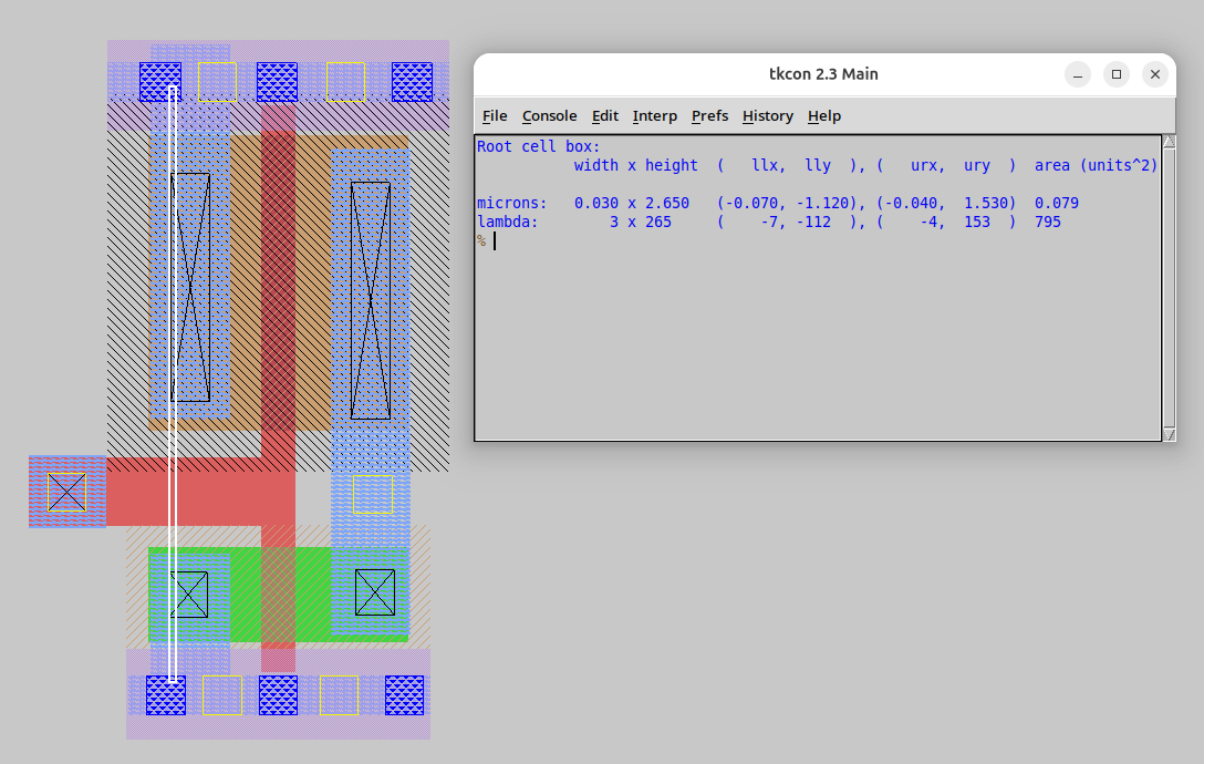


Figure 4: INVX1 Layout - Height $= 2.65\ \mu m$

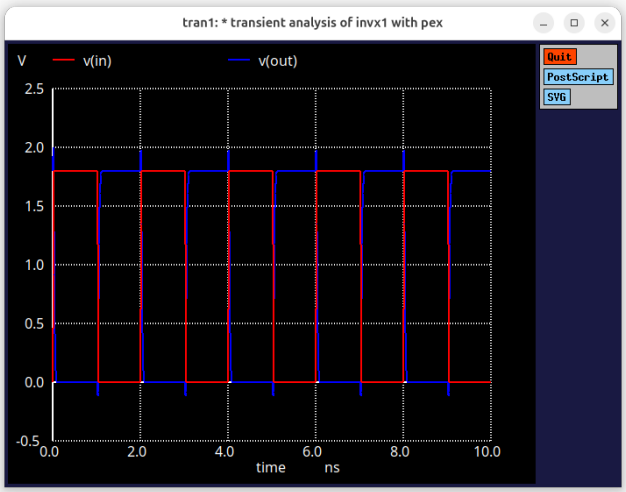
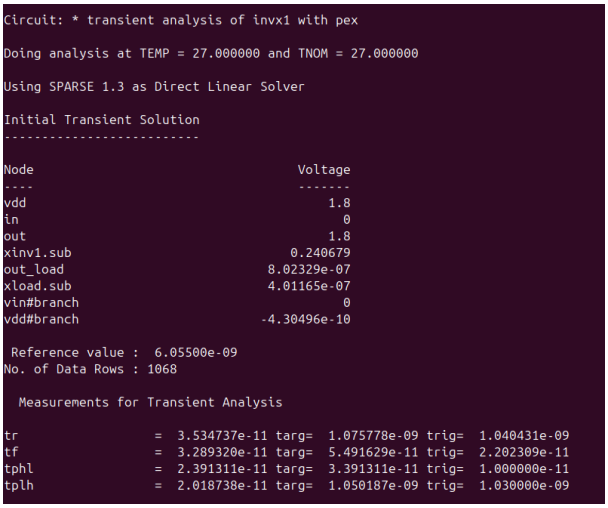


Figure 5: INVX1 Plot



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Circuit: * transient analysis of invx1 with pex

Doing analysis at TEMP = 27.000000 and TNOM = 27.000000

Using SPARSE 1.3 as Direct Linear Solver

Initial Transient Solution
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Node                                   Voltage
----                                   -------
vdd                                        1.8
in                                           0
out                                        1.8
xinv1.sub                             0.240679
out_load                           8.02329e-07
xload.sub                          4.01165e-07
vin#branch                                   0
vdd#branch                        -4.30496e-10

 Reference value :  6.05500e-09
No. of Data Rows : 1068

  Measurements for Transient Analysis

tr                 =  3.534737e-11 targ=  1.075778e-09 trig=  1.040431e-09
tf                 =  3.289320e-11 targ=  5.491629e-11 trig=  2.202309e-11
tphl               =  2.391311e-11 targ=  3.391311e-11 trig=  1.000000e-11
tplh               =  2.018738e-11 targ=  1.050187e-09 trig=  1.030000e-09
```

Figure 6: INVX1 NGSPICE Terminal

4 INVX2 Results

4.1 Device Parameters for INVX2

Table 3: Device Parameters for INVX2

PMOS Width	2.62 µm
PMOS Length	0.15 µm
NMOS Width	0.84 µm
NMOS Length	0.15 µm

4.2 Timing Results

Table 4: Timing Results for INVX2

Parameter	Assignment-02 (PEX)	Assignment-01 (Ideal)
Rise time t_r (ps)	20.91	20.33
Fall time t_f (ps)	20.02	19.25
t_{pHL} (ps)	17.30	17.64
t_{pLH} (ps)	14.71	14.85

4.3 Screenshots

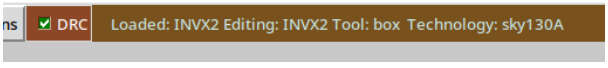

Figure 7: INVX2 DRC

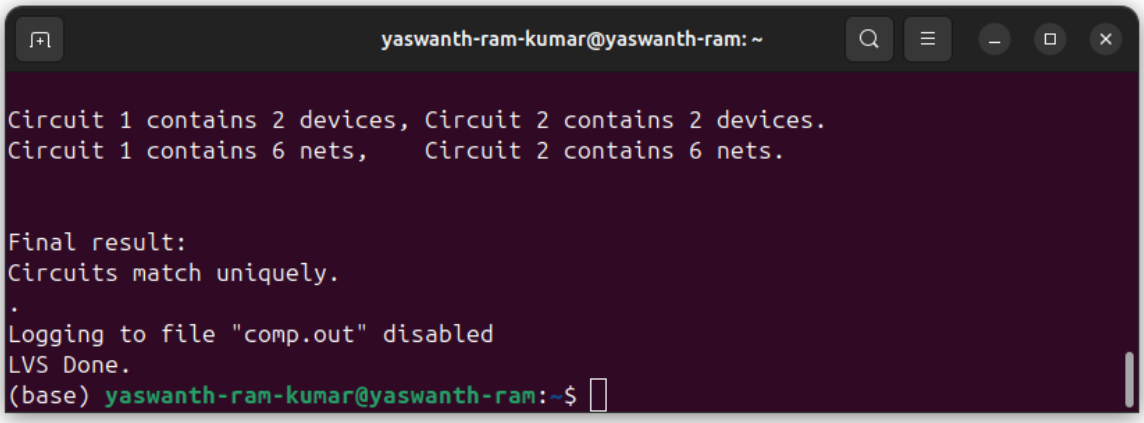

Figure 8: INVX2 LVS

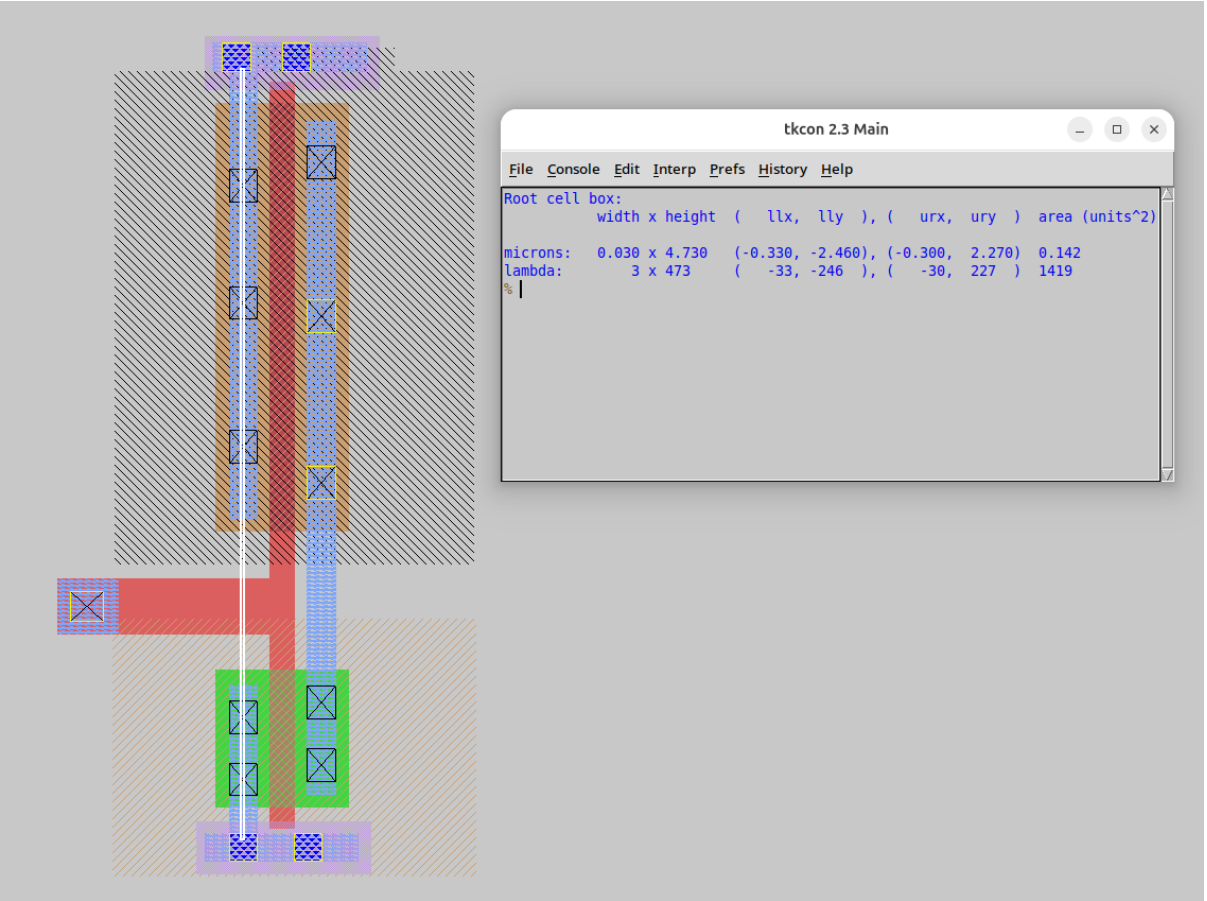

Figure 9: INVX2 Layout - Height $= 4.730\ \mu m$

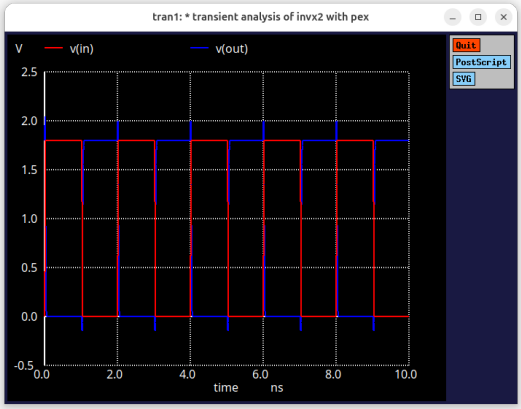

Figure 10: INVX2 Plot

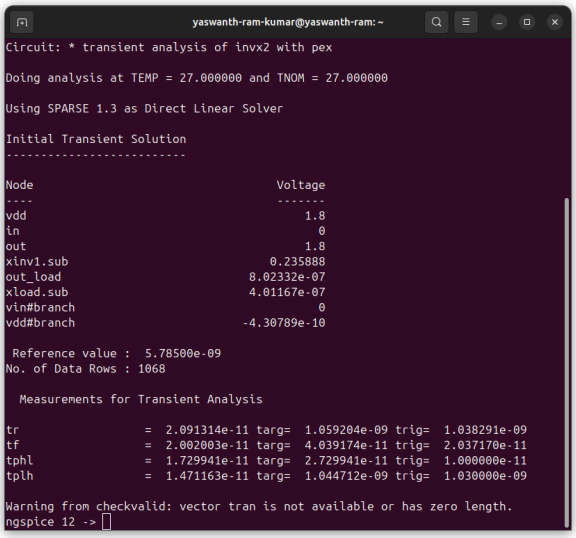

Figure 11: INVX2 NGSPICE Terminal

5 Conclusion

- Both INVX1 and INVX2 layouts are **DRC clean** and **LVS matched**.
- Parasitic effects slightly increase rise/fall times compared to ideal (Assignment-01) results.
- As expected, INVX2 shows better drive strength with reduced delays compared to INVX1.

Thank You

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