EE 671: VLSI DESIGN 2025-2026

Assignment 1: CMOS Inverter Design and Analysis

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1 Introduction

This assignment focuses on the design and simulation of CMOS inverters using the SkyWater 130nm PDK. The primary objectives include designing minimum-size and strength-2 inverters, analyzing their static and dynamic characteristics, and understanding the trade-offs in CMOS inverter design. All simulations were performed using NGSpice with a supply voltage of VDD = 1.8V.

2 Circuit Diagram

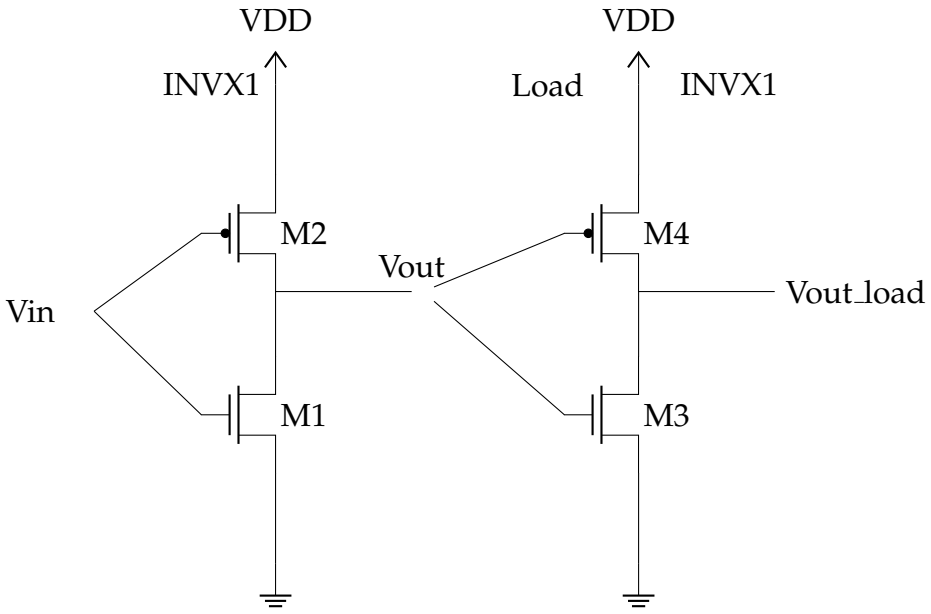

Figure 1: CMOS Inverter Circuit - INVX1 driving another INVX1 as load

Note:

All four code files have been attached at the end of the report, for the DC analysis part of both questions, determining the V_{IL} and V_{IH} was becoming difficult, so the required data of V_{in} vs V_{out} has been saved to a CSV file and from there all the relevant data has been calculated. For Q2, the main inverter is replaced with INVX2 (2× width) while the load remains INVX1, only widths are changed.

3 Methodology

3.1 Design Procedure

3.2 PMOS Width Calculation for Balanced Rise/Fall Times

For equal rise and fall times in a CMOS inverter, the drive strengths of PMOS and NMOS must be balanced. This requires:

$$\frac{\mu_n \cdot W_n}{L_n} = \frac{\mu_p \cdot W_p}{L_p} \tag{1}$$

Where μ_n and μ_p are electron and hole mobilities respectively.
Generally at room temperature:

- $\mu_n \approx 400$ cm^2/V·s (electron mobility)
- $\mu_p \approx 130$ cm^2/V·s (hole mobility)
- Mobility ratio: $\mu_n/\mu_p \approx 3.1$

Since $L_n = L_p = 0.15\mu$m, the width ratio becomes:

$$\frac{W_p}{W_n} = \frac{\mu_n}{\mu_p} \approx 3.1 \tag{2}$$

Therefore: $W_p = 3.1 \times 0.42\mu$m = 1.302μm
Through iterative simulation, $W_p = 1.31\mu$m was selected to achieve:

- tr = 29.37 ps
- tf = 29.43 ps
- Difference = 0.06 ps (well-balanced)

3.3 Source/Drain Area and Perimeter Calculations

Based on the diffusion layout (Figure 2 from assignment):

$$\text{Source/Drain Area:} \quad \text{AS = AD = W} \times 2L_{min} = \text{W} \times 0.3\mu\text{m}^2 \tag{3}$$

$$\text{Source/Drain Perimeter:} \quad \text{PS = PD = 2} \times (\text{W} + 2L_{min}) = 2 \times (\text{W} + 0.3)\mu\text{m} \tag{4}$$

For INVX1: AS = AD = 0.42 × 0.3 = 0.126 μm^2, PS = PD = 2 × (0.42 + 0.3) = 1.44 μm

3.4 Static Characteristics Extraction

The DC transfer characteristics were obtained through voltage sweep analysis:

- **VIL**: Input voltage where output slope = -1 (max noise immunity for logic '1')
- **VIH**: Input voltage where output slope = -1 (max noise immunity for logic '0')
- **VM**: Switching voltage where Vin = Vout (both transistors in saturation)
- **NML**: VIL - VOL (Low-level noise margin)
- **NMH**: VOH - VIH (High-level noise margin)

3.5 Dynamic Characteristics Measurement

Transient analysis with 20ps rise/fall time square wave input:

- **tr, tf**: 10%-90% rise and fall times of output
- **tphl, tplh**: 50% input to 50% output propagation delays

4 Results and Analysis

4.1 Q1: Minimum Size CMOS Inverter (INVX1)

4.1.1 Design Parameters

Table 1: INVX1 Design Parameters

Parameter	Value
PMOS Width (μm)	1.31
PMOS Length (μm)	0.15
NMOS Width (μm)	0.42
NMOS Length (μm)	0.15

4.1.2 Dynamic Characteristics

Table 2: INVX1 Dynamic Characteristics

Parameter	Value (ps)
Rise time, tr	29.37
Fall time, tf	29.43
Propagation delay (tphl)	23.06
Propagation delay (tplh)	19.36
Average propagation delay	21.21

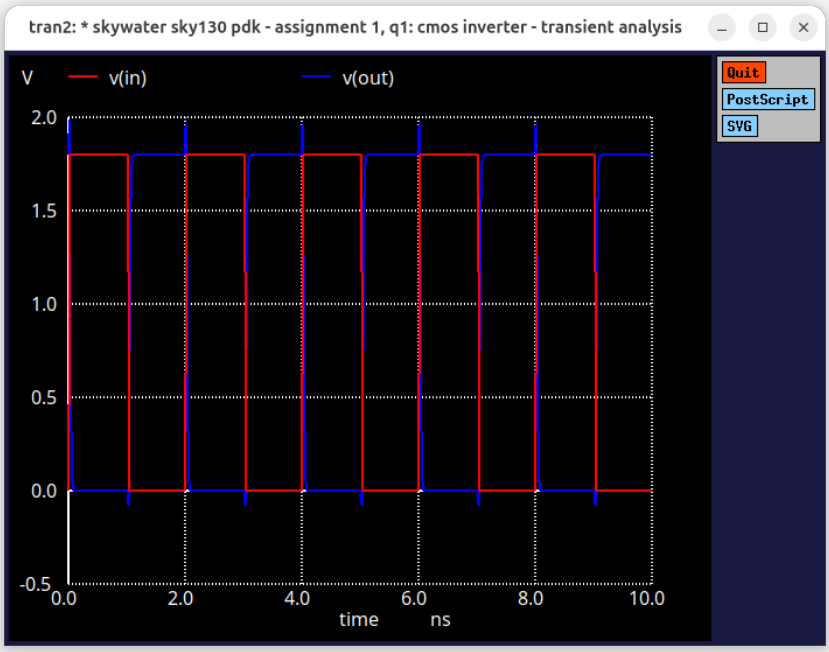

Figure 2: INVX1 Transient Response

4.1.3 Static Characteristics

Table 3: INVX1 Static Characteristics

Parameter	**Value (V)**
VIH	1.012
VIL	0.778
NMH	0.788
NML	0.778
Switching Voltage, VM	0.898
VOH	1.800
VOL	0.000

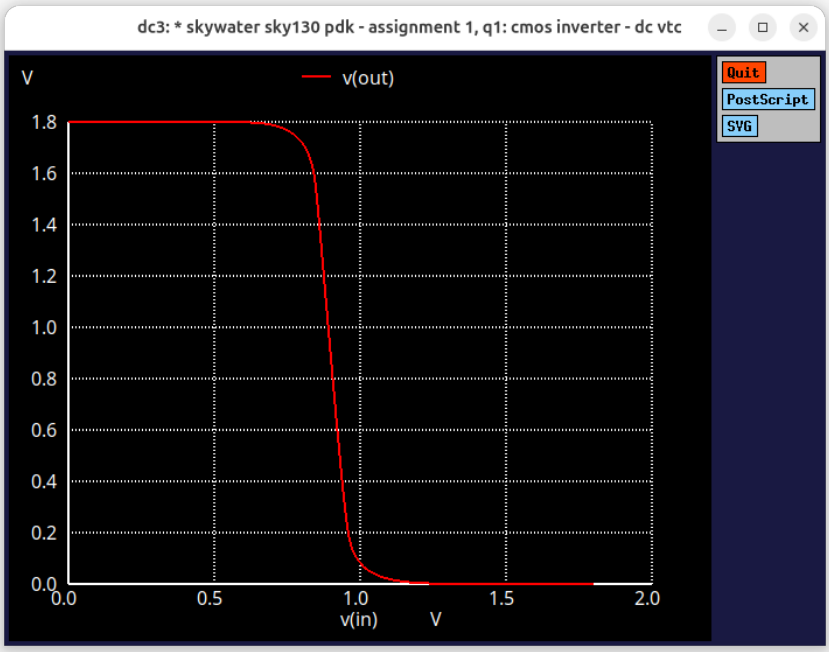

Figure 3: INVX1 DC Transfer Characteristics

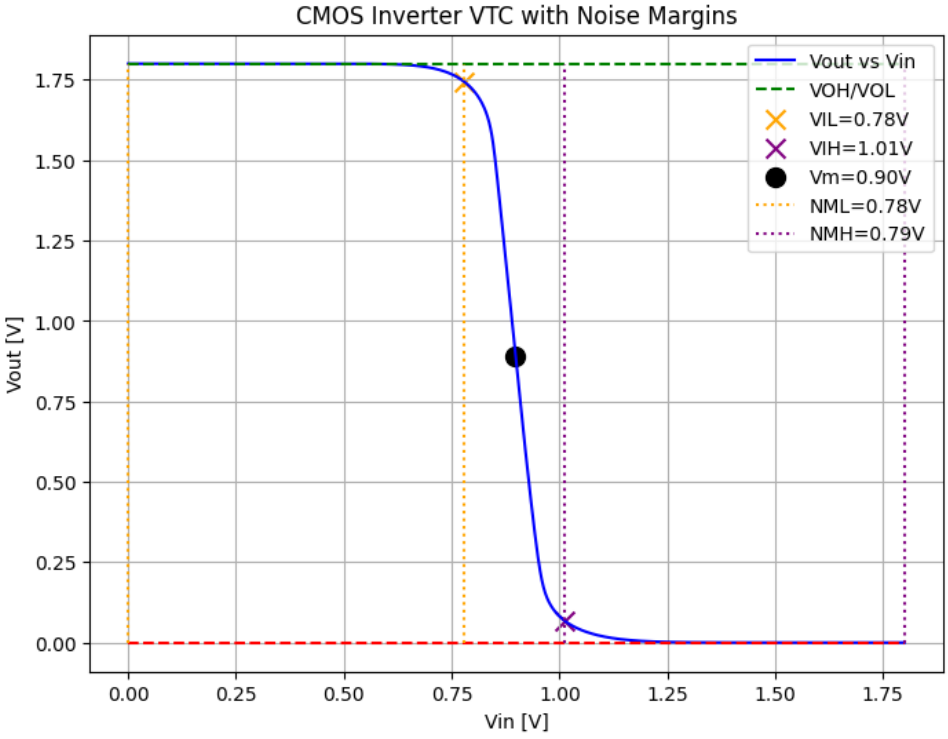

Figure 4: INVX1 Output vs Input Voltage

4.2 Q2: Strength-2 CMOS Inverter (INVX2)

4.2.1 Design Parameters

Table 4: INVX2 Design Parameters

Parameter	Value
PMOS Width (μm)	2.62
PMOS Length (μm)	0.15
NMOS Width (μm)	0.84
NMOS Length (μm)	0.15

4.2.2 Dynamic Characteristics

Table 5: INVX2 Dynamic Characteristics (loaded with INVX1)

Parameter	Value (ps)
Rise time, tr	20.33
Fall time, tf	19.25
Propagation delay (tphl)	17.64
Propagation delay (tplh)	14.85
Average propagation delay	16.25

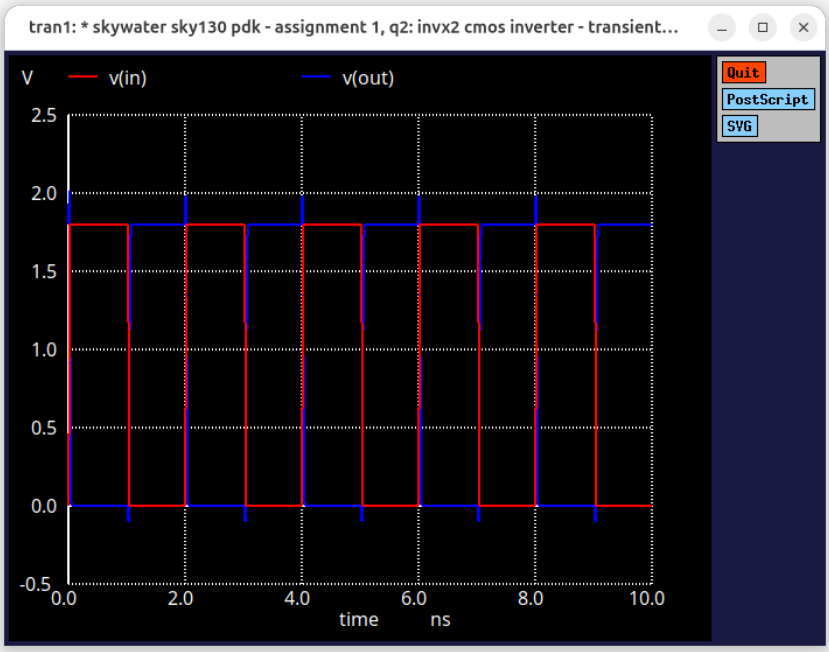

Figure 5: INVX2 Transient Response

4.2.3 Static Characteristics

Table 6: INVX2 Static Characteristics

Parameter	Value (V)
VIH	1.021
VIL	0.770
NMH	0.779
NML	0.770
Switching Voltage, VM	0.896
VOH	1.800
VOL	0.000

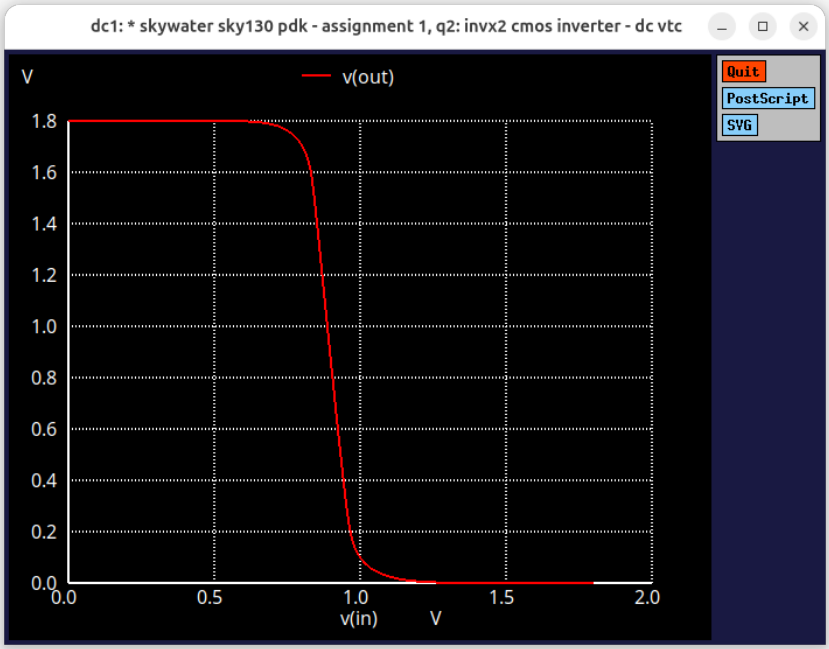

Figure 6: INVX2 DC Transfer Characteristics

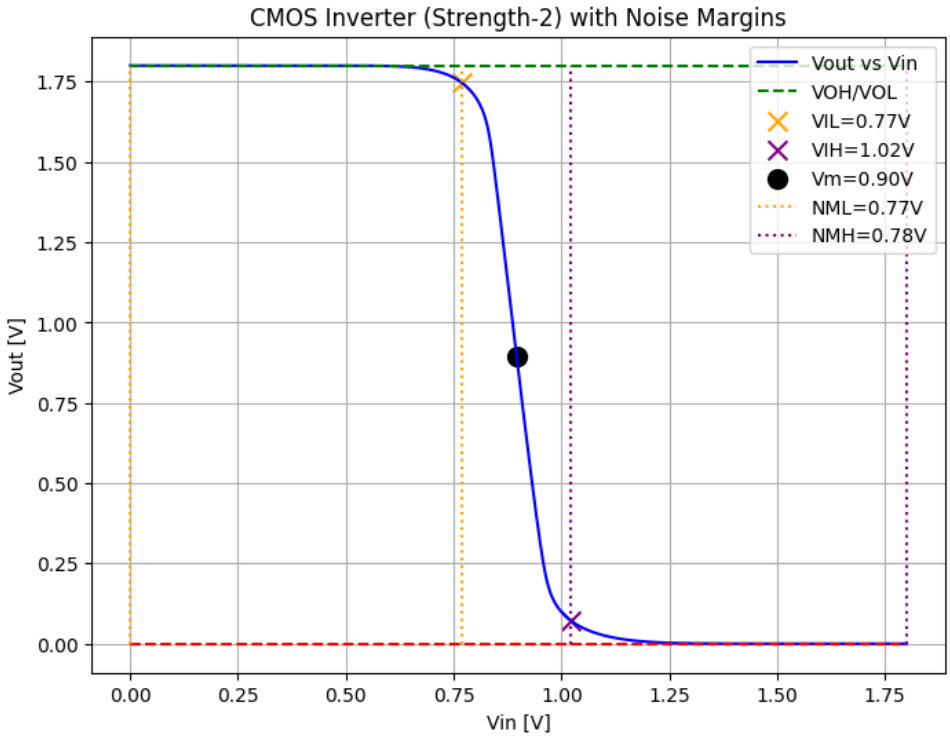

Figure 7: INVX2 Output vs Input Voltage

5 Discussion and Analysis

5.1 Performance Comparison

The strength-2 inverter (INVX2) demonstrates superior dynamic performance compared to the minimum-size inverter:

- **Speed Improvement**: INVX2 shows approximately 23% reduction in average propagation delay (16.25ps vs 21.21ps)
- **Drive Capability**: Faster rise/fall times due to doubled transistor widths providing higher drive current
- **Static Characteristics**: Remain virtually unchanged, confirming proper transistor ratio scaling

5.2 Design Trade-offs

- **Area vs Speed**: INVX2 requires 2× silicon area but provides significant speed improvement
- **Power vs Performance**: Larger transistors increase parasitic capacitances and potentially static power
- **Noise Margins**: Both designs show excellent noise margins (>0.77V), indicating robust operation

6 Conclusion

The simulation results demonstrate the fundamental trade-offs in CMOS inverter design. The minimum-size inverter (INVX1) provides adequate performance with minimal area overhead, while the strength-2 inverter (INVX2) offers improved speed at the cost of increased silicon area. The balanced W/L ratios ensure symmetric switching characteristics and robust noise margins in both designs. These results validate the effectiveness of the SkyWater 130nm PDK for low-power digital circuit applications.

A NGSpice Code Listings

A.1 Q1: INVX1 Transient Analysis

Code Content:

```
* Assignment 1, Q1: CMOS Inverter - Transient Analysis
.lib ~/VLSI_Design/open_pdks/sources/sky130_fd_pr/models/sky130.lib.spice tt
* parameters
.param VDD=1.8
.param Lmin=0.15
.param Wn=0.42
.param Wp=1.31
.param ASn=Wn*0.3
.param ADn=Wn*0.3
.param PSn=2*(Wn+0.3)
.param PDn=2*(Wn+0.3)
.param ASp=Wp*0.3
.param ADp=Wp*0.3
.param PSp=2*(Wp+0.3)
.param PDp=2*(Wp+0.3)
Vdd vdd gnd DC {VDD}
Vin in gnd PULSE(0 {VDD} 0p 20p 20p 1n 2n)

* Main Circuit
Xinv1 in vdd gnd out not1_sub
Xload out vdd gnd out_load not1_sub

* Sub - Ckt Definition
.subckt not1_sub a vdd vss z
* NMOS
XM1 z a vss vss sky130_fd_pr__nfet_01v8 L={Lmin} W={Wn} AS={ASn} AD={ADn} PS={PSn} PD={PDn}
* PMOS
XM2 z a vdd vdd sky130_fd_pr__pfet_01v8 L={Lmin} W={Wp} AS={ASp} AD={ADp} PS={PSp} PD={PDp}
.ends not1_sub
.tran 1ps 10ns 0 10p
.param Vhalf={VDD/2}
.meas tran tr TRIG v(out) VAL='0.1*VDD' RISE=1 TARG v(out) VAL='0.9*VDD' RISE=1
.meas tran tf TRIG v(out) VAL='0.9*VDD' FALL=1 TARG v(out) VAL='0.1*VDD' FALL=1
.meas tran tpHL TRIG v(in) VAL='Vhalf' RISE=1 TARG v(out) VAL='Vhalf' FALL=1
.meas tran tpLH TRIG v(in) VAL='Vhalf' FALL=1 TARG v(out) VAL='Vhalf' RISE=1

.control
run
print tran tr tf tpHL tpLH
print param Wp
plot v(in) v(out)
.endc
.end
```

Listing 1: Q1 INVX1 Transient Analysis

A.2 Q1: INVX1 DC VTC Analysis

```
* Assignment 1, Q1: CMOS Inverter - DC VTC
.lib ~/VLSI_Design/open_pdks/sources/sky130_fd_pr/models/sky130.lib.spice
    tt

* parameters
.param VDD=1.8
.param Lmin=0.15
.param Wn=0.42
.param Wp=1.31
.param ASn=Wn*0.3
.param ADn=Wn*0.3
.param PSn=2*(Wn+0.3)
.param PDn=2*(Wn+0.3)
.param ASp=Wp*0.3
.param ADp=Wp*0.3
.param PSp=2*(Wp+0.3)
.param PDp=2*(Wp+0.3)

Vdd vdd gnd DC {VDD}
Vin in gnd DC 0

* Main Circuit
Xinv1 in vdd gnd out not1_sub
Xload out vdd gnd out_load not1_sub

* Sub - Ckt Definition
.subckt not1_sub a vdd vss z
* NMOS
XM1 z a vss vss sky130_fd_pr__nfet_01v8 L={Lmin} W={Wn} AS={ASn} AD={ADn}
    PS={PSn} PD={PDn}
* PMOS
XM2 z a vdd vdd sky130_fd_pr__pfet_01v8 L={Lmin} W={Wp} AS={ASp} AD={ADp}
    PS={PSp} PD={PDp}
.ends not1_sub

.dc Vin 0 {VDD} 0.001
.control
run
set wr_singlescale
wrdata inverter_vtc.csv v(in) v(out)
plot v(out) vs v(in)
.endc
.end
```

Listing 2: Q1 INVX1 DC VTC Analysis

A.3 Q2: INVX2 Transient Analysis

```
* Assignment 1, Q2: INVX2 CMOS Inverter - Transient Analysis
.lib ~/VLSI_Design/open_pdks/sources/sky130_fd_pr/models/sky130.lib.spice tt
* parameters
.param VDD=1.8
.param Lmin=0.15
.param Wn1=0.42
.param Wp1=1.31   ; INVX1 widths
.param Wn2=0.84
.param Wp2=2.62   ; INVX2 widths = 2 * INVX1
.param ASn1=Wn1*0.3
.param ADn1=Wn1*0.3
.param PSn1=2*(Wn1+0.3)
.param PDn1=2*(Wn1+0.3)
.param ASp1=Wp1*0.3
.param ADp1=Wp1*0.3
.param PSp1=2*(Wp1+0.3)
.param PDp1=2*(Wp1+0.3)
.param ASn2=Wn2*0.3
.param ADn2=Wn2*0.3
.param PSn2=2*(Wn2+0.3)
.param PDn2=2*(Wn2+0.3)
.param ASp2=Wp2*0.3
.param ADp2=Wp2*0.3
.param PSp2=2*(Wp2+0.3)
.param PDp2=2*(Wp2+0.3)
Vdd vdd gnd DC {VDD}
Vin in gnd PULSE(0 {VDD} 0p 20p 20p 1n 2n)
* Main Circuit
Xinv2 in vdd gnd out INVX2_sub
Xload out vdd gnd out_load INVX1_sub
* Sub - Ckt Defn
.subckt INVX1_sub a vdd vss z
XM1 z a vss vss sky130_fd_pr__nfet_01v8 L={Lmin} W={Wn1} AS={ASn1} AD={ADn1} PS={PSn1} PD={PDn1}
XM2 z a vdd vdd sky130_fd_pr__pfet_01v8 L={Lmin} W={Wp1} AS={ASp1} AD={ADp1} PS={PSp1} PD={PDp1}
.ends INVX1_sub
.subckt INVX2_sub a vdd vss z
XM1 z a vss vss sky130_fd_pr__nfet_01v8 L={Lmin} W={Wn2} AS={ASn2} AD={ADn2} PS={PSn2} PD={PDn2}
XM2 z a vdd vdd sky130_fd_pr__pfet_01v8 L={Lmin} W={Wp2} AS={ASp2} AD={ADp2} PS={PSp2} PD={PDp2}
.ends INVX2_sub
.tran 1ps 10ns 0 10p
.param Vhalf={VDD/2}
.meas tran tr TRIG v(out) VAL='0.1*VDD' RISE=1 TARG v(out) VAL='0.9*VDD' RISE=1
.meas tran tf TRIG v(out) VAL='0.9*VDD' FALL=1 TARG v(out) VAL='0.1*VDD' FALL=1
.meas tran tpHL TRIG v(in) VAL='Vhalf' RISE=1 TARG v(out) VAL='Vhalf' FALL=1
.meas tran tpLH TRIG v(in) VAL='Vhalf' FALL=1 TARG v(out) VAL='Vhalf' RISE=1
.control
run
```

```
print tran tr tf tpHL tpLH
print param Wn2 Wp2
plot v(in) v(out)
.endc
.end
```

Listing 3: Q2 INVX2 Transient Analysis

A.4 Q2: INVX2 DC VTC Analysis

```
* Assignment 1, Q2: INVX2 CMOS Inverter - DC VTC
.lib ~/VLSI_Design/open_pdks/sources/sky130_fd_pr/models/sky130.lib.spice
   tt

* parameters
.param VDD=1.8
.param Lmin=0.15
.param Wn1=0.42
.param Wp1=1.31   ; INVX1 widths
.param Wn2=0.84
.param Wp2=2.62   ; INVX2 widths = 2 * INVX1
.param ASn1=Wn1*0.3
.param ADn1=Wn1*0.3
.param PSn1=2*(Wn1+0.3)
.param PDn1=2*(Wn1+0.3)
.param ASp1=Wp1*0.3
.param ADp1=Wp1*0.3
.param PSp1=2*(Wp1+0.3)
.param PDp1=2*(Wp1+0.3)
.param ASn2=Wn2*0.3
.param ADn2=Wn2*0.3
.param PSn2=2*(Wn2+0.3)
.param PDn2=2*(Wn2+0.3)
.param ASp2=Wp2*0.3
.param ADp2=Wp2*0.3
.param PSp2=2*(Wp2+0.3)
.param PDp2=2*(Wp2+0.3)

Vdd vdd gnd DC {VDD}
Vin in gnd DC 0

* Main Circuit
Xinv2 in vdd gnd out INVX2_sub
Xload out vdd gnd out_load INVX1_sub

* Sub - Ckt Defn
.subckt INVX1_sub a vdd vss z
* NMOS
XM1 z a vss vss sky130_fd_pr__nfet_01v8 L={Lmin} W={Wn1} AS={ASn1} AD={ADn1
   } PS={PSn1} PD={PDn1}
* PMOS
XM2 z a vdd vdd sky130_fd_pr__pfet_01v8 L={Lmin} W={Wp1} AS={ASp1} AD={ADp1
   } PS={PSp1} PD={PDp1}
.ends INVX1_sub

.subckt INVX2_sub a vdd vss z
* NMOS
```

```
45 XM1 z a vss vss sky130_fd_pr__nfet_01v8 L={Lmin} W={Wn2} AS={ASn2} AD={ADn2
       } PS={PSn2} PD={PDn2}
46 * PMOS
47 XM2 z a vdd vdd sky130_fd_pr__pfet_01v8 L={Lmin} W={Wp2} AS={ASp2} AD={ADp2
       } PS={PSp2} PD={PDp2}
48 .ends INVX2_sub
49
50 .dc Vin 0 {VDD} 0.001
51 .control
52 run
53 set wr_singlescale
54 wrdata inverter_vtc_invx2.csv v(in) v(out)
55 plot v(out) vs v(in)
56 .endc
57 .end
```

Listing 4: Q2 INVX2 DC VTC Analysis