Standard Cell Library Characterization and Design

Team Number: 16

September 13, 2025

Contents

Chapter 1

Project Overview

1.1 Introduction

This project involves the characterization and design of three standard cells in the standard cell library, including Spice Netlist, layout, LEF, and Verilog views. The goal is to ensure all views are consistent and functional, with performance metrics matching the provided design criteria. The elements that we have designed and characterized include:

- Inverter of Strength 1
- NOR gate of Strength 1
- D-Flip Flop Of Strength 1

1.2 Project Objectives

- Design NGSpice circuit for each cell with the same rise/fall time as inverter 1x or 2x.
- Draw the layout using Magic and ensure zero DRC errors and LVS pass.
- Extract LEF, PEX netlist and perform timing, power, and input capacitance characterizations.
- Create HDL functional definition and validate it using the Icarus Verilog tool.

Chapter 2

Cell 1: INVERTER

2.1 Circuit Diagram

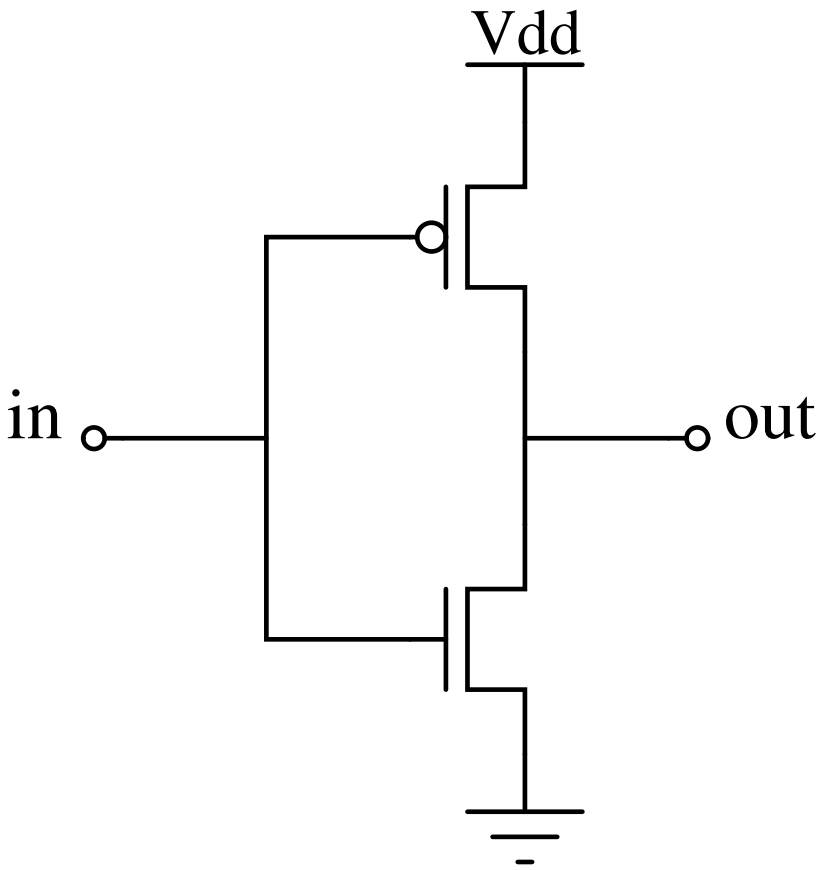


Figure 2.1: Circuit Diagram of Inverter with MOSFETs.

MOSFET	**Width (W)**	**Length (L)**
M1(NMOS)	0.42 μm	0.15 μm
M2(PMOS)	1.26 μm	0.15 μm

Table 2.1: MOSFET Width and Length for Inverter

2.2 Layout

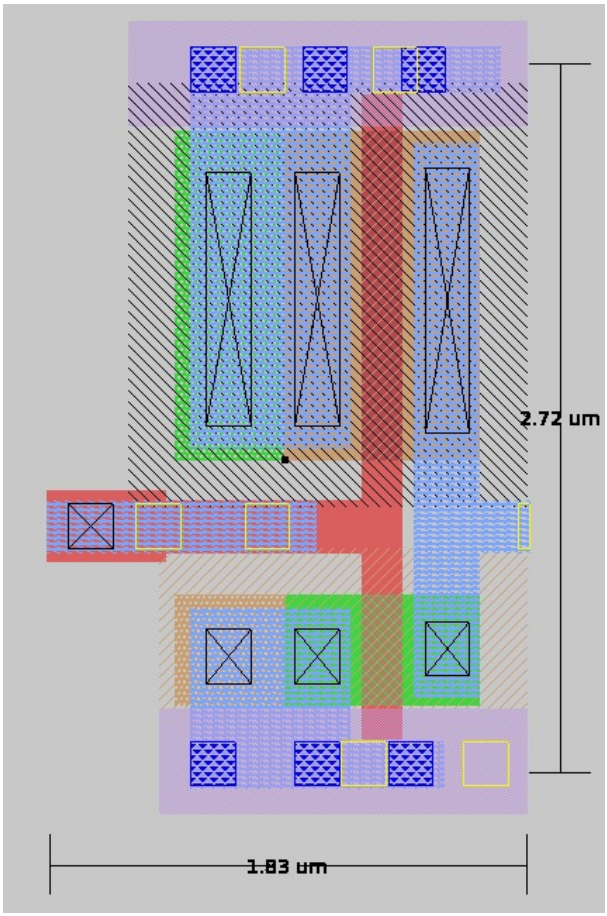


Figure 2.2: Inverter Layout (Width X Height: 1.83 μm x 2.72 μm).

2.2.1 Pex Netlist

```
* NGSPICE file created from INVX1.ext - technology: sky130A

.subckt INVX1 a vdd gnd y
X0 y a vdd vdd sky130_fd_pr__pfet_01v8 ad=0.378 pd=3.12 as=0.378 ps
    =3.12 w=1.26 l=0.15
**devattr s=3780,312 d=3780,312
X1 y a gnd gnd sky130_fd_pr__nfet_01v8 ad=0.126 pd=1.44 as=0.126 ps
    =1.44 w=0.42 l=0.15
**devattr s=1260,144 d=1260,144
C0 a vdd 0.15318f
C1 vdd y 0.12906f
C2 a y 0.03521f
C3 y gnd 0.17987f
C4 a gnd 0.36176f
C5 vdd gnd 0.53259f
.ends
```

2.3 DRC and LVS Results

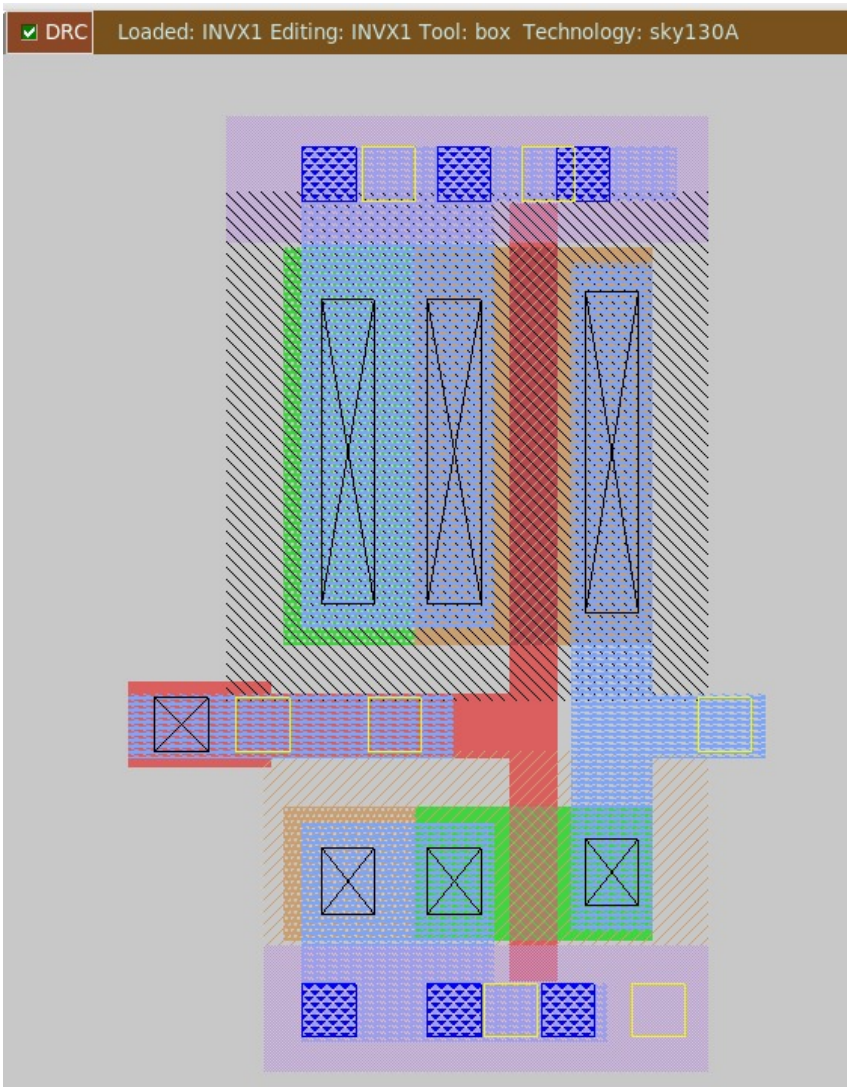


Figure 2.3: DRC Clean Screenshot for Inverter

```
Contents of circuit 1:  Circuit: 'INVX1'
Circuit INVX1 contains 2 device instances.
  Class: sky130_fd_pr__nfet_01v8 instances:   1
  Class: sky130_fd_pr__pfet_01v8 instances:   1
Circuit contains 4 nets.
Contents of circuit 2:  Circuit: 'INVX1'
Circuit INVX1 contains 2 device instances.
  Class: sky130_fd_pr__nfet_01v8 instances:   1
  Class: sky130_fd_pr__pfet_01v8 instances:   1
Circuit contains 4 nets.

Circuit 1 contains 2 devices, Circuit 2 contains 2 devices.
Circuit 1 contains 4 nets,    Circuit 2 contains 4 nets.


Final result:
Circuits match uniquely.
Property errors were found.

The following cells had property errors:
 INVX1

Logging to file "comp.out" disabled
LVS Done.
```

Figure 2.4: LVS Clean Screenshot for Inverter

2.4 Simulation Results

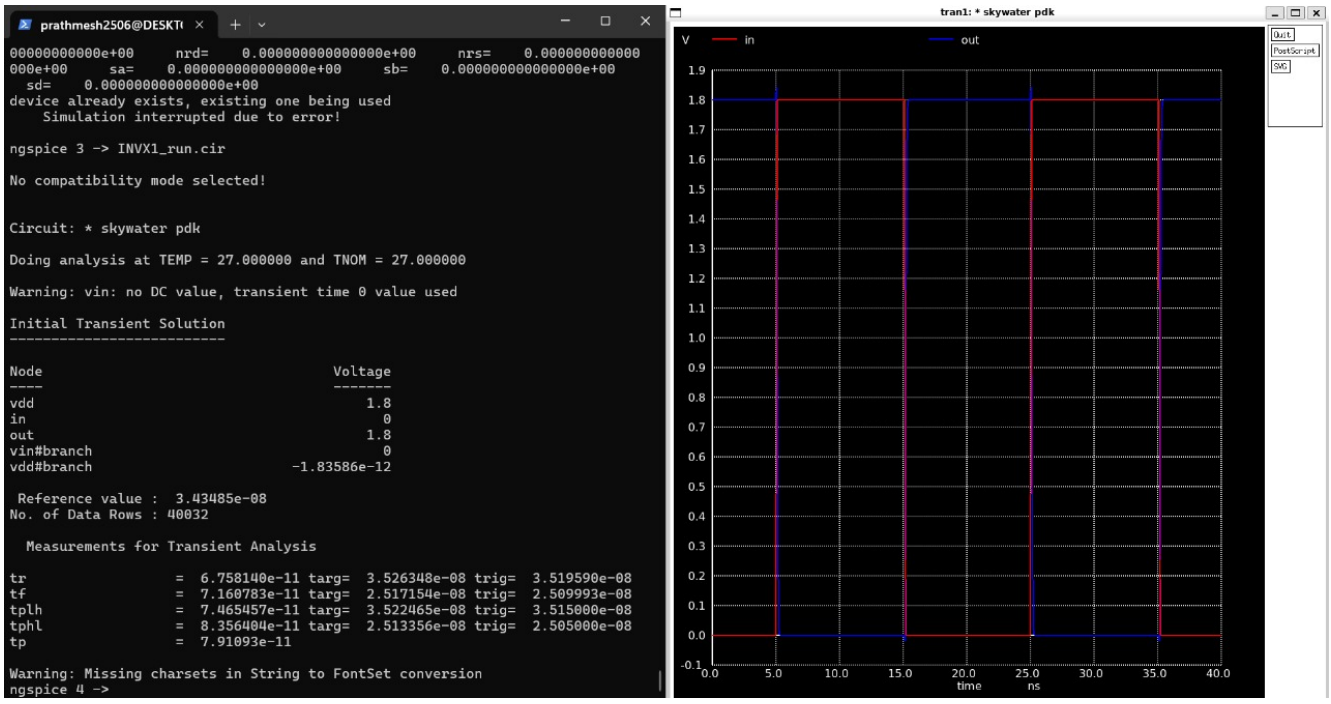


Figure 2.5: Simulation Waveform for Slew Rate of 100 ps and Load Capacitance of 10fF

2.5 Timing and Power Table

2.5.1 Input Pin Capacitances

Input Pin	Rise Cap (pF)	Fall Cap (pF)	Average Cap (pF)
A	1.95e⁻3	8.83e⁻3	5.39e⁻3

Table 2.2: Input pin capacitances for the inverter

2.5.2 Transition Time Table

Output Rise Transitions (in ns) [Input slew vs output capacitance]

Input Slew (ps)	0.5 fF	10 fF	100 fF
10	0.0112	0.0671	0.5974
100	0.0215	0.0675	0.5974
1000	0.0882	0.1824	0.6096

Table 2.3: Output rise transitions for related pin A

Output Fall Transitions (in ns) [Input slew vs output capacitance]

Input Slew (ps)	0.5fF	10fF	100fF
10	0.0115	0.0716	0.6405
100	0.0192	0.0716	0.6405
1000	0.0788	0.1736	0.6472

Table 2.4: Output fall transitions for related pin A

2.5.3 Propagation Delay Time Table

Cell Rise Delay (in ns) [Input slew vs output capacitance]

Input Slew (ps)	0.5fF	10fF	100fF
10	0.0133	0.0522	0.4140
100	0.0309	0.0746	0.4368
1000	0.0746	0.2168	0.6667

Table 2.5: Cell rise delay for related pin A

Cell Fall Delay (in ns) [Input slew vs output capacitance]

Input Slew (ps)	0.5fF	10fF	100fF
10	0.0171	0.0641	0.4999
100	0.0325	0.0835	0.5202
1000	0.0702	0.2126	0.7259

Table 2.6: Cell fall delay for related pin A

2.5.4 Static Power Table

Condition (A)	Power (nW)
0	3.294e^{-}3
1	108.6e^{-}3

Table 2.7: Static power table for inverter

2.5.5 Dynamic Power Table

Rise Power (in nW) [Input slew vs output capacitance]

Input Slew (ps)	0.5fF	10fF	100fF
10	359224	390483	396940
100	83467	209612	236172
1000	17838	68202	197730

Table 2.8: Rise power for related pin A

Fall Power (in nW) [Input slew vs output capacitance]

Input Slew (ps)	0.5fF	10fF	100fF
10	235086	177093	163881
100	30042	21771	16137
1000	3060	2646	2142

Table 2.9: Fall power for related A

Chapter 3

Cell 2: NOR3B

3.1 Circuit Diagram

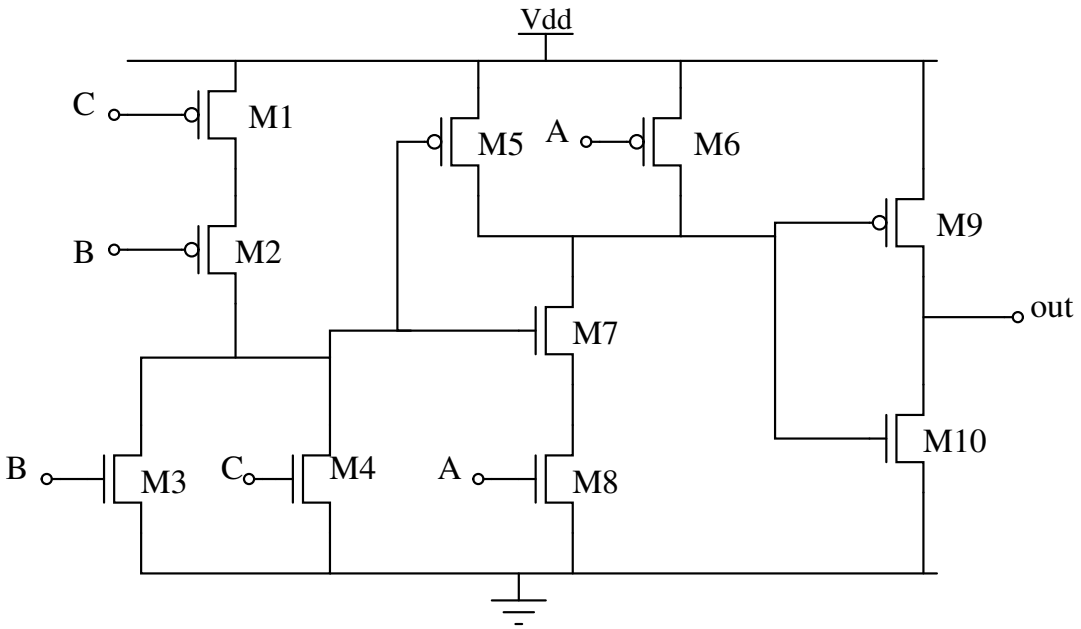


Figure 3.1: Circuit Diagram of NOR3B Circuit with MOSFETs.

MOSFET	Width (W)	Length (L)
M1 (PMOS)	2.52 μm	0.15 μm
M2 (PMOS)	2.52 μm	0.15 μm
M3 (NMOS)	0.42 μm	0.15 μm
M4 (NMOS)	0.42 μm	0.15 μm
M5 (PMOS)	0.63 μm	0.15 μm
M6 (PMOS)	0.63 μm	0.15 μm
M7 (NMOS)	0.42 μm	0.15 μm
M8 (NMOS)	0.42 μm	0.15 μm
M9 (PMOS)	1.26 μm	0.15 μm
M10 (NMOS)	0.42 μm	0.15 μm

Table 3.1: MOSFET Width and Length for NOR

3.2 Layout

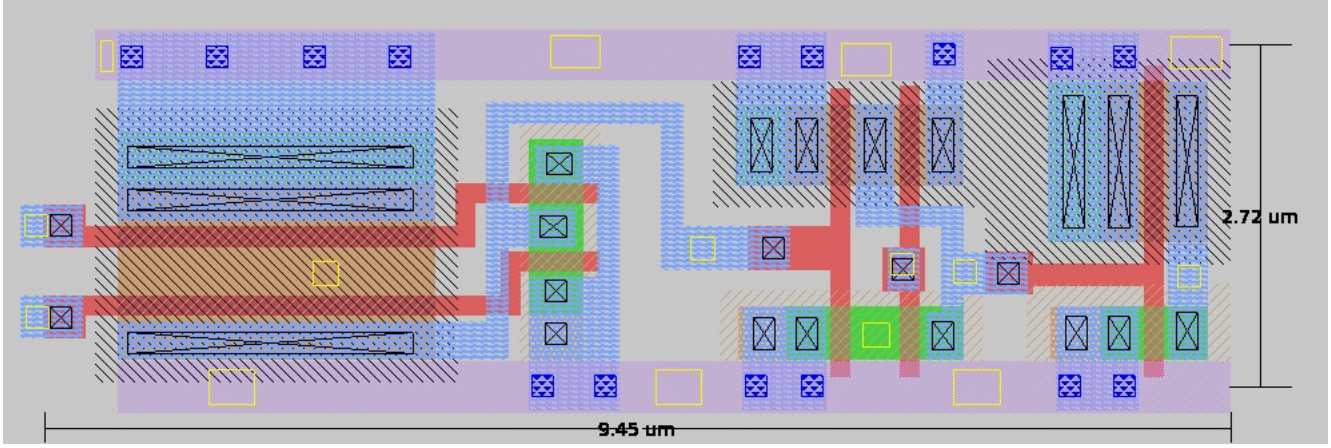


Figure 3.2: NOR3B Layout (Width X Height: 9.45 μm x 2.72 μm).

3.3 PEX Netlist

Listing 3.1: PEX Netlist for NOR3B Gate

```
1 * NGSPICE file created from NOR3B.ext - technology: sky130A
2 .subckt NOR3B A B C vdd gnd out
3 X0 y1 a n gnd sky130_fd_pr__nfet_01v8 ad=0.147 pd=1.54 as=0.084 ps=0.82
     w=0.42 l=0.15
4 X1 n y0 gnd gnd sky130_fd_pr__nfet_01v8 ad=0.084 pd=0.82 as=0.147 ps
    =1.54 w=0.42 l=0.15
5 X2 out y1 gnd gnd sky130_fd_pr__nfet_01v8 ad=0.147 pd=1.54 as=0.147 ps
    =1.54 w=0.42 l=0.15
6 X3 vdd b m vdd sky130_fd_pr__pfet_01v8 ad=0.882 pd=6.44 as=0.504 ps
    =2.92 w=2.52 l=0.15
7 X4 gnd b y0 gnd sky130_fd_pr__nfet_01v8 ad=0.147 pd=1.54 as=0.084 ps
    =0.82 w=0.42 l=0.15
8 X5 vdd a y1 vdd sky130_fd_pr__pfet_01v8 ad=0.2205 pd=1.61 as=0.126 ps
    =1.03 w=0.63 l=0.15
```

```
X6 y0 c gnd gnd sky130_fd_pr__nfet_01v8 ad=0.084 pd=0.82 as=0.147 ps
   =1.54 w=0.42 l=0.15
X7 out y1 vdd vdd sky130_fd_pr__pfet_01v8 ad=0.441 pd=3.22 as=0.441 ps
   =3.22 w=1.26 l=0.15
X8 y1 y0 vdd vdd sky130_fd_pr__pfet_01v8 ad=0.126 pd=1.03 as=0.2205 ps
   =1.61 w=0.63 l=0.15
X9 m c y0 vdd sky130_fd_pr__pfet_01v8 ad=0.504 pd=2.92 as=0.882 ps=5.74
    w=2.52 l=0.15
C0 c y0 0.07696f
C1 vdd y0 0.32438f
C2 b y0 0.0505f
C3 vdd c 0.0574f
C4 y1 y0 0.02332f
C5 b c 0.07795f
C6 y1 c 0
C7 a y0 0.06473f
C8 m y0 0.03568f
C9 out c 0
C10 b vdd 0.1077f
C11 y1 vdd 0.29943f
C12 n vdd 0.0011f
C13 y1 b 0
C14 a vdd 0.057f
C15 m vdd 0.03527f
C16 y1 n 0.00608f
C17 a y1 0.09435f
C18 a n 0.00114f
C19 out vdd 0.11829f
C20 out b 0
C21 out y1 0.03716f
C22 out a 0
C23 n gnd 0.00737f
C24 out gnd 0.16433f
C25 c gnd 0.29119f
C26 m gnd 0.01504f
C27 b gnd 0.26283f
C28 a gnd 0.16987f
C29 y0 gnd 1.00737f
C30 y1 gnd 0.41423f
C31 vdd gnd 2.34133f
.ends
```

3.4 DRC and LVS Results

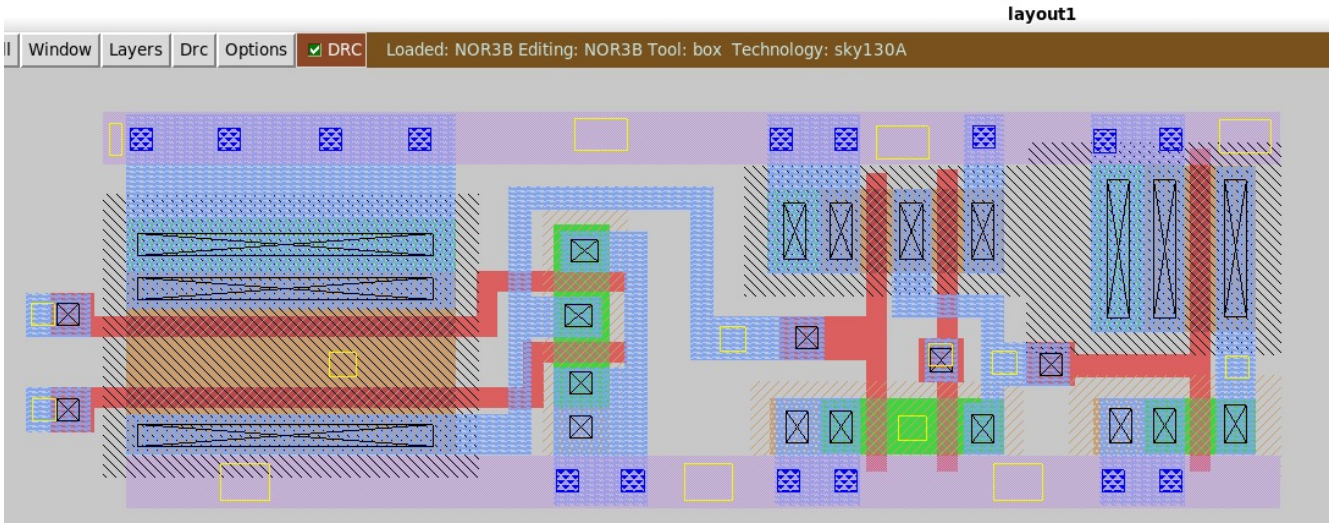


Figure 3.3: DRC Clean Screenshot for NOR3B

```
Contents of circuit 1:  Circuit: 'NOR3B'
Circuit NOR3B contains 10 device instances.
  Class: sky130_fd_pr__nfet_01v8 instances:   5
  Class: sky130_fd_pr__pfet_01v8 instances:   5
Circuit contains 10 nets.
Contents of circuit 2:  Circuit: 'NOR3B'
Circuit NOR3B contains 10 device instances.
  Class: sky130_fd_pr__nfet_01v8 instances:   5
  Class: sky130_fd_pr__pfet_01v8 instances:   5
Circuit contains 10 nets.

Circuit 1 contains 10 devices, Circuit 2 contains 10 devices.
Circuit 1 contains 10 nets,    Circuit 2 contains 10 nets.


Final result:
Circuits match uniquely.
Property errors were found.

The following cells had property errors:
 NOR3B

Logging to file "comp.out" disabled
LVS Done.
```

Figure 3.4: LVS Clean Screenshot for NOR3B

3.5 Simulation Results

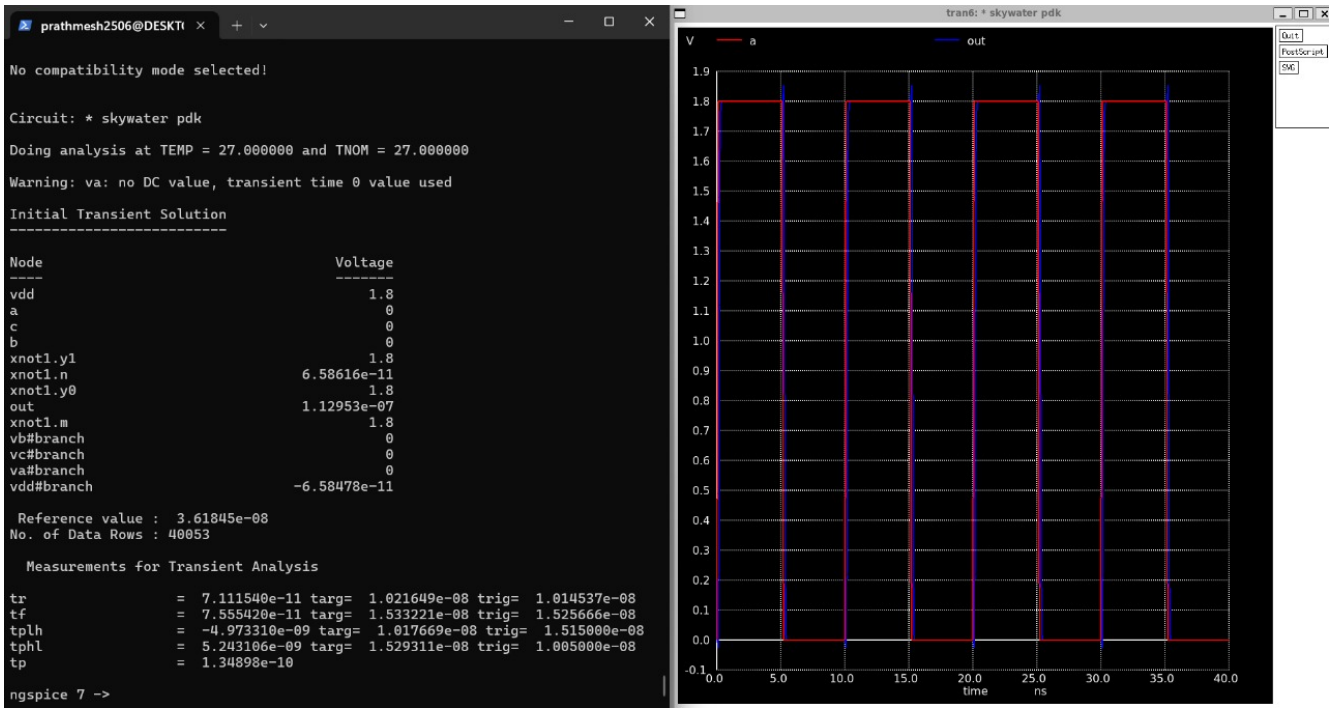


Figure 3.5: Simulation wrt a for Slew Rate of 100 ps and Load Capacitance of 10fF

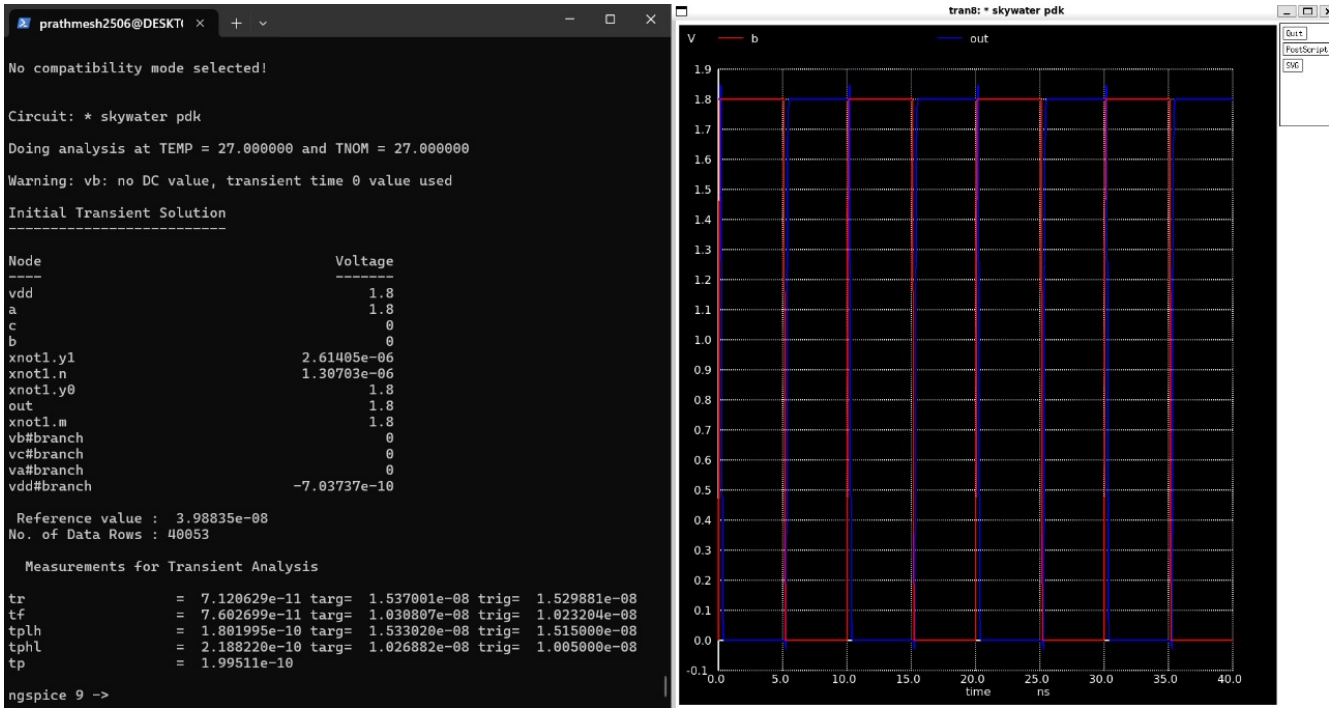


Figure 3.6: Simulation wrt b for Slew Rate of 100 ps and Load Capacitance of 10fF

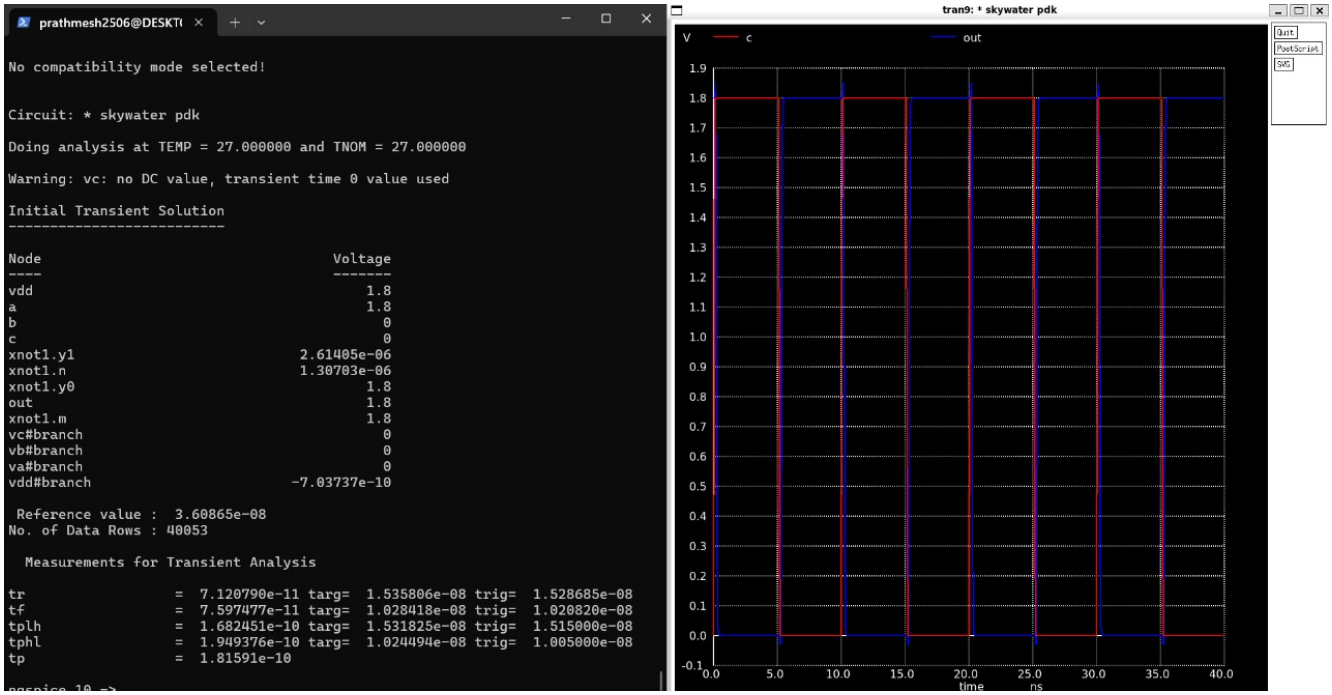


Figure 3.7: Simulation wrt c for Slew Rate of 100 ps and Load Capacitance of 10fF

3.5.1 Input Pin Capacitances

Input Pins	Rise Cap (pF)	Fall Cap (pF)	Average Cap (pF)
A	1.19e^{-}3pF	28.54e^{-}3pF	14.87e^{-}3pF
B	3.48e^{-}3pF	62.18e^{-}3pF	32.83e^{-}3pF
C	3.23e^{-}3pF	58.10e^{-}3pF	30.65e$^{\text{P}}$F

Table 3.2: Input Pin Capacitances for NOR3B Gate

3.5.2 Transition Time Tables

Output Rise Transitions (in ns) [Input slew vs output capacitance]

Related pin A: (i.e., other input pins are held constant)

Input Slew	0.5 fF	10 fF	100 fF
10ps	0.0190ns	0.0711ns	0.5987ns
100ps	0.0191ns	0.0711ns	0.5987ns
1000ps	0.0342ns	0.0792ns	0.5988ns

Table 3.3: Output Rise Transitions - Related pin A

Related pin B: (i.e., other input pins are held constant)

Input Slew	0.5 fF	10 fF	100 fF
10ps	0.0193ns	0.0712ns	0.5987ns
100ps	0.0193ns	0.0712ns	0.5987ns
1000ps	0.0203ns	0.0717ns	0.5987ns

Table 3.4: Output Rise Transitions - Related pin B

Related pin C: (i.e., other input pins are held constant)

Input Slew	0.5 fF	10 fF	100 fF
10ps	0.0193ns	0.0712ns	0.5987ns
100ps	0.0193ns	0.0712ns	0.5987ns
1000ps	0.0200ns	0.0715ns	0.5987ns

Table 3.5: Output Rise Transitions - Related pin C

Output Fall Transitions (in ns) [Input slew vs output capacitance]

Related pin A: (i.e., other input pins are held constant)

Input Slew	0.5 fF	10 fF	100 fF
10ps	0.0185ns	0.0755ns	0.6421ns
100ps	0.0186ns	0.0755ns	0.6421ns
1000ps	0.0332ns	0.0855ns	0.6429ns

Table 3.6: Output Fall Transitions - Related pin A

Related pin B: (i.e., other input pins are held constant)

Input Slew	0.5 fF	10 fF	100 fF
10ps	0.0192ns	0.0760ns	0.6423ns
100ps	0.0192ns	0.0760ns	0.6423ns
1000ps	0.0194ns	0.0761ns	0.6423ns

Table 3.7: Output Fall Transitions - Related pin B

Related pin C: (i.e., other input pins are held constant)

Input Slew	0.5 fF	10 fF	100fF
10ps	0.0191ns	0.0759ns	0.6423ns
10ps	0.0191ns	0.0759ns	0.6423ns
100ps	0.0195ns	0.0761ns	0.6424ns

Table 3.8: Output Fall Transitions - Related pin C

3.5.3 Propagation Delay Time Tables

Cell Rise Delay (in ns) [Input slew vs output capacitance]

Related pin A: (i.e., other input pins are held constant)

Input Slew	0.5 fF	10fF	100fF
10ps	0.0637ns	0.1092ns	0.4717ns
100ps	0.0812ns	0.1266ns	0.4893ns
1000ps	0.1702ns	0.2271ns	0.5925ns

Table 3.9: Cell Rise Delay - Related pin A

Related pin B: (i.e., other input pins are held constant)

Input Slew	0.5fF	10fF	100fF
10ps	0.1143ns	0.1600ns	0.5226ns
100ps	0.1345ns	0.1802ns	0.5428ns
1000ps	0.2194ns	0.2658ns	0.6286ns

Table 3.10: Cell Rise Delay - Related pin B

Related pin C: (i.e., other input pins are held constant)

Input Slew	0.5fF	10fF	100fF
10ps	0.1053ns	0.1509ns	0.5136ns
100ps	0.1226ns	0.1682ns	0.5308ns
1000ps	0.1913ns	0.2374ns	0.6003ns

Table 3.11: Cell Rise Delay - Related pin C

Cell Fall Delay (in ns) [Input slew vs output capacitance]

Related pin A: (i.e., other input pins are held constant)

Input Slew	0.5fF	10fF	100fF
10ps	0.0687ns	0.1226ns	0.5590ns
100ps	0.0894ns	0.1431ns	0.5801ns
1000ps	0.2133ns	0.2791ns	0.7197ns

Table 3.12: Cell Fall Delay - Related pin A

Related pin B: (i.e., other input pins are held constant)

Input Slew	0.5fF	10fF	100fF
10ps	0.1147ns	0.2013ns	0.6388ns
100ps	0.1645ns	0.2188ns	0.6562ns
1000ps	0.3039ns	0.3581ns	0.7957ns

Table 3.13: Cell Fall Delay - Related pin B

Related pin C: (i.e., other input pins are held constant)

Input Slew	0.5fF	10fF	100fF
10ps	0.1241ns	0.1783ns	0.6157ns
100ps	0.1407ns	0.1949ns	0.6326ns
1000ps	0.2484ns	0.3027ns	0.7404ns

Table 3.14: Cell Fall Delay - Related pin C

3.5.4 Static Power

Condition	Power (nW)
000	0.118nW
001	0.901nW
010	0.456nW
011	0.124nW
100	1.266nW
101	0.906nW
110	0.461nW
111	0.129nW

Table 3.15: Static Power for NOR3B Gate

3.5.5 Dynamic Power

Rise Power (in nW) [Input slew vs output capacitance]

Related pin A: (i.e., other input pins are held constant)

Input Slew	0.5fF	10fF	100fF
10ps	138913nW	136017nW	135021nW
100ps	15850nW	15660nW	15300nW
1000ps	1890nW	1872nW	1818nW

Table 3.16: Rise Power - Related pin A

Related pin B: (i.e., other input pins are held constant)

Input Slew	0.5fF	10fF	100fF
10ps	542682nW	544030nW	545373nW
100ps	155250nW	176220nW	211654nW
1000ps	114387nW	190746nW	224128nW

Table 3.17: Rise Power - Related pin B

Related pin C: (i.e., other input pins are held constant)

Input Slew	0.5fF	10fF	100fF
10ps	397500nW	398043nW	401250nW
100ps	120767nW	177313nW	215000nW
1000ps	108725nW	187154nW	223839nW

Table 3.18: Rise Power - Related pin C

Fall Power (in nW) [Input slew vs output capacitance]

Related pin A: (i.e., other input pins are held constant)

Input Slew	0.5fF	10fF	100fF
10ps	189391nW	194478nW	195019nW
100ps	71730nW	63024nW	70020nW
1000ps	42876nW	23103nW	17568nW

Table 3.19: Fall Power - Related pin A

Related pin B: (i.e., other input pins are held constant)

Input Slew	0.5fF	10fF	100fF
10ps	456716nW	454030nW	452682nW
100ps	51498nW	50508nW	50400nW
1000ps	5661nW	5580nW	5490nW

Table 3.20: Fall Power - Related pin B

Related pin C: (i.e., other input pins are held constant)

Input Slew	0.5fF	10fF	100fF
10ps	365625nW	362812nW	360938nW
100ps	50985nW	50499nW	50328nW
1000ps	5661nW	5535nW	5508nW

Table 3.21: Fall Power - Related pin C

Chapter 4

Cell 3: D Flip Flop

4.1 Circuit Diagram

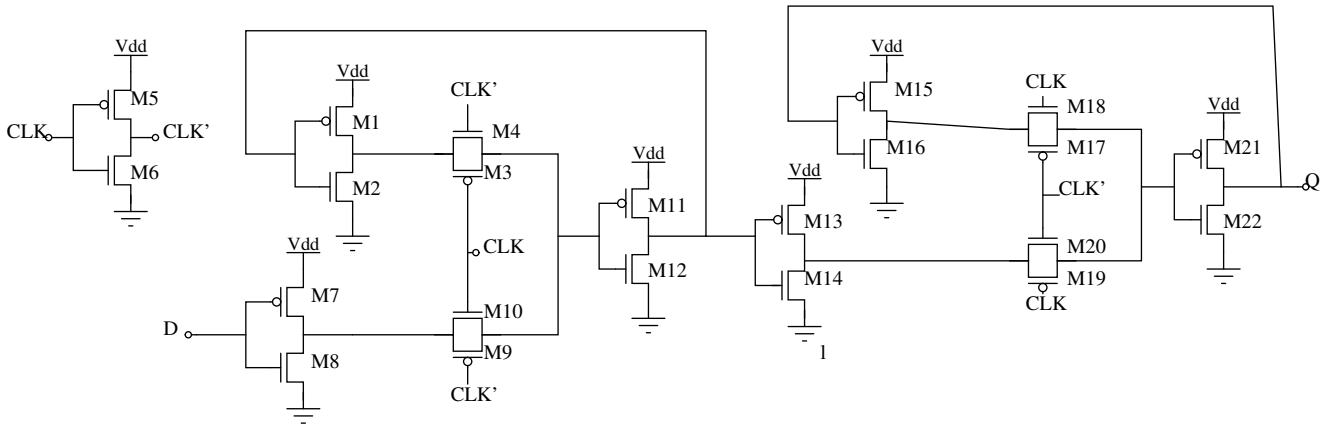


Figure 4.1: Circuit Diagram of D-Flip Flop Circuit with MOSFETs.

MOSFET	Width (W)	Length (L)
M1 (PMOS)	1.05 μm	0.15 μm
M2 (NMOS)	0.42 μm	0.15 μm
M3 (PMOS)	1.05 μm	0.15 μm
M4 (NMOS)	0.42 μm	0.15 μm
M5 (PMOS)	1.05 μm	0.15 μm
M6 (NMOS)	0.42 μm	0.15 μm
M7 (PMOS)	1.05 μm	0.15 μm
M8 (NMOS)	0.42 μm	0.15 μm
M9 (PMOS)	1.05 μm	0.15 μm
M10 (NMOS)	0.42 μm	0.15 μm
M11 (PMOS)	1.05 μm	0.15 μm
M12 (NMOS)	0.42 μm	0.15 μm
M13 (PMOS)	1.05 μm	0.15 μm
M14 (NMOS)	0.42 μm	0.15 μm
M15 (PMOS)	1.05 μm	0.15 μm
M16 (NMOS)	0.42 μm	0.15 μm
M17 (PMOS)	1.05 μm	0.15 μm
M18 (NMOS)	0.42 μm	0.15 μm
M19 (PMOS)	1.05 μm	0.15 μm
M20 (NMOS)	0.42 μm	0.15 μm
M21 (PMOS)	1.05 μm	0.15 μm
M22 (NMOS)	0.42 μm	0.15 μm

Table 4.1: MOSFET Width and Length for D flip flop

4.2 Layout

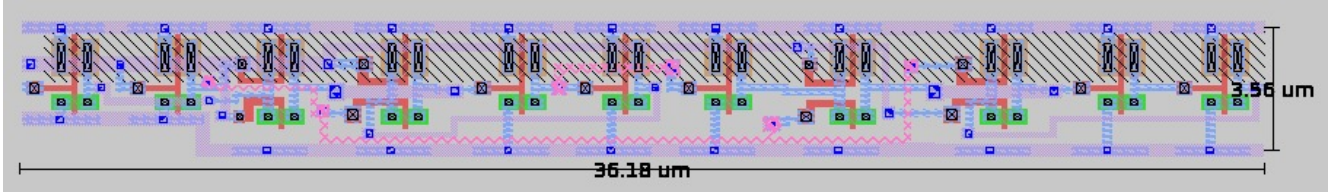


Figure 4.2: D flip flop Layout (Width X Height: 36.18 μm x 3.56 μm).

4.3 PEX Netlist

Listing 4.1: PEX Netlist for D Flip Flop

```
1 * NGSPICE file created from dff.ext - technology: sky130A
2
3 .subckt dff D Q Vdd GND CLK
4 X0 a_1315_0# a_615_n40# GND SUB sky130_fd_pr__nfet_01v8 ad=0.252u pd
    =2.04u as=0.252u ps=2.04u w=0.42 l=0.15
5 **devattr s=2520,204 d=2520,204
6 X1 a_15_0# D Vdd w_n79_81# sky130_fd_pr__pfet_01v8 ad=0.63u pd=3.3u as
    =0.63u ps=3.3u w=1.05 l=0.15
```

```
**devattr s=6300,330 d=6300,330
X2 a_2640_n40# Q Vdd w_n79_81# sky130_fd_pr__pfet_01v8 ad=0.63u pd=3.3u as=0.63u ps=3.3u w=1.05 l=0.15
**devattr s=6300,330 d=6300,330
X3 a_1915_0# a_1315_0# GND SUB sky130_fd_pr__nfet_01v8 ad=0.252u pd=2.04u as=0.252u ps=2.04u w=0.42 l=0.15
**devattr s=2520,204 d=2520,204
X4 a_2275_n40# CLK a_1915_0# w_n79_81# sky130_fd_pr__pfet_01v8 ad=0.63u pd=3.3u as=0.63u ps=3.3u w=1.05 l=0.15
**devattr s=6300,330 d=6300,330
X5 a_615_n40# CLK a_900_n40# w_n79_81# sky130_fd_pr__pfet_01v8 ad=0.63u pd=3.3u as=0.63u ps=3.3u w=1.05 l=0.15
**devattr s=6300,330 d=6300,330
X6 a_2275_n40# a_315_0# a_2640_n40# w_n79_81# sky130_fd_pr__pfet_01v8 ad=0.63u pd=3.3u as=0.63u ps=3.3u w=1.05 l=0.15
**devattr s=6300,330 d=6300,330
X7 a_15_0# D GND SUB sky130_fd_pr__nfet_01v8 ad=0.252u pd=2.04u as=0.252u ps=2.04u w=0.42 l=0.15
**devattr s=2520,204 d=2520,204
X8 a_615_n40# CLK a_15_0# SUB sky130_fd_pr__nfet_01v8 ad=0.252u pd=2.04u as=0.252u ps=2.04u w=0.42 l=0.15
**devattr s=2520,204 d=2520,204
X9 a_2640_n40# Q GND SUB sky130_fd_pr__nfet_01v8 ad=0.252u pd=2.04u as=0.252u ps=2.04u w=0.42 l=0.15
**devattr s=2520,204 d=2520,204
X10 a_315_0# CLK Vdd w_n79_81# sky130_fd_pr__pfet_01v8 ad=0.63u pd=3.3u as=0.63u ps=3.3u w=1.05 l=0.15
**devattr s=6300,330 d=6300,330
X11 a_315_0# CLK GND SUB sky130_fd_pr__nfet_01v8 ad=0.252u pd=2.04u as=0.252u ps=2.04u w=0.42 l=0.15
**devattr s=2520,204 d=2520,204
X12 a_900_n40# a_1315_0# GND SUB sky130_fd_pr__nfet_01v8 ad=0.252u pd=2.04u as=0.252u ps=2.04u w=0.42 l=0.15
**devattr s=2520,204 d=2520,204
X13 a_615_n40# a_315_0# a_15_0# w_n79_81# sky130_fd_pr__pfet_01v8 ad=0.63u pd=3.3u as=0.63u ps=3.3u w=1.05 l=0.15
**devattr s=6300,330 d=6300,330
X14 a_1315_0# a_615_n40# Vdd w_n79_81# sky130_fd_pr__pfet_01v8 ad=0.63u pd=3.3u as=0.63u ps=3.3u w=1.05 l=0.15
**devattr s=6300,330 d=6300,330
X15 a_2275_n40# a_315_0# a_1915_0# SUB sky130_fd_pr__nfet_01v8 ad=0.252u pd=2.04u as=0.252u ps=2.04u w=0.42 l=0.15
**devattr s=2520,204 d=2520,204
X16 a_900_n40# a_1315_0# Vdd w_n79_81# sky130_fd_pr__pfet_01v8 ad=0.63u pd=3.3u as=0.63u ps=3.3u w=1.05 l=0.15
**devattr s=6300,330 d=6300,330
X17 a_615_n40# a_315_0# a_900_n40# SUB sky130_fd_pr__nfet_01v8 ad=0.252u pd=2.04u as=0.252u ps=2.04u w=0.42 l=0.15
**devattr s=2520,204 d=2520,204
X18 a_2275_n40# CLK a_2640_n40# SUB sky130_fd_pr__nfet_01v8 ad=0.252u pd=2.04u as=0.252u ps=2.04u w=0.42 l=0.15
**devattr s=2520,204 d=2520,204
X19 a_1915_0# a_1315_0# Vdd w_n79_81# sky130_fd_pr__pfet_01v8 ad=0.63u pd=3.3u as=0.63u ps=3.3u w=1.05 l=0.15
**devattr s=6300,330 d=6300,330
X20 Q a_2275_n40# GND SUB sky130_fd_pr__nfet_01v8 ad=0.252u pd=2.04u as=0.252u ps=2.04u w=0.42 l=0.15
**devattr s=2520,204 d=2520,204
```

```
X21 Q a_2275_n40# Vdd w_n79_81# sky130_fd_pr__pfet_01v8 ad=0.63u pd=3.3
    u as=0.63u ps=3.3u w=1.05 l=0.15
**devattr s=6300,330 d=6300,330
C0 a_2275_n40# a_2640_n40# 0.34947f
C1 GND a_315_0# 0.96389f
C2 a_15_0# a_900_n40# 0
C3 w_n79_81# a_615_n40# 0.23212f
C4 a_1315_0# a_315_0# 0.11978f
C5 Vdd D 0.02997f
C6 a_15_0# Vdd 0.1547f
C7 CLK D 0.05426f
C8 Vdd a_2640_n40# 0.26598f
C9 w_n79_81# GND 0.05348f
C10 a_15_0# CLK 0.5725f
C11 GND a_1915_0# 0.07177f
C12 CLK a_2640_n40# 0.08364f
C13 w_n79_81# a_1315_0# 0.37047f
C14 Q a_2640_n40# 0.07415f
C15 a_1315_0# a_1915_0# 0.03978f
C16 a_900_n40# a_615_n40# 0.34642f
C17 a_2275_n40# GND 0.10727f
C18 w_n79_81# a_315_0# 0.66457f
C19 a_1315_0# a_2275_n40# 0
C20 a_1915_0# a_315_0# 0.1387f
C21 a_900_n40# GND 0.74367f
C22 Vdd a_615_n40# 0.13124f
C23 CLK a_615_n40# 0.39025f
C24 a_1315_0# a_900_n40# 0.20492f
C25 a_15_0# D 0.03545f
C26 Vdd GND 0.16744f
C27 a_2275_n40# a_315_0# 0.16603f
C28 CLK GND 0.38752f
C29 w_n79_81# a_1915_0# 0.08888f
C30 a_1315_0# Vdd 0.23839f
C31 Q GND 0.06112f
C32 CLK a_1315_0# 0.20406f
C33 a_900_n40# a_315_0# 0.25447f
C34 w_n79_81# a_2275_n40# 0.26179f
C35 a_2275_n40# a_1915_0# 0.11564f
C36 Vdd a_315_0# 0.21525f
C37 CLK a_315_0# 0.79928f
C38 a_15_0# a_615_n40# 0.11685f
C39 w_n79_81# a_900_n40# 0.08915f
C40 a_900_n40# a_1915_0# 0.00279f
C41 Q a_315_0# 0.00111f
C42 D GND 0.05535f
C43 a_15_0# GND 0.45782f
C44 a_2640_n40# GND 0.73259f
C45 w_n79_81# Vdd 0.70498f
C46 Vdd a_1915_0# 0.13342f
C47 w_n79_81# CLK 0.97851f
C48 CLK a_1915_0# 0.2298f
C49 a_1315_0# a_2640_n40# 0
C50 a_900_n40# a_2275_n40# 0
C51 w_n79_81# Q 0.15778f
C52 a_2275_n40# Vdd 0.24253f
C53 D a_315_0# 0
C54 a_15_0# a_315_0# 0.29308f
```

```
C55 CLK a_2275_n40# 0.26506f
C56 a_2640_n40# a_315_0# 0.08126f
C57 a_2275_n40# Q 0.04137f
C58 a_900_n40# Vdd 0.14489f
C59 GND a_615_n40# 0.10457f
C60 CLK a_900_n40# 0.28083f
C61 a_1315_0# a_615_n40# 0.05555f
C62 w_n79_81# D 0.06365f
C63 w_n79_81# a_15_0# 0.06268f
C64 w_n79_81# a_2640_n40# 0.10226f
C65 CLK Vdd 2.19875f
C66 a_2640_n40# a_1915_0# 0
C67 a_1315_0# GND 0.10536f
C68 Vdd Q 0.16313f
C69 a_615_n40# a_315_0# 0.19623f
C70 CLK Q 0
C71 GND SUB 4.15839f
C72 Vdd SUB 3.10979f
C73 Q SUB 0.35838f
C74 CLK SUB 1.57637f
C75 D SUB 0.31352f
C76 a_2640_n40# SUB 0.45571f
C77 a_1915_0# SUB 0.15037f
C78 a_900_n40# SUB 0.36373f
C79 a_15_0# SUB 0.16791f
C80 a_2275_n40# SUB 0.57273f
C81 a_1315_0# SUB 0.81502f
C82 a_615_n40# SUB 0.55324f
C83 a_315_0# SUB 2.53323f
C84 w_n79_81# SUB 6.09654f
.ends
```

4.4 DRC and LVS Results

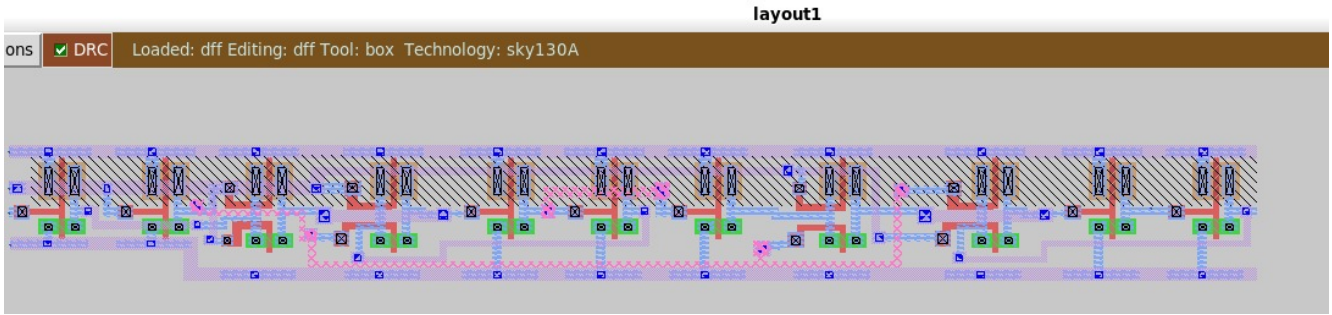


Figure 4.3: DRC Clean Screenshot for D flip flop

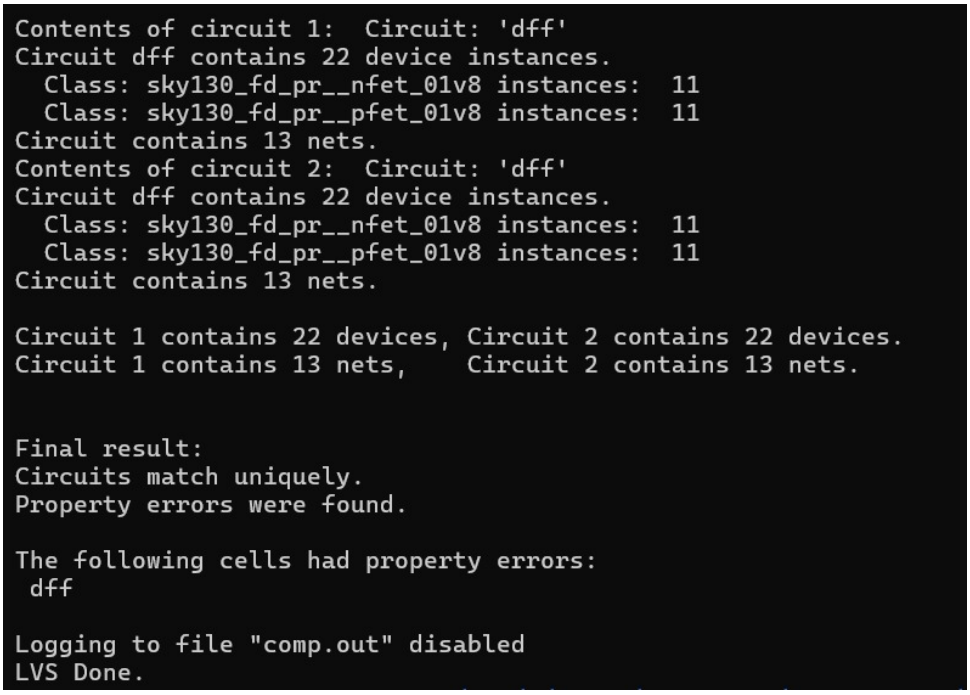
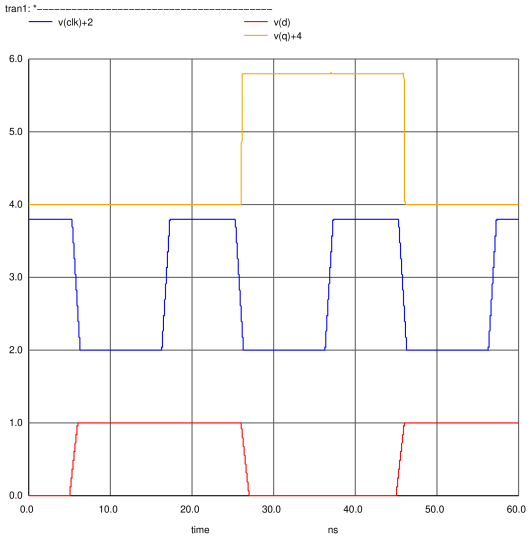
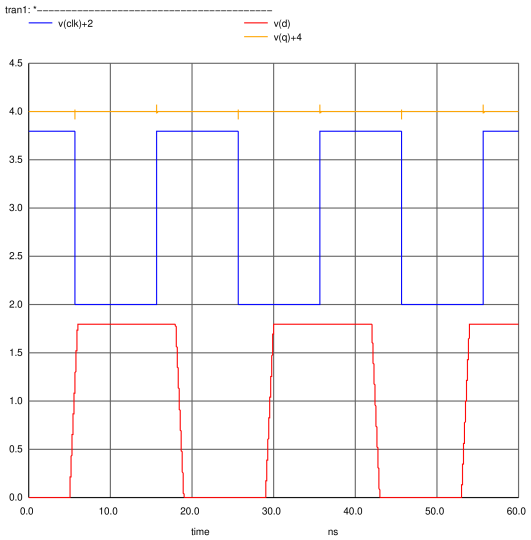


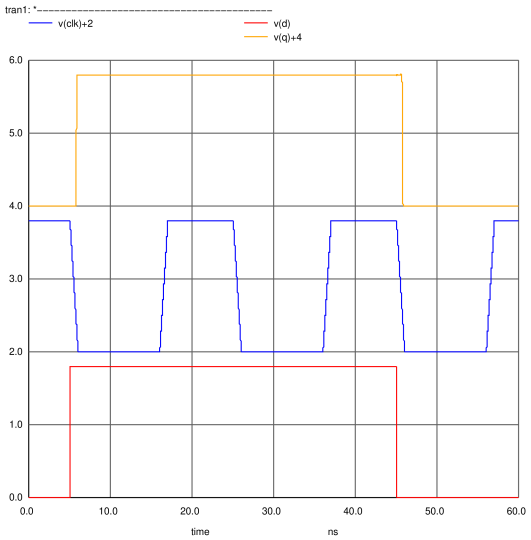
Figure 4.4: LVS Clean Screenshot for D Flip Flop

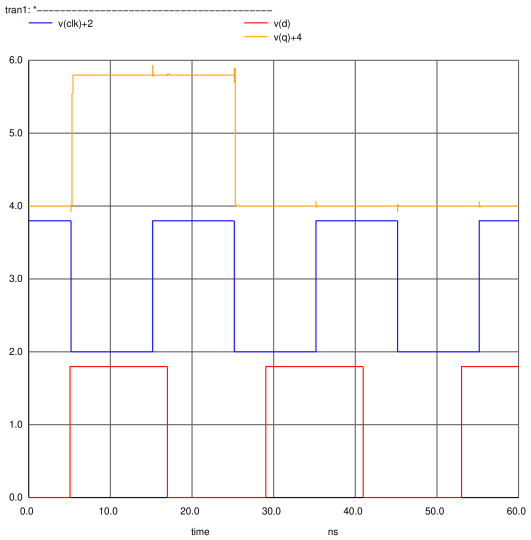
For the purpose of LVS verification, we modified the bulk terminals in the layout. Multiple device-level variations were attempted to resolve the issue; however, the problem persisted. Therefore, only the bulk connections were modified, and no other changes were made to the layout.

4.5 Simulations (Explanations and Graphs)









simulation waveforms for setup

4.6 Timing and Power Table

4.6.1 Input Pin Capacitances

Input Pins	Rise Cap (pF)	Fall Cap (pF)	Average Cap (pF)
D	4.07852e⁻15F	4.16548e⁻15F	4.12e⁻15F
CLK	2.17360e⁻14F	1.69172e⁻14F	1.93e⁻14F

Table 4.2: Input Pin Capacitances for D Flip Flop

4.6.2 Set-up Time Constraints

Rise Constraint

	10ps	1000ps
10ps	210ps	0ps
1000ps	641ps	301ps

Table 4.3: Set-up Time Constraints (Rise Constraint in ns) [Input slew vs CLK slew]

Fall Constraint

	10ps	1000ps
10ps	81ps	0ps
1000ps	193ps	0ps

Table 4.4: Set-up Time Constraints (Fall Constraint in ns) [Input slew vs CLK slew]

4.6.3 Hold Time Constraints

Rise Constraint (Hold)

	10ps	1000ps
10ps	15ps	0ps
1000ps	28ps	10ps

Table 4.5: Hold Time Constraints (Rise) [Input slew vs CLK slew]

Fall Constraint (Hold)

	10ps	1000ps
10ps	5ps	0ps
1000ps	12ps	0ps

Table 4.6: Hold Time Constraints (Fall) [Input slew vs CLK slew]

4.6.4 Transition Times

Output Rise Transitions

	10ps	**100ps**	**1000ps**
0.5fF	0.0470ns	0.0470ns	0.0470ns
10fF	0.0958ns	0.0958ns	0.0960ns
100fF	0.6075ns	0.6077ns	0.6095ns

Table 4.7: Output Rise Transitions (in ns) [Input slew vs Output Capacitance, Related pin D: other input pins held constant]

Output Fall Transitions

	10ps	**100ps**	**1000ps**
0.5fF	0.0415ns	0.0415ns	0.0415ns
10fF	0.0956ns	0.0956ns	0.0956ns
1000fF	0.6142ns	0.6142ns	0.6142ns

Table 4.8: Output Fall Transitions (in ns) [Input slew vs Output Capacitance, Related pin D: other input pins held constant]

4.6.5 CLK-to-Q Delay Time Table

Cell Rise Delay

	10ps	**100ps**	**1000ps**
0.5fF	0.114ns	0.114ns	0.114ns
10fF	0.154ns	0.154ns	0.154ns
100fF	0.499ns	0.499ns	0.499ns

Table 4.9: Cell Rise Delay (in ns) [Input slew vs Output Capacitance, Related pin D: other input pins held constant]

Cell Fall Delay

	10ps	**100ps**	**1000ps**
0.5fF	0.084ns	0.084ns	0.084ns
10fF	0.133ns	0.133ns	0.133ns
100fF	0.521ns	0.521ns	0.521ns

Table 4.10: Cell Fall Delay (in ns) [Input slew vs Output Capacitance, Related pin D: other input pins held constant]

4.6.6 Static Power

Condition (CLK, D)	Power (nW)
00	57007nW
01	72209nW
10	62010nW
11	66648nW

Table 4.11: Static Power (all possible input combinations of CLK and D)

4.6.7 Dynamic Power Table

Rise Power (in nW) [Input slew vs output capacitance]

	10ps	100ps	1000ps
0.5fF	1010770nW	1010800nW	1010700nW
10fF	1001400nW	1001490nW	1001640nW
100fF	993400nW	993684nW	993590nW

Table 4.12: Dynamic Rise Power

Fall Power (in nW) [Input slew vs output capacitance]

	10ps	100ps	1000ps
0.5fF	1531030nW	1538660nW	1538860nW
10fF	1541940nW	1542010nW	1542100nW
100fF	1538420nW	1538540nW	1538660nW

Table 4.13: Dynamic Fall Power

Chapter 5

Verilog Implementation and Verification

5.1 Introduction

This chapter presents the Verilog HDL implementations for the three standard cells designed in this project. Each cell has been implemented with appropriate timing models and verified using testbenches with Icarus Verilog simulator.

5.2 Inverter Verilog Implementation

5.2.1 Inverter Module

Listing 5.1: Inverter Verilog Module

```
module inverter (
    input  wire a,
    output wire y
);

    assign y = ~a;

endmodule
```

5.3 NOR3B Gate Verilog Implementation

5.3.1 NOR3B Module

Listing 5.2: 3-Input NOR Gate Verilog Module

```
module nor3_bubbled (
    input  wire a, // This is bubbled
    input  wire b,
    input  wire c,
    output wire y
);

    wire a_inv;
    assign a_inv = ~a;
```

```
10
11      // NOR of (a_inv, b, c)
12      assign y = ~(a_inv | b | c);
13
14  endmodule
```

5.4 D Flip-Flop Verilog Implementation

5.4.1 D Flip-Flop with Negative Edge

Listing 5.3: D Flip-Flop with Negative Edge

```
1  module dff_negedge (
2      input  wire clk,
3      input  wire d,
4      output reg  q
5  );
6
7      always @(negedge clk) begin
8          q <= d;
9      end
10
11 endmodule
```

Chapter 6

Team Contributions

- **Jaswin:** Designed the D flip-flop (negative-edge triggered) in Magic and collaborated in making it fully functional.
- **Yaswanth:** Simulated the D flip-flop, performed its characteristics analysis, and collaborated in making it fully functional.
- **Prathmesh:** Designed the 3-input NORB gate, implemented its SPICE and Magic layouts, and performed all the characteristics analysis.
- **Jithin:** Contributed to report writing, designed the inverter1, and implemented all Verilog designs.

Together with this, we all engaged in a lot of discussion, within ourselves as well as with other teams and collaborated to this project.

Chapter 7

References

- NGSpice documentation : `http://ngspice.sourceforge.net/docs.html`
- Magic VLSI documentation : `http://opencircuitdesign.com/magic/index.html`
- "CMOS VLSI Design : A Circuits and Systems Perspective" by Neil Weste and David Harris
- Lecture Slides and Notes from the course EE-671