

EE 671: VLSI DESIGN

Assignment 2: Layout with Magic and LVS Check for CMOS Inverter

Yaswanth Ram Kumar

23B1277

Under the guidance of
Prof Lakshmeesha Somappa

1 Introduction

This assignment focuses on the layout and simulation of CMOS inverters using the **Magic** along with **NGSPICE**. Both the Inverters of strength 1 (INVX1) and strength 2 (INVX2) are laid out in Magic and parasitic extraction (PEX) files have been generated to model parasitics. Also **Netgen** is used for LVS check. Finally, transient analysis is performed to compare rise time, fall time and propagation delays against results from Assignment-01.

2 Circuit Diagram

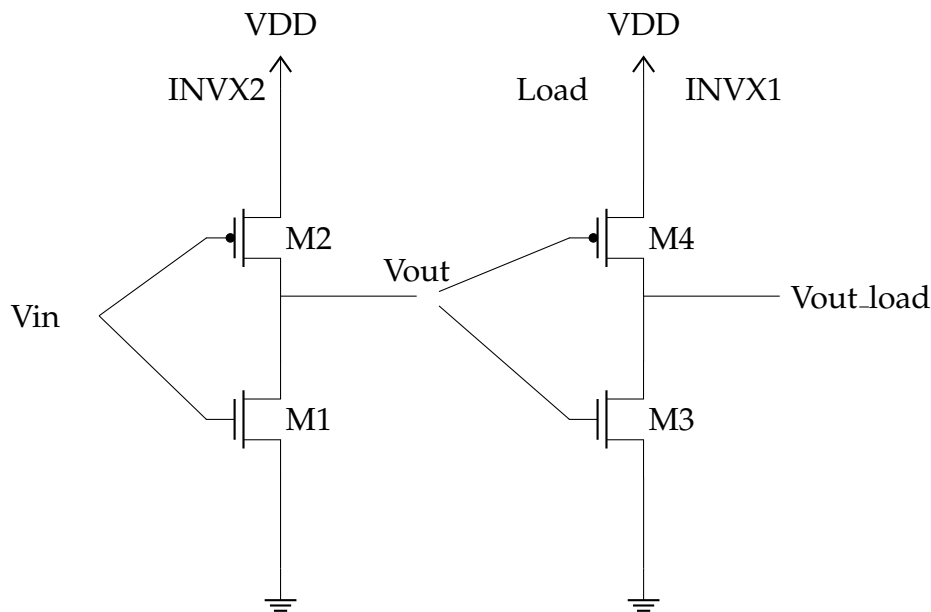


Figure 1: CMOS Inverter Circuit: INVX2 driving INVX1 as load

All files related to this assignment and Assignment-01 are maintained in this GitHub repository: [Yaswanth2747/VLSI-Design](https://github.com/Yaswanth2747/VLSI-Design).

3 INVX1 Results

3.1 Design Parameters

Table 1: INVX1 Design Parameters

Parameter	Value
PMOS Width (μm)	1.31
PMOS Length (μm)	0.15
NMOS Width (μm)	0.42
NMOS Length (μm)	0.15

3.2 Timing Results

Table 2: Timing Results for INVX1

Parameter	Assignment-02 (PEX)	Assignment-01 (Ideal)
Rise time t_r (ps)	35.35	29.37
Fall time t_f (ps)	32.89	29.43
t_{pHL} (ps)	23.91	23.06
t_{pLH} (ps)	20.19	19.36

3.3 Screenshots for INVX1

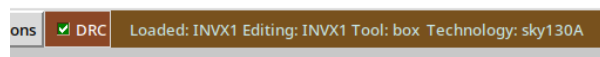


Figure 2: INVX1 DRC

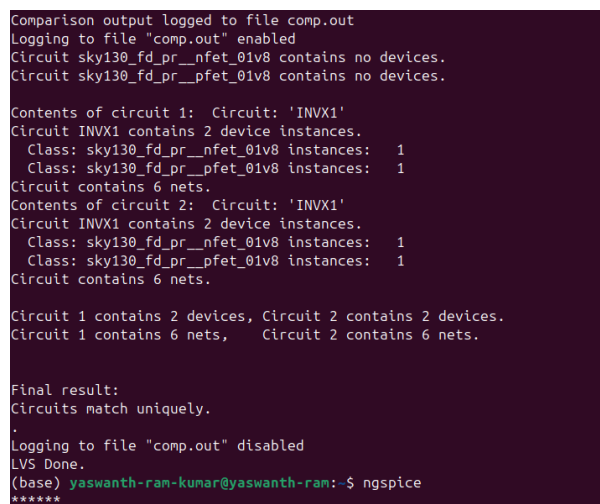


Figure 3: INVX1 LVS

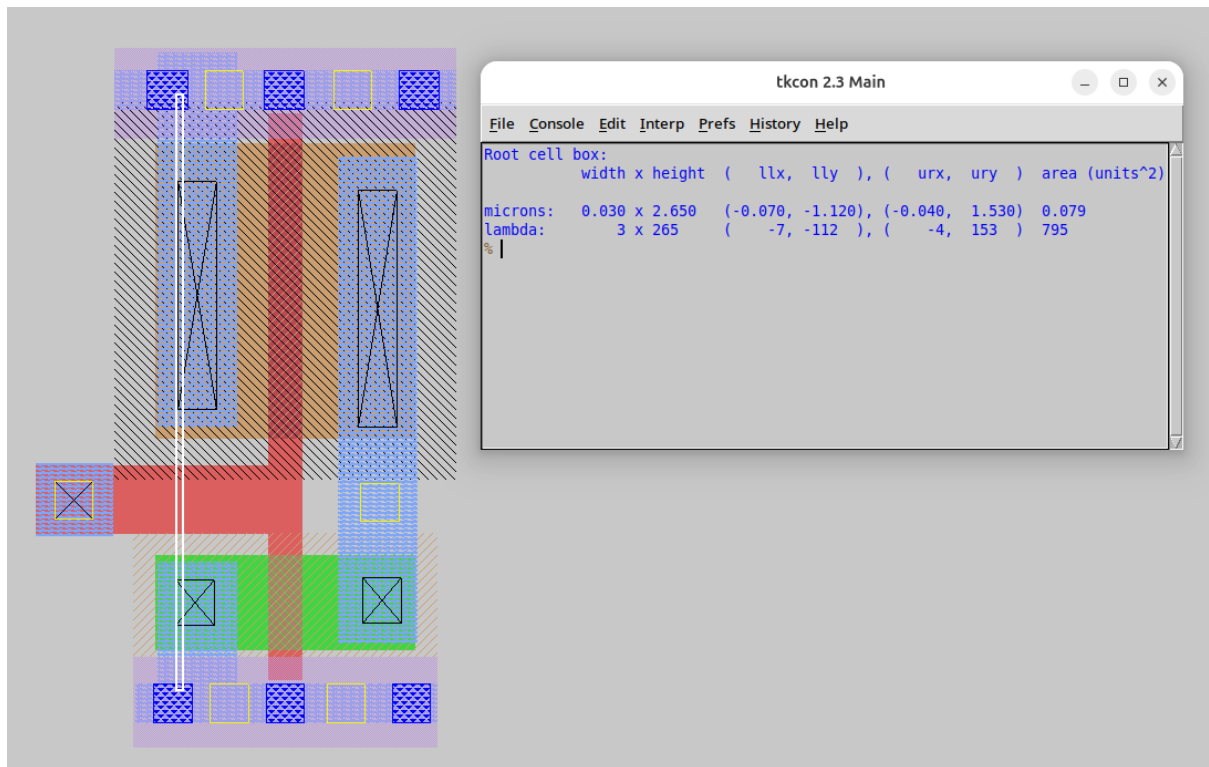
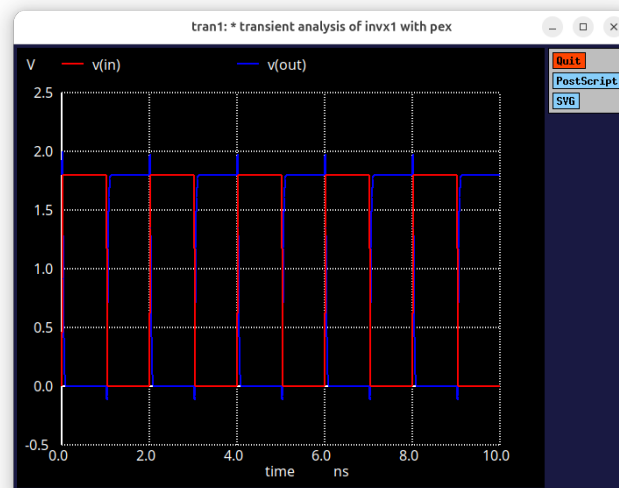
Figure 4: INVX1 Layout - Height = $2.65 \mu\text{m}$ 

Figure 5: INVX1 Plot

```

Circuit: * transient analysis of invx1 with pex
Doing analysis at TEMP = 27.000000 and TNOM = 27.000000
Using SPARSE 1.3 as Direct Linear Solver
Initial Transient Solution
-----
Node              Voltage
-----
vdd                1.8
in                 0
out                1.8
xin1.sub           0.240679
out_load           8.02329e-07
xload.sub          4.01165e-07
vin#branch         0
vdd#branch         -4.30496e-10

Reference value : 6.05500e-09
No. of Data Rows : 1068

Measurements for Transient Analysis
tr      = 3.534737e-11 targ= 1.075778e-09 trig= 1.040431e-09
tf      = 3.289320e-11 targ= 5.491629e-11 trig= 2.202309e-11
tphl    = 2.391311e-11 targ= 3.391311e-11 trig= 1.000000e-11
tplh    = 2.018738e-11 targ= 1.050187e-09 trig= 1.030000e-09

```

Figure 6: INVX1 NGSPICE Terminal

4 INVX2 Results

4.1 Device Parameters for INVX2

Table 3: Device Parameters for INVX2

PMOS Width	2.62 μm
PMOS Length	0.15 μm
NMOS Width	0.84 μm
NMOS Length	0.15 μm

4.2 Timing Results

Table 4: Timing Results for INVX2

Parameter	Assignment-02 (PEX)	Assignment-01 (Ideal)
Rise time t_r (ps)	20.91	20.33
Fall time t_f (ps)	20.02	19.25
t_{pHL} (ps)	17.30	17.64
t_{pLH} (ps)	14.71	14.85

4.3 Screenshots

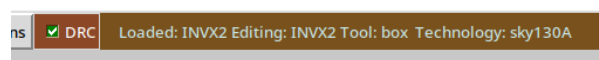
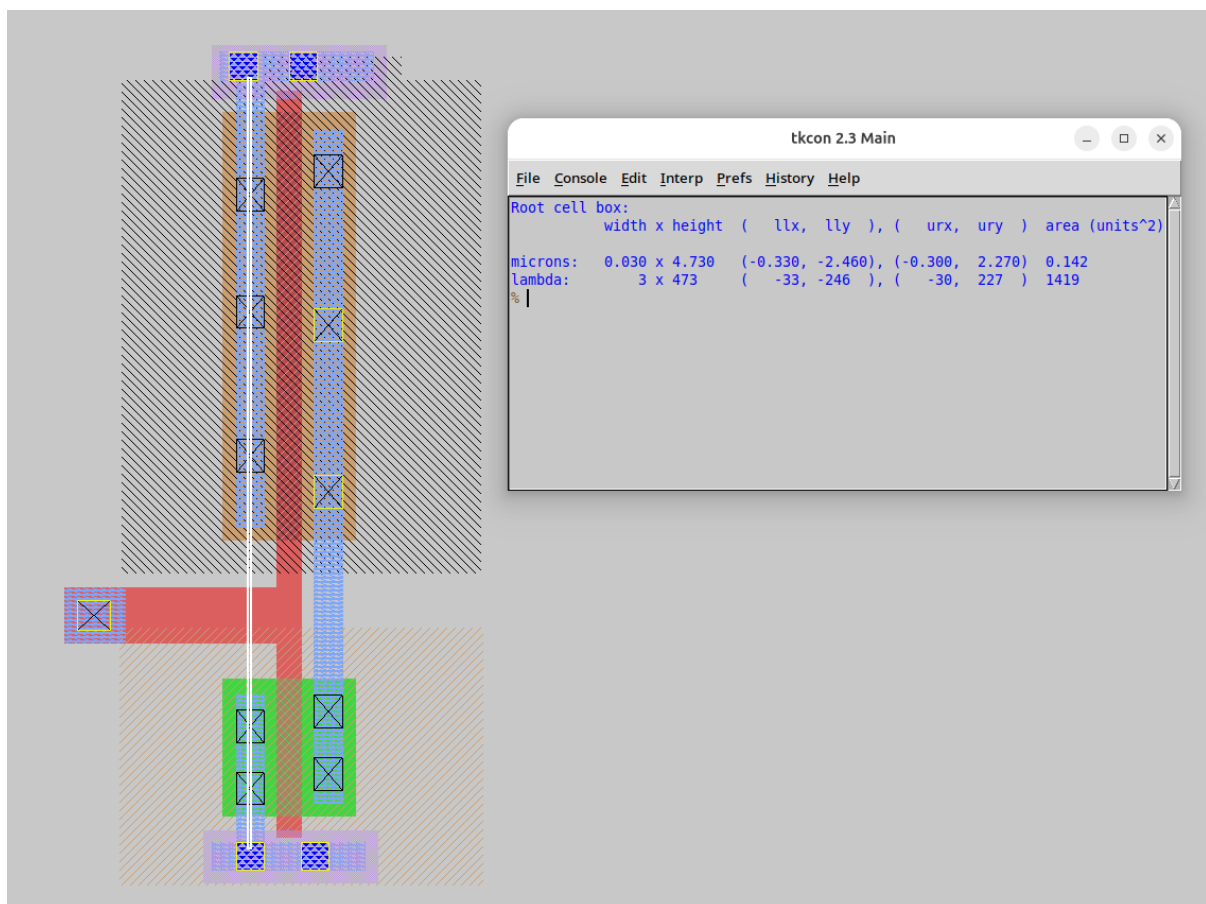


Figure 7: INVX2 DRC

```
yaswanth-ram-kumar@yaswanth-ram: ~  
Circuit 1 contains 2 devices, Circuit 2 contains 2 devices.  
Circuit 1 contains 6 nets,   Circuit 2 contains 6 nets.  
  
Final result:  
Circuits match uniquely.  
.  
Logging to file "comp.out" disabled  
LVS Done.  
(base) yaswanth-ram-kumar@yaswanth-ram:~$
```

Figure 8: INVX2 LVS

Figure 9: INVX2 Layout - Height = 4.730 μm

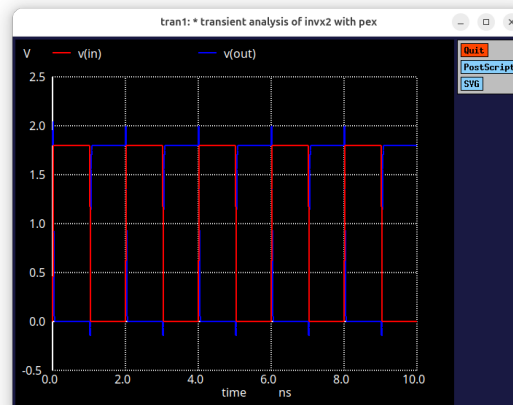


Figure 10: IN VX2 Plot

```

yaswanth-ram-kumar@yaswanth-ram: ~
Circuit: * transient analysis of invx2 with pex
Doing analysis at TEMP = 27.000000 and TNOM = 27.000000
Using SPARSE 1.3 as Direct Linear Solver
Initial Transient Solution
-----
Node          Voltage
-----
vdd            1.8
in              0
out            1.8
xinvi1.sub     0.235888
out_load       8.02332e-07
xload.sub      4.01167e-07
vin#branch     0
vdd#branch     -4.30789e-10

Reference value : 5.78500e-09
No. of Data Rows : 1068

Measurements for Transient Analysis
tr      = 2.091314e-11 targ= 1.059204e-09 trig= 1.038291e-09
tf      = 2.002003e-11 targ= 4.039174e-11 trig= 2.037170e-11
tphl    = 1.729941e-11 targ= 2.729941e-11 trig= 1.000000e-11
tplt    = 1.471163e-11 targ= 1.044712e-09 trig= 1.030000e-09

Warning from checkValid: vector tran is not available or has zero length.
ngspice 12 ->

```

Figure 11: IN VX2 NGSPICE Terminal

5 Conclusion

- Both IN VX1 and IN VX2 layouts are **DRC clean** and **LVS matched**.
- Parasitic effects slightly increase rise/fall times compared to ideal (Assignment-01) results.
- As expected, IN VX2 shows better drive strength with reduced delays compared to IN VX1.

Thank You

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