For Sequential cells, the following characterizations have to be performed and filled.

1. **Input pin capacitances:**

|  |  |  |  |
| --- | --- | --- | --- |
| **Input Pins** | **Rise Cap (pF)** | **Fall Cap (pF)** | **Average Cap (pF)** |
| D | 4.08e-03 | 4.16e-03 | 4.12e-03 |
| CLK | 2.17e-02 | 1.69e-02 | 1.93e-02 |

1. **Set-up Time Table:**

**(i) Rise Constraint** **(in ns)** [Input slew vs CLK slew].

|  |  |  |
| --- | --- | --- |
|  | **10 ps** | **1000 ps** |
| **10 ps** | 0.201 | 0 |
| **1000 ps** | 0.641 | 0.301 |

**(ii) Fall Constraint** **(in ns)** [Input slew vs CLK slew].

|  |  |  |
| --- | --- | --- |
|  | **10 ps** | **1000 ps** |
| **10 ps** | 0.081 | 0 |
| **1000 ps** | 0.193 | 0 |

1. **Hold Time Table:**

**(i) Rise Constraint** **(in ns)** [Input slew vs CLK slew].

|  |  |  |
| --- | --- | --- |
|  | **10 ps** | **1000 ps** |
| **10 ps** | 0.015 | 0 |
| **1000 ps** | 0.028 | 0.01 |

**(ii) Fall Constraint** **(in ns)** [Input slew vs CLK slew].

|  |  |  |
| --- | --- | --- |
|  | **10 ps** | **1000 ps** |
| **10 ps** | 0.005 | 0 |
| **1000 ps** | 0.012 | 0 |

1. **Transition Time Table (for Q output, CLK will have minimum slew of 10 ps):** (please strictly consider 20% and 80% of VDD for transition time)

**(i) Output Rise Transitions** **(in ns)** [Input slew vs output capacitance].

**Related pin D**: (i.e., other input pins are held constant)

|  |  |  |  |
| --- | --- | --- | --- |
|  | **10 ps** | **100 ps** | **1000 ps** |
| **0.5 fF** | 0.047 | 0.047 | 0.047 |
| **10 fF** | 0.0958 | 0.0958 | 0.0960 |
| **100 fF** | 0.6075 | 0.6077 | 0.6095 |

**(ii) Output Fall Transitions** **(in ns)** [Input slew vs output capacitance].

**Related pin D**: (i.e., other input pins are held constant)

|  |  |  |  |
| --- | --- | --- | --- |
|  | **10 ps** | **100 ps** | **1000 ps** |
| **0.5 fF** | 0.0415 | 0.0415 | 0.0415 |
| **10 fF** | 0.0956 | 0.0956 | 0.0956 |
| **100 fF** | 0.6142 | 0.6142 | 0.6139 |

1. **CLK-to-Q Delay Time Table**: (delay between clock transition and data transition. Use 50% of CLK to 50% of output to simulate propagation delay).

**(i) Cell Rise Delay (in ns)** [Input slew vs output capacitance].

**Related pin D**: (i.e., other input pins are held constant)

|  |  |  |  |
| --- | --- | --- | --- |
|  | **10 ps** | **100 ps** | **1000 ps** |
| **0.5 fF** | 0.114 | 0.114 | 0.114 |
| **10 fF** | 0.154 | 0.154 | 0.154 |
| **100 fF** | 0.499 | 0.499 | 0.499 |

**(ii) Cell Fall Delay (in ns)** [Input slew vs output capacitance].

**Related pin D**: (i.e., other input pins are held constant)

|  |  |  |  |
| --- | --- | --- | --- |
|  | **10 ps** | **100 ps** | **1000 ps** |
| **0.5 fF** | 0.084 | 0.084 | 0.084 |
| **10 fF** | 0.133 | 0.133 | 0.133 |
| **100 fF** | 0.521 | 0.521 | 0.521 |

1. **Static Power (all possible input combinations of CLK and D).**

|  |  |
| --- | --- |
| **Condition (CLK, D)** | **Power (nW)** |
| 00 | 57007 |
| 01 | 72209 |
| 10 | 62010 |
| 11 | 66648 |

1. **Dynamic Power Table: (CLK will have minimum slew of 10 ps)**

**(i) Rise Power (in nW)** [Input slew vs output capacitance].

**Related pin D**: (i.e., other input pins are held constant)

|  |  |  |  |
| --- | --- | --- | --- |
|  | **10 ps** | **100 ps** | **1000 ps** |
| **0.5 fF** | 1010770 | 1010800 | 1010700 |
| **10 fF** | 1001400 | 1001490 | 1001640 |
| **100 fF** | 993400 | 993684 | 993590 |

**(ii) Fall Power (in nW)** [Input slew vs output capacitance].

**Related pin D**: (i.e., other input pins are held constant)

|  |  |  |  |
| --- | --- | --- | --- |
|  | **10 ps** | **100 ps** | **1000 ps** |
| **0.5 fF** | 1531030 | 1538660 | 1538860 |
| **10 fF** | 1541940 | 1542010 | 1542100 |
| **100 fF** | 1538420 | 1538540 | 1538660 |