PROFILE OF NOAH HÜSSER

BASICS
Nationality: CH
Date of Birth: 12th January 1991

CONTACT
yatekii@yatekii.ch
+41 79 960 7130
Eggenstrasse 3

5616 Meisterschwanden
Switzerland

ACTIVITIES
Ju Jitsu, Programming,
Electronics, Reading

SKILLS

PROFESSIONAL
Software Development
Embedded Systems
FPGA Programming
Electronical Prototyping
Project Management

LANGUAGES
German *mother tongue*
English *fluent*
French *experienced*

TOOLS

ENGINEERING
Altium/KiCad
Shell
Jupyter, Scipy, Numpy, Pandas
MATLAB
Inventor

PROGRAMMING
frequently used
Python, C,
VHDL, TCL,
JavaScript, SQL, LaTeX

used in the past
Java, C#, PHP, C++, Bash

MISCELLANEOUS
Git/SVN
Microsoft Office
Photoshop / InDesign

EDUCATION

FHNW BRUGG-WINDISCH
BsC in EE and IT
Feb 2016 – present | Brugg-Windisch, CH

ETH ZÜRICH
BsC in Electrical Engineering and Information Technology
Sep 2013 – Feb 2016 | Zürich, CH

ALTE KANTONSSCHULE AARAU
Matura
Graduated 2012 | Aarau, CH

PRACTICAL EXPERIENCE

ABB MICAFIL
Intern Software Development
Jul 2016 – present | Altstetten, CH
Development of various APIs and a CAD tool in VB/C#.

BASTLI
President
Feb 2016 – Oct 2016 | Zürich, CH
Active Member
Sep 2013 – present | Zürich, CH
Bastli is the student's electronics lab at ETH Zürich. With Bastli we realize various, cool engineering projects. Most of the things we create are assembled from parts salvaged from the Junkyard. Impressions on what we do at *www.bastli.ch*.

NEXUS TELECOM
Low Level C Programmer
Mai 2014 – Mai 2015 | Zürich, CH
Diverse work on their main C library with focus on porting it from 32 to 64 bit.

AFC AG - AIR FLOW CONSULTING
Internship as a Programmer
Dec 2012 – Apr 2013 | Zürich, CH
Creation of various tools in Python, C# and VB, working as a one man team.

WAPPLE.CH
Webdesigner and Co-Founder
Jan 2007 – present | Zürich, CH
Webdesign for individuals, associations and companies in cooperation with a friend.

PUBLICATIONS AND PROJECTS

DESIGN AND IMPLEMENTATION OF AN FPGA BASED DATA LOGGING AND FAULT RECORDING SYSTEM FOR PWM RECTIFIERS
Group Thesis at ETH Zürich
Sep 2015 – Dec 2015 | Zürich, CH

- Recursive trigger logic to detect special signal patterns (VHDL)
- Kernel module for data reading and processing on an ARM Core A9 (C)
- GUI to retrieve data over the network, filter and display it (C++, Python, Qt5)