Data Conversion Chain — 20-02-2017

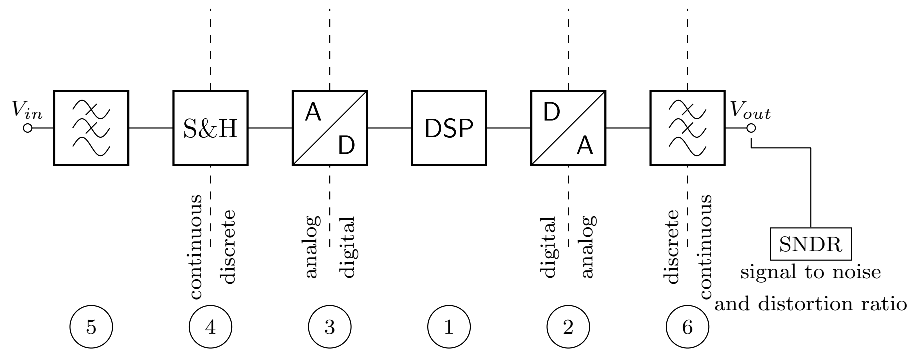


Figure 1: A typical signal chain

1 DSP

The equivalent ouput voltage can be expressed with 1. It's maximum can be described with 2

$$V_{eq} = V_{ref}\Big(\sum_{i=1}^{N} b_i 2^{-i}\Big) \tag{1}$$

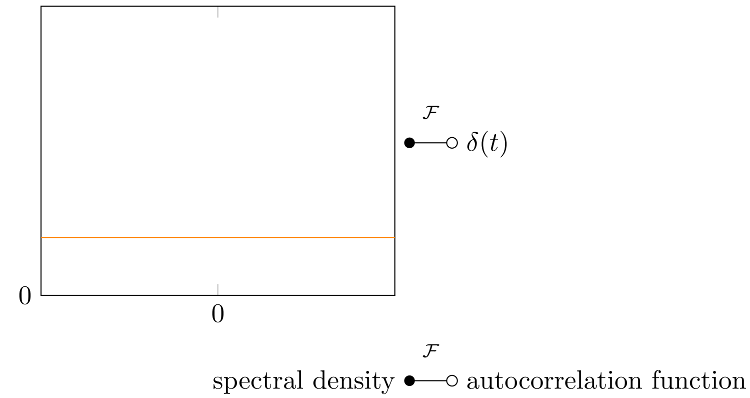
$$V_{eq} = V_{ref}\Big(1 - 2^{-N}\Big) \tag{2}$$

This is a representation in UINT. In most realworld impelemntations INT using 2's complement is required. Sometimes if there is peak currents, Gray-Code is to be used to minimize peak currents!

The quantizer-error is defined with equation 3.

$$V_e = V_{in} - V_{eq} \tag{3}$$

It is assumed that the error behaves like white noise[1] because the digital signal is a sequence of pulses. If this is fourier transformed a constant spectral density is received.



Since the quantizer error has the probability density function of white noise, it can be depicted with the function seen in 2.

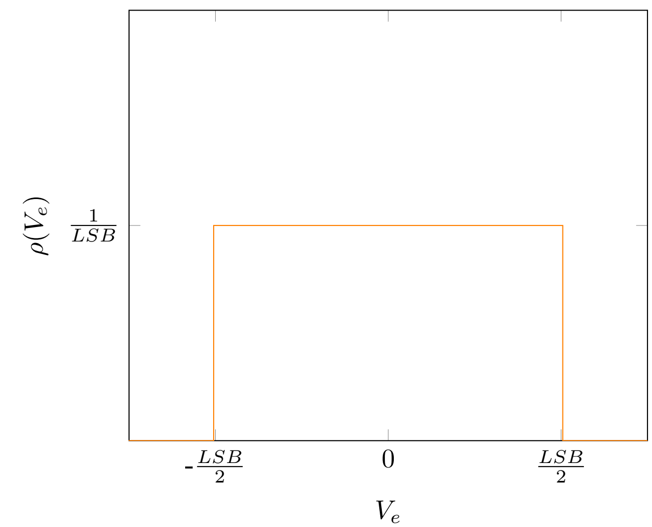


Figure 2: Probability density function of the quatizer error

With the knowledge of the fact that the variance equals the RMS[2] value, depicted in equation 4 and thus 8, we can now find the SNR[3] value with solving equation 11

$$(rms)^2 = \sigma, \ \sigma \text{ is the standard deviation} \tag{4}$$

[1] White noise means that the noise has the same amplitude for every frequency.
[2] root mean square
[3] signal to noise ratio

$$\sigma_e^2 = \int_{-\infty}^{+\infty} V_e^2 \rho(V_e) dV_e \tag{5}$$

$$= \int_{-\frac{LSB}{2}}^{+\frac{LSB}{2}} \frac{V_e^2}{LSB} dV_e \tag{6}$$

$$= \frac{1}{LSB} \frac{1}{3} V_e^3 \Big|_{-\frac{LSB}{2}}^{+\frac{LSB}{2}} \tag{7}$$

$$= \frac{LSB^2}{12} = \frac{1}{12} V_{ref}^2 2^{-2N} \tag{8}$$

$$SNR = \frac{V_{sig,rms}^2}{V_{n,rms}^2} \tag{9}$$

$$= \frac{\left(\frac{V_{ref}}{2} \frac{1}{\sqrt{2}}\right)^2}{\frac{1}{12} V_{ref}^2 2^{-2N}} \tag{10}$$

$$= N \cdot 6.02dB + 1.76dB \tag{11}$$

Using this equation a statement about the ENOB[4] can be made, having a look at the SNR equation optained. This is given in 12.

$$N_{eff} = ENOB = \frac{SNDR - 1.76dB}{6.02dB} \tag{12}$$

2 D/A

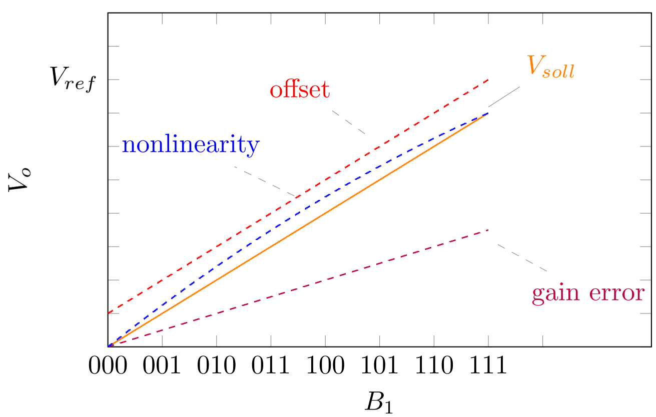


Figure 3: Output of a DAC and possible errors

There is two kinds of nonlinearities:

- INL: integral nonlinearity: $V_{soll} - V_{ist}$
- DNL: differential nonlinearity: $\Delta V_{soll} - \Delta V_{ist}$

[4]effective number of bits

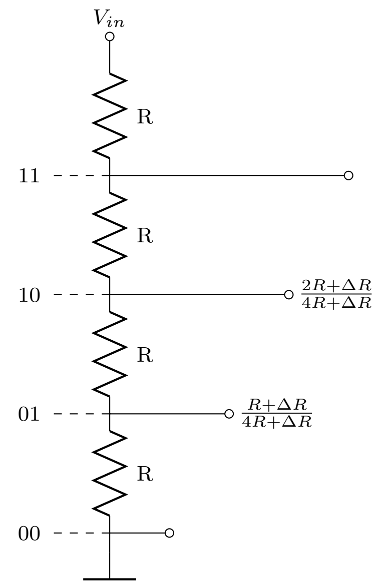


Figure 4: Resistor ladder to implement a dac

In figure 4 the DNL can be calculated as given in equation 15.

$$\Delta V_{ist} = \frac{R + \Delta R}{2^N R + \Delta R} \tag{13}$$

$$\Delta V_{soll} = \frac{R}{2^N R} \tag{14}$$

$$\frac{\Delta R}{2^N R} V_{ref} = \frac{\Delta R}{R} [LSB] \tag{15}$$

A DAC has monotone behavior if $DNL \in [-1, 1]$, which means that a higher B_1 always results in a higher V_o. If a DAC has "no missing codes" guaranteed, all digital values result in a different V_o. So no digital value will ever be skipped.

③ A/D

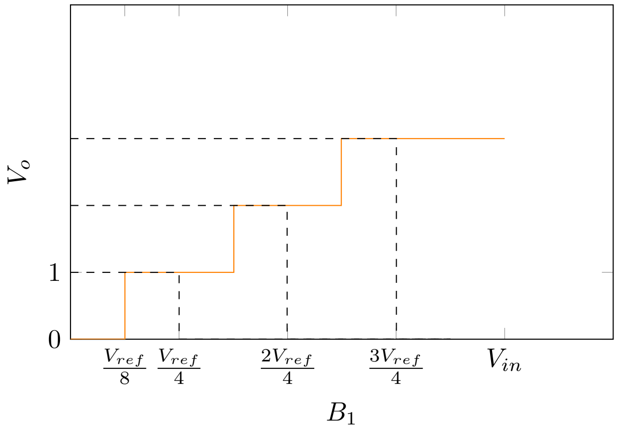


Figure 5: Output of a DAC and possible errors

In 5 the thresholds are in the middle of the coded values. This is a very important criteria. For some ADCs the thresholds are intentionally chosen to be not in the middle. For example in the Lloyd-Max-Quantizer which uses μ-low compression.

④ S&H

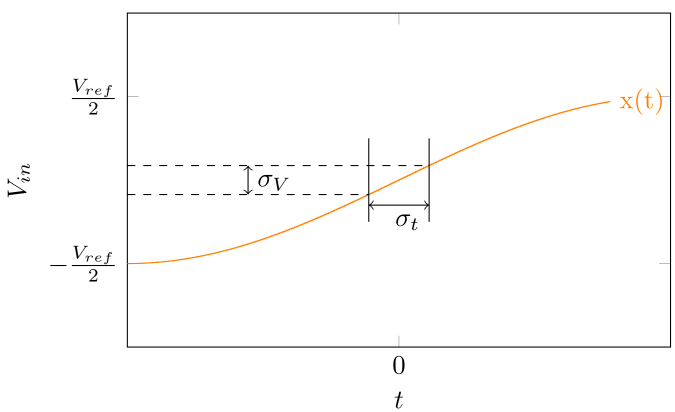


Figure 6: Sample & Hold input

Figure 6 shows the high importance of a clock that has close to no jiiter. Equation 19 shows how much σ_V jiters from the σ_t jiter.

$$x(t) = \frac{V_{ref}}{2} sin(2\pi f t) \tag{16}$$
$$\approx \frac{V_{ref}}{2} 2\pi f t \Big|_{t \to 0} \tag{17}$$
$$\dot{x} \approx V_{ref} \pi f \tag{18}$$
$$\sigma_V = \dot{x}\sigma_t = V_{ref}\pi f \sigma_t \tag{19}$$

$$SNR_{max} = \frac{\sigma_{sig}^2}{\sigma_V^2} \tag{20}$$
$$= \frac{\left(\frac{V_{ref}}{2\sqrt{2}}\right)^2}{\left(V_{ref}\pi f \sigma_t\right)^2} \tag{21}$$
$$= \frac{1}{8\pi^2 f^2 \sigma_t} \tag{22}$$

So as 20 shows, the maximum SNR possible to be reached is already upper bound by the clock jiter!

⑤⑥ LP